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[Continued on next page]

(54) Title: AUTO-ZEROED AMPLIFIER WITH LOW INPUT LEAKAGE

(57) Abstract: An apparatus comprises an amplifier (340) having an inverting input and a non-inverting input; a capacitor coupled (350) to the inverting input of the amplifier; an input voltage conveyance control circuit (309), having a first switch (310) and a second switch (315), the first switch coupled to the capacitor, and the second switch coupled to the non-inverting input of the amplifier; a reference voltage conveyance control circuit (318) having a third switch (333) and a fourth switch (335), wherein a shared node (331) is coupled between the third switch and the fourth switch, the fourth switch coupled to the non-inverting input of the amplifier; a fifth switch (370) coupled to an output of the amplifier; a leakage control circuit (399) having a sixth switch (395) and a seventh switch (397), the sixth switch coupled between the inverting amplifier input and the fifth switch, the seventh switch coupled to the sixth switch and the capacitor; and a first resistor, a feedback resistor (360), coupled from the output of the amplifier to the first switch.

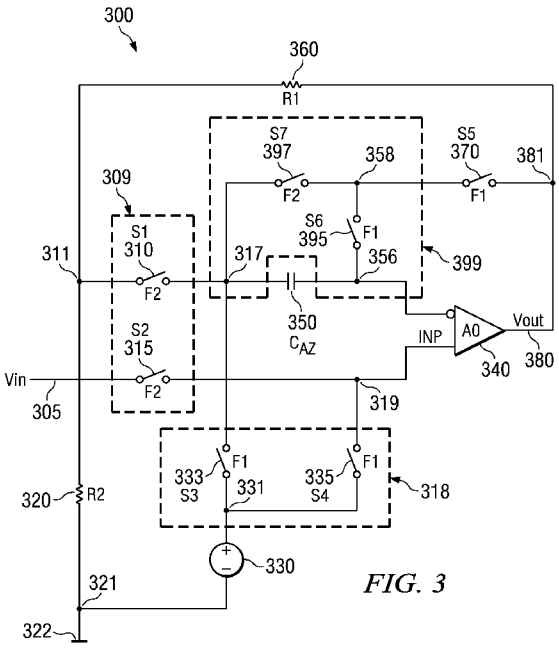

FIG. 3

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AUTO-ZEROED AMPLIFIER WITH LOW INPUT LEAKAGE

[0001] This is directed, in general, to an auto-zeroed amplifier and, more specifically, to an auto-zeroed amplifier with a low leakage into the offset-hold capacitor.

BACKGROUND

[0002] FIG. 1 illustrates a prior art auto-zeroed amplifier 100. Generally, auto-zeroed amplifiers are often used to decrease amplifier voltage offset.

[0003] In the auto-zeroed amplifier 100, a Vin 105 is coupled to a switch S2 115. The switch S2 115 is coupled to a node 119, which is in turn coupled to a non-inverting input of an amplifier auto-zeroed ("A0") 140. A Vout 180 of the amplifier AO 140 is coupled to a switch S5 170 through a node 181. The switch S5 170 is coupled into an inverting input of the amplifier A0 140 through a node 151.

[0004] The node 181 is also coupled to resistor R1 160. The resistor R1 160 is coupled to a node 111, and the node 111 is coupled to a switch S1 110 and a resistor R2 120. The switch S1 110 is coupled to a node 117. The resistor R2 120 is coupled to a node 121, and from the node 121 to a ground 122. The node 121 is also coupled to a negative terminal of a voltage source 130, a positive terminal of which is coupled to a node 131. The node 131 is in turn coupled to a switch S3 133, and also to a switch S4 135. The switch S3 133 is coupled to the switch S1 110 through the node 117, and the switch S4 135 is coupled to the switch S2 115 at a node 119, which is in turn coupled to a non-inverting input of the amplifier A0 140. A capacitor AZ 150 is coupled between the node 117 and the node 151.

[0005] The auto-zeroed amplifier 100 can work as follows:

[0006] During a phase one ("F1"), the "auto-zero" configuration, the auto-zeroed amplifier 100 is in an "auto-offset" configuration and an offset of amplifier A0 140 is integrated over capacitor AZ 150.

[0007] During a phase two ("F2") configuration of auto-zeroing, the "hold" configuration, the capacitor AZ 150 is electrically connected feedback through R1 160, because

switch S1 110 is closed. Vin 105 is connected to the non-inverting input of the amplifier A0 140, as switch S2 115 is closed. The offset between the inverting and non-inverting inputs of the amplifier A0 140 is therefore integrated over the capacitor AZ 150. Therefore, the signal Vin is amplified with a higher accuracy as compared to non-offset compensated amplifiers.

[0008] However, there are disadvantages with the auto-zeroed amplifier 100. In the auto-zeroed amplifier 100, there is a leakage current through switch S5 170 during "F2", there is a leakage current onto the capacitor AZ 150, thereby changing its voltage, effectively changing the offset of the amplifier 100. The voltage across S5 170, when open during "F2", is equal to the difference between Vin 105, and Vout 180, and can be quite large, causing large leakage current through the switch S5 170. In other words, the amplifier operates as an amplifier during "F2"; however, leakage through switch S5 170 caused by this quite large voltage is a limiting operation time between instances of auto-zeroing periods "F1".

[0009] FIG. 2 illustrates a prior art sample / long hold system. A Vin 205 is coupled to a switch S0 210. The switch S0 210 is coupled to a node 212. A switch S1 215 is also coupled to the node 212. A switch S2 220 is also coupled to the node 212, as is its body diode. The switch S1 215 is coupled to a node 217, and the node 217 is coupled to an inverting input of an amplifier A0 230. The node 217 is also coupled to a Vout 235 of the amplifier A0 230. The switch S2 220 is coupled to a node 222. The node 222 is coupled to a capacitor C0 225 and a non-inverting input of the amplifier A0 230. The capacitor C0 225 is also coupled to a ground 227.

[0010] The sample/long hold 200 can work as follows:

[0011] During a phase "F0", the "sample" configuration, the switch 210, and 220 are closed, which conveys the voltage Vin 205 to both the capacitor C0 225 and the non-inverting input of the amplifier A0 230. The amplifier A0 230 is a unity gain amplifier, as output 235 is shorted to the inverting input 217.

[0012] During a "hold" phase "F0 not", the switch 215 is shut, and the switches S0 210 and S2 220 are open. Voltage drop across switch 220 is equal to the voltage offset of the amplifier A0 (a few milliVolts), hence the ensuring small leakage through this switch and long hold time. However, this is a sample/hold circuit and not directly usable in auto-zeroed amplifier of FIG. 1.

This sample and hold circuit avoids the transistor leakage problem of FIG. 1, as it is not an auto-correct circuit;, however, therefore, it does not autocorrect.

[0013] Therefore, it would be advantageous to combine the auto-zero compensation of FIG. 1 with the sample and hold of FIG. 2 that addresses at least some of the concerns of the usage of the prior art.

SUMMARY

[0014] A first aspect provides an apparatus, comprising: an amplifier having an inverting input and a non-inverting input; a capacitor coupled to the inverting input of the amplifier; an input voltage conveyance control circuit, having a first switch and a second switch, the first switch coupled to the capacitor, and the second switch coupled to the non-inverting input of the amplifier; a reference voltage conveyance control circuit having a third switch and a fourth switch, wherein a shared node is coupled between the third switch and the fourth switch, the fourth switch coupled to the non-inverting input of the amplifier; a fifth switch coupled to an output of the amplifier; a leakage control circuit having a sixth switch and a seventh switch, the sixth switch coupled between the inverting amplifier input and the fifth switch, the seventh switch coupled to the sixth switch and the capacitor; and a first resistor coupled from the output of the amplifier to the first switch.

[0015] A second aspect provides a system including an auto-zeroed amplifier system having an inverting input and a non-inverting input, the system comprising: a capacitor coupled to the inverting input of the auto-zeroed amplifier; an input voltage conveyance control circuitry, having a first switch and a second switch, the first switch coupled to the capacitor, and the second switch coupled to the non-inverting input of the auto-zeroed amplifier; a reference voltage conveyance control circuit having a third switch and a fourth switch, wherein a shared node is coupled between the third switch and the fourth switch, the fourth switch coupled to the non-inverting input of the amplifier; a fifth switch coupled to the output of the auto-zeroed amplifier; a leakage control circuit comprising a sixth switch and a seventh switch, the sixth switch coupled between the inverting auto-zeroed amplifier and the fifth switch, the seventh switch coupled to the sixth switch and the capacitor; a first resistor coupled from the output of the auto-zeroed amplifier to the first switch; a second resistor coupled from the first resistor to ground; and a voltage source coupled between the ground and the reference voltage conveyance

control circuitry, wherein a shared node of the reference voltage conveyance control circuitry is also coupled to a positive output of the reference voltage.

[0016] A third aspect provides a system including an auto-zeroed differential amplifier, having an inverting input, a non-inverting input, and a common mode voltage input; the system comprising: a high side auto-zero capacitor coupled to the inverting input of the auto-zeroed amplifier; a low side auto-zeroed capacitor coupled to the inverting input of the auto-zeroed amplifier; high side input voltage conveyance control circuit, having a high side first switch and a high side second switch, the high side first switch coupled to the high side capacitor, and the high side second switch coupled to the non-inverting input of the amplifier; low side input voltage conveyance control circuit, having a low side first switch and a low side second switch, the low side first switch coupled to the low side capacitor, and the low side second switch coupled to the non-inverting input of the amplifier; high side reference voltage conveyance control circuit having a high side third switch and a high side fourth switch, wherein a shared node is coupled between the high side third switch and the high side fourth switch, the high side fourth switch coupled to the inverting input of the amplifier; low side reference voltage conveyance control circuit having a low side third switch and a low side fourth switch, wherein a shared node is coupled between the low side third switch and the low side fourth switch, the fourth switch coupled to the non-inverting input of the amplifier; high side fifth switch coupled to a positive output of the amplifier; low side fifth switch coupled to a negative output of the amplifier; high side leakage control circuit having a high side sixth switch and a high side seventh switch, the high side sixth switch coupled between the inverting amplifier input and the high side fifth switch, the high side seventh switch coupled to the sixth switch and the high side capacitor ; and a low side leakage control circuit having a low side sixth switch and a low side seventh switch, the low side sixth switch coupled between the inverting amplifier input and the low side fifth switch, the low side seventh switch coupled to the low side sixth switch and the low side capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 illustrates a prior art auto-zeroed amplifier 100;

[0018] FIG. 2 illustrates a prior art sample and hold amplifier 200;

[0019] FIG. 3 illustrates an auto-zeroed amplifier with a low leakage current 300 constructed according to principles of the invention; and

[0020] FIG. 4 illustrates a differential auto-zeroed amplifier with a low leakage current 400 constructed according to principles of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0021] Turning to FIG. 3, illustrated is one aspect of an auto-zeroed amplifier with a low leakage current 300 constructed according to principles of the present Application.

[0022] Generally, in the auto-zeroed amplifier 300, as shall be discussed below, a voltage across a switch S7 397 of a leakage control circuit 399 is enabled and disabled in inverse phases "F2", "F1" to a coupled switch S6 395 of the leakage control circuit 399, thereby limiting a voltage across the switch S6 395, to a voltage across capacitor AZ 350, thereby substantially reducing the maximum voltage across the switch S6 395 when open. Substantially reducing the maximum voltage across switch S6 395 when open during an "F0" phase, thereby substantially decreases its leakage current to the capacitor AZ 350, thereby substantially increasing operating parameters of an F0 operation time.

[0023] The auto-zeroed amplifier 300, a band gap amplifier, allows for a significant increase in length of an "F0" on time, when compared to the prior art amplifiers 100 and 200, which can be from 10's of us to 10's of ms

[0024] In the auto-zeroed amplifier 300, a Vin 305 is coupled to a switch S2 315. The switch S2 315 is coupled to a node 319, which is in turn coupled to non-inverting input of an auto-zeroed amplifier 340. A Vout 380 of the auto-zeroed amplifier 380 is coupled to a switch S5 370 through a node 381. The switch S5 370 is coupled into a leakage control circuit 399. The various switches of the auto-zeroed amplifier 300 can be, for example, PMOS switches.

[0025] The leakage control circuit 399 includes a node 358 coupled to the switch S5 370. The node 358 is also coupled to a switch S7 397 within the leakage control circuit 399. The switch S7 397 is coupled to a node 317. The switch S6 395, also within the leakage control circuit 399, is coupled to a node 356. The nodes 317 and 356 are coupled to the capacitor AZ 350, which is used for integration of offset of amplifier 300 during F0.

[0026] The node 381 is also coupled to a feedback resistor R1 360. The feedback resistor R1 360 is coupled to a node 311, the node 311 is coupled to both a switch S1 310 of an input voltage conveyance control circuit 309 and a resistor R2 320. The switch S1 310 is coupled to the node 317. The resistor R2 320 is coupled to a node 321, and from a node 321 to a ground 322. The node 321 is also coupled to a negative terminal of a voltage source 330, a positive

terminal of which is coupled to a node 331 of a reference voltage control circuit 318. The node 331 is, in turn, coupled to a switch S3 333, and also to a switch S4 335, also in the reference voltage control circuit 318. The switch S 333 is coupled to the node 317, and the switch S4 335 is coupled to the node 319.

[0027] Generally, the voltage across the capacitor AZ 350 is substantially equal to the amplifier A0 offset. Consequently, the voltage across switch S6 395 is also substantially equal to the A) offset, thereby decreasing leakage through the switch S6 395, and therefore substantially increasing hold time between auto-zeroing periods. The offfset can be 0-5 mV.

[0028] The auto-zeroed amplifier 300 can work as follows:

[0029] During a phase one ("F1"), the auto-zeroed amplifier 300 is in an "auto-zero" configuration, and the offset of amplifier A0 340 is integrated over the capacitor AZ 150. The switches S3 333 and S4 335 are closed, and therefore convey the reference voltage 330 to the nodes 317 and 319, respectively. An offset of the amplifier A0 340 is integrated over the capacitor AZ 350. The switch S5 370 and switch S6 395 are closed, thereby inverting the value of the output Vout 380 to a single feedback of substantially unity gain.

[0030] During a phase two ("F2"), a "low-leakage hold phase" configuration, the capacitor AZ 350 is connected in series with the inverting input, as switch S2 315 is closed, Vin 305 is connected to the non-inverting input of the amplifier A0 340, as the switch S2 315 is closed. The offset between the inverting and non-inverting inputs of the amplifier A0 340 is therefore integrated over the capacitor AZ 350.

[0031] Moreover, in the auto-zeroed amplifier 300, the switch S7 397 is also closed during "F2", the "low leakage hold phase" configuration. Because of the closing of switch S7 397 during "F2", during "F2" the voltage across the closed switch S7 397 is therefore coupled in parallel to the capacitor AZ 350 and the open S6 switch 395, which therefore applies a limit of a low maximum ceiling of voltage to open switch S6 395. Therefore, only a few milli-volts or micro-volts will typically be applied across the switch S6 395 during "F2", as opposed to prior art switches of the auto-zeroed amplifier 100 wherein a difference across a switch is the difference between an output of the amplifier A0 140 and an inverting input node of the amplifier A0 140, thereby significantly decreasing the voltage across open switch S6 395 as compared to the voltage across the prior art S6 170 also opened during "F2" phase.

[0032] This, in turn, allows for a significantly lowered leakage current to the capacitor AZ 350, thereby increasing usage time. Advantageously, limiting the voltage across the switch S6 370 in this circuit when this switch is open changes limits its leakage current, thereby improving functionality of the auto-zeroed amplifier 300.

[0033] FIG. 4 illustrates a differential auto-zeroed amplifier 400. Principles of construction and operation of the auto-zeroed amplifier 400 are generally analogous to those of the auto-zeroed amplifier 300, except that the auto-zeroed amplifier 300 is a single-ended amplifier, and the auto-zeroed amplifier 400 is a differential amplifier. As is illustrated, a positive differential side 401 is mirrored in a negative differential side 403. The "F1" and "F2" phases of the positive differential side 401 can be applied by analogy to the negative differential side 403.

[0034] During phase "F1", a "differential auto zero" configuration of the differential auto-zeroed amplifier 400, the capacitors AZ 450, 451 are electrically connected between the VCM (input common mode voltage or ground or reference) and amplifier A0 440 out+ and amplifier A0 440 out- through a third high side switch S3 415 and a third low side switch 418 of a differential voltage reference conveyance circuit 414. In the auto-zeroed amplifier 400 the conveyed reference voltage is the common mode voltage. Offsets of the inverting and non-inverting inputs of the amplifier A0 440 are integrated across are integrated across the capacitors AZ 450, 451. C2+, C2-? Can have a few pFvalue for small die area.

[0035] During the phase "F2", a "differential hold" configuration of the differential auto-zeroed amplifier 400, the voltage across open switch s6+ 495 of an upper side leakage control circuit 499 is shorted in parallel thereby limiting the voltages across these open switches S6+ 495 and S6- , for an active phase, thereby decreasing leakage current into the capacitor AZ+ 450 and the capacitor AZ- 451. Switches are shown as closed/open according to phases.

[0036] Those skilled in the art to which this application relates will appreciate that many other embodiments and variations are possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

an amplifier having an inverting input and a non-inverting input;

a capacitor coupled to the inverting input of the amplifier;

an input voltage conveyance control circuit, having a first switch and a second switch, the first switch coupled to the capacitor, and the second switch coupled to the non-inverting input of the amplifier;

a reference voltage conveyance control circuit having a third switch and a fourth switch, wherein a shared node is coupled between the third switch and the fourth switch, the fourth switch coupled to the non-inverting input of the amplifier;

a fifth switch coupled to an output of the amplifier;

a leakage control circuit having a sixth switch and a seventh switch, the sixth switch coupled between the inverting amplifier input and the fifth switch, the seventh switch coupled to the sixth switch and the capacitor; and

a first resistor, coupled from the output of the amplifier to the first switch, wherein the first resistor is a feedback resistor.

2. The apparatus of Claim 1, wherein the shared node of the input voltage conveyance control circuit is also coupled to a positive output of a reference voltage.

3. The apparatus of Claim 1, wherein the sixth switch is a PMOS switch.

4. The apparatus of Claim 1, wherein the sixth switch when open, has a voltage that is substantially equal to a sum of the closed switch voltage of the seventh switch and the capacitor.

5. The apparatus of Claim 4, wherein a voltage across the capacitor has bled into it a current that is proportional to the voltage cross the sixth switch when open, voltage that is substantially equal to the closed switch voltage of the seventh switch summed to the capacitor voltage.

6. The apparatus of Claim 1, further comprising wherein the first and second switches of the input conveyance control circuitry are opposite in logic state from the third and fourth switches of the reference voltage conveyance control circuitry, and wherein the sixth switch of the leakage control circuit are in a same logic state as the reference voltage conveyance control circuitry, and the seventh switch of the leakage control circuit is in a same logic state as the input voltage conveyance control circuitry.

7. The apparatus of Claim 1, further comprising a second resistor coupled to the first resistor, the second resistor also coupled to a ground.

8. A system including an auto-zeroed amplifier system having an inverting input and a non-inverting input, the system comprising:

a capacitor coupled to the inverting input of the auto-zeroed amplifier;

an input voltage conveyance control circuitry, having a first switch and a second switch, the first switch coupled to the capacitor, and the second switch coupled to the non-inverting input of the auto-zeroed amplifier;

a reference voltage conveyance control circuit having a third switch and a fourth switch, wherein a shared node is coupled between the third switch and the fourth switch, the fourth switch coupled to the non-inverting input of the amplifier;

a fifth switch coupled to the output of the auto-zeroed amplifier;

a leakage control circuit comprising a sixth switch and a seventh switch, the sixth switch coupled between the inverting auto-zeroed amplifier and the fifth switch, the seventh switch coupled to the sixth switch and the capacitor;

a first resistor coupled from the output of the auto-zeroed amplifier to the first switch, wherein the first resistor is a feedback resistor;

a second resistor coupled from the first resistor to ground; and

a voltage source coupled between the ground and the reference voltage conveyance control circuitry;

wherein a shared node of the reference voltage conveyance control circuitry is also coupled to a positive output of the reference voltage.

9. The system of Claim 8, further comprising wherein the third, fourth, fifth and sixth switches are in a closed state at a same time, and the first, second, and seventh switches are in an open state at that same time.

10. The system of Claim 8, further comprising wherein the third, fourth, fifth and sixth switches are open at a same time, and the first second and seventh switches are in an open state at that same time.

11. The auto zeroed amplifiers of Claim 8, wherein the sixth switch is a PMOS switch.

12. The system of Claim 8, wherein the sixth switch when open, has a voltage that is substantially equal to the closed switch voltage of the seventh switch.

13. The system of Claim 13, wherein a voltage across the capacitor has bled into it a current that is proportional to the voltage cross the sixth switch when open, wherein that voltage that is substantially equal to the closed switch voltage of the seventh switch summed with the voltage of the capacitor.

14. The system of Claim 8, wherein the amplifier is a single ended amplifier.

15. A system including an auto-zeroed differential amplifier, having an inverting input, a non-inverting input, and a common mode voltage input; the system comprising:

a high side auto-zero capacitor coupled to the inverting input of the auto-zeroed amplifier;

a low side auto-zero capacitor coupled to the inverting input of the auto-zeroed amplifier;

a high side input voltage conveyance control circuit, having a high side first switch and a high side second switch, the high side first switch coupled to the high side capacitor, and the high side second switch coupled to the non-inverting input of the amplifier;

a low side input voltage conveyance control circuit, having a low side first switch and a low side second switch, the low side first switch coupled to the low side capacitor, and the low side second switch coupled to the non-inverting input of the amplifier;

a high side reference voltage conveyance control circuit having a high side third switch and a high side fourth switch, wherein a shared node is coupled between the high side third switch and the high side fourth switch, the high side fourth switch coupled to the inverting input of the amplifier;

a low side reference voltage conveyance control circuit having a low side third switch and a low side fourth switch, wherein a shared node is coupled between the low side third switch and the low side fourth switch, the fourth switch coupled to the non-inverting input of the amplifier;

a high side fifth switch coupled to a positive output of the amplifier;

a low side fifth switch coupled to a negative output of the amplifier;

a high side leakage control circuit having a high side sixth switch and a high side seventh switch, the high side sixth switch coupled between the inverting amplifier input and the high side fifth switch, the high side seventh switch coupled to the sixth switch and the high side capacitor; and

a low side leakage control circuit having a low side sixth switch and a low side seventh switch, the low side sixth switch coupled between the inverting amplifier input and the low side fifth switch, the low side seventh switch coupled to the low side sixth switch and the low side capacitor.

16. The system of Claim 15, further comprising wherein a second high side capacitor is coupled from the high side output of the amplifier to the first high side switch.

17. The system of Claim 15, wherein the high side sixth switch and the low side sixth switch are both PMOS switches.

18. The system of Claim 15, further comprising:

a high side third capacitor coupled between the high side first switch and a high side input voltage; and

a low side third capacitor coupled between the low side first switch and a low side input voltage.

19. The system of Claim 15, further comprising wherein the high side sixth switch when open, has a voltage that is substantially equal to the closed switch voltage of the high side seventh switch.

20. The system of Claim 19, wherein a voltage across the capacitor has bled into it a current that is proportional to the voltage cross the sixth switch when open, a voltage that is substantially equal to the closed switch voltage of the seventh switch.

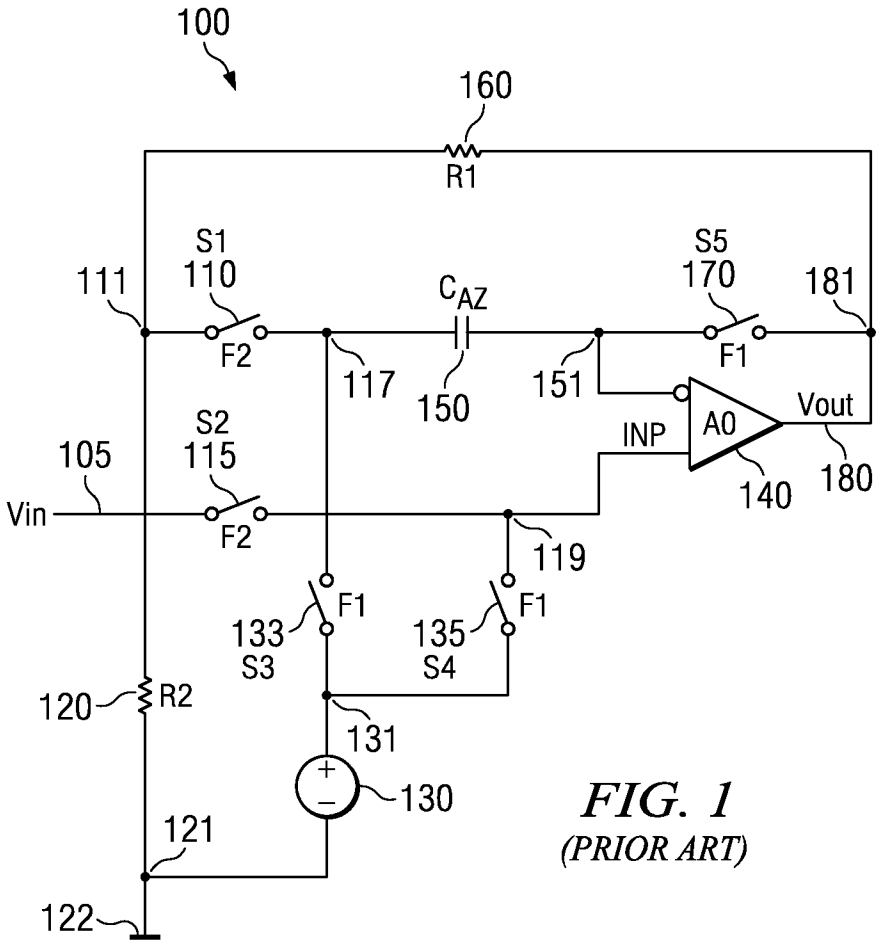


FIG. 1
(PRIOR ART)

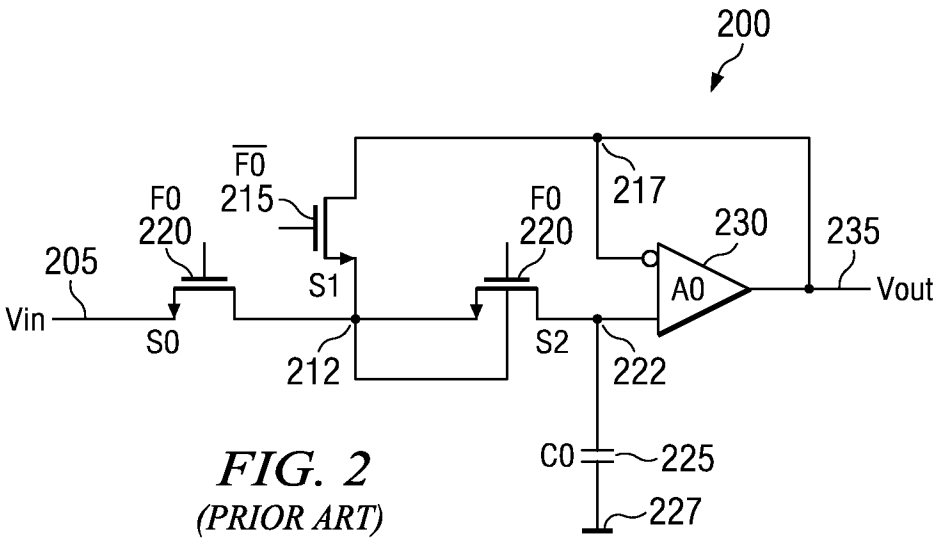
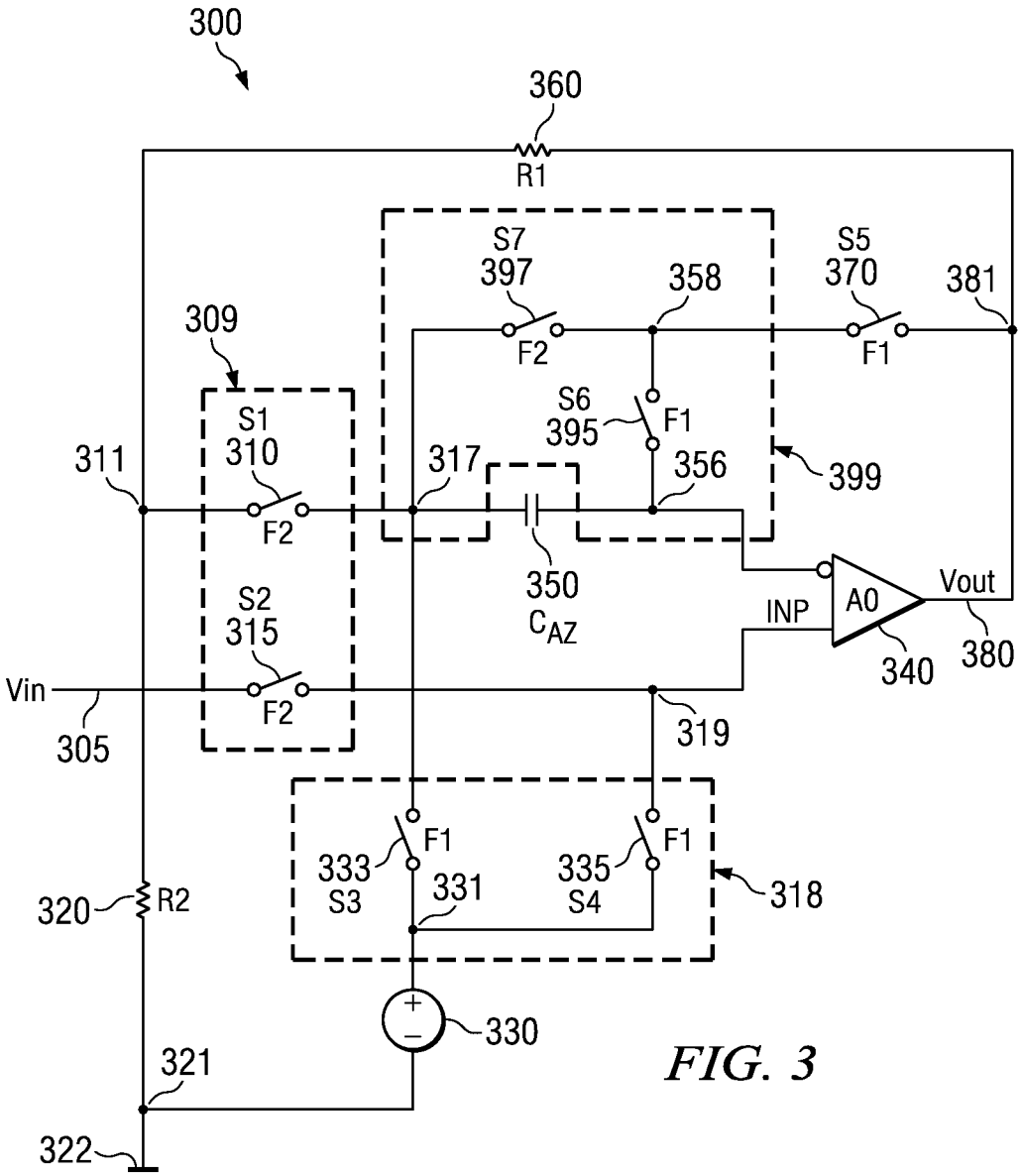


FIG. 2
(PRIOR ART)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F2
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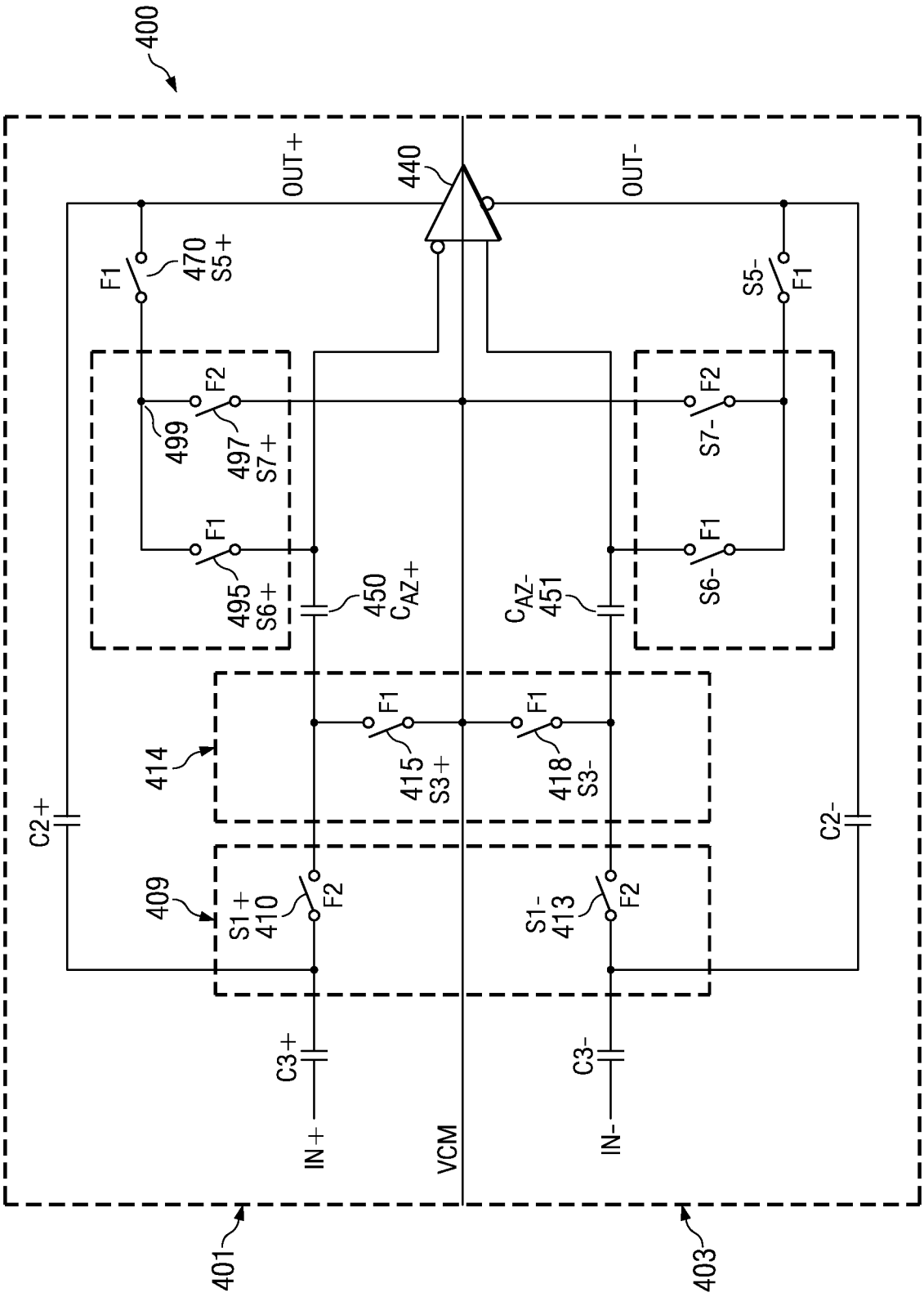
FIG. 3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S6-
F1
414
F1
415
S3+
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S3-
C2+
C2-
409
S1+
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S1-
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C3+
C3-
IN+
VCM
IN-
401
403

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/031151

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/45(2006.01)i, H03F 3/70(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F 3/45; H03F 3/70; G06G 7/18; G09G 3/36; H03M 1/12; H03H 19/00; G02F 1/133; H01L 21/8238; H01L 27/092; H03K 17/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: leakage, amp, inverting, non-inverting, switch.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2010-0040581 A (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE et al.) 20 April 2010 See abstract; claim 1; paragraph [0037]; and figure 2.	1-20
A	JP 2010-028160 A (YOKOGAWA ELECTRIC CORP.) 04 February 2010 See abstract; claims 1-3; paragraph [0019]; and figures 1, 3, 6.	1-20
A	US 2008-0186077 A1 (MATTHEW C. GUYTON et al.) 07 August 2008 See abstract; paragraphs [0044]-[0047]; and figures 2B, 4A-4B.	1-20
A	JP 2001-067047 A (TEXAS INSTR JAPAN LTD.) 16 March 2001 See abstract; paragraphs [0034]-[0036]; and figures 7-8.	1-20
A	JP 2005-005620 A (TOYOTA INDUSTRIES CORP. et al.) 06 January 2005 See abstract; paragraphs [0064]-[0070]; and figure 6.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 June 2013 (21.06.2013)	**21 June 2013 (21.06.2013)**

Name and mailing address of the ISA/KR
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/031151

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2010-0090756 A1	15.04.2010
		US 7847625 B2	07.12.2010
JP 2010-028160 A	04.02.2010	None	
US 2008-0186077 A1	07.08.2008	US 7564273 B2	21.07.2009
		WO 2008-097400 A1	14.08.2008
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		EP 1635393 A1	15.03.2006
		KR 10-2006-0017869 A	27.02.2006
		US 2006-0180840 A1	17.08.2006
		WO 2004-112143 A1	23.12.2004