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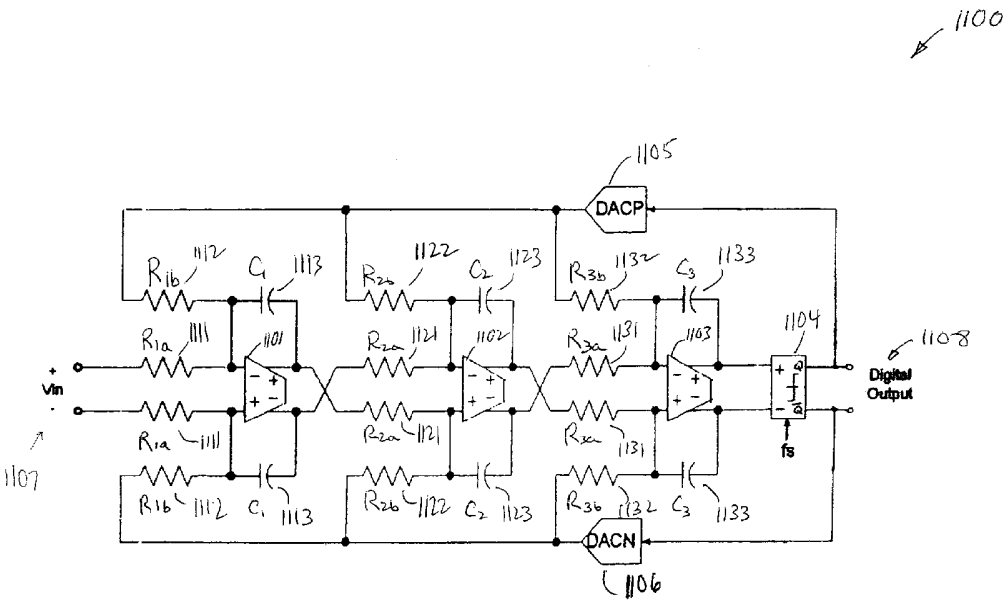
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(54) Title: LOW VOLTAGE DIGITAL TO ANALOG CONVERTER, COMPARATOR, AND SIGMA-DELTA MODULATOR CIRCUITS



(57) Abstract: Circuits that operate with power supplies of less than 1 Volt are presented. More particularly, circuits that operate with supply voltages near or lower than the threshold voltage of the transistors in those circuits are presented. Various circuits embodiments such as operational transconductance amplifiers (1101, 1102, 1103), biasing circuits, integrators (1113, 1123, 1133), continuous-time sigma delta modulators, track-and-hold circuits, and others are presented. The techniques and circuits can be used in a wide range of applications and various transistors from metal-oxide-semiconductor to bipolar junction transistors may implement the techniques presented herein.

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LOW VOLTAGE DIGITAL TO ANALOG CONVERTER, COMPARATOR, AND SIGMA-DELTA MODULATOR CIRCUITS

Cross Reference to Related Applications

This application claims the benefit of United States Provisional Patent Application Nos. 60/611,601, 60/627,070, and 60/704,466, respectively filed on September 20, 2004, November 12, 2004, and August 1, 2005, which are hereby incorporated by reference herein in their entireties.

Background of the Invention

The present invention relates to circuits that can operate at low supply voltages. More particularly, the present invention provides circuits that function with supply voltages near or lower than the threshold voltage of transistors used in the circuit.

For some time, a trend in semiconductor circuits has been to decrease the feature size of transistors and to place more transistors in the same size area of silicon. This trend of decreasing feature size promises to bring the features of transistors into the nano-scale range so that the intrinsic speed of the devices, and thus the signal processing capability, can keep increasing. With continually shrinking feature size, supply voltages for circuits have also experienced a downward trend in order to maintain reliability, to reduce power density, and to avoid thermal problems. This downward trend in power supply voltages is beneficial for digital circuits because it reduces power consumption quadratically. However, the threshold voltages at which transistors operate have not decreased proportionally to the supply voltages because the transistors' threshold voltages cannot be reduced as aggressively. This is the case because lower threshold values create static leakage (i.e., unwanted electron/hole flow when a device is off) that would result in unacceptable circuit operation. Therefore, it is desirable to provide analog circuits that can operate with supply voltages near or lower than the threshold voltage of the transistors in those circuits.

Summary of the Invention

Various circuits that operate with power supplies of less than 1 Volt are presented. More particularly, circuits that operate with supply voltages near or lower than the threshold voltage of the transistors in those circuits are presented. These circuits include operational transconductance amplifiers, biasing circuits, integrators, continuous-time sigma delta modulators, track-and-hold circuits, and others. The techniques and circuits can be used in a wide range of applications, and various transistors from metal-oxide-semiconductor to bipolar junction transistors may be used to implement the techniques presented herein.

In accordance with certain embodiments of the present invention, digital-to-analog converters (DACs) are provided. Features of these DACs include: a first PMOS transistor having a gate coupled to an input signal, a source coupled to a first reference voltage, a drain, and a body coupled to a bias voltage; a first NMOS transistor having a gate coupled to the input signal, a drain coupled to the drain of the first PMOS transistor, a source, and a body coupled to a bias voltage; and a second NMOS transistor having a gate coupled to a clock signal, a drain coupled to the source of the first NMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

In accordance with certain embodiments of the present invention, digital-to-analog converters (DACs) are provided. Features of these DACs include: a NMOS transistor having a gate coupled to an input signal, a source coupled to a first reference voltage, a drain, and a body coupled to a bias voltage; a first PMOS transistor having a gate coupled to the input signal, a drain coupled to the drain of the NMOS transistor, a source, and a body coupled to a bias voltage; and a second PMOS transistor having a gate coupled to a clock signal, a drain coupled to the source of the first PMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

In accordance with certain embodiments of the present invention, comparators are provided. Features of these comparators include: a differential pair of transistors, wherein each transistor has a body coupled to an input signal, a gate coupled to a clock signal, a source coupled to a first reference voltage, and a drain; an active load coupled to the drain of each transistor of the differential pair of transistors; a first

cross-coupled pair of transistors, wherein each transistor has a source coupled to the first reference voltage, a gate coupled to an inverse of the clock signal, and a drain, and wherein the body of one of the transistors of the first cross-coupled pair of transistors is coupled to the drain of the other of the transistors of the first cross-coupled pair of transistors, and the body of the other of the transistors of the first cross-coupled pair of transistors is coupled to the drain of the one of the transistors of the first cross-coupled pair of transistors; and a second cross-coupled pair of transistors, wherein each transistor has a source coupled to a second first reference voltage, a gate coupled to the clock signal, and a drain coupled to the drains of the first cross-coupled pair of transistors, and wherein the body of one of the transistors of the second cross-coupled pair of transistors is coupled to the drain of the other of the transistors of the second cross-coupled pair of transistors, and the body of the other of the transistors of the second cross-coupled pair of transistors is coupled to the drain of the one of the transistors of the second cross-coupled pair of transistors.

In accordance with certain embodiments of the present invention, sigma-delta modulators are provided. Features of these sigma-delta modulators include: a first operational transconductance amplifier (OTA) having a first input and a first output; a capacitor coupled having a first side and a second side, wherein the first side is coupled to the first input of the first OTA and the second side is coupled to the first output of the first OTA; a comparator having an input coupled to the first output of the first OTA, having a clock input coupled to a clock signal, and having an output;

a digital-to-analog converter having an input coupled to the output of the comparator and having an output; and a resistor having a first side and a second side, wherein the first side is coupled to the output of the digital-to-analog converter and the second side is coupled to the first input of the first OTA and the first side of the capacitor, wherein the coupling, between (i) the digital-to-analog converter and (ii) the first side of the capacitor and the first input of the first OTA, enters a high impedance state based on the clock signal.

In accordance with certain embodiments of the present invention, sigma-delta modulators are provided. Features of these sigma-delta modulators include: a plurality of operational transconductance amplifiers (OTAs), each having a first input and a first output; a plurality of capacitors, each having a first side and a second side,

wherein the first side of each of the plurality of capacitors is coupled to the first input of a corresponding one of the plurality of OTAs and the second side of each of the plurality of capacitors is coupled to the first output of the corresponding one of the plurality of OTAs; a comparator having an input coupled to the first output of one of the plurality of OTAs, having a clock input coupled to a clock signal, and having an output; a digital-to-analog converter having an input coupled to the output of the comparator and having a plurality of outputs; and a plurality of resistors, each coupled between a corresponding one of the plurality of outputs of the digital-to-analog converter and the first input of one of the corresponding plurality of OTAs, wherein each coupling, between (i) a corresponding one of the plurality of outputs of the digital-to-analog converter and (ii) the first side of the corresponding capacitor and the first input of the corresponding one of the plurality of OTAs, enters a high impedance state based on the clock signal.

In accordance with certain embodiments of the present invention, sigma-delta modulators are provided. Features of these sigma-delta modulators include: a plurality of operational transconductance amplifiers (OTAs), each having a first input and a first output; a plurality of capacitors, each having a first side and a second side, wherein the first side of each of the plurality of capacitors is coupled to the first input of a corresponding one of the plurality of OTAs and the second side of each of the plurality of capacitors is coupled to the first output of the corresponding one of the plurality of OTAs; a comparator having an input coupled to the first output of one of the plurality of OTAs, having a clock input coupled to a clock signal, and having an output; a plurality of digital-to-analog converters, each having an input coupled to the output of the comparator and having an output; and a plurality of resistors, each coupled between the output of a corresponding one of the plurality of digital-to-analog converters and the first input of one of the corresponding plurality of OTAs, wherein each coupling, between (i) the output of a corresponding one of the plurality of digital-to-analog converters and (ii) the first side of the corresponding capacitor and the first input of the corresponding one of the plurality of OTAs, enters a high impedance state based on the clock signal.

Other features of these embodiments of the present invention are provided below.

Brief Description of the Drawings

The above and other advantages of the present invention will be apparent upon consideration of the following detailed description, taken in conjunction with accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 is a schematic diagram of an Operational Transconductance Amplifier (OTA) with a bulk input in accordance with certain embodiments of the present invention;

FIGS. 2A and 2B are schematic diagrams of a two-stage OTA in accordance with certain embodiments of the present invention;

FIG. 3A is schematic diagram of another embodiment of a two-stage OTA with a gate input in accordance with certain embodiments of the present invention;

FIG. 3B is schematic diagram of an OTA configured with resistors for controlling the common mode voltages associated with the OTA in accordance with certain embodiments of the present invention;

FIG. 4 is a schematic diagram of biasing circuitry in accordance with certain embodiments of the present invention;

FIG. 5A is a graph of transfer characteristics of an operational transconductance amplifier in accordance with certain embodiments of the present invention;

FIG. 5B is a schematic diagram of a Schmitt-trigger oscillator in accordance with certain embodiments of the present invention;

FIG. 6 is a schematic diagram of a low-voltage damped tunable integrator in accordance with certain embodiments of the present invention;

FIG. 7 is a block diagram of a filter in accordance with certain embodiments of the present invention;

FIG. 8A is a schematic diagram of a filter in accordance with certain embodiments of the present invention;

FIG. 8B is a schematic diagram of a voltage controlled oscillator in accordance with certain embodiments of the present invention;

FIG. 9 is a schematic diagram of a track and hold circuit in accordance with certain embodiments of the present invention;

FIG. 10 is a schematic diagram of another gate-input OTA in accordance with certain embodiments of the present invention;

FIGS. 11A and 11B are schematic diagrams of a continuous-time sigma delta modulator in accordance with certain embodiments of the present invention;

FIGS. 12A and 12B are schematic diagrams of digital-to-analog converters (DACs) in accordance with certain embodiments of the present invention; and

FIG. 13 is a schematic diagram of a comparator in accordance with certain embodiments of the present invention.

Detailed Description of the Invention

The present invention relates to circuits that can operate at low supply voltages. More particularly, the present invention provides circuits that function near or lower than the threshold voltage of its transistors without relying upon internal voltage boosting. Low-voltage techniques which may be used in various combinations are automatic biasing to control gains and signal swings, the use of weakly inverted devices, the input of a signal at the body of a transistor, and the application of forward body bias to lower voltage thresholds. The transistors used in the composition of the various circuits presented herein may be fabricated with 0.18 μm process technologies down to nanometer process technologies. CMOS technology may be used. In accordance with the present invention, the circuits illustrated and described herein may be used as circuits of discrete components or integrated circuits as would be appreciated by one skilled in the art.

As the invention is described herein, reference is made to various forms of transistors. These transistors may include metal oxide semiconductor field effect transistor (MOSFET), such as PMOS and NMOS transistors, as well as any other suitable form of transistor. In certain applications within transistors, as will be

apparent to one of ordinary skill in the art, these transistors may be used as switches. In such cases, the use of the term "input" in connection with such switching transistors in the specification and claims shall mean the terminal at which current flows into the transistor (e.g., the source in a PMOS transistor and the drain in an NMOS transistor), and the term "output" in connection with such switching transistors in the specification and claims shall mean the terminal at which current flows out of the transistor (e.g., the drain in a PMOS transistor and the source in an NMOS transistor).

Also, as the invention is described herein, reference is made to various resistors and capacitors. These resistors and capacitors may be implemented with transistor-based equivalents as known in the art when appropriate.

Generally speaking, the voltage threshold of a transistor is the voltage required to switch the transistor from a blocking state to a conducting state, and the voltage threshold typically varies from a couple of hundred millivolts to a volt in standard enhancement devices (e.g., transistors formed using standard CMOS processes). In a transistor, weak inversion, moderate inversion and strong inversion describe different characteristic states of transistor operation. Weak inversion is when a transistor is dominated by a diffusion current (i.e., a current caused by a free movement of electrons), moderate inversion is when a transistor has both a diffusion current and a drift current (i.e., a current caused by an electric field), and strong inversion is when a drift current dominates. For example, in a metal oxide semiconductor field effect transistor (MOSFET), weak inversion is when there is no channel in the device and the drain of the transistor is more reversed biased than the source.

In order to operate a transistor in moderate inversion (i.e., such that it is partially turned-on) when used in a half-volt circuit, the full supply voltage may have to be applied as a gate bias. However, an input signal to the transistor in this case will typically not be able to swing higher than this gate bias because it is at the maximum supply voltage, and thus portions of the input signal may be lost.

To overcome this problem, in accordance with the present invention, an input signal may be applied to the body (or bulk) of a transistor. Applying the input signal at the body of the transistor may allow the input signal to swing while the gate of the

transistor is being used to put it in weak-to-moderate inversion mode of operation. The body may also be forward biased to lower the transistor's threshold voltage.

As set forth below, various differential mode amplifiers are presented. A differential mode amplifier preferably responds only to the differential voltage between its two inputs, with a voltage that is common to the two inputs (i.e., has the same amplitude and phase) being cancelled out. This is common-mode rejection. This common signal voltage is referred to as a common-mode voltage. Common-mode rejection ratio (CMRR) is the ratio of the differential mode gain over the common mode gain – see, e.g., Gray, Hurst, Lewis & Meyer, Analysis and design of analog integrated circuits, and B. Razavi, Design of analog CMOS circuits, which are hereby incorporated by reference herein in their entireties. A fully differential amplifier which is characterized by having two inputs and two outputs may use a common-mode feedback (CMFB) loop to control the common-mode voltages at different nodes and to suppress the common-mode voltage components present at different stages of an amplifier.

FIG. 1 illustrates a schematic of a low-voltage differential gain stage in accordance with certain embodiments of the present invention. As shown, the two inputs V_{in}^+ and V_{in}^- are at the body junctions of transistors M_{1A} **114** and M_{1B} **116** (which form a differential pair). Outputs V_{out}^+ and V_{out}^- are taken from output terminals of transistors M_{1A} **114** and M_{1B} **116**. The transconductances of the bodies (g_{mb}) of these devices provide the input transconductances. Transistors M_{1A} **114** and M_{1B} **116** are loaded by transistors M_{2A} **118** and M_{2B} **120** (which act as current sources and an active load), respectively.

Resistors R_A **122** and R_B **124** feed back a signal corresponding to the output common-mode voltage to the gates of transistors M_{1A} **114**, M_{1B} **116**, M_{3A} **126**, and M_{3B} **128** in order to provide common-mode rejection. A level shift is maintained by transistor M_4 **130** pulling a current though resistors R_A **122** and R_B **124** so that a level shift is created between node **140** and the common-mode voltage at nodes **141** and **142**. Transistor M_4 **130** and resistors R_A **122** and R_B **124** form a level shift bias circuit. This level shift allows the outputs, V_{out}, of the circuit to be biased at one level while node 140 is at a second bias voltage so that operation of the transistors M_{1A} **114**, M_{1B} **116**, M_{3A} **126**, and M_{3B} **128** may be in moderate inversion. For example, with a

MOSFET, a level shift between the output common-mode voltage at 0.25 Volts and the gate bias at 0.07 Volts allows the gate-to-source voltage, V_{GS}, to be set. The relationship between V_{GS} and the threshold voltage is a determining factor of the inversion level in a MOSFET. Therefore, by pulling a current through R_A **122** and R_B **124** with transistor M_4 **130**, the inversion level and operating characteristics of the circuit can be modified through a level shift.

As shown, the body inputs of transistors M_{3A} **126** and M_{3B} **128** are cross-coupled to the drains of these transistors in order to add a negative resistance to the output of the circuit (i.e., at V_{out}^+ and V_{out}^-) and thereby boost the differential DC gain. This cross coupling may decrease the common-mode gain as well. Transistors M_{3A} **126** and M_{3B} **128** form a cross-coupled pair.

The following two equations give the differential and common-mode DC gain for the circuit illustrated in FIG. 1, where g_{mbN} is the body transconductance of transistor N, g_{mN} is the gate transconductance of transistor N, and g_{dsN} is the output conductance of transistor N.

$$A_{diff} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + g_{ds2} + 1/R - g_{mb3}}$$

$$A_{cm} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + g_{ds2} + g_{mb3} + g_{m1} + g_{m3}}$$

In certain embodiments, M_{3A} **126** and M_{3B} **128** may be sized so that g_{mb3} cancels out approximately 60 percent of $g_{ds1} + g_{ds3} + g_{ds2} + 1/R$, which may result in a differential gain boost of 8 dB. Furthermore, operation near the weak to moderate inversion boundary may provide a relatively large transconductance of the body (g_{mb}), which may be useful when inputting signals to the body of a transistor because of a consequent gain increase.

As shown, where an input common-mode is at $V_{DD}/2$ (i.e., $V_{in}+$ and $V_{in}-$ being equal to 0.25 Volts in common mode), a forward bias on, for example, the body-source junction (V_{BS}) of a MOSFET may be introduced. A larger forward bias voltage may lead to greater threshold voltage reduction, but the body (or bulk) leakage current may increase exponentially with the amount of forward bias and the

temperature. This body leakage current can be limited by constraining the forward bias voltage V_{BS} to about 0.4 Volts, and such a forward bias may effectively lower the voltage threshold and increase the inversion level from those typically associated with a transistor. The use of body bias may be accomplished without much risk of latch-up because the supply voltage limits the voltages in the circuit, which in certain embodiments is less than 1 Volt. For example, a supply voltage V_{DD} of 0.5 Volts may not be enough to forward-bias parasitic pn junctions to a sufficient degree to allow latching to occur.

FIG. 2 illustrates a two-stage differential operational transconductance amplifier (OTA) **210** in accordance with certain embodiments of the present invention. In other embodiments, more stages may be cascaded in a similar fashion to two-stage amplifier **210**. Two-stage OTA **210** may be broken down into stage one **212** and stage two **214**. As described herein and shown in the figures, stage two transistors and resistors are denoted with a prime symbol.

The circuits of stage one **212** and stage two **214** are similar to circuit 100 of FIG. 1. However, Miller compensation capacitors Cc **216** with series resistors Rc **218** are added for zero cancellation to stabilize the amplifier. Bias currents have also been applied at bias inputs biasn **220** and biasi **222** and are reflected throughout the OTA by current mirrors composed of transistors M_2 **224**, M_{2A} **226**, M_{2B}' **228**, M_4 **230**, M_4 **232**, and M_4' **234**. For example, biasn may be 40 μA and biasi may be 4 μA.

The frequency response of OTA **210** may have a gain-bandwidth product approximately given by $g_{mb1}/(2\pi Cc)$, where g_{mb1} is the body transconductance of the input transistors of the first stage, and may have a second pole given by $g'_{mb1}/(2\pi C_L)$, where g'_{mb1} is the body transconductance of the input transistors of the second stage and C_L **260** is a load capacitance.

As recited above, the transistors of OTA **210** operate in a similar fashion to the transistors described in connection with FIG. 1. As shown, transistors M_{1A} **236** and M_{1B} **238** and transistors M_{1A}' **244** and M_{1B}' **246** each form a differential pair which takes the input for the respective stage. Transistors M_{3A} **240** and M_{3B} **242** and transistors M_{3A}' **248** and M_{3B}' **250** form a cross-coupled pair. Level shifters as described herein may be formed from stage one **214** resistors R_A **252** and R_B **254**

along with transistor M_4 **232**, and stage two **214** resistors R_A' **256** and R_B' **258** along with transistor M_4' **234**. Transistors M_{2A} **225** and M_{2B} **226** and transistors M_{2A}' **227** and M_{2B}' **228** form an active load for transistors M_{3A} **240** and M_{3B} **242** and transistors M_{3A}' **248** and M_{3B}' **250**, respectively.

An example of some values for transistor sizes and other components for OTA **210** can be found below:

Transistors	Width (μm)	Length (μm)	Resistors	Value
M1A,M1B	240	0.5	RA,RB	100kΩ
M2A,M2B	75	0.5	Rc	6.5kΩ
M3A, M3B	40	0.5	Capacitors	Value
M4	3.5	1	Cc	6pF

FIG. 2B illustrates a symbolic representation of the circuit described above in connection with FIG. 2A. Alternatively, the circuit described in connection with FIG. 2A can be represented more simply as shown in FIG. 1B.

FIG. 3A illustrates another two-stage differential OTA **300** in accordance with certain embodiments of the present invention. OTA **300** consists of first stage circuit **346** cascaded with a similar second stage circuit **348** to obtain a greater DC gain. As may be appreciated by one skilled in the art, additional stages can be added as desired to change the gain as well as other characteristics of the circuit. A two-stage example was chosen to illustrate how additional stages may be added in accordance with certain embodiments of the invention.

In FIG. 3A, the DC output CM voltage may be set to 0.4 Volts at the drains of transistors M_{1A} **310** and M_{1B} **312**, respectively, to bias second stage circuit **348**. Likewise, the DC output CM of second stage circuit **348** may be set to 0.25 Volts to accommodate a maximum output signal swing between ground and the supply (where the supply is 0.5 Volts DC in this example).

Transistors M_{1A} **310** and M_{1B} **312** are a differential pair that amplifies differential inputs V_{in}^+ **314** and V_{in}^- **316**. Devices M_{2A} **318**, M_{2B} **320**, M_{3A} **322**, and M_{3B} **324** (which may be PMOS devices) form an active load and are used to load transistors M_{1A} **310** and M_{1B} **312**. The gates and bodies of devices M_{2A} **318**, M_{2B} **320**, M_{3A} **322**, and M_{3B} **324** are coupled to add their body-source transconductances to the

overall transconductance of the respective transistors, as well as to lower their voltage thresholds V_T.

Devices M_{2A} **318**, M_{2B} **320**, M_{3A} **322**, and M_{3B} **324** may be DC biased at about 0.1 Volts to forward bias the transistor's junction and bring the transistors close to or in moderate inversion during operation. Transistor M_7 **326**, which is coupled to transistors M_{1A} **310** and M_{1B} **312**, may pull a level-shifting current through resistors R_{1A} **328** and R_{1B} **330**. This level-shifting current allows the output voltage to swing into positive and negative values because the output common-mode voltage of the OTA can be set without compromising its inversion level. In this way, resistors R_{1A} **328** and R_{1B} **330** also set the output common-mode voltage at transistors M_{2A} **318** and M_{2B} **320**. Transistors M_{2A} **318** and M_{2B} **320** may also provide local common-mode feedback.

In some embodiments, the bodies of transistors M_{1A} **310** and M_{1B} **312** are biased through the generation of a bias voltage V_{bn} **332**, which is discussed in further detail with reference to FIG. 4 below.

As also shown in FIG. 3A, a common-mode feed-forward (CMFF) cancellation path may be provided through M_{5A} **334**, M_{5B} **336**, M_6 **338**, M_{3A} **322**, and M_{3B} **324** to add an additional load to input transistors M_{1A} **310** and M_{1B} **312**. The gates of M_{5A} **334** and M_{5B} **336** are coupled to the gates of transistors M_{1A} **310** and M_{1B} **312**. As shown, the transistors of the CMFF cancellation path may receive a bias voltage, V_{bn}, at their body terminals to forward bias the transistors. Alternatively, the bodies of the transistors may be coupled to their gates.

As illustrated, a cross-coupled pair, M_4 **340** and M_{4B} **342**, may be used with the differential pair M_{1A} **310** and M_{1B} **312** to decrease the output conductance and increase its DC gain. The body voltage of the cross-coupled pair, V_{NR} **344**, sets the gain of the amplifier. The cross-coupled pair also provides a negative resistance load to the first stage of the amplifier. The amount of negative resistance may be controlled through the bodies of the cross-coupled pair by changing the voltage threshold of transistors M_4 **340** and M_{4B} **342**. The generation of V_{NR} **344** is discussed in further detail with reference to FIG. 5B below.

As illustrated, second stage circuit **348** includes transistors M_{8A} **350**, M_{8B} **352**, M_{11A} **354**, M_{11B} **356**, M_{12A} **358**, M_{12B} **360**, M_{14} **362** M_{9A} **364**, M_{9B} **366**, M_{13} **368**, M_{10A} **370**, and M_{10B} **372**, resistors R_{2A} **374** and R_{2B} **376**. Transistors M_{8A} **350** and M_{8B} **352** form a differential pair, transistors M_{11A} **354** and M_{11B} **356** form a cross-coupled pair, transistors M_{9A} **364** and M_{9B} **366** act as an active load, transistors M_{12A} **358**, M_{12B} **360**, M_{13} **368**, M_{10A} **370**, and M_{10B} **372** form a CMFF cancellation path, and transistor M_{14} **362** and resistors R_{2A} **374** and R_{2B} **376** form a level shifting circuit. These transistors and resistors operate in a similar fashion to the corresponding transistors and resistors of first stage circuit **346** as described herein.

For a CM of 0.25 Volts DC, the gates of devices M_{11A} **354** and M_{11B} **356** are connected to the inputs of the stage. The bodies of devices M_{11A} **354** and M_{11B} **356** may be cross-coupled to boost the differential gain, and devices M_{11A} **354** and M_{11B} **356** may be sized conservatively so that devices M_{11A} **354** and M_{11B} **356** need not be tuned.

Operational Transconductance Amplifier (OTA) **300** may be stabilized with Miller capacitors Cc **378** and series resistors **380** across the second stage.

An example of some values for transistor sizes and other components for the circuit **300** of FIG. 3A can be found below:

First Stage			Second stage		
Transistors	W (μm)	L (μm)	Transistors	W (μm)	L (μm)
M1A,M1B	72	0.36	M8A,M8B	100	0.36
M2A,M2B	270	0.36	M9A,M9B	240	0.36
M3A, M3B	270	0.36	M10A, M10B	240	0.36
M4,M4B	9	0.36	M11A,M11B	25	0.36
M5A,M5B	9	0.36	M12A,M12B	10	0.36
M6	67.5	0.36	M13	48	0.36
M7	64	0.36	M14	32	0.36
Resistors and Capacitors					
R1A,R1B	25 kΩ		R2A,R2B	20 kΩ	
			Rc	2 kΩ	
			Cc	3 pF	

FIG. 4 illustrates bias circuitry **400** for generating V_{bn} and V_L: As shown, this circuitry is formed from portions **420**, **432**, and **434** that generate Vamp, V_{bn}, and V_L, respectively.

Turning to portion **420**, which generates V_{amp}, it can be seen that this portion is made up of resistors **470** and **471**, error amplifiers **411**, **412**, and **413**, capacitor **418**, and resistor **419**. Resistors **470** and **471** form a voltage divider that is used to generate a voltage Vx at node **414**. Error amplifiers **411**, **412**, and **413** are each formed from an inverter configuration of transistors **415** and **416** that amplifies the difference between its input voltage (e.g., Vx at node **414** for amplifier **411**) and the switching threshold voltage of the inverter. In this way, a correction voltage is generated at the output of the inverter. The switching threshold of the inverter is the input voltage at which the inverter may swing from a high output to a low output, and vice-versa. The switching threshold can be set by sizing the transistors in the inverter, and can be modified by changing the voltage threshold of the transistors. In preferred embodiments, the switching threshold may be set to $V_{DD}/2$.

More particularly, error amplifiers **411**, **412**, and **413**, capacitor **418**, and resistor **419** work together as follows. If the switching threshold of error amplifier **411** increases above Vx, the output voltage of error amplifier **411** and input voltage of error amplifier **412** increases, which causes the output voltage of error amplifier **412** and the input of error amplifier **413** to decrease. This then causes the output of error amplifier **413** to increase. Because the body biases of transistors **416** are coupled to the output of error amplifier **413** (i.e., V_{amp}), as V_{amp} increases, the switching threshold decreases. The switching threshold decreases because the voltage at the body of transistors **416** increases, which changes the voltage threshold of each transistor and subsequently its switching threshold. As shown, capacitor **418** and resistor **419** are coupled to the input and output of error amplifier **413** to create a feedback loop that stabilizes the error amplifier's switching threshold voltage. In this way, V_{amp} generating circuit **420** allows the switching threshold to be set, using V_{amp}, independently of variations in process and temperature. V_{amp} is provided to the error amplifiers **460**, **461**, **462**, and **463** in portions **432** and **434** of circuitry **400** so that those error amplifiers will operate independently of process and temperature.

Although illustrated in FIG. 4 as being a single transistor, if desirable transistor **415** may be implemented using two transistors with their drains and sources connected in parallel as shown in FIG. 4, with the drain of one gate connected to node **414**, with the other gate connected to V_{amp}, and with their bodies either floating or connected to ground.

Turning to portion **432** of circuitry **400**, it can be seen that this portion is made up of OTA **426**, error amplifiers **460** and **461**, and capacitor **462**. OTA **426** is preferably a replica of an OTA which circuitry **400** is being used to bias. As shown, the input to OTA **426** is a reference voltage of 0.4 Volts. Error amplifier **460** compares the output of OTA **426** to a reference voltage of 0.25 Volts. Error amplifier **461** similarly compares the output of error amplifier **460** to a reference voltage of 0.25 Volts. The output of error amplifier **461** (i.e., V_{bn}) is then coupled back to the bias input of OTA **426**. Capacitor **462** is coupled between the inverting input and the output of error amplifier **461** to stabilize V_{bn}. In this way, a bias voltage (i.e., V_{bn}) is generated that causes the output of OTA **426** to equal 0.25 Volts. This bias voltage can then be used to control the operation of other OTAs independently of process and temperature. For example, using this bias voltage, the bodies of transistors M_{1A} **310** and M_{1B} **312** (FIG. 3A) may be placed in forward bias and their voltage thresholds lowered so that OTA **300** can function with a supply voltage of less than 1 Volt.

Turning to portion **434** of circuitry **400**, it can be seen that this portion is made up of resistors **480** and **481**, transistor **442**, error amplifiers **462** and **463**, and capacitor **482**. As illustrated, resistors **480** and **481** and transistor **442** create a variable voltage V_Z at the node between resistors **480** and **481** based upon the signal, V_L, generated at the gate and body of transistor **442**. This variable voltage is then provided to the inverting input of error amplifier **462**. Error amplifier **462** compares this voltage to a voltage reference of 0.25 Volts. Error amplifier **462** similarly compares the output of error amplifier **462** to a voltage reference of 0.25 Volts. The output of error amplifier **463** then drives the signal, V_L, provided to the gate and body of transistor **442**. Capacitor **482** is coupled between the inverting input and output of error amplifier **463** to stabilize V_L. In this way, a control voltage (i.e., V_L) can be provided to establish when an IR (i.e., voltage) drop occurs and transfer the drop with

an appropriate ratio to level shifters M_7 **326**, R_{1A} **328**, R_{1B} **330** and M_{14} **358**, R_{2A} **360**, R_{2B} **362** (FIG. 3A) independently of process and temperature.

Referring back to FIG. 3A, it can be seen that body voltage V_{NR} **344** at the bodies of transistors M_4 **340** and M_{4B} **342** can be used to determine the amplifier gain. If the current drawn by transistors M_4 **340** or M_{4B} **342** is too large, OTA **300** may develop a hysteresis (i.e., where changes in the input may not produce the expected change in the output until the change becomes large and there is a sudden jump in the output to the expected value). The hysteresis may cause OTA **300** to behave like a Schmitt-trigger.

FIG. 5 illustrates the DC transfer characteristics that may be realized with an operational transconductance amplifier **300** as illustrated in FIG. 3A. As shown, when the transconductance gain of transistor M_4 **340** or M_{4B} **342**, g_{m4}, increases, the gain lines may approach a slope of infinity, and split (i.e., gain lines with increasing values and decreasing values have different values along the x-axis for the same values on the y-axis). This hysteresis behavior of OTA **300** may be undesirable.

In order to address this situation, a Schmitt-trigger oscillator (or bistable multi-vibrator) **500**, as shown in FIG. 5B, may be used to control the transconductance of the cross-coupled pair of the OTA and prevent this hysteresis behavior. As illustrated, oscillator **500** includes a replica OTA **502** (which is a replica of an OTA that this circuit is being used to control), resistors **504**, **506**, and **508**, capacitors **510**, **512**, and **514**, and XNOR gate **516**. Schmitt-trigger oscillator **500** oscillates at a frequency given by $f_0 = 1/(2RC)\cdot 1/\ln((1+\beta)/(1-\beta))$, where $\beta = V_{hyst}/V_{HL}$, and where V_{hyst} may be the difference between the trigger voltages for the rising and falling cases, and where V_{HL} is the difference between the high and low outputs. The onset of oscillation may be detected in Schmitt-trigger oscillator **500** through an XNOR gate **516**.

XNOR gate **516** has an output that decreases when oscillations are present. Therefore, if the oscillator amplitude increases, V_{NR} is reduced, and, when the oscillator amplitude decreases, V_{NR} is increased. In practice, because the determined V_{NR} may cause oscillations in Schmitt-trigger oscillator **500** that are too fast for XNOR gate **516** to respond, a feedback loop **518** may be used to keep these

unintended oscillations down. The resulting V_{NR} may be reduced through a gain less than, but close to, one, and applied to an OTA to keep the small-signal gain positive in the OTA.

FIG. 3B illustrates a circuit **390** including the OTA **300** described above in connection with FIG. 3A along with resistors R_b **392**, R_f **394** and R_i **396**. As shown, resistors **392** may be used without affecting the overall gain of operational transconductance amplifier (OTA) **300**, if $R_f << A\cdot(R_i \parallel R_f \parallel R_b)$ where R_i is the value of resistors **396**, R_f is the value of resistors **394**, R_b is the value of resistors **392**, and A is the open-loop DC gain of the amplifier. For example, if V_{DD} is 0.5 Volts and the input and output of OTA **300** are 0.25 Volts, to push $V_{cm,vg}$ to 0.4 Volts, $R_b = 2/3\cdot(R_1 \parallel R_2)$. The output common-mode level, $V_{cm,o}$, may be set to $V_{DD}/2$ so the output voltage signal may swing about the same magnitude in either direction. In certain embodiments, where more than one stage is used in the circuit design, the $V_{cm,o}$ of the previous stage, may drive the input of the next stage. Resistors **392** can also be replaced by current sources implemented with transistors -- see, e.g., K. Bult, "Analog Design In Deep Sub-Micron CMOS," Proceedings European Solid-State Circuits Conference (ESSCIRC), September 2000, pp. 11–17, and S. Karthikeyan, S. Mortezapour, A. Tammineedi, and E. Lee, "Low Voltage Analog Circuit Design Based On Biased Inverting Opamp Configuration," IEEE Trans. Circuits Syst. II, vol. 47, no. 3, pp. 176–184, March 2000, which are hereby incorporated by reference herein in their entireties.

FIG. 6 illustrates a low-voltage tunable damped integrator **610** in accordance with certain embodiments of the present invention. As shown, integrator **610** includes an OTA **626**, which may be identical to the first stage of the OTA described above in connection with FIG. 3A. In order to turn on the gate-input devices of OTA **626** when the CM voltages of integrator **610** inputs (V_{in}^- **612** and V_{in}^+ **614**) and outputs (V_{out}^+ **616** and V_{out}^- **618**) are both $V_{DD}/2$ (i.e., 0.25 Volts), a common level virtual ground $V_{cm,vg}$ across the inputs of OTA **626** may be manipulated. Such a common level virtual ground may be maintained by supply resistors **622** to V_{DD} (i.e., 0.5 Volts) at the inputs of OTA **626**. Supply resistors **622** may be used without affecting the overall gain of integrator **610**, if $R_2 << A\cdot(R_1 \parallel R_2 \parallel R_b)$ as mentioned above in connection with FIG. 1B. The output common-mode level, $V_{cm,o}$, may be set to $V_{DD}/2$

so the output voltage signal may swing about the same magnitude in either direction. In certain embodiments, where more than one stage is used in the circuit design, the $V_{cm,o}$ of the previous stage, may drive the input of the next stage.

The tuning capacitors may be able to compensate for possible manufacturing variations in the transistors within integrator **610**. As shown, transistors **628** and **640** may be used as tunable capacitances between gate node **630** and source/drain node **632** and gate node **638** and source/drain node **642**, respectively. Gate nodes **630** and **638** are at 0.4 Volts and source/drain nodes **632** and **642** are at 0.25 Volts with the capacitance being tuned through the body voltage of transistors **628** and **640** (i.e., V_{tune}). Fixed shunt capacitors, C_{fixed} **636**, across OTA **626** may reduce the voltage dependence and improve the density of integrator **610**. For example, if C_{fixed} **636** is a 1 pF capacitor, the tuning range of transistors **628** and **640** may be from 0.8 pF to 1.2 pF for a tune voltage from 0 to 0.5 Volts.

FIG. 7 illustrates, on a block diagram level, how an integrated fifth-order, low-pass, elliptic filter **700** may implemented in accordance with certain embodiments of the invention. As shown integrated filter **700** may include elliptic filter **710**, voltage controlled oscillator **712**, XOR gate **714**, filter **716**, biasing circuitry **718**, **720**, **722**, and **726**, and resistors **732** and **734**.

Fifth-order low-pass filter **700** may be constructed using a combination of the techniques discussed earlier, for example, using tunable capacitors, low-voltage OTAs, and a multiple stage amplifier design. Low-pass filter **710** may be implemented as described below in connection with FIG. 8A. Voltage-controlled oscillator **712** may be implemented as described below in connection with FIG. 8B. A phase lock loop (PLL) including VCO **712**, an XOR gate **714**, and an external loop filter **716** is used to tune filter **710**, thereby changing the operating characteristics. XOR gate **714** is used as a phase detector by comparing the output of VCO **712** with the output of another clock. The output of XOR **714** may be filtered by external loop filter **716**. Error amplifier biasing circuitry **718** may be used to generate V_{amp} for V_L biasing circuitry **720** and V_{bn} circuitry **722,** which all may be constructed as set forth above in connection with FIG. 4. The V_L biasing circuitry may generate a level shifting voltage V_L that is used by the OTAs in V_{bn} circuitry **722** and V_{NR} circuitry **726**, which may be constructed as set forth above in connection with FIG. 4 and FIG.

5B, respectively. As shown, V_{bn} circuitry **722** may use a V_{ref} of 0.4 Volts and generate a V_{bn} used to forward bias certain transistors in the low-voltage circuit as described above. V_{NR} circuitry **726** may use V_{bn}, V_L, R_1 **732**, and R_2 **734** to generate V_{NR} as shown in FIGS. 3 and 5B.

FIG. 8A illustrates low-voltage fifth order low-pass elliptic filter **710** in accordance with certain embodiments of the present invention. As shown, filter **710** is composed of five OTAs **810**, **812**, **814**, **816**, and **818**. These OTAs may be substantially identical to the OTA illustrated in connection with FIG. 3A. Each OTA may additionally use V_{tune}, V_{neg}, V_{bn}, and V_L (not shown in FIG. 8A) as provided by supporting circuitry shown in FIG. 7 and discussed in connection with FIGS. 3, 4 and 5B. Filter **710** is designed with multiple resistors and capacitors as known in the art to achieve the desired operational characteristics.

An example of some values for transistor sizes and other components for the circuit **710** of FIG. 8A can be found below:

Resistors	Value (kΩ)	Capacitors	Value (pF)
R	300	C1	9.2
R1	30	C2	13.1
R2	50	C3	20.2
R3	40	C4	8.8
R4	66.7	C5	5.3
R5	57.2	C6	1.8
		C7	5.7
		C8	2.9

FIG. 8B illustrates an embodiment of a low-voltage, voltage-controlled oscillator (VCO) **712** in accordance with certain embodiments of the present invention. As shown, VCO **712** may be constructed using tunable integrators formed from OTAs **820**, **822**, and **824** (as described herein) and resistors R_a **826**, R_b **828**, R_{VDD} **830**, and capacitors C_a **838** matched to those in the filter with which the VCO is being used (e.g., the filter described above in connection with FIG. 8A). The oscillator frequency, f_0, is chosen to be close to the second zero of the filter, 280 kHz. The OTAs have enough gain-bandwidth to set a phase lag of 60 degrees per stage

along with the required gain of greater than 1, at f_0, to reliably sustain oscillations. The oscillator has a nominal frequency of oscillation given by:

$$f_0 = \frac{\sqrt{3}}{2\pi R_a C_a}$$

and oscillations are possible only when $R_a \geq 2R_b$. For example, the following values may be used in certain embodiments of the invention: R_a = 427 kΩ; R_b = 207 kΩ; R_{VDD} = 93 kΩ; and Ca = 2.3 pF.

FIG. 9 is an illustration of a track-and-hold circuit **910** implemented using an Operational Transconductance Amplifier (OTA) **912** in accordance with certain embodiments of the present invention. OTA **912** may be implemented using the OTA described above in connection with FIG. 3A. As previously described herein, OTA **912** may be designed to have a high gain for an input common-mode voltage of 0.4 Volts and an output common-mode voltage of 0.25 Volts. At terminals V_{in}^- **914** and V_{in}^+ **916**, the common-mode is 0.25 Volts. R_1 **918**, R_2 **920**, and R_3 **922** may be sized so as to provide a bias voltage of 0.4 Volts at node **924** and node **926** for some embodiments of this circuit. Selections of these resistors are described above in connection with FIG. 1B. Other bias voltages may be used in different implementations of this circuit. In order to implement the circuit with unity gain, R_1 **918** and R_2 **920** may be equally sized. Alternatively, R_1 **918** and R_2 **920** can be sized differently to provide non-unity gain in the circuit. Thus, for example, R_1 **918** and R_2 **920** may be equally sized, and R_3 **922** may be one-third the size of R_1 **918** and R_2 **920** in the circuit illustrated.

Capacitor C_1 **928** may be sized such that capacitors C_1 **928** and C_2 **930** and resistors R_1 **918** and R_2 **920**, maintain the relation $R_1C_1 = R_2C_2$. This relation allows a pole introduced by R_2 **920** and C_2 **930** to be cancelled by a zero introduced by R_1 **918** and C_1 **928**. C_2 **930** may be sized as large as possible given the size of the OTA **912** and the speed and noise requirements of circuit **910**.

Although specific examples of component requirements are set forth above, these requirements may be altered to implement different embodiments of this circuit. For example, with a different embodiment of OTA **912**, other voltage levels may be

appropriate. As with previously mentioned embodiments of OTAs, OTA **912** may use tuning and biasing circuitry as shown in FIG. 4.

In operation, circuit **910** may track a voltage presented at inputs **914** and **916** or hold a voltage for a time. When M_1 **932** is closed and M_2 **934** is open, the circuit may track at terminals V_{out}^- **936** and V_{out}^+ **938** the voltages at terminals V_{in}^- **914** and V_{in}^+ **916**. When M_2 **934** is closed and M_1 **932** is open, the circuit may hold the last voltage tracked at terminals V_{in}^- **914** and V_{in}^+ **916**. M_1 **932** and M_2 **934** should not be closed at the same time. Transistors M1 **932**, M2 **934**, **940**, and **942** may have a gate to body coupling to lower the voltage threshold and to operate the gates closer to moderate inversion. In some embodiments, sample-and-hold architecture **910** may be extended to develop a pipelined Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) or may be the first stage in a switched-operational amplifier realization of a switched-capacitor circuit.

FIG. 10 illustrates a gate-input operational transconductance amplifier **1010** with intrinsic common-mode rejection. The first stage of OTA **1010** uses PMOS input transistors M_1 **1012** and M_2 **1014** that form a differential pair and that operate with a DC common-mode input of 0.1 Volts. The signal common-mode (not shown) is $V_{DD}/2$ (i.e., 0.25 Volts). The difference between the signal common-mode and the DC common-mode input (i.e., the virtual ground) is maintained by the resistor technique shown in FIG. 1B where OTA **100** is replaced by OTA **1010**. As illustrated, level-shifting and common-mode biasing techniques are used similarly to that described above. The output common-mode of OTA **1010** is set to 0.1 Volts to ensure proper biasing of the outputs connected to transistors M_7 **1016** and M_8 **1018**. Transistors M_3 **1020** and M_4 **1022** form active loads that act as current source loads for the differential-mode signal. Resistors Rc **1024** detect the output common-mode voltage of the stage and feed it back to the gates of transistors M_3 **1020** and M_4 **1022** so that transistors M_3 **1020** and M_4 **1022** are diode connected for common-mode signals. The cross-coupled transistors M_5 **1026** and M_6 **1028** act as differential negative resistance loads to improve the DC gain. For common-mode signals, transistors M_5 **1026** and M_6 **1028** are diode connected. A bias voltage Vc1 **1030** to the bodies of input transistors M_1 **1012** and M_2 **1014** is used to control the DC output common-mode level as discussed above in connection with the OTA of FIG. 3A.

As shown, transistors M_3 **1020**, M_4 **1022**, M_5 **1026**, and M_6 **1028** are body-gate coupled so that the body transconductances of the transistors add to their gate transconductances. The resulting forward bias on the source-body junction reduces the voltage threshold and raises the inversion level of the device to being close to moderate inversion.

The DC current ibias1 may be generated in a similar manner to that shown in FIG. 4 for V_L. As illustrated, ibias1 is used to create a voltage shift across resistors Rc **1024** to bias the gate of M_3 **1020** and M_4 **1022**.

The DC gains in differential-mode, A_{diff}, and in common-mode, A_{cm}, for one stage may be given by:

$$A_{diff} = \frac{g_{m1}}{[g_{ds1} + g_{ds3} + g_{ds5} + 1/R_1 - (g_{m5} + g_{mb5})]}$$

$$A_{cm} = \frac{g_{m1}}{[g_{m3} + g_{mb3} + g_{m5} + g_{mb5} + g_{ds1} + g_{ds3} + g_{ds5}]}$$

where g_{mi}, g_{mbi}, and g_{dsi} denote the transconductance, body transconductance and output conductance of device M_i respectively. Transconductance g_{m3} is usually larger than transconductance g_{m1} by a factor close to the electron hole mobility ratio, typically about two to three, when M_3 **1020** and M_4 **1022** operate at the about the same current level as M_1 **1012** and M_2 **1014**. The common-mode gain, A_{cm}, which is typically intrinsically smaller than one, is reduced due to loading by the output conductances and transconductances of M_5 **1026** and M_6 **1028**.

The negative differential conductance in M_5 **1026** and M_6 **1028** may be conservatively sized such that it cancels out 60 percent of the output conductance and provides a DC gain boost around 8 dB. Alternatively, the body terminals of M_5 **1026** and M_6 **1028** can be connected to a body voltage, V_{NR}, as described above in connection with transistors M_{4A} **340** and M_{4B} **342** of FIG. 3A and as described in FIGS. 5A and 5B.

As shown in FIG. 10, stage two of OTA **1010** has a similar topology to that the first stage. In fact, transistors M_9 **1036**, M_{10} **1038**, M_{11} **1040**, and M_{12} **1042** operate in a similar manner to transistors M3 **1020**, M4 **1022**, M5 **1026**, and M6 **1028**. Some differences between the two stages may include the output common-mode voltage and the biasing chosen for Vc2 **1044** and ibias2 **1046**. For example, stage two biasing may be different than stage one biasing when certain operational characteristics are desired. In between the two stages, Miller compensation may be used. Series resistors Rz **1050** for the capacitors Cc **1048** may further be used to move the zero due to Cc **1048** to improve the phase margin and stability.

An example of some values for transistor sizes and other components for the circuit of FIG. 10 can be found below:

First Stage			Second stage		
Transistors	W (μm)	L (nm)	Transistors	W (μm)	L (nm)
M1	388	500	M1	388	500
M2	388	500	M2	388	500
M3	388	500	M3	388	500
M4	388	500	M4	388	500
M5	12	500	M5	240	500
M6	12	500	M6	240	500
Resistors and Capacitors			Currents		
Rc	33 kΩ		ibais1	12.75 uA	
Rz	4 kΩ		ibais2	3 uA	
Cc	3.1 pF				

FIGS. 11A and 11B illustrate third-order, continuous-time sigma-delta (ΣΔ) modulators **1110** and **1140** in accordance with certain embodiments of the present invention. ΣΔ modulators **1110** and **1140** are implemented in a fully differential form with active RC integrators.

As shown, modulator **1110** includes OTAs **1101**, **1102**, **1103**, clocked comparator **1104**, digital-to-analog converters (DACs) **1105**, resistors **1111**, **1112**, **1121**, **1122**, **1131**, and **1132**, and capacitors **1113**, **1123**, and **1133**. Modulator **1140** includes OTAs **1101**, **1102**, **1103**, clocked comparator **1104**, digital-to-analog converters (DACs) **1141**, resistors **1111**, **1112**, **1121**, **1122**, **1131**, and **1132**, and capacitors **1113**, **1123**, and **1133**.

OTAs **1101**, **1102**, and **1103** may be implemented using a body-input, two-stage OTA with Miller compensation. Such an OTA is illustrated, for example, in connection with FIG. 2A above. OTAs **1101**, **1102**, and **1103** may additionally or alternatively be implemented using any other suitable OTAs, such as those described in connection with FIGS. 1 and 3A.

The ratios of the resistors coupled to each amplifier (e.g., R_{1a} **1111** / R_{1b} **1112** for error amplifier **1101**) represent the modulator coefficients. The modulator coefficients may be obtained from a discrete-time prototype modulator through an impulse-invariant transformation with the feedback DAC waveform being taken into account, for example as described in James A. Cherry and W. Martin Snelgrove, "Excess Loop Delay in Continuous-Time Delta–Sigma Modulators", IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, vol. 46, no. 4, pp.376-389, April 1999, which is hereby incorporated by reference herein in its entirety.

In some embodiments, the component values shown in the following table may be used. These component values have been selected for a signal bandwidth of 25 KHz, which is suitable for audio applications. Preferably, high–resistivity polysilicon layer resistors and metal-insulator-metal (MIM) capacitors are used. Obviously, other values and types of resistors and capacitors could be used in accordance with the invention.

Component	Value	Component	Value
R_{1a}	275 kΩ	R_{3b}	93 kΩ
R_{1b}	86 kΩ	C_1	31.25 pF
R_{2a}	88 kΩ	C_2	7.8 pF
R_{2b}	145 kΩ	C_3	5.2 pf
R_{3a}	66 kΩ		

In some embodiments of the present invention, pulse shaping and time delay are used to modify performance of ΣΔ modulators **1110** and **1140**. Return-to-zero pulse shaping (i.e., the output of DACs **1105** and **1141** in the modulators are cleared after certain clock cycles) is used to avoid inter-symbol-interference (or the memory

effect) that can exist in continuous-time ΣΔ modulators. A ten percent time delay (or any other suitable delay) on the DAC waveforms may be used to minimize the effect of parasitic loop delays and to allow the comparator outputs to fully settle.

More particularly, a return-to-open technique may be used to implement return-to-zero pulse shaping in accordance with the present invention. This technique leaves the outputs of the DACs floating (or open-circuited). Because the DAC outputs are open-circuited, current will not flow to the integrating capacitors C_1 **1113**, C_2 **1123**, and C_3 **1133** from the DACs. Rather, during the floating intervals, the DAC output voltages are pulled either down or up, through the resistors to the amplifier's input level, which is set in some embodiments to $V_{DD}/2$.

FIGS. 12A and 12B illustrate DACPs **1105** and **1106** and DACNs **1141** and **1142**, respectively, which implement the return-to-open technique, in accordance with certain embodiments of the present invention. As shown, these DACs include transistors **1216**, **1218**, **1220**, **1222**, **1230**, **1232**, and **1234**. The body terminals of these transistors are biased at 0.25 Volts. The reference voltages (i.e., the positive and negative rails) are 0.5 Volts and 0 Volts. In other embodiments, different biasing and reference voltages may be appropriate for operation of the circuits.

The operation of the DACs is described as follows. A clock input φ is provided to the gates of transistors **1220**, **1222**, and **1234**. Transistors **1216**, **1218**, and **1220** form a tri-state buffer. When the clock φ is low transistor **1220** turns off, and node **1224** is reset to 0.5 Volts by transistor **1222**. When the clock φ is high, node **1224** may be coupled to 0.5 Volts or 0 Volts depending on the value of the input and the corresponding states of transistors **1216** and **1218**. .

As shown in FIG. 12A, the signal at node **1224** is buffered by buffer stage **1236**. Thus, when clock φ is low, transistor **1234** turns off and causes the output to float. When clock φ is high, the output buffers the signal at node **1224**.

As shown in FIG. 12B, in some embodiments, a split-buffering technique may be used with ΣΔ modulators to avoid inter-stage signal coupling. In modulator **1100**, when one buffer is used, the internal signals of the integrators may couple at the outputs of the DACs and thereby degrade the performance of the modulator. With a

split-buffer approach, buffers **1236**, **1238**, and **1240** of FIG. 12B are used to separate each integrator and to avoid coupling, as shown in FIG. 11B.

Although FIGS. 11B and 12B illustrate DACs with multiple outputs, multiple DACs each with a single output that are connected to the same comparator may also be used to implement this aspect of the present invention. Also, although the DACs in FIGS. 12A and 12B are illustrated as incorporating circuitry for creating a high impedance between (i) the DACs and (ii) the capacitors and OTAs as illustrated herein, this high impedance could be created by any suitable circuitry between these points.

In some embodiments, a low jitter external clock may be used and an internal circuit may generate different phases of the clock if the continuous-time modulator is sensitive to clock jitter in the return-to-open circuit.

Comparator **1104** in continuous-time ΣΔ modulators **1110** and **1140** serves two purposes, sampling and comparison, and may be a clocked or a latched comparator. FIG. 13 illustrates one embodiment of a comparator **1104** that may be used in accordance with certain embodiments of the present invention. As shown, comparator **1104** consists of two stages, namely pre-amplifier **1312** and latch **1314**. Both stages use the body terminals as inputs. In certain embodiments, because the bodies of both PMOS and NMOS transistors are used to pass signals in both stages, a CMOS process with both n-well and p-well, or a triple-well option, may be used.

As illustrated, pre-amplifier **1312** includes clock signal φ, inverse clock signal $\overline{\varphi}$, and transistors **1320**, **1322**, **1324**, and **1326**. The gates of transistors **1320** and **1322** are coupled to clock signal φ, while the gates of transistors **1324** and **1326** are coupled to inverse clock signal $\overline{\varphi}$. As shown, transistors **1320** and **1322** form a differential pair and transistors **1324** and **1326** form an active load. In operation when clock φ is low, transistors **1320** and **1322** turn on and amplify the input. The amplified signal may then be stored in the parasitic capacitors at the output nodes. When clock φ is high, transistors **1320** and **1322** turn off and transistors **1324** and **1326** turn on. Transistors **1324** and **1326** have their body terminal connected to ground.

Latch **1314** includes clock signal φ, inverse clock signal $\overline{\varphi}$, transistors **1328** and **1330** (which form a cross-coupled pair), and transistors **1332** and **1334** (which form a cross-coupled pair). When clock φ is high, cross-coupled transistors **1328** and **1330** turn on and the input signal is latched. When clock φ is low, transistors **1328** and **1330** turn off and transistors **1332** and **1334** turn on, which allows for a new input signal to be latched. Latch **1314** may be a regenerative circuit whose speed is proportional to the Gm of the transistors used in latch **1314** and a load capacitor (not shown).

Other embodiments, extensions, and modifications of the ideas presented above are comprehended and within the reach of one versed in the art upon reviewing the present disclosure. Accordingly, the scope of the present invention in its various aspects should not be limited by the examples and embodiments presented above. The individual aspects of the present invention, and the entirety of the invention should be regarded so as to allow for such design modifications and future developments within the scope of the present disclosure. The present invention is limited only by the claims that follow.

What is claimed is:

1. A digital-to-analog converter (DAC) comprising:

a first PMOS transistor having a gate coupled to an input signal, a source coupled to a first reference voltage, a drain, and a body coupled to a bias voltage;

a first NMOS transistor having a gate coupled to the input signal, a drain coupled to the drain of the first PMOS transistor, a source, and a body coupled to a bias voltage; and

a second NMOS transistor having a gate coupled to a clock signal, a drain coupled to the source of the first NMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

2. The DAC of claim 1, further comprising a second PMOS transistor having a gate coupled to the clock signal, a source coupled to the first reference voltage, a drain coupled to the drain of the first PMOS transistor, and a body coupled to the bias voltage.

3. The DAC of claim 1, further comprising a first buffer, comprising:

a third PMOS transistor having a gate coupled to the drain of the first PMOS transistor, a source coupled to a first reference voltage, an drain, and a body coupled to a bias voltage;

a third NMOS transistor having a gate coupled to the drain of the first PMOS transistor, a drain coupled to the drain of the third PMOS transistor, a source, and a body coupled to a bias voltage; and

a fourth NMOS transistor having a gate coupled to the clock signal, a drain coupled to the source of the third NMOS transistor, an source coupled to a second reference voltage, and a body coupled to a bias voltage.

4. The DAC of claim 3, further comprising a second buffer, comprising:

a fourth PMOS transistor having a gate coupled to the drain of the first PMOS transistor, a source coupled to a first reference voltage, an drain, and a body coupled to a bias voltage;

a fifth NMOS transistor having a gate coupled to the drain of the first PMOS transistor, a drain coupled to the drain of the fourth PMOS transistor, a source, and a body coupled to a bias voltage; and

a sixth NMOS transistor having a gate coupled to the clock signal, a drain coupled to the source of the fifth NMOS transistor, an source coupled to a second reference voltage, and a body coupled to a bias voltage.

5. The DAC of claim 1, wherein the first reference voltage is a half volt and the second reference voltage is zero volts.

6. The DAC of claim 1, wherein the DAC is incorporated in a sigma-delta modulator that implements a return-to-open technique.

7. The DAC of claim 6, wherein the sigma-delta modulator comprises a operational transconductance amplifier, comprising:

an active load;

a differential pair of transistors having a first transistor and a second transistor, each of the first transistor and the second transistor having a source, having a gate coupled to the first input of the OTA, having a body coupled to a bias voltage, and having a drain coupled to the first output of the OTA and the active load; and

a level shift bias circuit that creates a common mode feedback and that is coupled to the drain of the first transistor, the drain of the second transistor, and the active load.

8. A digital-to-analog converter comprising:

a NMOS transistor having a gate coupled to an input signal, a source coupled to a first reference voltage, a drain, and a body coupled to a bias voltage;

a first PMOS transistor having a gate coupled to the input signal, a drain coupled to the drain of the NMOS transistor, a source, and a body coupled to a bias voltage; and

a second PMOS transistor having a gate coupled to a clock signal, a drain coupled to the source of the first PMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

9. The DAC of claim 8, further comprising a second NMOS transistor having a gate coupled to the clock signal, a source coupled to the first reference voltage, a drain coupled to the source of the PMOS transistor, and a body coupled to the bias voltage.

10. The DAC of claim 8, further comprising a first buffer, comprising:

a third NMOS transistor having a gate coupled to the drain of the first NMOS transistor, a source coupled to a first reference voltage, an drain, and a body coupled to a bias voltage;

a third PMOS transistor having a gate coupled to the drain of the first NMOS transistor, a drain coupled to the drain of the third NMOS transistor, a source, and a body coupled to a bias voltage; and

a fourth PMOS transistor having a gate coupled to the clock signal, a drain coupled to the source of the third PMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

11. The DAC of claim 10, further comprising a second buffer, comprising:

a fourth NMOS transistor having a gate coupled to the drain of the first NMOS transistor, a source coupled to a first reference voltage, an drain, and a body coupled to a bias voltage;

a fifth PMOS transistor having a gate coupled to the drain of the first NMOS transistor, a drain coupled to the drain of the fourth NMOS transistor, a source, and a body coupled to a bias voltage; and

a sixth PMOS transistor having a gate coupled to the clock signal, a drain coupled to the source of the fifth PMOS transistor, a source coupled to a second reference voltage, and a body coupled to a bias voltage.

12. The DAC of claim 8, wherein the first reference voltage is a half volt and the second reference voltage is zero volts.

13. The DAC of claim 8, wherein the DAC is incorporated in a sigma-delta modulator that implements a return-to-open technique.

14. The DAC of claim 13, wherein the sigma-delta modulator comprises a operational transconductance amplifier having a first input and a first output, comprising:

an active load;

a differential pair of transistors having a first transistor and a second transistor, each of the first transistor and the second transistor having a source, having a gate coupled to the first input of the OTA, having a body coupled to a bias voltage, and having a drain coupled to the first output of the OTA and the active load; and

a level shift bias circuit that creates a common mode feedback and that is coupled to the drain of the first transistor, the drain of the second transistor, and the active load.

15. A comparator comprising:

a differential pair of transistors, wherein each transistor has a body coupled to an input signal, a gate coupled to a clock signal, a source coupled to a first reference voltage, and a drain;

an active load coupled to the drain of each transistor of the differential pair of transistors;

a first cross-coupled pair of transistors, wherein each transistor has a source coupled to the first reference voltage, a gate coupled to an inverse of the clock signal, and a drain, and wherein the body of one of the transistors of the first cross-coupled pair of transistors is coupled to the drain of the other of the transistors of the first cross-coupled pair of transistors, and the body of the other of the transistors of the first cross-coupled pair of transistors is coupled to the drain of the one of the transistors of the first cross-coupled pair of transistors; and

a second cross-coupled pair of transistors, wherein each transistor has a source coupled to a second first reference voltage, a gate coupled to the clock signal, and a drain coupled to the drains of the first cross-coupled pair of transistors, and wherein the body of one of the transistors of the second cross-coupled pair of transistors is coupled to the drain of the other of the transistors of the second cross-coupled pair of transistors, and the body of the other of the transistors of the second cross-coupled pair of transistors is coupled to the drain of the one of the transistors of the second cross-coupled pair of transistors.

16. The comparator of claim 15, wherein the first reference voltage is a half volt and the second reference voltage is zero volts.

17. The comparator of claim 15, wherein the DAC is incorporated in a sigma-delta modulator that implements a return-to-open technique.

18. The comparator of claim 17, wherein the sigma-delta modulator comprises a operational transconductance amplifier having a first input and a first output, comprising:

an active load;

a differential pair of transistors having a first transistor and a second transistor, each of the first transistor and the second transistor having a source, having a gate coupled to the first input of the OTA, having a body coupled to a bias voltage, and having a drain coupled to the first output of the OTA and the active load; and

a level shift bias circuit that creates a common mode feedback and that is coupled to the drain of the first transistor, the drain of the second transistor, and the active load.

19. A sigma-delta modulator, comprising:

a first operational transconductance amplifier (OTA) having a first input and a first output;

a capacitor coupled having a first side and a second side, wherein the first side is coupled to the first input of the first OTA and the second side is coupled to the first output of the first OTA;

a comparator having an input coupled to the first output of the first OTA, having a clock input coupled to a clock signal, and having an output;

a digital-to-analog converter having an input coupled to the output of the comparator and having an output; and

a resistor having a first side and a second side, wherein the first side is coupled to the output of the digital-to-analog converter and the second side is coupled to the first input of the first OTA and the first side of the capacitor;

wherein the coupling, between (i) the digital-to-analog converter and (ii) the first side of the capacitor and the first input of the first OTA, enters a high impedance state based on the clock signal.

20. The sigma-delta modulator of claim 1, further comprising a second OTA.

21. A sigma-delta modulator, comprising:

a plurality of operational transconductance amplifiers (OTAs), each having a first input and a first output;

a plurality of capacitors, each having a first side and a second side, wherein the first side of each of the plurality of capacitors is coupled to the first input of a corresponding one of the plurality of OTAs and the second side of each of the plurality of capacitors is coupled to the first output of the corresponding one of the plurality of OTAs;

a comparator having an input coupled to the first output of one of the plurality of OTAs, having a clock input coupled to a clock signal, and having an output;

a digital-to-analog converter having an input coupled to the output of the comparator and having a plurality of outputs; and

a plurality of resistors, each coupled between a corresponding one of the plurality of outputs of the digital-to-analog converter and the first input of one of the corresponding plurality of OTAs,

wherein each coupling, between (i) a corresponding one of the plurality of outputs of the digital-to-analog converter and (ii) the first side of the corresponding capacitor and the first input of the corresponding one of the plurality of OTAs, enters a high impedance state based on the clock signal.

22. A sigma-delta modulator, comprising:

a plurality of operational transconductance amplifiers (OTAs), each having a first input and a first output;

a plurality of capacitors, each having a first side and a second side, wherein the first side of each of the plurality of capacitors is coupled to the first input of a corresponding one of the plurality of OTAs and the second side of each of the plurality of capacitors is coupled to the first output of the corresponding one of the plurality of OTAs;

a comparator having an input coupled to the first output of one of the plurality of OTAs, having a clock input coupled to a clock signal, and having an output;

a plurality of digital-to-analog converters, each having an input coupled to the output of the comparator and having an output; and

a plurality of resistors, each coupled between the output of a corresponding one of the plurality of digital-to-analog converters and the first input of one of the corresponding plurality of OTAs,

wherein each coupling, between (i) the output of a corresponding one of the plurality of digital-to-analog converters and (ii) the first side of the corresponding capacitor and the first input of the corresponding one of the plurality of OTAs, enters a high impedance state based on the clock signal.

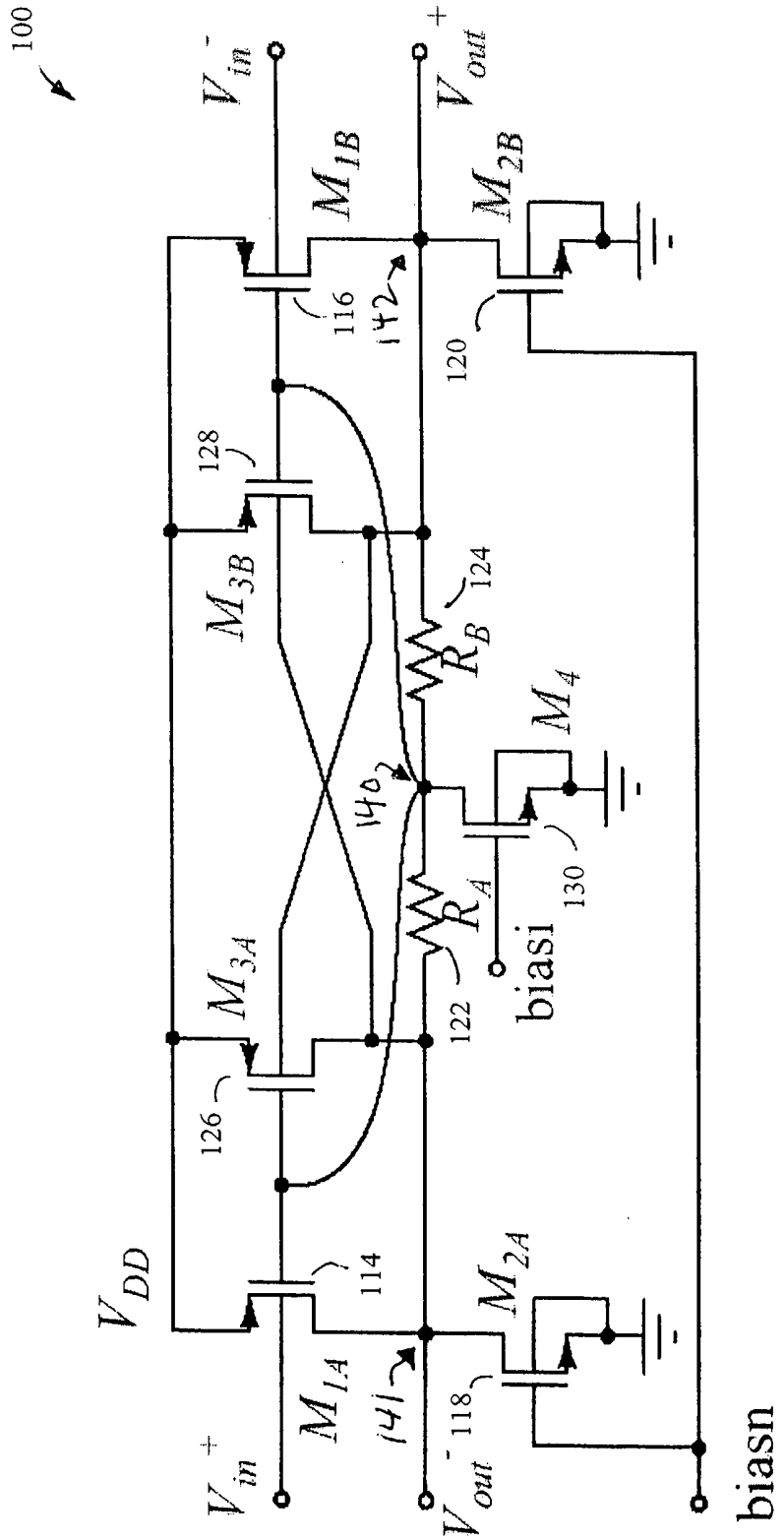

100
V_{in}^-
V_{out}^+
M_{1B}
M_{2B}
116
142
120
128
M_{3B}
124
R_B
M_4
140
130
R_A
biasi
122
M_{3A}
126
V_{DD}
114
M_{2A}
M_{1A}
141
118
V_{in}^+
V_{out}^-
biasn

FIG. 1

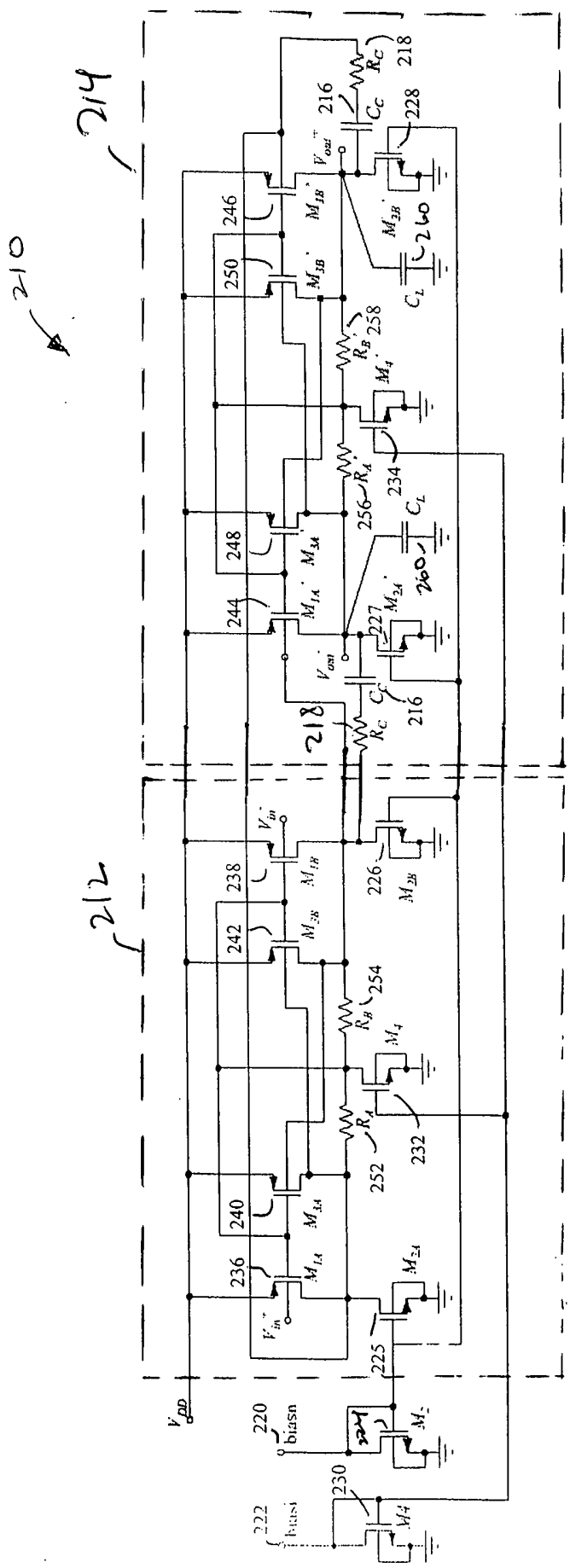

210
214
212
218
216
220
biasn
222
biasp
230
225
226
227
228
232
234
236
238
240
242
244
246
248
250
252
254
256
258
260
240

FIG. 2A

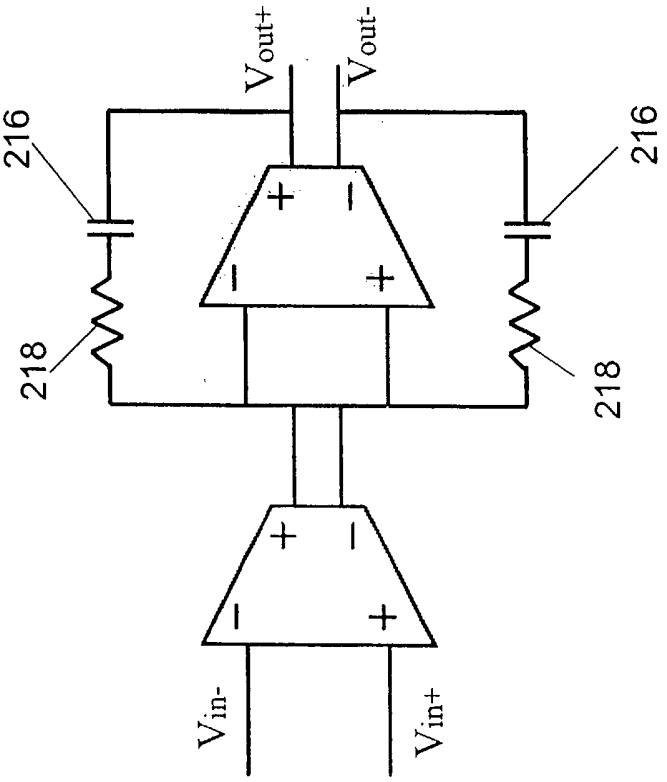


FIG. 2B

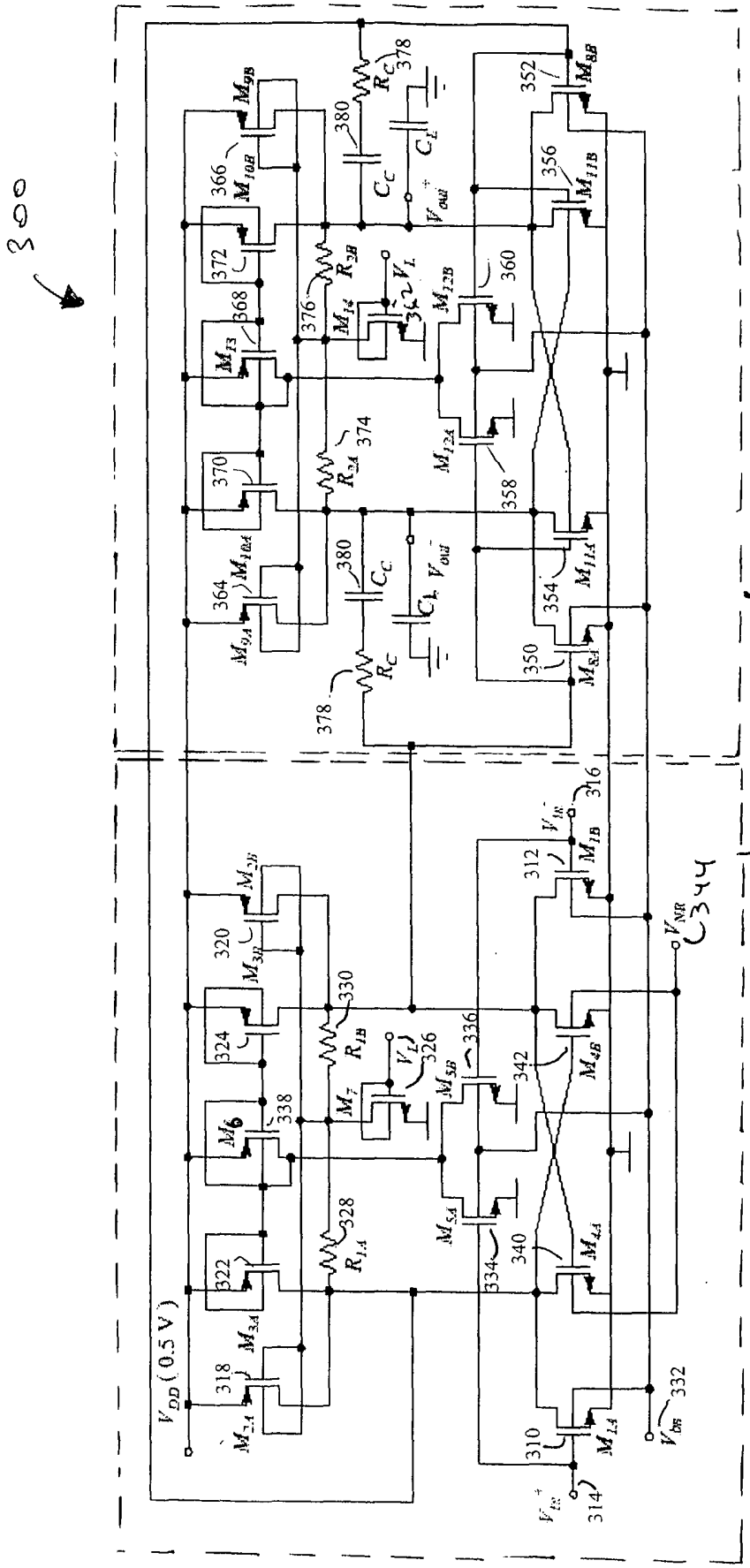

300
348
346
344
V_{DD} (0.5 V)
V_{IP}
V_{IN}
V_{NR}
V_{PR}
V_{OUT}
V_L
C_C
C_L
R_C
R_{1A}
R_{1B}
R_{2A}
R_{2B}
R_{3A}
R_{3B}
R_{4A}
R_{4B}
M_{1A}
M_{1B}
M_{2A}
M_{2B}
M_{3A}
M_{3B}
M_{4A}
M_{4B}
M_5
M_6
M_7
M_8
M_9
M_{10}
M_{11}
M_{12}
M_{13}
M_{14}
310
312
314
316
318
320
322
324
326
328
330
332
334
336
338
340
342
344
346
348
350
352
354
356
358
360
362
364
366
368
370
372
374
376
378
380

FIG. 3A

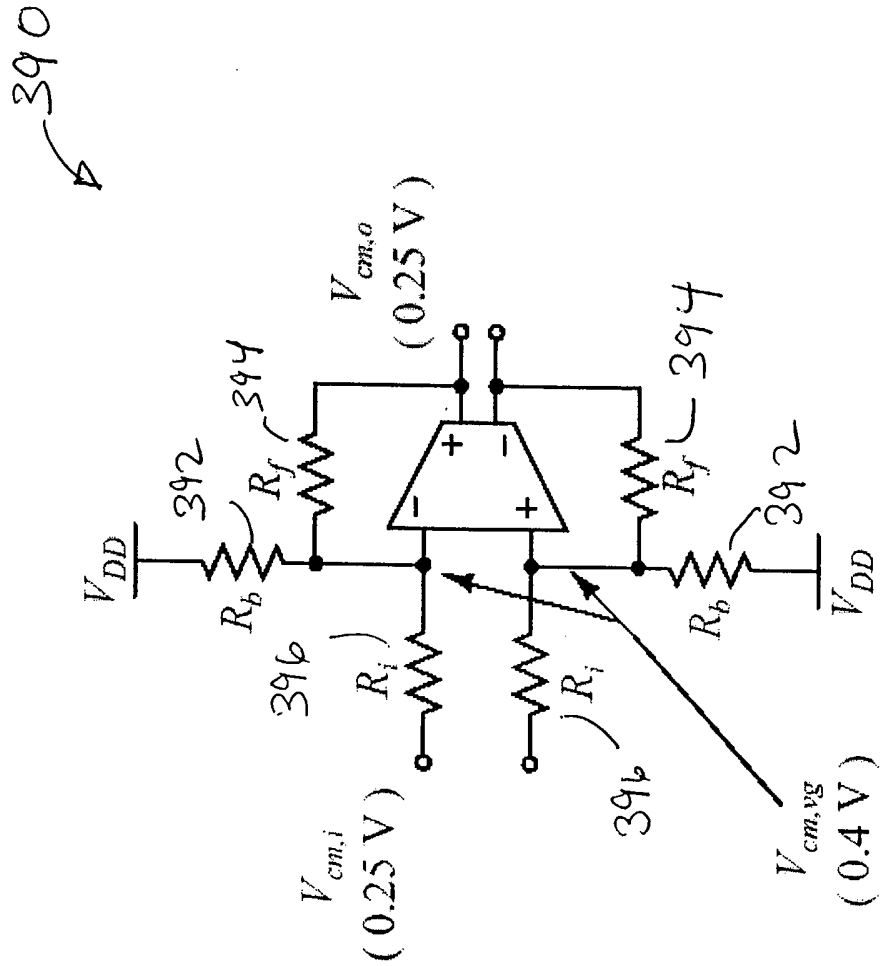


FIG. 3B

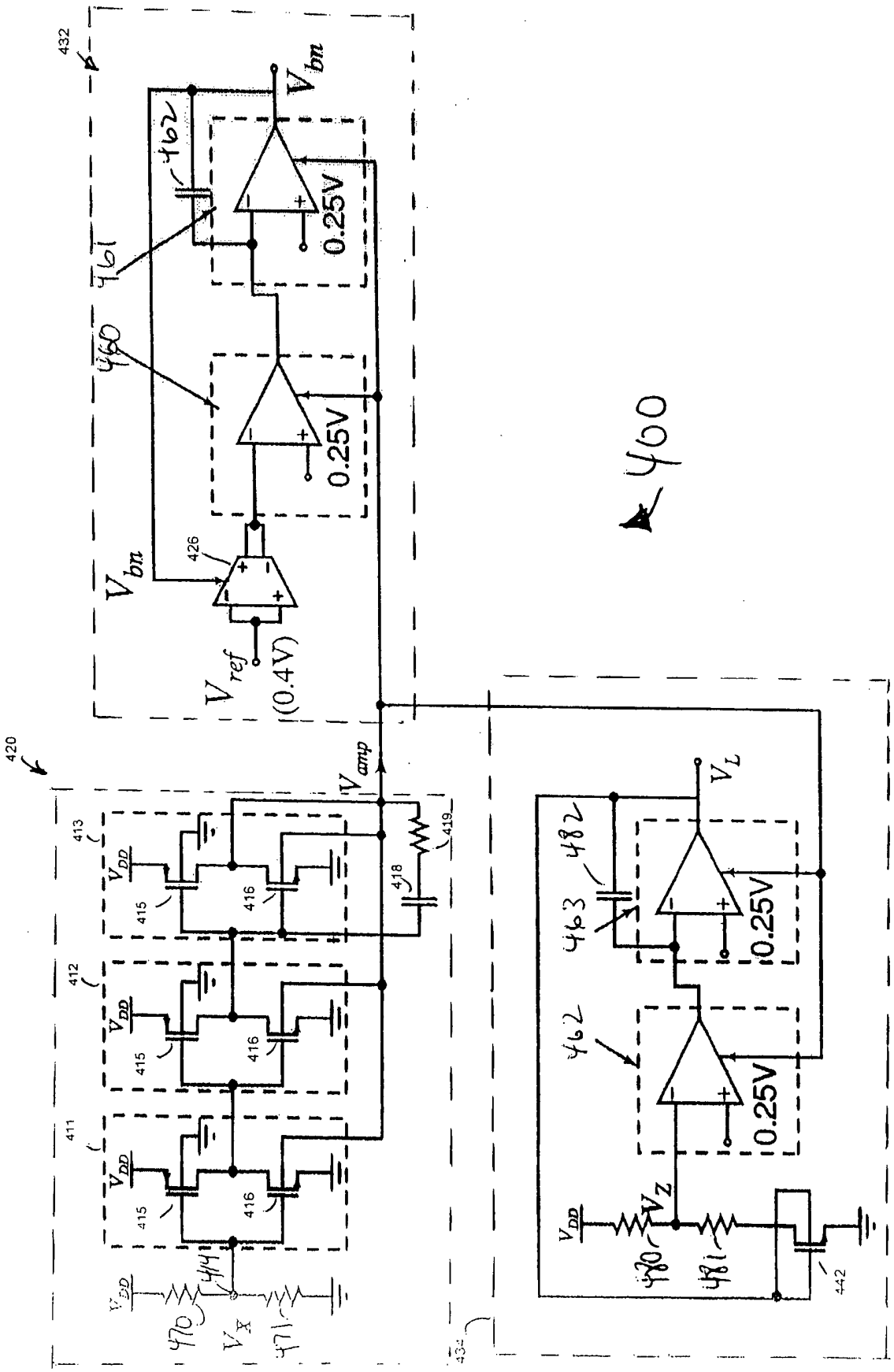

400
420
432
434
V_{bn}
V_{ref}
(0.4V)
V_{amp}
V_L
V_Z
V_X
V_{DD}
0.25V
460
461
462
463
470
471
480
481
482
411
412
413
414
415
416
418
419
426
442

FIG. 4

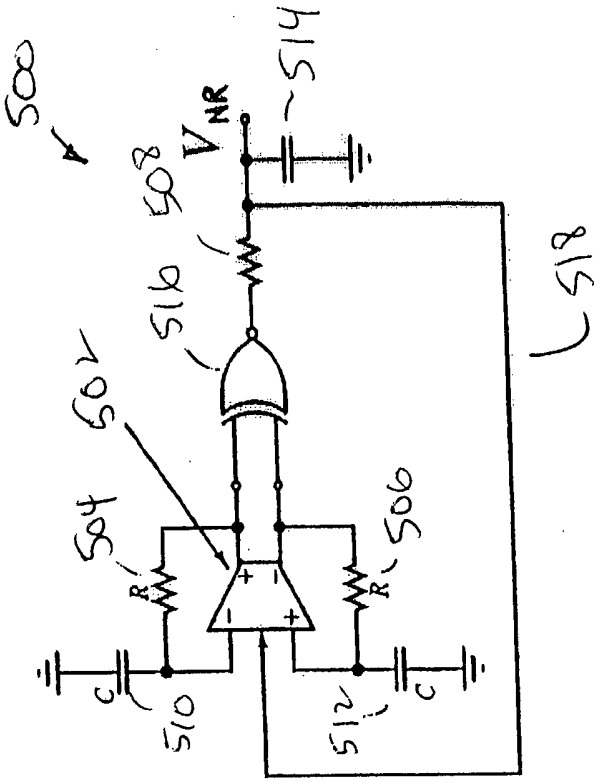

500
502
504
506
508
510
512
514
516
518
V_{NR}
R
C

FIG. 5B

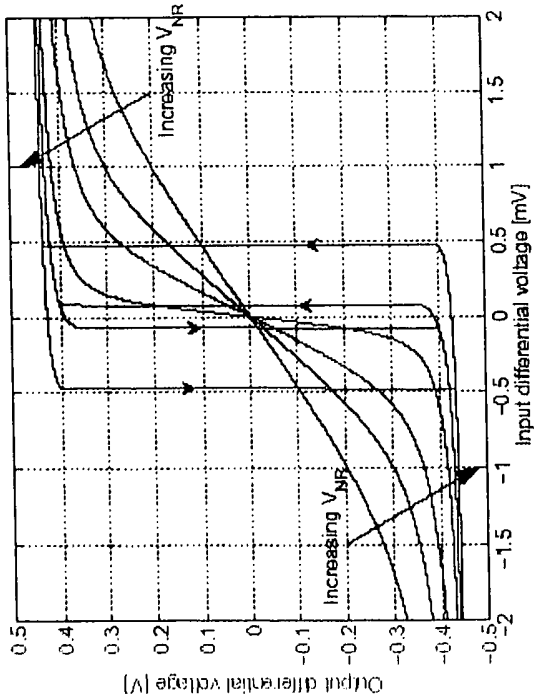

Increasing V_{NR}
Increasing V_{NR}
Output differential voltage [V]
Input differential voltage [mV]
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2

FIG. 5A

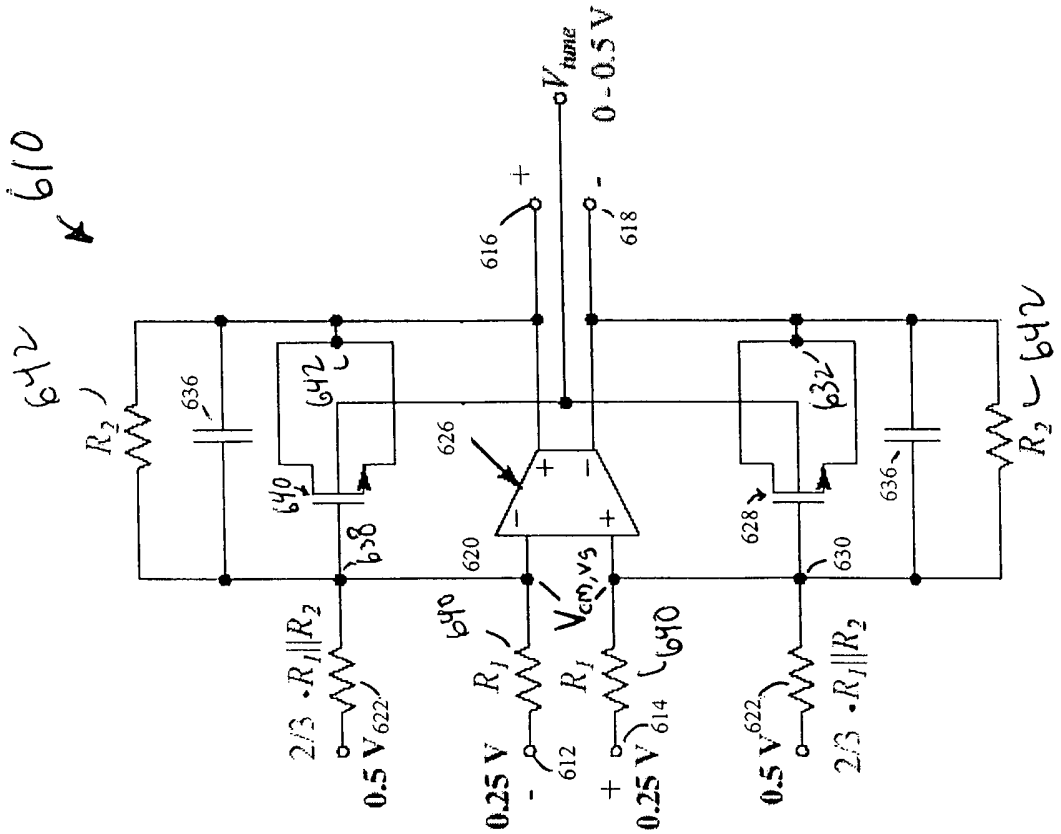

610
642
R_2
636
642
640
638
626
620
616
618
V_{tune}
0 - 0.5 V
632
628
630
636
642
R_2
$2/3 \cdot R_1 || R_2$
0.5 V 622
640
R_1
0.25 V
612
$V_{cm,vs}$
R_1
640
0.25 V 614
0.5 V 622
$2/3 \cdot R_1 || R_2$

FIG. 6

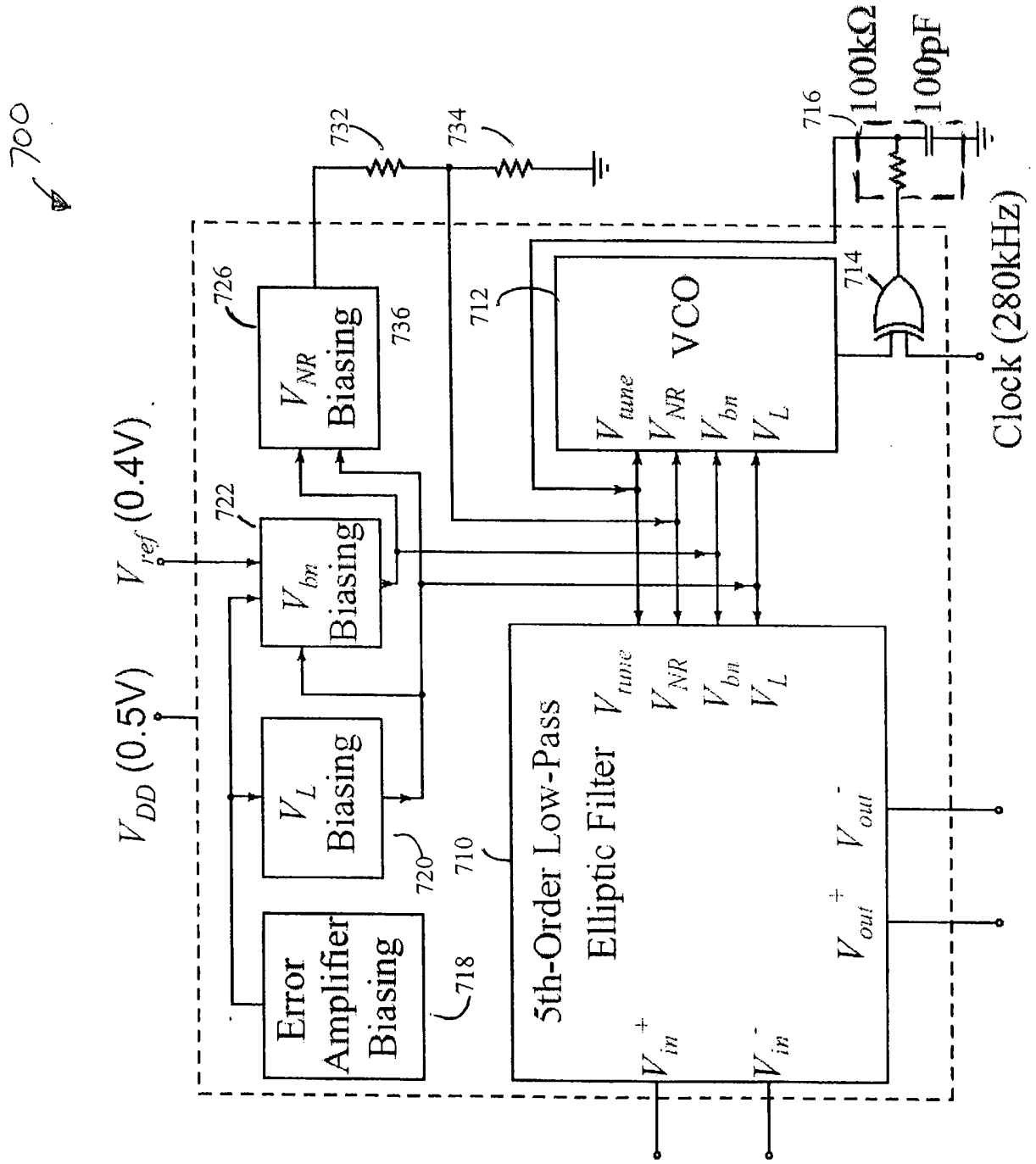

700
V_{DD} (0.5V)
V_{ref} (0.4V)
722
V_{bn} Biasing
726
V_{NR} Biasing
736
732
734
V_L Biasing
720
710
Error Amplifier Biasing
718
5th-Order Low-Pass Elliptic Filter
V_{tune}
V_{NR}
V_{bn}
V_L
V_{in}^+
V_{in}^-
V_{out}^+
V_{out}^-
712
VCO
V_{tune}
V_{NR}
V_{bn}
V_L
714
716
100kΩ
100pF
Clock (280kHz)

FIG. 7

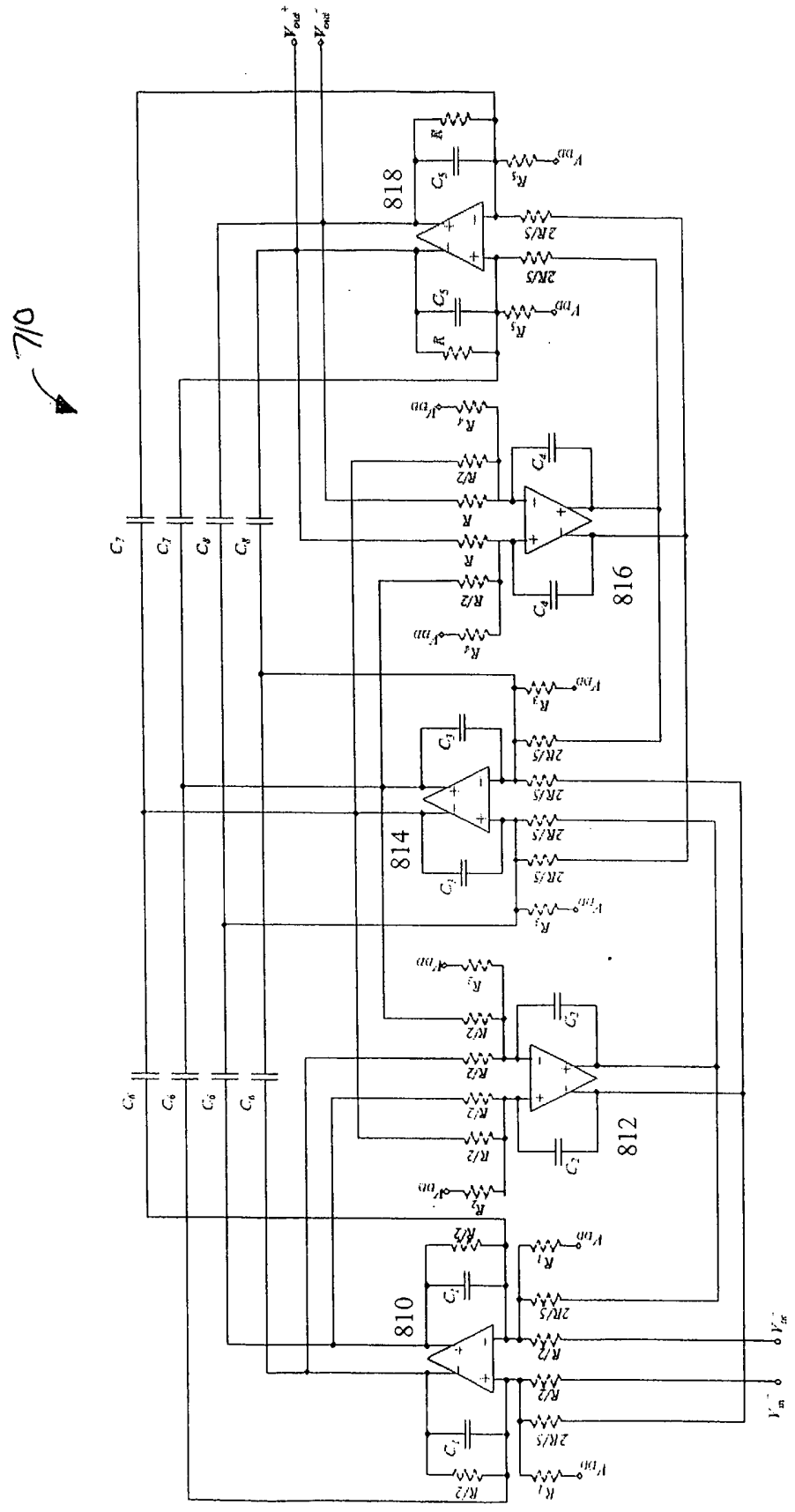


FIG. 8A

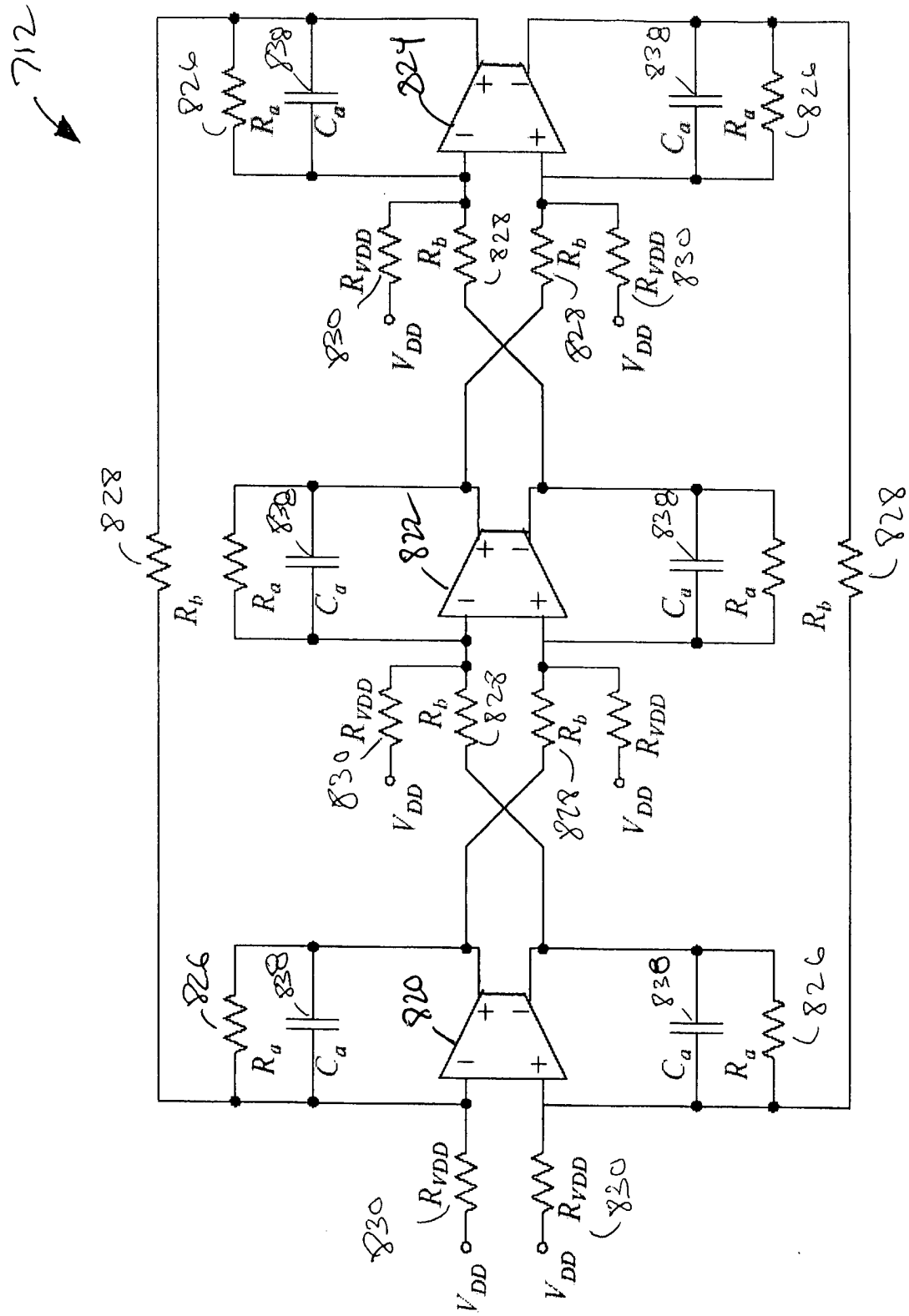


FIG. 8B

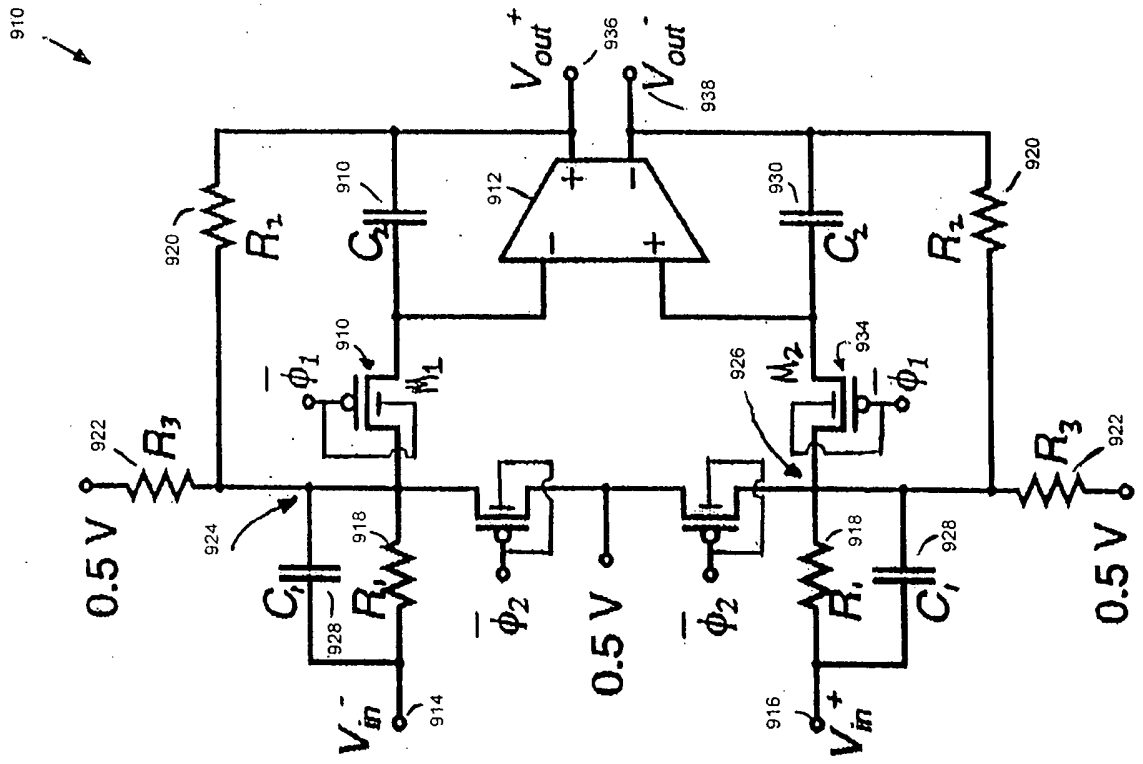

910
V_{out}^+
936
V_{out}^-
938
912
910
920
R_2
C_2
930
926
M_2
934
ϕ_1
M_1
922
R_3
0.5 V
924
C_1
928
R_1
918
ϕ_2
V_{in}^-
914
V_{in}^+
916

FIG. 9

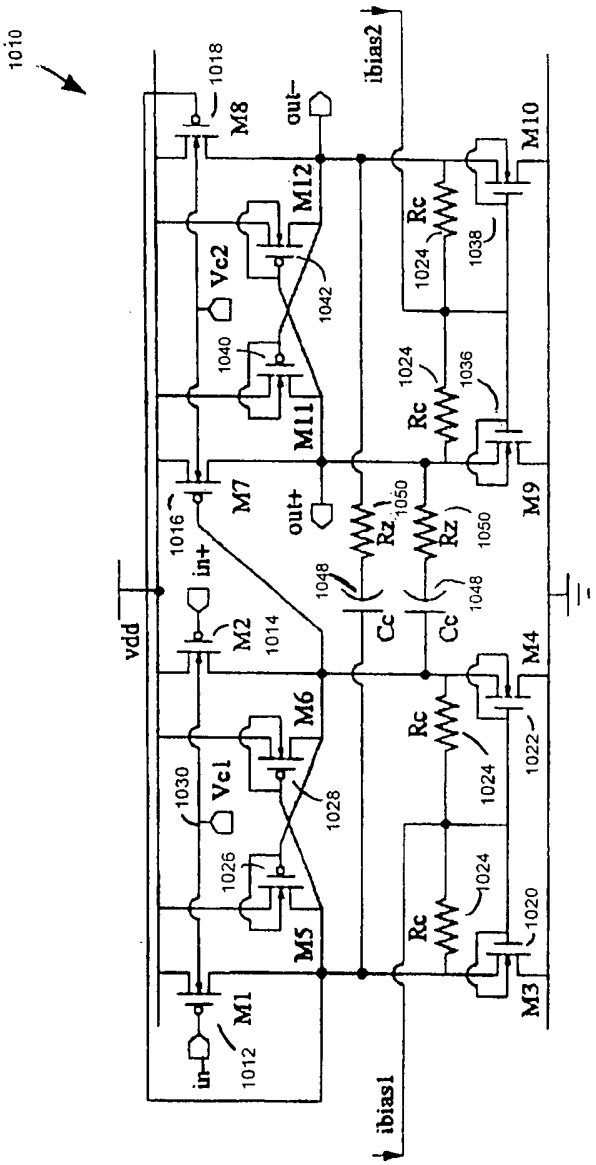

1010
vdd
in+
in-
out+
out-
ibias1
ibias2
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
Vc1
Vc2
Rc
Rz
Cc
1012
1014
1016
1018
1020
1022
1024
1026
1028
1030
1036
1038
1040
1042
1048
1050

FIG. 10

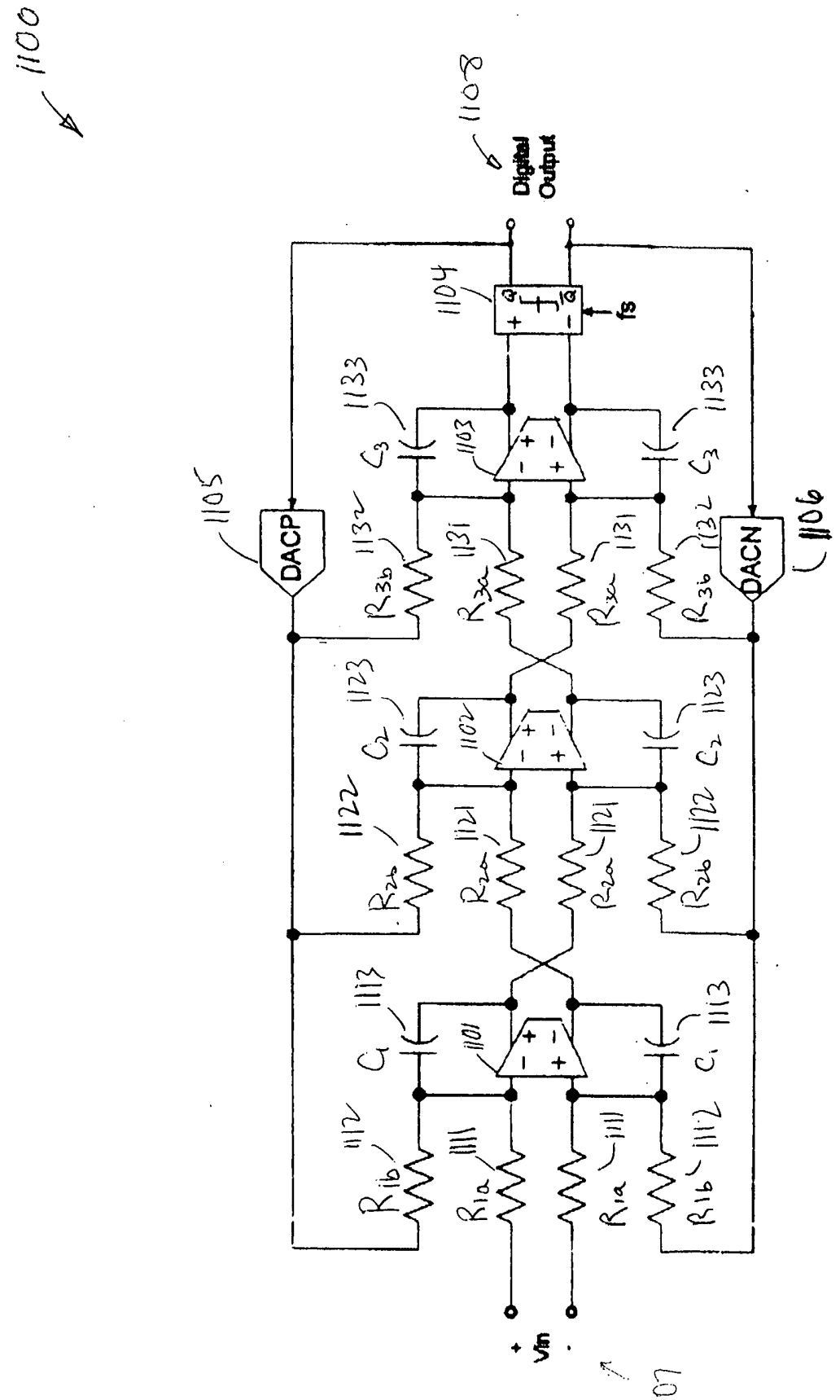

1100
1108
Digital Output
1104
fs
1105
DACP
1106
DACN
1133
C3
1103
1132
R3b
1131
R3a
1123
C2
1102
1122
R2b
1121
R2a
1113
C1
1101
1112
R1b
1111
R1a
+ Vin -
1107

FIG 11A

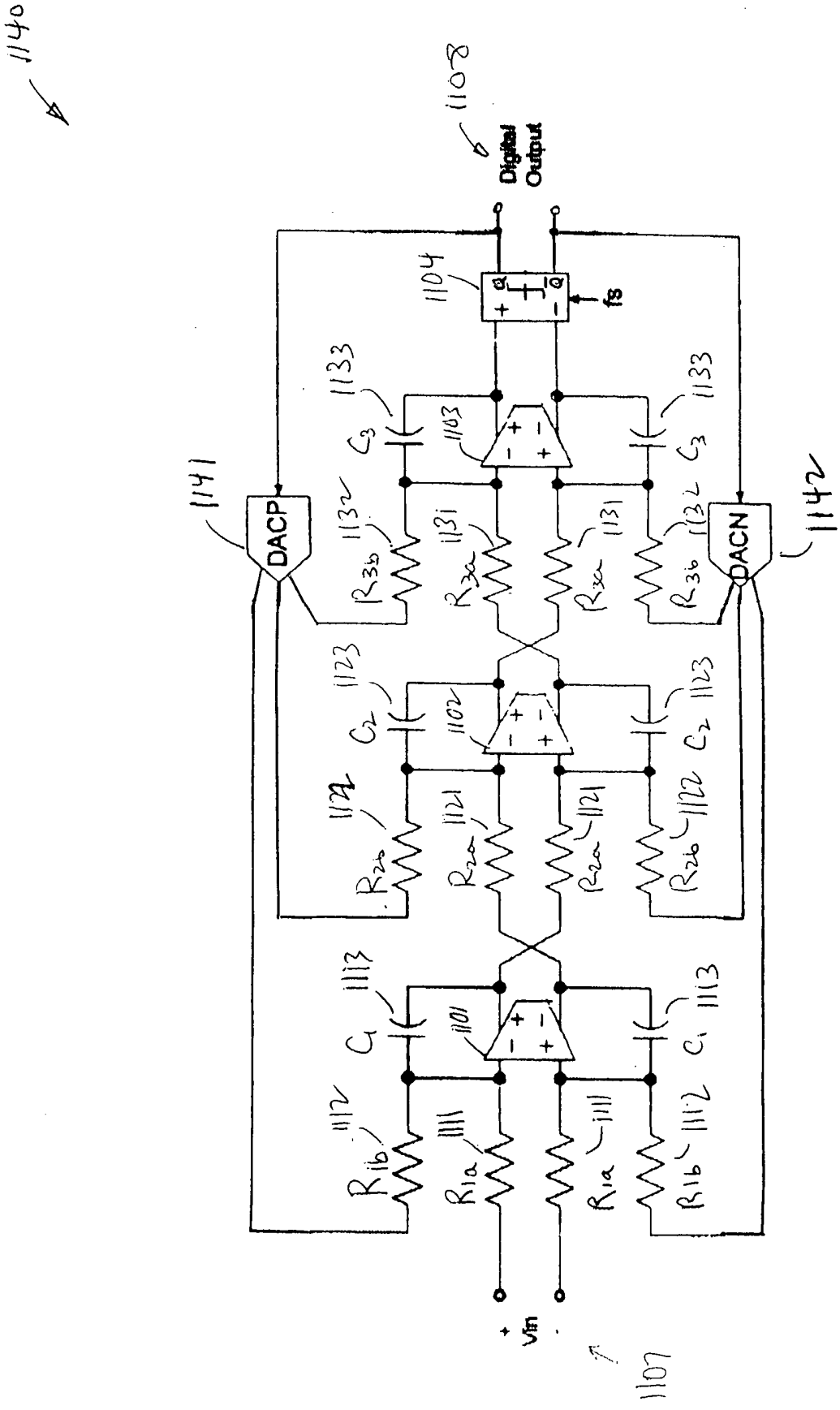

1140
1108
Digital Output
1104
fs
1133
1103
1141
DACP
1132
1131
1142
DACN
1123
1102
1122
1121
1113
1101
1112
1111
+ Vin
1107

FIG. 11B

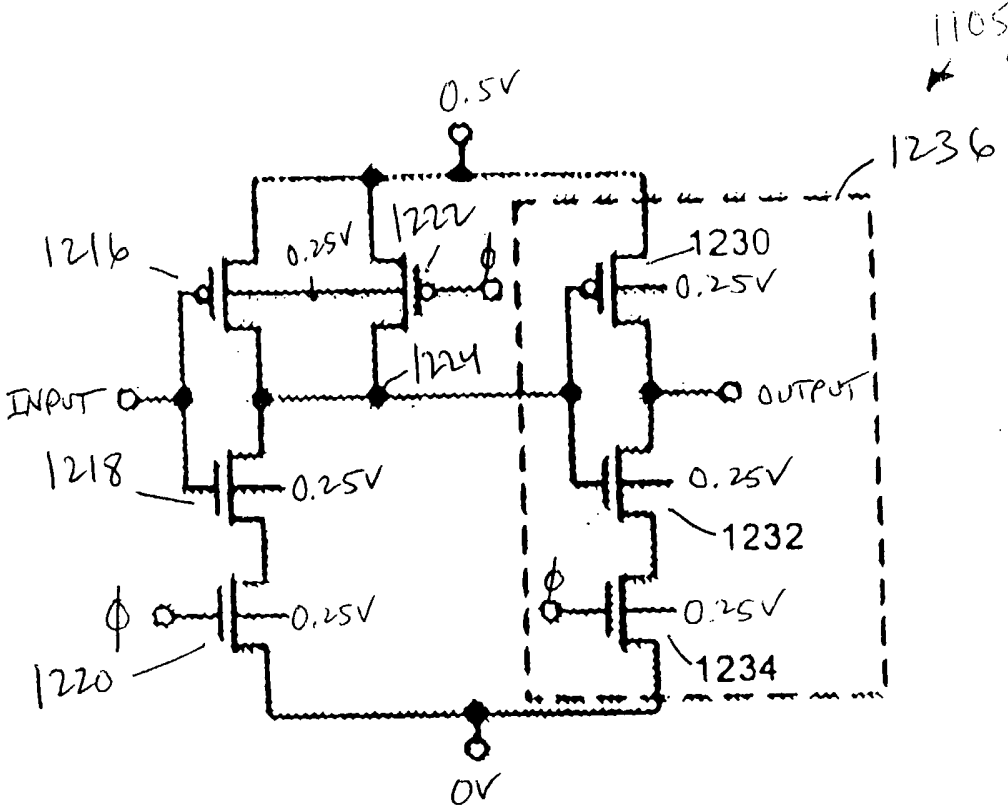

1105/1106
0.5V
1236
1222
1216
0.25V
1230
0.25V
1224
INPUT
OUTPUT
1218
0.25V
0.25V
1232
0.25V
0.25V
1234
1220
0V

FIG. 12A

1141/1142

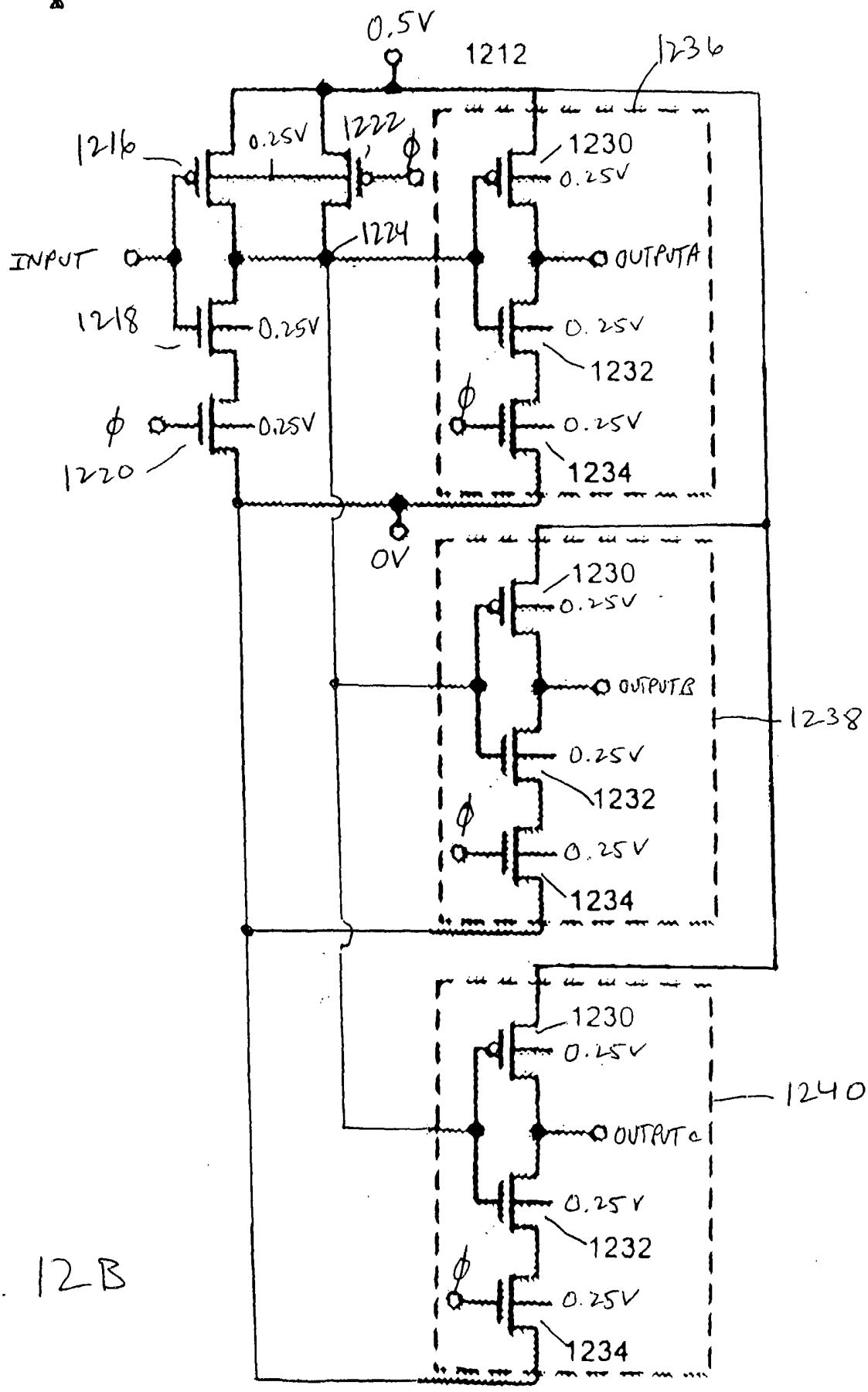


FIG. 12B

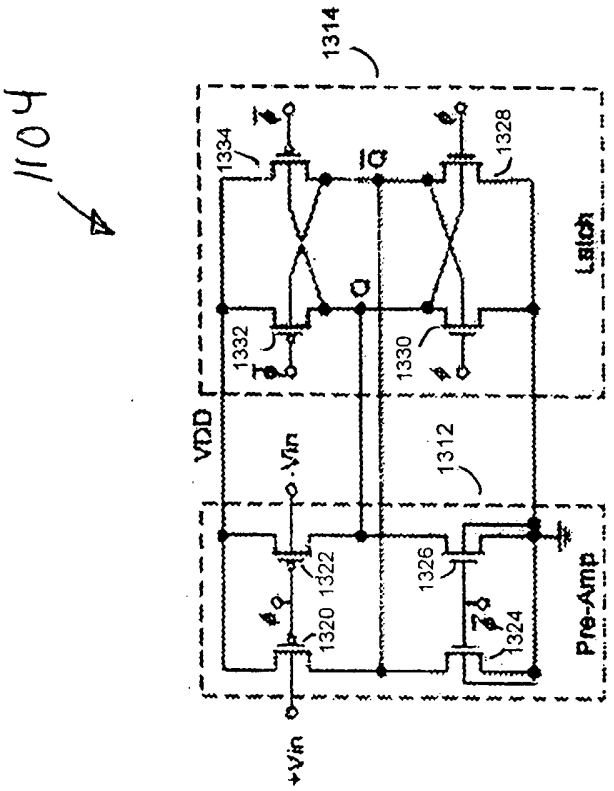

1104
1314
1334
1328
Latch
Q
1332
1330
VDD
Vin
1312
1326
1322
1320
1324
Pre-Amp
+Vin

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/33623

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H03K 3/037
USPC - 327/170
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 327/108, 109, 110, 111, 112; 327/170, 215; 327/434, 435, 436, 437; 326/81, 82; 341/126, 127, 133
IPC(8) :

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
U.S. Patent and Trademark Office Patent Full-Text and Full-Page Database; PatentCafe ICO semantic search engine of US Patent, US Published Applications, WIPO, Great Britain, Japan, Germany, European Patent Office (EPO).

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0108879 A1 (CHOI) 10 June 2004 (10.06.2004) see entire document	15
X	US 2004/0113669 A1 (WODNICKI) 17 June 2004 (17.06.2004) see entire document	1-2, 8-9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search
19 January 2006 (19.01.2006)

Date of mailing of the international search report
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