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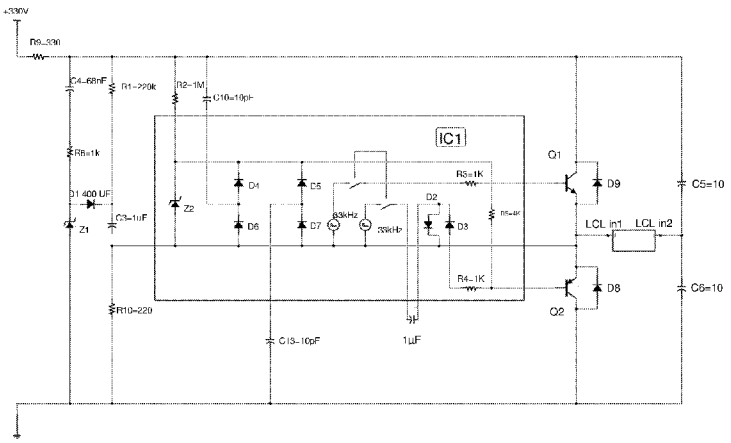
Figure 4



(57) Abstract: A power adaptor which comprises an input for connection to an AC power supply, a resonant circuit (LCL) coupled to the input that provides an output suitable for driving a load (LCL), at least one half-bridge drive circuit (Ql, Q2) for providing a drive signal to the resonant circuit, and a switch controller (ICl) for the half-bridge drive circuit. The switch controller (ICl) is adapted to provide one or more of the following, in at least one mode: (i) to provide the high-side switch and the low-side switch with on-times of different durations, (ii) to provide the high-side switch and the low-side switch with on-times that overlap, and (iii) to provide the high-side switch and the low- side switch with on-times that are synchronous. This may be utilised to control the current delivered to the output without any need to change the frequency at which the resonant circuit is driven.

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Title – Improvements relating to Power Adaptors

This invention relates to power adaptors, and particularly to power adaptors for solid state light sources.

LEDs are light sources that are being developed to replace conventional lighting systems, such as fluorescent and incandescent lights, in order to provide more energy efficient systems. Since an incandescent light source typically consumes 60-100W and has a short lifetime, an LED bulb would be the excellent substitute with considerably less power dissipation and longer life. There has therefore been much research into the development of an LED bulb compatible with TRIAC dimmers, which are common in lighting systems.

A major issue with TRIAC dimmable LED bulbs is dimmer compatibility. The conventional TRIAC dimmer was designed to handle hundreds of watts induced by incandescent bulbs. An LED bulb consuming much less power will interact with those dimmers composed of high-power devices. If the interaction between dimmer and LED bulb is not stabilized, visible flicker is perceptible.

In order to prevent visible flicker, a conventional TRIAC dimmer needs a latching current at firing and a holding current during the TRIAC turn-on after firing. If those two currents are not met, the TRIAC dimmer misfires and the LED light source flickers.

The latching and holding currents are different between different dimmer models. The typical range of latching and holding currents is around 5 ~ 50 mA. Those operating requirements do not cause problems when incandescent bulbs are used, due to their high power consumption. However, an LED bulb with much less output power cannot maintain this amount of current over the whole line cycle without additional circuitry.

Another issue is the large current spike generated upon firing of a conventional TRIAC dimmer, which is commonly called current inrush. Such a current spike is

generated as a result of the rapid charging of the capacitors of the power adaptor, and has the disadvantage of causing oscillations in the line current. As discussed above, a TRIAC dimmer requires a latching current during firing and a holding current after firing, and if these current levels are not met then the dimmer may misfire, resulting in flickering of the solid state light source. Therefore, such oscillations in line current may result in the required current levels not being met and the dimmer misfiring, or may even result in damage being caused to the TRIAC dimmer.

There has now been devised an improved power adaptor which overcomes or substantially mitigates the above-mentioned and/or other disadvantages associated with the prior art.

According to a first aspect of the invention, there is provided a power adaptor comprising an input for connection to an AC power supply, a resonant circuit coupled to the input that provides an output suitable for driving a load, at least one half-bridge drive circuit for providing a drive signal to the resonant circuit, and a switch controller for the half-bridge drive circuit, the half-bridge drive circuit having a high-side switch and a low-side switch, and the switch controller being adapted to provide one or more of the following, in at least one mode:

(i) to provide the high-side switch and the low-side switch with on-times of different durations,

(ii) to provide the high-side switch and the low-side switch with on-times that overlap, and

(iii) to provide the high-side switch and the low-side switch with on-times that are synchronous.

The present invention is advantageous principally because the switch controller providing the high-side switch and the low-side switch with on-times of different durations, on-times that overlap, and/or on-times that are synchronous, may be utilised to control the current delivered to the output without any need to change the frequency at which the resonant circuit is driven. This enables the current at the output to be controlled without changing the frequency at which the resonant

circuit is driven, and therefore without any change to the resonant circuit itself.

The high-side switch and the low-side switch having on-times of different durations may be utilised to control the current drawn from the input. In particular, the high-side switch and the low-side switch may have on-times of different durations, ie asymmetric on-times, such that the degree of asymmetry between the high-side switch and the low-side switch determines the current drawn from the input. It has been found that the greater the degree of asymmetry between the on-times of the high-side switch and the low-side switch, the less current drawn from the input.

The current drawn at the input may be substantially equal to the current provided at the output, for example if there is no overlap between the on-times of the high- and low-side switches. This enables dimming control effected by the switch controller, without the need to change the frequency at which the resonant circuit is driven, and therefore without any need to change the resonant circuit itself. In particular, in order to reduce the current drawn from the input and the current provided at the output, the on-times of the high-side switch and the low-side switch may be varied relative to each other, for example such that the on-time of the high-side switch is shorter than the on-time of the low-side switch.

The high-side switch and the low-side switch having on-times of different durations, ie asymmetric on-times, may be utilised to determine the waveform of the current drawn at the input, eg to provide dimmer compatibility and/or reduce harmonic distortion. In particular, this may be achieved by the switch controller providing the high-side switch and the low-side switch with on-times of different durations, ie asymmetric on-times, and varying the degree of asymmetry between the high-side switch and the low-side switch during each input cycle to determine the waveform of the current drawn from the input.

An overlap between the on-times of the switches may be utilised to create a load condition in the period of overlap, in each input cycle, which may increase the current drawn at the input relative to the current delivered to the output in the period of overlap, in each input cycle. This enables the current at the output to be

reduced without reducing the current drawn at the input, for example. In addition, it enables a latch current for a dimmer switch to be drawn in each input cycle, in the period of overlap, and a lower hold current to be drawn subsequently, in each input cycle, without any need to change the frequency at which the resonant circuit is driven. Since the latch current for a conventional dimmer switch in a mains supply (eg 85mA) typically only needs to be drawn for a few hundred µs, relative to the hold current (eg 50mA) that is typically drawn for a few ms, the additional current (35mA) that is not provided to the output would result in acceptably small losses, eg 100-200mW on 230V mains supply. This control may also help reduce the voltage reduction problems seen just after the TRIAC of a conventional dimmer switch fires, and may therefore negate the need for snubber circuits and their associated losses.

The power adaptor may also have a mode in which no power is provided at the output, but the power adaptor provides a load condition to the input, by the switch controller providing the high-side switch and the low-side switch with simultaneous on-times.

The greater the duration of the overlap for the on-times or the duration of the simultaneous on-times, the lower the resistance or dynamic impedance of the load provided. This is particularly advantageous for solid state light sources, eg LEDs. In particular, this load condition may provide a DC path, which prevents false start-up conditions. This enables use with dimmers, and also prevents glowing occurring from a pickup supply.

The switch controller may utilise any combination of the above configurations of on-times to provide the desired current draw at the input and the required current at the output.

Where the power adaptor has a mode in which a load condition is generated by overlapping or synchronous on-times of the switches, the controller may be adapted to determine whether the impedance of the load condition will be acceptable for the voltage of the power supply. The controller is preferably,

therefore, adapted to monitor the voltage of the power supply.

The power adaptor may be adapted to switch between two or more modes, which each provide a different configuration of on-times for the high-side switch and the low-side switch. Since the present invention enables different modes without changing the frequency at which the resonant circuit is driven, the resonant circuit is preferably driven at, or approximately at, its resonant frequency or a sub-harmonic thereof in each mode.

The power adaptor may be adapted to monitor the input voltage, and alter the ratio between the current provided at the output and the resistance across the input, based on that input voltage. In particular, this ratio may be altered proportionally based on the input voltage, such that sudden changes in current and/or input resistance are not created when switching modes. Where the power adaptor is adapted for use with a mains supply and solid state light sources, these sudden changes in current and/or input resistance may cause ringing or harmonics on the mains, possible flicker on the output, and may result in dimmer incompatibility. The ratio may be altered by changing the amount of overlap of the on-times of the high- and low-side switches.

The high- and low-side switches are preferably bipolar junction transistors (BJTs), which are typically less expensive than field-effect transistors (FETs). Furthermore, since BJTs have limited gain, there is a reduced risk of damage to the switches from current inrush relative to FETs, which have infinite gain and require damping circuits.

For some applications, for example power adaptors for driving solid state light sources, eg LEDs, that are compatible with conventional dimmer switches (eg TRICS and SCR switches), it is preferable for the power adaptor to maintain a substantially constant current input for varying input voltages.

The resonant circuit may therefore be an LCL series-parallel resonant circuit. The LCL series-parallel resonant circuit comprises a first inductor L1 and a first

capacitor C1 in series, and a parallel load leg including a second inductor L2. The first inductor L1 and first capacitor C1 are connected in series between two input terminals of the resonant circuit, and the load leg is connected in parallel across the first capacitor C1, wherein the load leg comprises the second inductor L2 and an output for driving the load, which are connected in series.

Power adaptors utilising an LCL series-parallel resonant circuit are described in WO 2008/120019, WO 2010/041067, WO 2010/139992, WO 2011/083336 and WO 2012/010900, the teaching of each of which are incorporated herein by reference in their entirety.

The use of an LCL series-parallel resonant circuit provides a power adaptor suitable for solid state light sources, such as LEDs, that has a substantially constant current draw and high efficiency. In particular, the output current becomes independent of output voltage and if the power adaptor is powered by a low frequency sine voltage input, and the output voltage is constant, ie an LED load, the input current becomes a low frequency, substantially square wave ideal for drive by a TRIAC dimmer as it maintains the hold current at the lowest possible power whilst providing the LED with a current source that varies in brightness with the low frequency input voltage, ie it makes the LED act like a lamp bulb and enables control by a TRIAC dimmer at vastly reduced power and high power factor relative to other power adaptor technology.

The load may therefore be one or more LEDs, and the input may be drawn from a TRIAC or SCR dimmer.

It has also been found that the second inductor of the LCL series-parallel resonant circuit may be reduced significantly, or even removed, where a high voltage LED(s) are used. Hence, the resonant circuit may be an LC resonant circuit that provides an output suitable for driving a solid state light source, the LC resonant circuit being driven at a frequency, and optionally with a dead band, that causes the LC resonant circuit to draw a substantially constant current from the AC power supply. By “substantially constant current” with respect to an AC power supply is

meant a substantially square-wave current draw.

It has been found that the LC resonant circuit may be driven to provide the same properties of the LCL series-parallel resonant circuit discussed above, but only where the LED has a voltage comparable, eg at least +/-50%, or preferably +/-25%, to the rms voltage of the AC power supply.

It may be desirable to provide a low mains current total harmonic distortion (I_{THD}), eg less than 15%, for certain markets and/or lamp types. In these embodiments, rather than a substantially constant current draw from the mains supply, the power adaptor may be adapted to draw a substantially sinusoidal current waveform from the mains supply. This may be achieved by the switch controller providing the high-side switch and the low-side switch with on-times of different durations, ie asymmetric on-times, and varying the degree of asymmetry between the high-side switch and the low-side switch during each input cycle to determine the waveform of the current drawn from the input. In particular, it has been found that the greater the degree of asymmetry between the on-times of the high-side switch and the low-side switch, the less current drawn from the input. In addition, where the resonant circuit includes DC link capacitors that are charged on the rising half of the mains supply input cycle, more current would be drawn on the rising edge of the mains supply input cycle. As such, it may be necessary to delay the power increase on the rising side of the half cycle to compensate for this, whereas on the falling side of the mains voltage, the power may decrease as the voltage decreases.

In presently preferred embodiments, the high-side switch and the low side switch of the half-bridge drive circuit are arranged with their respective emitter or source terminals connected at the centre of the half bridge.

Since, in this embodiment, the switching voltage applied to the base or gate terminal of a transistor is referenced relative to the voltage at the emitter or source terminal, this enables a common reference in the form of a floating ground. This removes any need for a level shifter circuit, which is a high voltage circuit that is

typically expensive and results in power loss, and hence reduced efficiency. The invention therefore reduces cost and increases efficiency relative to the prior art. In addition, the invention enables the drive circuitry to be at low voltage, and enables the same drive circuitry to drive both the high- and low-side switches. Indeed, according to a further aspect of the invention, there is provided a half-bridge drive circuit comprising a high-side switch and a low side switch, each having an emitter or source terminal, wherein the high-side switch and the low side switch are arranged with their respective emitter or source terminals connected at the centre of the half bridge.

The high-side switch is preferably an NPN bipolar junction transistor (BJT), or a similarly functioning transistor. The low-side switch is preferably a PNP bipolar junction transistor (BJT), or a similarly functioning transistor. The transistors being bipolar junction transistors (BJTs) may enable the switch controller to be at low voltage, eg less than 5V, eg 2V. Where an integrated circuit is provided, a low voltage power supply may be formed by one or more diodes and an energy storage device such as a capacitor.

The switches are typically configured with a switching voltage at the base or gate terminal that is determined relative to the voltage at the emitter or source terminal. The connection between the emitter or source terminals of the high-side switch and the low side switch preferably therefore provides a common reference for the switching voltage of the high-side switch and the low-side switch in the form of a floating ground. The collector or drain terminals of the high-side switch and the low side switch may be connected to the positive supply voltage and normal ground, eg 0V, respectively, of the circuit.

The low-side switch preferably has a negative switching voltage at the base/gate of the switch that is determined relative to a common reference in the form of a floating ground. The negative switching voltage may be generated by a charge-pump, for example.

The switch controller preferably takes the form of an integrated circuit. The ground

connection of the switch controller is preferably connected to the emitter or source terminals of the high-side switch and the low side switch, such that the ground connection of the switch controller has a reference common to the high-side switch and the low side switch in the form of a floating ground.

The switch controller is preferably provided with a local supply, or a bootstrap from the normal ground, or the capacitors that would typically be connected across the high- and low-side switches may be adapted to provide power to the switch controller, these may feed the charge pump diodes on the microprocessor.

This embodiment of the invention is particularly advantageous when used to drive an LCL series-parallel resonant circuit. This arrangement enables the half-bridge drive circuit to function without any feedback, eg from an inductor to an oscillator drive. This arrangement also removes the need for any feedback transformers, which are large and expensive. The present invention is also particularly advantageous to the LCL circuit as it allows the use of a low voltage process.

The switch controller may include a low voltage process integrated circuit, and the high-side switch and the low-side switch may be external of the integrated circuit. The switch controller may include a microprocessor, and the ESD diodes on the ports of the microprocessor are utilised as charge pump diodes in the provision of a power supply for the microprocessor.

The switch controller may be configured to also control an output stage, such as a rectifier circuit having multiple modes of operation, as described in WO 2011/083336 A2 and WO 2012/010900 A2. This is enabled by this embodiment of the invention because the switch controller is referenced to a centre point of the half-bridge drive circuit, ie the floating ground, which will have a similar, or the same, potential as the reference of the output stage.

Since the resonant circuit may draw the bulk of the overshoot current when in or near resonance, reverse parallel diodes across the drive transistor(s) may be absent. This is advantageous because the reverse parallel diodes need to be high

voltage diodes. However, in order to minimise the effect of not having the reverse parallel diodes, diodes connected between a common point between the transistors and the base terminals of the transistors may be utilised to provide base extraction current for fast turn off.

The power adaptor according to the invention is particularly advantageous in relation to the driving of solid state light sources from a mains supply including a conventional dimmer switch. In addition, however, the control discussed above may be used in other fields, for example in relation to motor control. In particular, the present invention enables bi-directional motor control, for example, and driving DC and high frequency AC motors, for example.

International Patent Application WO2010/041067, the teaching of which is hereby incorporated by reference in its entirety, describes improvements in power adapters that are useful in driver circuits for LED solid state lighting systems. Such systems are referred as "RAIS" technology, and incorporate an LCL series-parallel resonant circuit comprising a first inductor L1 and a first capacitor C1 in series, and a parallel load leg including a second inductor L2. The first inductor L1 and first capacitor C1 are connected in series between two input terminals of the resonant circuit, and the load leg is connected in parallel across the first capacitor C1, wherein the load leg comprises the second inductor L2 and an output for driving the load, which are connected in series. The LCL circuit is connected to an output rectifier bridge (denoted 24 in Figure 4 of WO2010/041067).

To prevent the flickering of dimmed solid state lighting systems, RAIS technology provides the ideal waveform for the type of dimmer that is in use. RAIS has two different modes of operation, depending on which type of dimmer is in use, and these two modes are referred to as "double hold" and "half power".

For leading edge, eg TRIAC, dimmers, the current for operation is drawn at full power for only the first 90° of the 180° mains power cycle; and this is the double hold application of RAIS. When a dimmer is switched on, the RAIS technology sends a resonant waveform to the output bridge, and this process lasts for the

duration of the on time of the dimmer. However, the modified output bridge shorts out this signal for approximately the second half, or longer if different dimming curves are required, resulting in the current being drawn at the input for approximately one-half the time expected.

Trailing edge dimmers, however, draw current for operation at half power for the entire mains cycle; this is the half power mode of operation of RAIS. A rectifier circuit that enables this mode of operation to be implemented is described in International Patent Application WO2011/083336, the teaching of which is hereby incorporated by reference in its entirety.

Clearly, in order the appropriate mode of operation to be selected, there is a need to be able to identify which type of dimmer is in use. A known method of achieving this requires the input voltage waveform to be monitored. In particular, such a method requires a connection to VDC (rectified mains AC current). The input voltage waveform is monitored and if a fast edge is detected, it is determined that the dimmer in use is a TRIAC dimmer. This then prompts the RAIS technology to use the double hold mode of operation. If no fast edge is detected, the dimmer is determined to be trailing edge and the half power mode of operation is used.

It has now been found that it is possible to identify the type of dimmer, and hence the required mode of operation, without monitoring the input voltage waveform.

According to a further aspect of the invention there is provided a power adaptor comprising an input for connection to an AC power supply and a resonant circuit coupled to the input that provides an output suitable for driving a load, wherein the resonant circuit generates resonant waveform, the power adapter being adapted to monitor the resonant waveform so as to detect variations in the resonant waveform.

Variations in the resonant waveform may have the form of gaps, rapid changes or other variations. The waveform may be monitored by various means which will be evident to those skilled in the art, eg by coupling the signal at AC1 into a suitable

processor, timing circuit or the like. The waveform may take the form of a train of pulses.

The presence or absence of variations in the resonant waveform may be indicative of the type of power reducing device to which the power adapter is connected. The presence of gaps, variations or rapid changes in the resonant waveform may be indicative of dimmer retriggering and the presence of a leading edge (eg TRIAC) dimmer. This then leads to activation of the double hold mode of operation.

Where no such variation in the resonant waveform is detected, the power adapter operates in the half power mode. To enable this, the power adapter may comprise a rectifier of the type described in WO2011/083336.

An advantage of the invention is that it does not require connection to a monitor circuit, which may therefore be omitted. The VDC connection 3 of Figure 1 is therefore not required in this aspect of the invention, in which instead the resonant waveform is monitored at AC1 and/or AC2. The system is therefore much better suited to isolated circuits.

The invention is further advantageous in that gaps, variations or rapid changes in the resonant waveform can be detected within 1-3 mains half cycles. Thus, the double hold mode of operation is activated quickly, with the result that flickering of the solid state lighting system is imperceptible by the human eye.

Furthermore, in the case where one low power lamp is connected to a dimmer, if the dimmer becomes unstable and false triggers, the lamp draws power in the double hold manner as described above. In the invention, as more lamps are added, the dimmer stabilises and draws its current across the full cycle providing a better power factor (PF) for the line. This will balance out the power factor of the single lamp systems that draw slightly lower power factor.

A power adaptor comprising an input for connection to an AC power supply and a

resonant circuit coupled to the input that provides an output suitable for driving a load, wherein the resonant circuit has a first mode of operation, and a second mode of operation is provided in which at least one of the inductance and capacitive components of the resonant circuit is modified or removed.

The power adaptor according to the invention is advantageous principally because the resonant circuit may be configured to supply power at two different levels, whilst optimising efficiency in both modes of operation.

The resonant circuit is preferably an LCL series-parallel resonant circuit. The LCL series-parallel resonant circuit comprises a first inductor L1 and a first capacitor C1 in series, and a parallel load leg including a second inductor L2. The first inductor L1 and first capacitor C1 are connected in series between two input terminals of the resonant circuit, and the load leg is connected in parallel across the first capacitor C1, wherein the load leg comprises the second inductor L2 and an output for driving the load, which are connected in series.

Power adaptors utilising an LCL series-parallel resonant circuit are described in WO 2008/120019, WO 2010/041067, WO 2010/139992, WO 2011/083336 and WO 2012/010900, the teaching of each of which are incorporated herein by reference in their entirety.

The use of an LCL series-parallel resonant circuit provides a power adaptor suitable for solid state light sources, such as LEDs, that has a substantially constant current draw and high efficiency. In particular, the output current becomes independent of output voltage and if the power adaptor is powered by a low frequency sine voltage input, and the output voltage is constant, ie an LED load, the input current becomes a low frequency, substantially square wave ideal for drive by a TRIAC dimmer as it maintains the hold current at the lowest possible power whilst providing the LED with a current source that varies in brightness with the low frequency input voltage, ie it makes the LED act like a lamp bulb and enables control by a TRIAC dimmer at vastly reduced power and high power factor relative to other power adaptor technology.

The load is preferably, therefore, one or more LEDs, and the input may be drawn from a TRIAC dimmer.

The power adaptor may have a second mode of operation in which the capacitive component of the resonant circuit is reduced. This may be achieved using an electronic switch, eg a transistor or a thyristor, for removing a capacitor from the resonant circuit. For example, the capacitive component of the resonant circuit may be provided by at least two capacitors in parallel, with at least one of the capacitors being removable from the resonant circuit using the electronic switch. The electronic switch may be controlled by a controller, such as an integrated circuit. This second mode of operation may be utilised to provide lower power to the load, relative to the first mode of operation.

The first mode of operation may therefore be configured to provide a higher current draw, and hence a higher power draw, relative to the second mode of operation. The first mode of operation may therefore be used to draw the latch current of a TRIAC dimmer, and a dead band in the driving signal for the resonant circuit may then be introduced and/or varied to draw the (usually lower) hold current of the TRIAC dimmer. For stable, low power lamps, however, the second mode of operation may be utilised.

When entering the second mode of operation, the frequency of the drive signal for the resonant circuit will typically need to be varied, and/or any dead band will typically need to be varied, in order for the modified resonant circuit to function.

This second mode of operation allows for a much lower power for use by low power lamps, allowing the double hold principle to be used where the resonant circuit is used with mains supply, trailing edge and leading edge dimmers, where the lamp is stable. If instability is detected or it's preferred to switch modes on detection of the leading edge, the mode can be changed back to the first mode of operation, thereby drawing significantly higher power and the required hold current.

An alternative configuration comprises an LCL series-parallel resonant circuit with a capacitance across its output. This capacitance is described in WO 2011/083336 as being present to reduce conducted emissions when driving solid state light sources, such as LEDs. In this configuration, the power adaptor may have a second mode of operation in which the capacitive component of the LCL resonant circuit is removed. In this second mode of operation, the LCL resonant circuit changes to an LC resonant circuit comprised of the remaining inductors of the LCL resonant circuit in series with the capacitance across its output. It has been found that the LC resonant circuit may be driven to provide the same properties of the LCL series-parallel resonant circuit discussed above, but only where the LED has a voltage comparable, eg at least +/-50%, or preferably +/-25%, to the rms voltage of the AC power supply.

The following features are believed to be advantageous in relation to power adaptors comprising resonant circuits, and not just the two mode configuration described above. Hence, according to a further aspect of the invention, there is provided a power adaptor comprising an input for connection to an AC power supply and a resonant circuit coupled to the input that provides an output suitable for driving a load, wherein the power adaptor includes one or more of the features set out below.

The power adaptor may introduce a dead band into the driving signal for the resonant circuit, for example to decrease the power to the LED(s), and still draw the same current. The dead band may therefore be used to allow a lower amount of power to the LED(s), where the overall power is increased to allow the latch current to be drawn, which is often higher than the hold current. This removes the need for RC bleeder circuits.

The resonant circuit may be driven by one or more drive transistors, and preferably two transistors – a high-side transistor and a low-side transistor. The transistors may be driven by any appropriate drive circuit, which would typically include an oscillator, but are preferably driven by a controller, such as an

integrated circuit. The transistors may be bipolar junction transistors (BJTs), which feature enables the drive circuit to be at low voltage, eg less than 5V, eg 2V. Where an integrated circuit is provided, a low voltage power supply may be formed by one or more diodes and an energy storage device such as a capacitor.

The gain of the drive transistors may be utilised to provide fast start with high efficiency, with resistors feeding the base terminals of the drive transistors, which then charge an energy storage device such as a capacitor at a rate determined by the resistors and the gain of the drive transistors.

The pulse width of the high-side and low-side transistors may differ to account for different turn off times, eg between NPN and PNP transistors. For example, the pulse width of the high-side drive transistor may be wider than that of the low-side drive transistor to accommodate the greater base storage time of the low side PNP transistor.

Since the resonant circuit draws the bulk of the overshoot current when in or near resonance, reverse parallel diodes across the drive transistor(s) may be absent. This is advantageous because the reverse parallel diodes need to be high voltage diodes. However, in order to minimise the effect of not having the reverse parallel diodes, diodes connected between a common point between the transistors and the base terminals of the transistors may be utilised to provide base extraction current for fast turn off.

As discussed above, it has now been found that the second inductor of the LCL series-parallel resonant circuit may be reduced significantly, or even removed, where a high voltage LED(s) are used. Hence, according to a further aspect of the invention, there is provided a power adaptor comprising an input for connection to an AC power supply and an LC resonant circuit coupled to the input that provides an output suitable for driving a solid state light source, the LC resonant circuit being driven at a frequency, and optionally with a dead band, that causes the LC resonant circuit to draw a substantially constant current from the AC power supply.

By “substantially constant current” with respect to an AC power supply is meant a substantially square-wave current draw.

It has been found that the LC resonant circuit may be driven to provide the same properties of the LCL series-parallel resonant circuit discussed above, but only where the LED has a voltage comparable, eg at least +/-50%, or preferably +/-25%, to the rms voltage of the AC power supply.

According to a further aspect of the invention, there is provided a power adaptor for a solid state light source comprising an active damping circuit, wherein the active damping circuit has a resistive load in parallel with a constant current circuit.

The power adaptor according to this aspect of the invention is advantageous principally because the active damping circuit damps the current spike or current inrush associated with the firing of a TRIAC in a TRIAC dimmer, whilst maintaining high efficiency by means of the constant current circuit when no current spike or current inrush is present. This is advantageous over prior art arrangements principally because there are two damping circuits active continuously, with no timing or delay between their activation, which combine to maintain high efficiency. Furthermore, prior art arrangements comprising a FET across a resistive load have been found to suffer from current ringing when the switch is activated – the present invention solves this problem.

When a current spike or current inrush is present, the current may be limited by the resistive load plus the constant current from the constant current circuit. When no current spike or current inrush is present, the constant current circuit feeds the power adaptor. This aspect of the invention is particularly advantageous for power adaptors that draw a substantially constant current, for example utilise an LCL series-parallel resonant circuit or an LC resonant circuit, as discussed above. The constant current circuit is adapted to feed a resonant circuit of the power adaptor, eg the LCL resonant circuit, at a current greater than that needed by the resonant circuit, such that the voltage drop across the constant current circuit is minimised.

Example embodiments of the invention will now be described in detail, by way of illustration only, with reference to the accompanying drawings, in which

Figure 1 shows a switch controller and a half-bridge drive circuit of a first embodiment of a power adaptor according to the invention;

Figure 2 shows an LCL series-parallel resonant circuit and DC link capacitors of the first embodiment of the power adaptor according to the invention;

Figure 3a-3f show examples of different waveforms for the high-side switch and the low-side switch of the half-bridge drive circuit of an embodiment of the power adaptor according to the invention;

Figure 4 shows a second embodiment of a power adaptor according to the invention;

Figure 5 is an example of a low-voltage process half bridge drive integrated circuit (IC) suitable for use in the circuit of Figure 5 as IC1;

Figure 6 shows a third embodiment of a power adaptor according to the invention;

Figure 7 is a circuit of a fourth embodiment of a power adaptor according to the invention; and

Figure 8 is a circuit of a fifth embodiment of a power adaptor according to the invention.

An embodiment of a power adaptor according to the invention comprises an input rectifier stage (not shown in the Figures), a switch controller (RAIS-DH) and a half bridge drive circuit (HSD,LSD) (shown in Figure 1), and an LCL series-parallel resonant circuit (L1,C1,L2) and an output rectifier stage (shown in Figure 2). The high-side switch, Q1, is an NPN BJT transistor, and the low-side switch, Q2, is PNP BJT transistor. Q1 and Q2 are arranged with their emitters/sources

connected to a common point, which forms a floating ground for both Q1 and Q2. This common point also provides the output of the half-bridge drive circuit which, in this embodiment, is fed to an LCL series-parallel resonant circuit suitable for driving a solid state light source (of the form described in detail in GB 2449616 B8 and WO 2010/041067 A1).

Q1 and Q2 are each switched by providing a switching pulse to the respective base/gate, the voltage of the switching pulse being referenced to the emitter/source of the switch. When Q1 is switched on, the floating ground will be at the positive supply voltage, eg 330V, and the voltage at the base/gate of Q1 will be positive typ relative to the floating ground and hence the emitter/source voltage. When Q2 is switched on, the floating ground will be at normal ground, eg 0V, and the voltage at the base/gate of Q1 will be negative relative to the floating ground and hence the emitter/source voltage.

The switches Q1 and Q2 are driven by a switch controller, which is an integrated circuit designated RAIS-DH, that is also referenced to the floating ground. Since the switch controller RAIS-DH is driving BJT transistors, which require +-0.7V, the switch controller can be powered at 2V. In order to switch on Q1, the switch controller provides a positive pulse to the base/gate of Q1, relative to the floating ground (at the positive supply voltage, eg 330V) and hence the emitter/source voltage. In order to switch on Q2, he switch controller provides a negative pulse to the base/gate of Q2, relative to the floating ground (at normal ground, eg 0V) and hence the emitter/source voltage.

Q1 forms the high-side drive (HSD) and Q2 forms the low-side drive (LSD) for an LCL series-parallel resonant circuit (shown in Figure 2), which provides an output suitable for driving a solid state light source. The switch controller is configured to manipulate the current drawn at the input, the current delivered to the output, and/or the impedance of the power adaptor, by controlling the on-times of the high-side drive (HSD) and the low-side drive (LSD). This is described in detail above.

Examples of waveforms of the high-side drive (HSD) and the low-side drive (LSD) are shown in Figure 3. Figure 3a shows a conventional symmetric drive signal, with no overlapping, whereas Figures 3b-3f shown drive waveforms according to the invention.

Figure 3b shows the high-side drive (HSD) and the low-side drive (LSD) with on-times of different durations, ie asymmetric on-times. The degree of asymmetry between the high-side switch and the low-side switch determines the current drawn from the input. It has been found that the greater the degree of asymmetry between the on-times of the high-side switch and the low-side switch, the less current drawn from the input. Hence, the waveform of Figure 3b will cause less current to be drawn at the input than the waveform of Figure 3a. Furthermore, since there is no overlap between the on-times of the high-side drive (HSD) and the low-side drive (LSD), substantially the same current will be provided at the output.

Figure 3c shows the high-side drive (HSD) and the low-side drive (LSD) with on-times of different durations, ie asymmetric on-times, which also have a period of overlap. This overlap between the on-times of the switches creates a load condition in the period of overlap, in each input cycle, which increases the current drawn at the input relative to the current delivered to the output in the period of overlap, in each input cycle. This enables a latch current for a dimmer switch to be drawn in each input cycle, in the period of overlap, and a lower hold current to be drawn subsequently, in each input cycle, without any need to change the frequency at which the resonant circuit is driven. Since the latch current for a conventional dimmer switch in a mains supply (eg 85mA) typically only needs to be drawn for a few hundred μs, relative to the hold current (eg 50mA) that is typically drawn for a few ms, the additional current (35mA) that is not provided to the output would result in acceptably small losses, eg 100-200mW on 230V mains supply. This control also helps reduce the voltage reduction problems seen just after the TRIAC of a conventional dimmer switch fires, and therefore negates the need for snubber circuits and their associated losses.

Figure 3d shows the high-side drive (HSD) and the low-side drive (LSD) with the same period of overlap as the waveform of Figure 3c, but with a significantly greater asymmetry between the on-times of the switches. Hence, the waveform of Figure 3d will provide the same change between a higher latch current and a lower hold current, in each input cycle, but with less current being drawn at the input and correspondingly less current being provided to the output, across the whole input cycle, relative to the waveform of Figure 3c, due to the greater asymmetry between the high-side drive (HSD) and the low-side drive (LSD).

Figures 3e and 3f each show the high-side drive (HSD) and the low-side drive (LSD) being provided with simultaneous on-times, which each provide a load condition to the input. However, the greater the duration of the overlap for the on-times or the duration of the simultaneous on-times, the lower the resistance or dynamic impedance of the load provided. Hence, the waveform of Figure 3f provides a lower resistance or dynamic impedance than the waveform of Figure 3e. This is particularly advantageous for solid state light sources, eg LEDs. In particular, this load condition may provide a DC path, which prevents false start-up conditions. This enables use with dimmers, and also prevents glowing occurring from a pickup supply.

The power adaptor according to the invention is particularly advantageous in relation to the driving of solid state light sources from a mains supply including a conventional dimmer switch. In addition, however, the control discussed above may be used in other fields, for example in relation to motor control. In particular, the present invention enables bi-directional motor control, for example, and driving DC and high frequency AC motors, for example.

A second embodiment of a power adaptor according to the invention is shown in Figure 4. The high-side switch, Q1, is an NPN transistor (or an n-channel FET), and the low-side switch, Q2, is PNP transistor (or a p-channel FET). Q1 and Q2 are arranged with their emitters/sources connected to a common point, which forms a floating ground for both Q1 and Q2. This common point also provides the output of the half-bridge drive circuit which, in this embodiment, is fed to an LCL

series-parallel resonant circuit suitable for driving a solid state light source (of the form described in detail in GB 2449616 B8 and WO 2010/041067 A1).

Q1 and Q2 are each switched by providing a switching pulse to the respective base/gate, the voltage of the switching pulse being referenced to the emitter/source of the switch. When Q1 is switched on, the floating ground will be at the positive supply voltage, eg 330V, and the voltage at the base/gate of Q1 will be positive, 1-20V, +5V typical relative to the floating ground and hence the emitter/source voltage. When Q2 is switched on, the floating ground will be at normal ground, eg 0V, and the voltage at the base/gate of Q1 will be negative 1-20V, -5V typical relative to the floating ground and hence the emitter/source voltage.

The switches Q1 and Q2 are driven by an integrated circuit, IC1, which is also referenced to the floating ground. In order to switch on Q1, IC1 provides a +5V pulse to the base/gate of Q1, relative to the floating ground (at the positive supply voltage, eg 330V) and hence the emitter/source voltage. In order to switch on Q2, IC1 provides a -5V pulse to the base/gate of Q2, relative to the floating ground (at normal ground, eg 0V) and hence the emitter/source voltage.

The negative voltage switching pulse provided to the base/gate of Q2 is generated by a charge pump formed by C7, D1 and D2, which is driven by IC1. The charge-pump generates a -5V switching pulse when the input voltage from IC1 drops from 5V to 0V, and then returns to 5V. In particular, when the input voltage from IC1 drops from 5V to 0V, the voltage across C7 is held at 5V, which pulls the output of the charge pump to -5V. When the input voltage from IC1 returns to 5V, the output returns to 0V.

The floating ground will vary with the output of the half-bridge drive circuit, between the positive supply voltage, eg 330V, and normal ground, eg 0V. IC1 is initially powered by R1, C3 and R10. Once the output starts switching, it can utilise a bootstrap circuit (C4, R6, Z1 and D3) to provide a floating positive supply or a wattles capacitive supply fed via C10,C13. These capacitors can be those that

would be present, in any event, across the switches.

It is also noted that where a bipolar junction transistor (BJT) is used, the PNP device may have a much slower turn-off time. The resistor R5 has therefore been added to provide a base extraction current to address this. If a slow NPN device is used, this technique may also be used for that device.

Relative to the prior art, the invention removes the need for a level shifter, which is a high voltage circuit that is typically expensive and results in power loss, and hence reduced efficiency. The invention therefore reduces cost and increases efficiency relative to the prior art. In addition, the invention enables the drive circuitry (IC1) to be at low voltage, and enables the same drive circuitry to drive both the high- and low-side switches.

Figure 5 shows a simple integrated circuit implementation of the embodiment of Figure 4.

Figure 6 shows a further embodiment of the invention including a microprocessor, in which the ESD diodes on the ports of the microprocessor are utilised in the provision of a power supply for the microprocessor.

The circuit shown in Figure 7 is a power adaptor comprising an input recitifier bridge, an LCL series parallel circuit (L1, L2m C1b and C11) driven by an integrated circuit U1 and transistors Q1 and Q2, and an output rectifier bridge. This type of power adaptor is described in WO 2008/120019, WO 2010/041067, WO 2010/139992, WO 2011/083336 and WO 2012/010900.

This configuration provides a power adaptor suitable for solid state light sources, such as LEDs, that has a constant current draw and high efficiency. In particular, the output current becomes independent of output voltage and if the power adaptor is powered by a low frequency sine voltage input, and the output voltage is constant, ie an LED load, the input current becomes a low frequency, substantially square wave ideal for drive by a TRIAC dimmer as it maintains the

hold current at the lowest possible power whilst providing the LED with a current source that varies in brightness with the low frequency input voltage, ie it makes the LED act like a lamp bulb and enables control by a TRIAC dimmer at vastly reduced power and high power factor relative to other power adaptor technology.

The capacitance of the LCL series-parallel resonant circuit shown in Figure 1 is provided by C1b and C11, which are connected in parallel. In addition, however, the circuit shown in Figure 7 provides the possibility of switching C11 out of the circuit using thyristor Q4, which is controlled by integrated circuit U1 via level shifter Q3. Where C11 is switched out, the capacitance of the LCL series-parallel resonant circuit is significantly reduced to the capacitance of C1b only.

The power adaptor may therefore have a first mode where the capacitance of the LCL series-parallel resonant circuit is provided by C1b and C11, and a second mode where the capacitance of the LCL series-parallel resonant circuit is provided by C1b only and is therefore much lower. The first mode provides a higher current draw, and hence a higher power draw, relative to the second mode. The first mode may therefore be used to draw the latch current, and the dead band may then be varied to draw the (usually lower) hold current. For stable, low power lamps, however, the second mode may be utilised.

When entering the second mode by switching C11 out of the circuit, the integrated circuit U1 changes the drive frequency and dead band to that required for the modified resonant circuit to work. This allows for a much lower power for use by low power lamps, allowing the double hold principle to be used where the resonant circuit is used with mains supply, trailing edge and leading edge dimmers, where the lamp is stable. If instability is detected or it's preferred to switch modes on detection of the leading edge, the mode can be changed by switching C11 back into the circuit, thereby drawing significantly higher power and the required hold current.

The circuit shown in Figure 7 may be modified to enable the capacitance of the LCL series-parallel resonant circuit to be switched out entirely, thereby leaving an

LC resonant circuit. This may be achieved by removing C1b entirely, or enabling it to be switched out of the circuit by the integrated circuit U1. In this modified configuration, the LCL resonant circuit changes to an LC resonant circuit comprised of L1+L2 in series with C9. The integrated circuit U1 changes the drive frequency and dead band to that required for the LC resonant circuit to work. It has been found that the LC resonant circuit may be driven to provide the same properties as those of the LCL series-parallel resonant circuit discussed above, but only where the LED has a voltage comparable, eg at least +/-50%, or preferably +/-25%, to the rms voltage of the AC power supply.

For both of these alternatives, a dead band in the driving signal fed to the resonant circuit may be used to decrease the power to the LED and still draw the same current. The dead band may therefore be used to allow a lower amount of power to the LED, where the overall power is increased to allow the latch current to be drawn, which is often higher than the hold current. This removes the need for RC bleeder circuits.

Since the integrated circuit U1 is driving BJT transistors, which require +-0.7V, the integrated circuit can be 2V. The integrated circuit's power may therefore be extracted by three forward biased diodes D11B, D12A, D12B. The volt drop across these diodes is stored in C3 for the integrated circuit U1.

The gain of the transistors Q1 and Q2 may be used for fast start with high efficiency. In particular, R6 and R7 feeds the base of Q1and Q2, which charges C3 at a rate set by R6 and R7 multiplied by the gain of the transistors Q1 and Q2. A few micro amperes loss in efficiency may therefore become a few milli amperes of charge for C3.

A further possible modification of the circuit shown in Figure 7 is to reduce the inductance of L2 significantly, or even remove L2 entirely, thereby leaving an LC resonant circuit formed by L1 and C1b+C11. It has been found that the LC resonant circuit may be driven to provide the same properties as those of the LCL series-parallel resonant circuit discussed above, but only where the LED has a

voltage comparable, eg at least +/-50%, or preferably +/-25%, to the rms voltage of the AC power supply.

The circuit shown in Figure 8 is a power adaptor comprising an LCL series parallel circuit (L1, L2 and C1) driven by an integrated circuit IC1 and transistors Q1 and Q2, and an output rectifier bridge. This type of power adaptor is described in WO 2008/120019, WO 2010/041067, WO 2010/139992, WO 2011/083336 and WO 2012/010900.

This circuit also includes an active damping circuit for limiting the current when high inrush currents are active. The active damping circuit comprises a resistor (R2) for damping the current spike or current inrush associated with the firing of a TRIAC, together with a constant current circuit formed by Q5, R10, D1 and D2. When high inrush currents are active, the current is limited by R2 plus the constant current from the constant current circuit. When the circuit does not see high inrush, the constant current circuit feeds the LCL resonant circuit. The constant current circuit is adapted to feed the LCL resonant circuit at a current greater than that needed by the resonant circuit, such that the voltage drop across the constant current circuit is minimised.

Claims

1. A power adaptor comprising an input for connection to an AC power supply, a resonant circuit coupled to the input that provides an output suitable for driving a load, at least one half-bridge drive circuit for providing a drive signal to the resonant circuit, and a switch controller for the half-bridge drive circuit, the half-bridge drive circuit having a high-side switch and a low-side switch, and the switch controller being adapted to provide one or more of the following, in at least one mode:

(i) to provide the high-side switch and the low-side switch with on-times of different durations,

(ii) to provide the high-side switch and the low-side switch with on-times that overlap, and

(iii) to provide the high-side switch and the low-side switch with on-times that are synchronous.

2. A power adaptor as claimed in Claim 1, wherein the switch controller provides the high-side switch and the low-side switch with on-times of different durations, ie asymmetric on-times, such that the degree of asymmetry between the high-side switch and the low-side switch at least partially determines the current drawn from the input.

3. A power adaptor as claimed in Claim 2, wherein the current drawn at the input is substantially equal to the current provided at the output.

4. A power adaptor as claimed in Claim 1 or Claim 2, wherein the switch controller is adapted to vary the degree of asymmetry between the high-side switch and the low-side switch during each input cycle to determine the waveform of the current drawn from the input.

5. A power adaptor as claimed in any preceding claim, wherein the switch controller provides the high-side switch and the low-side switch with on-times that overlap, which creates a load condition in the period of overlap, in each input

cycle, and increases the current drawn at the input relative to the current delivered to the output in the period of overlap, in each input cycle.

6. A power adaptor as claimed in Claim 5, wherein the power adaptor is adapted to drive a solid state light source, and is adapted to cause a latch current for a dimmer switch to be drawn in each input cycle, in the period of overlap, and a lower hold current to be drawn subsequently, in each input cycle, with the resonant circuit being driven at substantially the same frequency.

7. A power adaptor as claimed in any preceding claim, wherein the power adaptor has a mode in which no power is provided at the output, but the power adaptor provides a load condition to the input, by the switch controller providing the high-side switch and the low-side switch with simultaneous on-times.

8. A power adaptor as claimed in any preceding claim, wherein the power adaptor has a mode in which a load condition is generated by overlapping or synchronous on-times of the switches, and the controller is adapted to monitor the voltage of the power supply and determine whether the impedance of the load condition will be acceptable for the voltage of the power supply.

9. A power adaptor as claimed in any preceding claim, wherein the power adaptor is adapted to switch between two or more modes, which each provide a different configuration of on-times for the high-side switch and the low-side switch.

10. A power adaptor as claimed in Claim 9, wherein the resonant circuit is driven at, or approximately at, its resonant frequency or a sub-harmonic thereof in each mode.

11. A power adaptor as claimed in any preceding claim, wherein the power adaptor is adapted to monitor the input voltage, and alter the ratio between the current provided at the output and the resistance across the input, based on that input voltage.

12. A power adaptor as claimed in Claim 11, wherein the ratio between the current provided at the output and the resistance across the input is altered proportionally based on the input voltage, such that sudden changes in current and/or input resistance are not created when switching modes.

13. A power adaptor as claimed in any preceding claim, wherein the high- and low-side switches are bipolar junction transistors (BJTs).

14. A power adaptor as claimed in any preceding claim, wherein the resonant circuit is an LCL series-parallel resonant circuit.

15. A power adaptor as claimed in any preceding claim, wherein the power adaptor is adapted to maintain a substantially constant current input for varying input voltages.

16. A power adaptor as claimed in any one of Claims 1 to 14, wherein the power adaptor is adapted to draw a substantially sinusoidal current waveform from the mains supply by the switch controller providing the high-side switch and the low-side switch with on-times of different durations, ie asymmetric on-times, and varying the degree of asymmetry between the high-side switch and the low-side switch during each input cycle to provide the current drawn from the input with a substantially sinusoidal waveform.

17. A power adaptor as claimed in any preceding claim, wherein the high-side switch and the low side switch of the half-bridge drive circuit are arranged with their respective emitter or source terminals connected at the centre of the half bridge.

18. A power adaptor as claimed in Claim 17, wherein the high-side switch is an NPN bipolar junction transistor (BJT), and the low-side switch is a PNP bipolar junction transistor (BJT).

19. A power adaptor as claimed in any preceding claim, wherein the switch

controller takes the form of an integrated circuit, and the ground connection of the switch controller is connected to the emitter or source terminals of the high-side switch and the low side switch, such that the ground connection of the switch controller has a reference common to the high-side switch and the low side switch in the form of a floating ground.

20. A power adaptor as claimed in any preceding claim, wherein the power adaptor is adapted to drive solid state light sources from a mains supply including a conventional dimmer switch.

21. A power adaptor as claimed in any preceding claim, wherein the power adaptor is adapted to drive a motor.

22. A half-bridge drive circuit comprising a high-side switch and a low side switch, each having an emitter or source terminal, wherein the high-side switch and the low side switch are arranged with their respective emitter or source terminals connected at the centre of the half bridge.

23. A half-bridge drive circuit as claimed in Claim 22, wherein the circuit is adapted to enable both the high-side switch and the low side switch to be turned on together, such that a load is generated.

24. A half-bridge drive circuit as claimed in Claim 23, wherein the high-side switch and the low side switch are driven by drive circuitry, which includes at least an oscillator, and this drive circuitry is configured to turn on both the high-side switch and the low side switch to generate a load at any one of the following, or any combination of multiples thereof:

(a) at startup of the half-bridge drive circuit;

(b) when power is absent for a pre-determined amount of time; and

(c) when power is absent.

25. A half-bridge drive circuit as claimed in any preceding claim, wherein the circuit drives an LCL series-parallel resonant circuit.

26. A half-bridge drive circuit as claimed in Claim 25, wherein the half-bridge drive circuit is driven using an oscillator, without any feedback to the oscillator.

27. A half-bridge drive circuit as claimed in any one of Claims 22 to 26, wherein the high-side switch and the low side switch are driven by drive circuitry, which includes at least an oscillator, and this drive circuitry is configured to provide a reduced power mode by replacing a series of pulses with a period in which both the high-side switch and the low side switch are turned off.

28. A half-bridge drive circuit as claimed in Claim 27, wherein a half-power mode is provided by replacing a series of pulses with a period in which both the high-side switch and the low side switch are turned off, the period being substantially the same as the period of the replaced series of pulses.

29. A half-bridge drive circuit as claimed in any one of Claims 22 to 28, wherein the high-side switch and the low side switch are driven by drive circuitry, which includes at least an oscillator, and this drive circuitry is configured to provide a mode in which power is drawn for only a first part of an AC input cycle, eg 90° of a 180° mains power cycle.

30. A half-bridge drive circuit as claimed in Claim 29, wherein power is drawn for approximately a first half of an AC input cycle.

31. A half-bridge drive circuit as claimed in any one of Claims 22 to 30, wherein the circuit includes a low voltage process integrated circuit, and the high-side switch and the low side switch are external of the integrated circuit

32. A half-bridge drive circuit as claimed in any one of Claims 22 to 31, wherein the circuit includes a microprocessor, and the ESD diodes on the ports of the microprocessor are utilised as charge pump diodes in the provision of a power supply for the microprocessor.

33. A half-bridge drive circuit as claimed in any one of Claims 22 to 32, wherein the high-side switch is an n-channel field-effect transistor (FET), an NPN bipolar junction transistor (BJT), or a similarly functioning transistor.

34. A half-bridge drive circuit as claimed in any one of Claims 22 to 33, wherein the low-side switch is a p-channel field-effect transistor (FET), a PNP bipolar junction transistor (BJT), or a similarly functioning transistor.

35. A half-bridge drive circuit as claimed in any one of Claims 22 to 34, wherein the switches are configured with a switching voltage at the base or gate terminal that is determined relative to the voltage at the emitter or source terminal, and the connection between the emitter or source terminals of the high-side switch and the low side switch provides a common reference for the switching voltage of the high-side switch and the low-side switch in the form of a floating ground.

36. A half-bridge drive circuit as claimed in any one of Claims 22 to 35, wherein the low-side switch has a negative switching voltage at its base or gate terminal that is determined relative to a common reference in the form of a floating ground.

37. A half-bridge drive circuit as claimed in any one of Claims 22 to 36, wherein the high-side switch and the low side switch are driven by drive circuitry, which includes at least an oscillator.

38. A half-bridge drive circuit as claimed in any one of Claims 22 to 37, wherein the ground connection of the drive circuitry is connected to the emitter or source terminals of the high-side switch and the low-side switch, such that the ground connection of the drive circuitry has a reference common to the high-side switch and the low side switch in the form of a floating ground.

39. A half-bridge drive circuit as claimed in Claim 37 or Claim 38, wherein a capacitor connected across each of the high- and low-side switches provide power to the drive circuitry, once oscillating.

40. A half-bridge drive circuit as claimed in any one of Claims 37 to 39, wherein the drive circuitry is adapted to vary the deadband of the half-bridge drive circuit, thereby enabling the half-bridge drive circuit to draw the same current, but provide an output at a lower efficiency.

41. A half-bridge drive circuit as claimed in Claim 40, wherein a load condition is created by turning on both the high- and low-side switches at the same time.

42. A half-bridge drive circuit as claimed in any one of Claims 22 to 41, wherein the drive circuitry is configured to also control an output stage, such as a rectifier circuit having multiple modes of operation, as described in WO 2011/083336 A2 and WO 2012/010900 A2.

43. A power adaptor comprising a half-bridge drive circuit as claimed in any one of Claims 22 to 42.

44. A power adaptor as claimed in Claim 43, wherein the half-bridge drive circuit drives a resonant circuit for providing power to a load, such as a solid state light source, eg one or more LEDs.

45. A power adaptor as claimed in Claim 44, wherein the power adaptor also includes an output rectifier.

46. A power adaptor as claimed in any one of Claims 43 to 45, wherein the power adaptor comprises an input for connection to a mains power supply, and an LCL series-parallel resonant circuit coupled to the input that provides an output suitable for driving a load, wherein the half-bridge drive circuit drives the LCL series-parallel resonant circuit.

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Figure 1

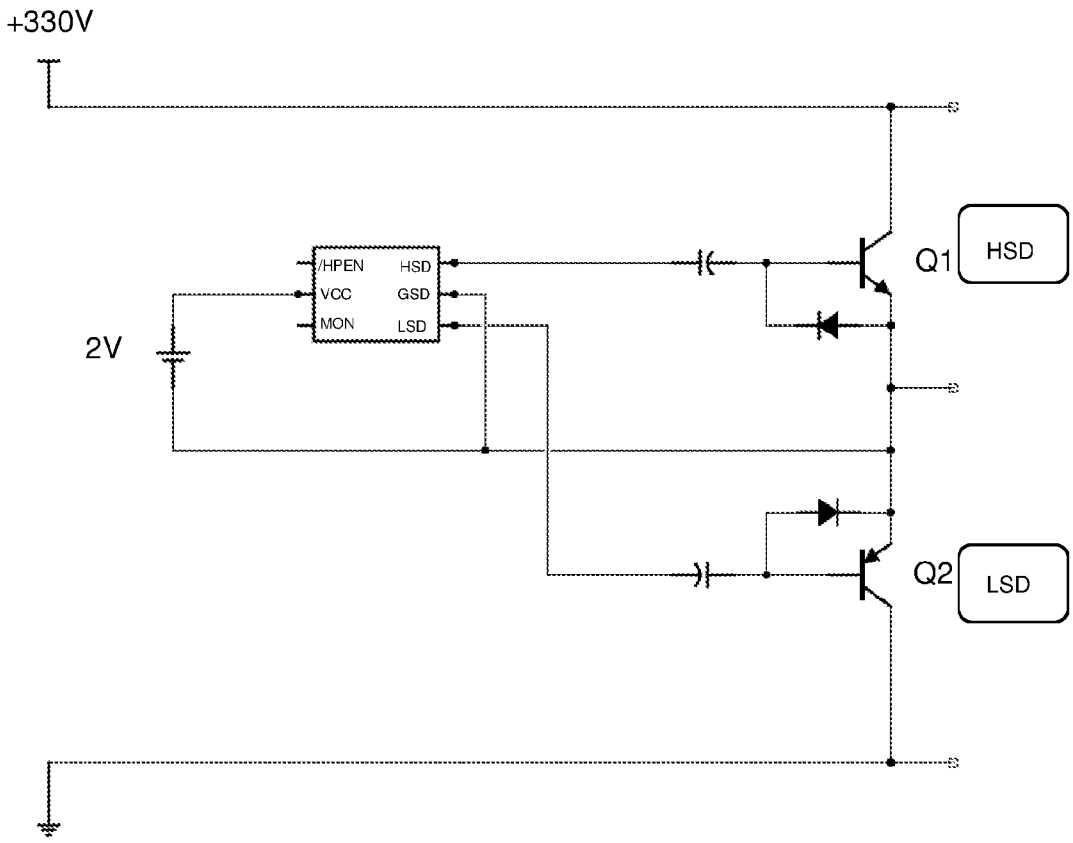

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Figure 2

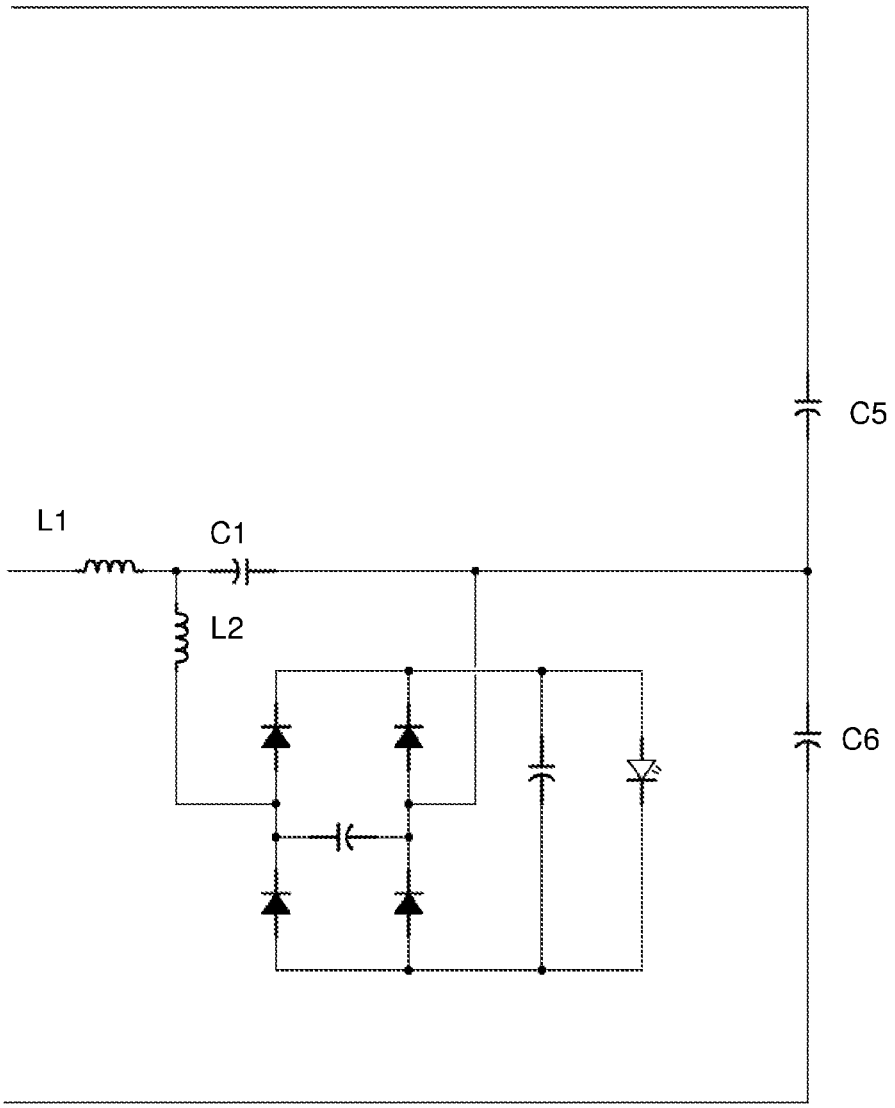

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Figure 3a

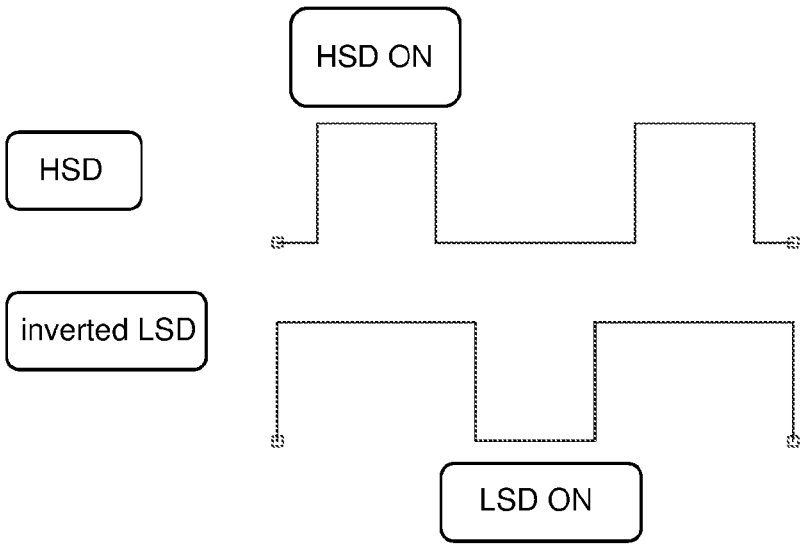


Figure 3b

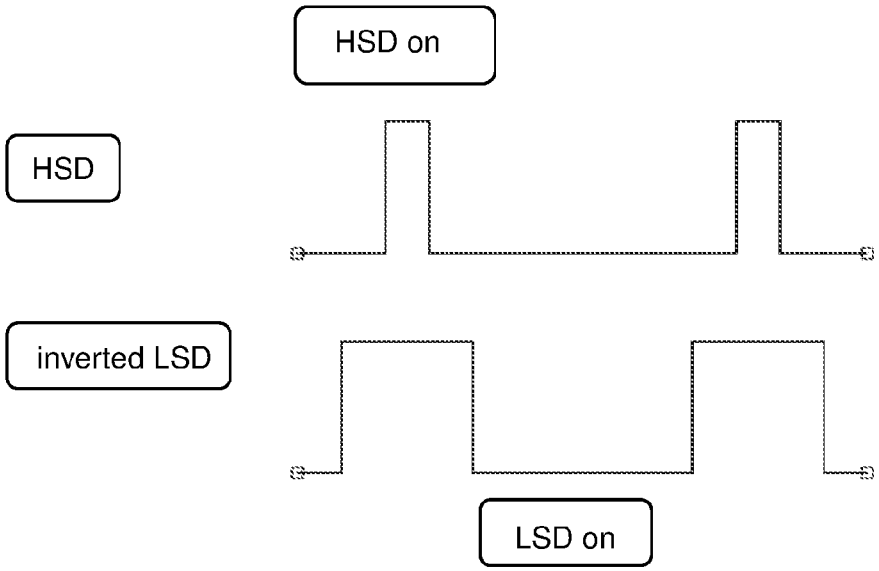


Figure 3c

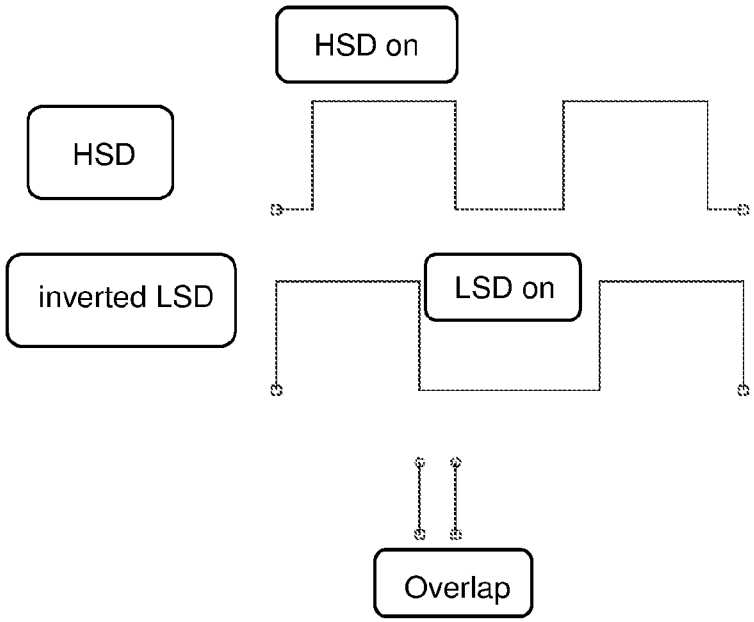
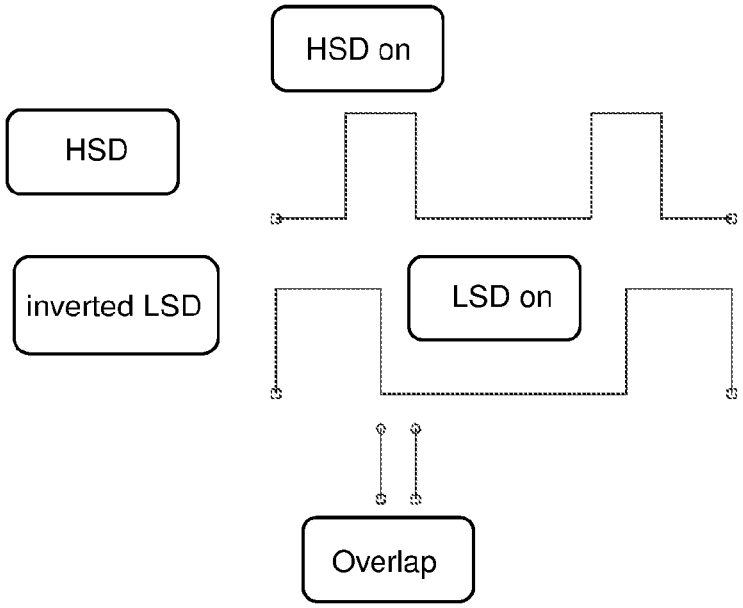


Figure 3d



5/10

Figure 3e

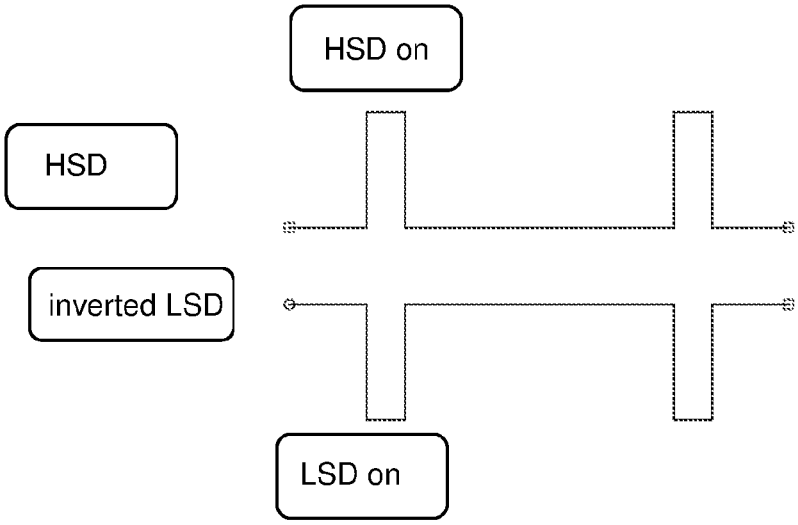
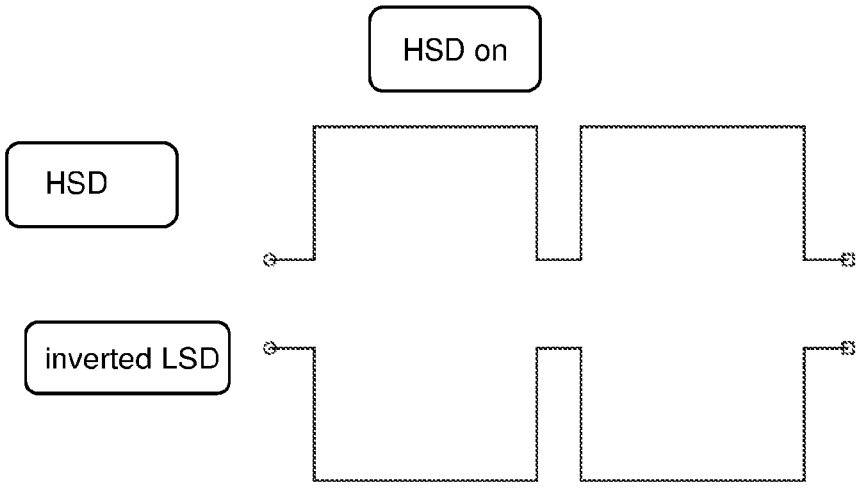


Figure 3f



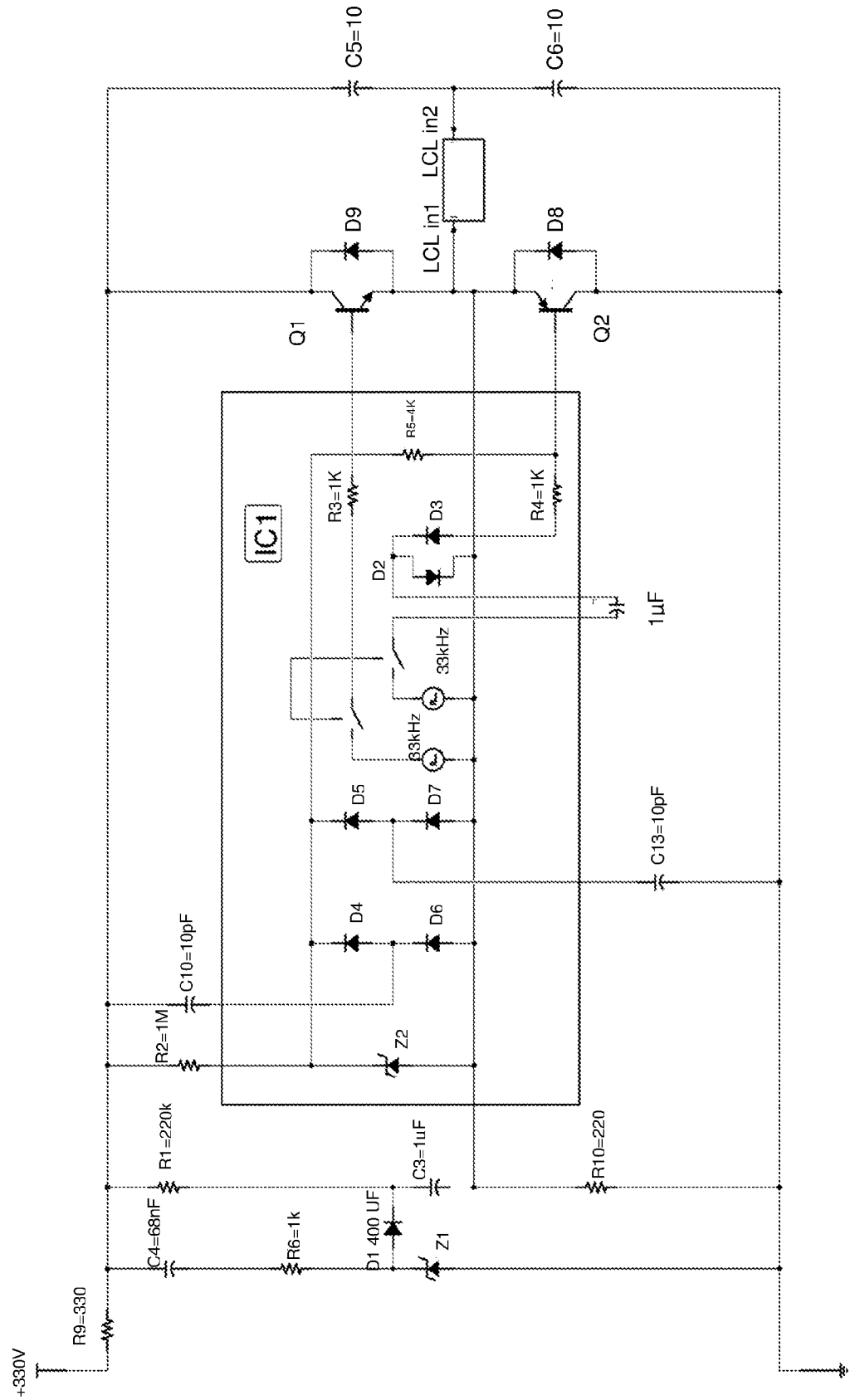

C5=10
C6=10
LCL in2
LCL in1
D9
D8
Q1
Q2
IC1
R5=4K
R3=1K
R4=1K
D3
D2
1µF
33kHz
33kHz
D5
D7
C13=10pF
D4
D6
C10=10pF
R2=1M
Z2
R1=220k
C3=1uF
R10=220
C4=68nF
R6=1k
D1 400 UF
Z1
R9=330
+330V

Figure 4

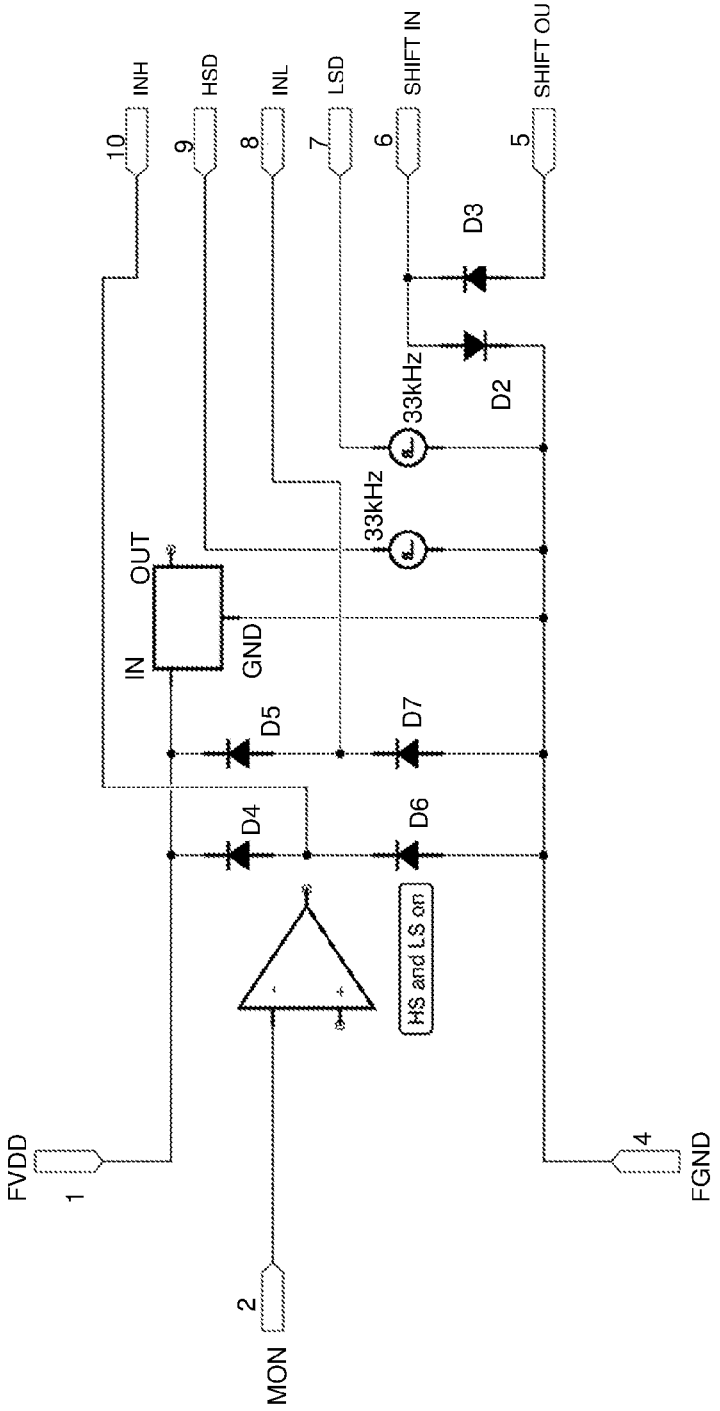

INH
HSD
INL
LSD
SHIFT IN
SHIFT OU
10
9
8
7
6
5
D3
D2
33kHz
33kHz
OUT
IN
GND
D5
D7
D4
D6
HS and LS on
FVDD
1
2
MON
4
FGND

Figure 5

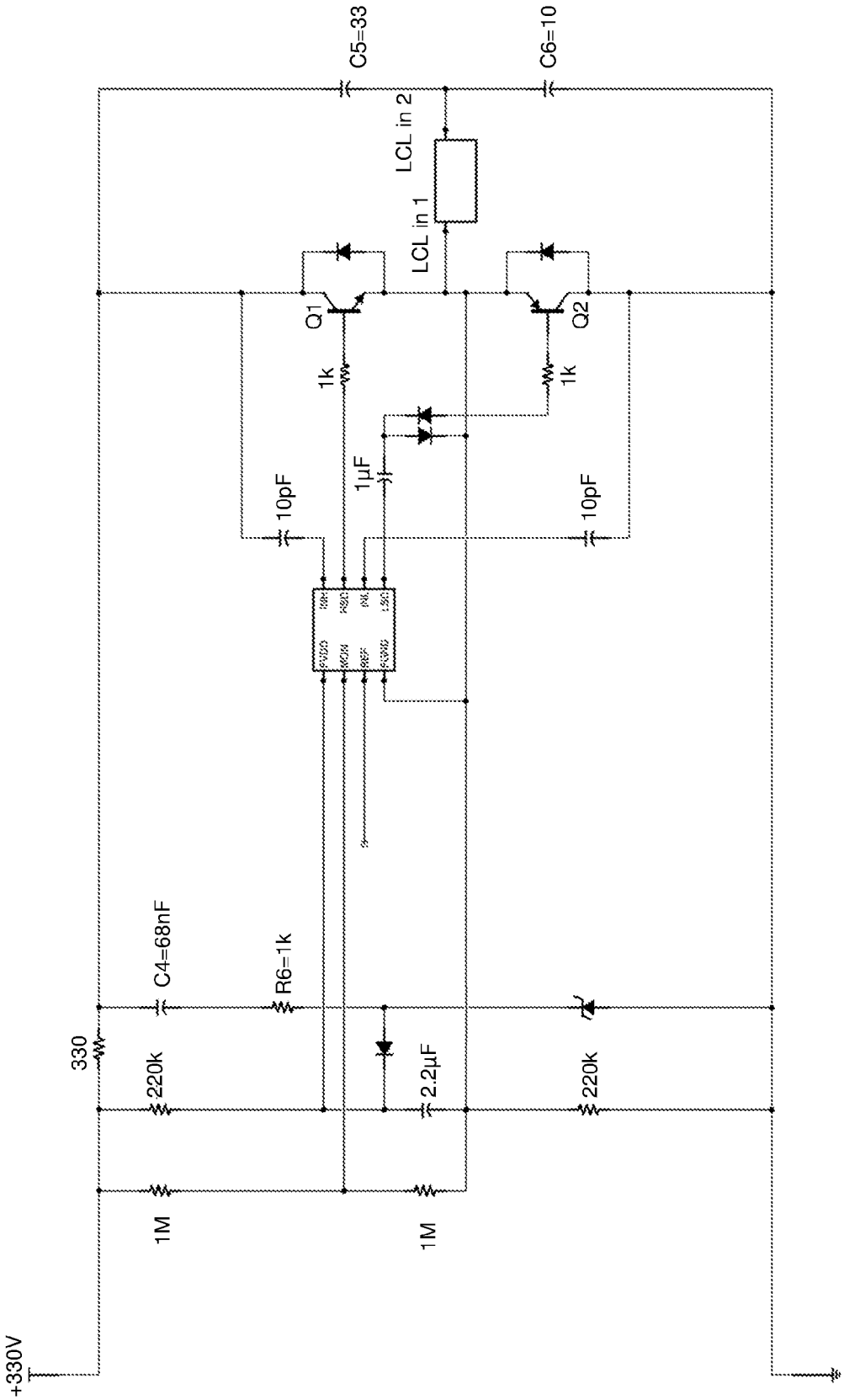

C5=33
C6=10
LCL in 2
LCL in 1
Q1
Q2
1k
1k
10pF
1µF
10pF
C4=68nF
R6=1k
330
220k
2.2µF
220k
1M
1M
+330V

Figure 6

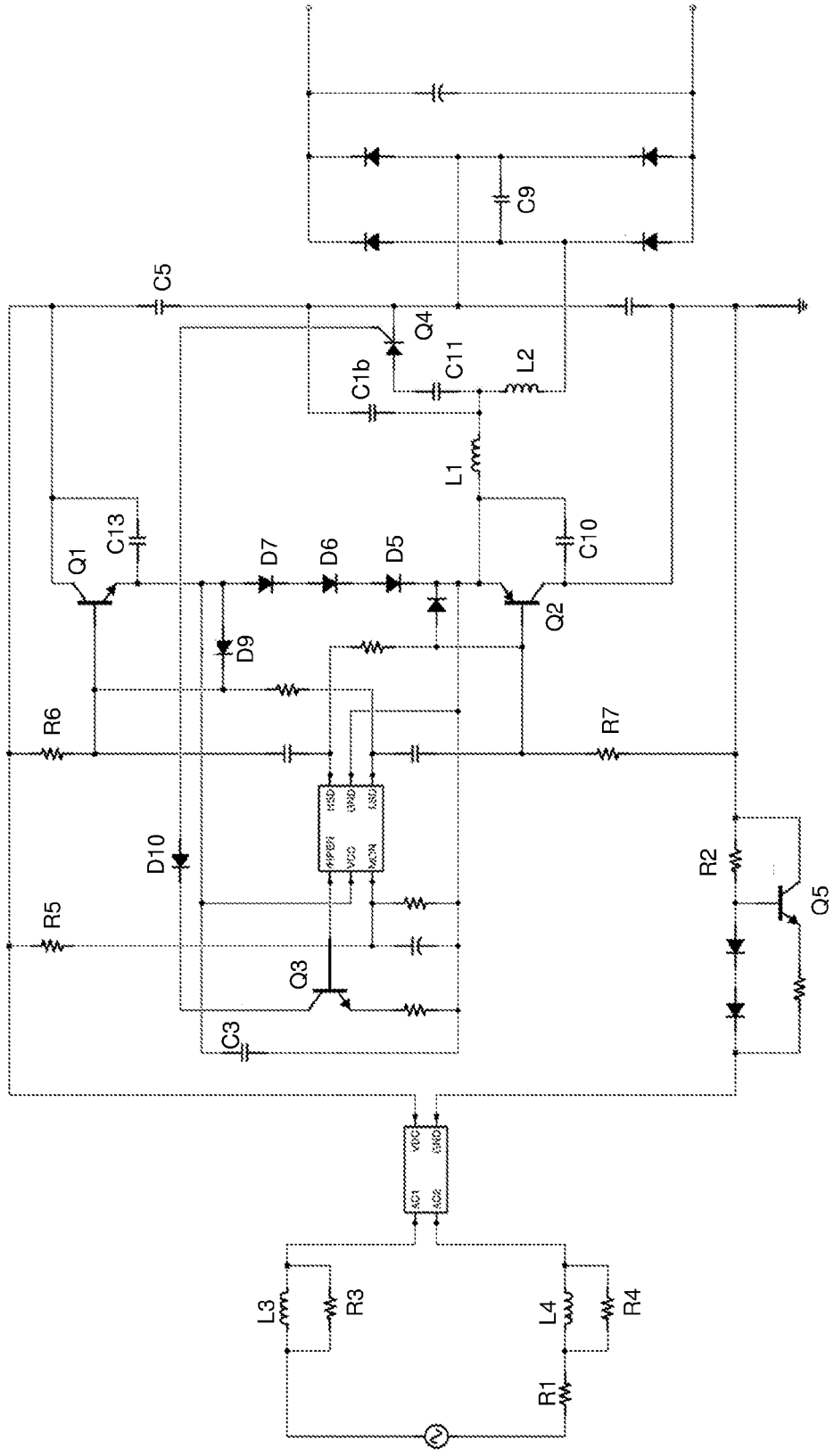

C9
C5
Q4
C11
L2
C1b
L1
C13
Q1
D7
D6
D5
C10
Q2
D9
R6
R7
D10
R2
Q5
R5
Q3
C3
L3
R3
L4
R4
R1

Figure 7

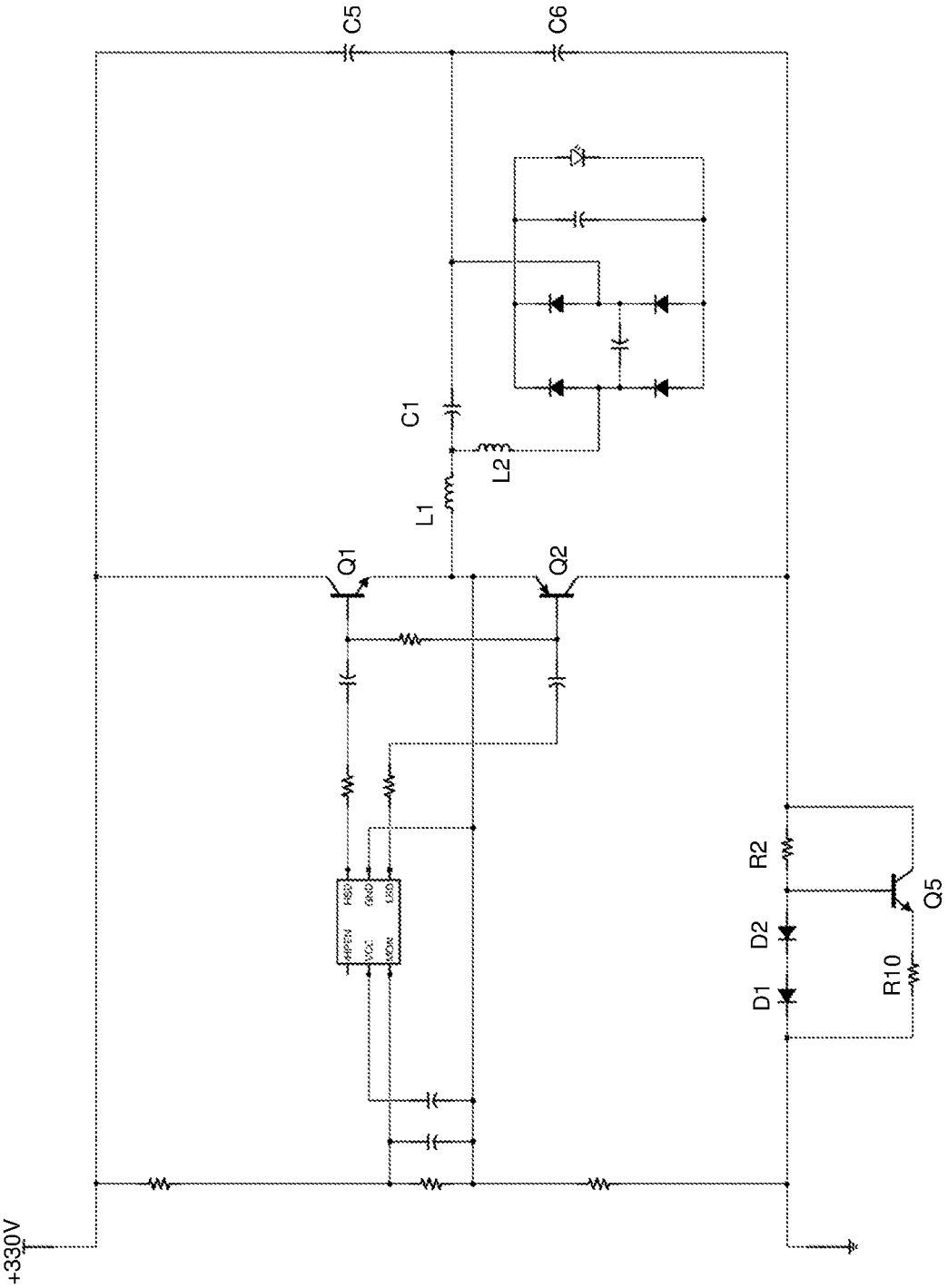


Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2014/051602

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05B33/08 H02M1/38 H02M5/275
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05B H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/249003 A1 (ESAKI SANA [JP] ET AL) 4 October 2012 (2012-10-04)	1-4,7, 9-22, 25-41, 43-46
A	page 1, paragraph 6 - page 5, paragraph 64; figures 1-5	5,6,8, 23,24

X	WO 2005/048658 A1 (PHILIPS INTELLECTUAL PROPERTY [DE]; KONINKL PHILIPS ELECTRONICS NV [NL] 26 May 2005 (2005-05-26) the whole document	1,22

X	US 2009/295300 A1 (KING RAY JAMES [US]) 3 December 2009 (2009-12-03) the whole document	1,22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 August 2014	26/08/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Burchielli, M

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2014/051602

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 42
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2014/051602

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012249003 A1	04-10-2012	CN 102740547 A	17-10-2012
		JP 2012221599 A	12-11-2012
		US 2012249003 A1	04-10-2012
WO 2005048658 A1	26-05-2005	CN 1879453 A	13-12-2006
		EP 1685745 A1	02-08-2006
		JP 5122141 B2	16-01-2013
		JP 2007511903 A	10-05-2007
		KR 20060115874 A	10-11-2006
		TW I393112 B	11-04-2013
		US 2007080652 A1	12-04-2007
		WO 2005048658 A1	26-05-2005
US 2009295300 A1	03-12-2009	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 42

Claim 42 relies on references to the description of other documents (WO 2011/083336 A2 and WO 2012/010900 A2) cited in the description of the present application, which is not allowed under Rule 6.2(a) PCT. In this respect, it is not understandable which is the subject-matter for which the protection is sought, and consequently a meaningful search is rendered impossible.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-IV, 7.2), should the problems which led to the Article 17(2) declaration be overcome.

摘要

一种电源适配器，包括：用于连接至 AC 电源的输入端；谐振电路(LCL)，其耦接至输入端且提供适合于驱动负载(LCL)的输出端；用于向谐振电路提供驱动信号的至少一个半桥驱动电路(Q1，Q2)；以及用于半桥驱动电路的开关控制器(IC1)。开关控制器(IC1)适于以至少一种模式提供以下动作中的一种或多种：(i)向高侧开关和低侧开关提供不同持续期的接通时间；(ii)向高侧开关和低侧开关提供重叠的接通时间；以及(iii)向高侧开关和低侧开关提供同步的接通时间。这可以用于控制传送至输出端的电流，而没有任何必要改变驱动谐振电路的频率。