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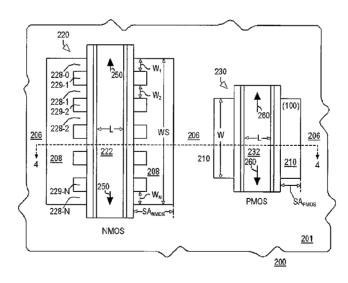
- (71) Applicant (for all designated States except US): FREESCALE SEMICONDUCTOR INC. [US/US]; 6501 William Cannon Drive West, Austin, Texas 78735 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): NGUYEN. Bich-yen [US/US]; 110 Laurelwood Drive, Austin, Texas 78733 (US). THEAN, Voon-vew [SG/US]; 10201 Lockleven Cove, Austin, Texas 78750 (US).
- (74) Agents: KING, Robert, L. et al.; 7700 W. Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

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(54) Title: SELECTIVE UNIAXIAL STRESS RELAXATION BY LAYOUT OPTIMIZATION IN STRAINED SILICON ON INSULATOR INTEGRATED CIRCUIT



(57) Abstract: An integrated circuit (200) includes NMOS and PMOS transistors (220, 230). The NMOS (220) has a strained channel having first and second stress values along first and second axes respectively. The PMOS (230) has a strained channel having third and fourth stress values along the first and second axes. The first value stress differs from the third value and the second value differs from the fourth value. The NMOS (220) and PMOS (230) have a common length (L) and effective width (W), but differ in length of diffusion (SA) and/ width of source/drain (WS). The NMOS WS may exceed the PMOS WS. The NMOS (220) may include multiple dielectric structures in the active layer underlying the gate The SA of the PMOS (230) may be less than the SA of the NMOS (220).



#### INTERNATIONAL SEARCH REPORT

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C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category*	Citation of document, with indication, where ap	propriate, of the relevant passages	Relevant to claim No.
X	US 2006/0043500 A1 (CHEN et al) 02 March 2006 (02	.03.2006), see whole document.	1-3, 5, 6, 15, 16, 19
Y			4, 7-14, 17-18, 20
Y	US 2005/0139872 A1 (CHIDAMBARAM et al) 30 June 2005 (30.06.2005), see whole document.   7-14, 20		
Υ	US 6,815,770 B1 (CHIEN et al) 09 November 2004 (09.11.2004), see whole document.		4, 8-10, 12-14, 17, 18
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