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(54) **Title**: COMPLIANT PRINTED CIRCUIT AREA ARRAY SEMICONDUCTOR DEVICE PACKAGE

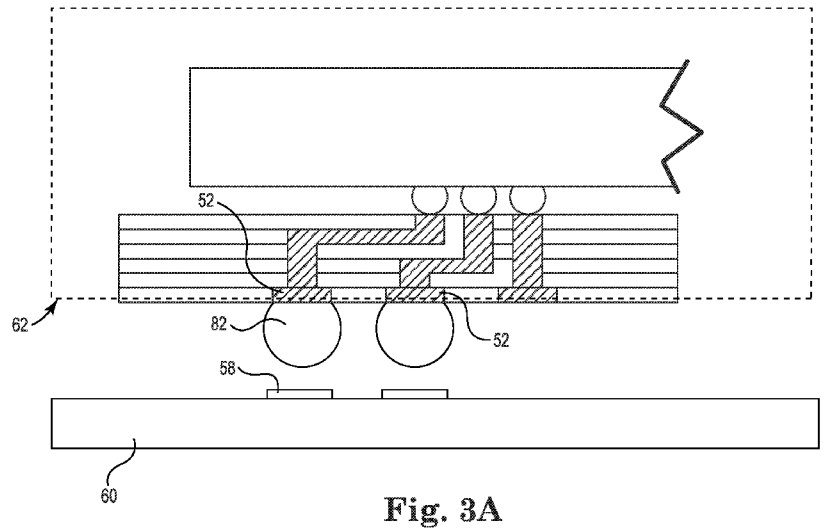

Fig. 3A

(57) **Abstract**: An integrated circuit (IC) package for an IC device, and a method of making the same. The IC package includes an interconnect assembly with at least one printed compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of printed conductive traces electrically coupling a plurality of the first and second contact members. The compliant layer is positioned to bias at least the first contact members against terminals on the IC device. Packaging substantially surrounds the IC device and the interconnect assembly. The second contact members are accessible from outside the packaging.

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COMPLIANT PRINTED CIRCUIT AREA ARRAY SEMICONDUCTOR DEVICE PACKAGE

Technical Field

[0001] The present disclosure relates to a compliant array integrated circuit (IC) device package, and in particular, to a compliant IC device package made using an additive printing process.

Background of the Invention

[0002] Traditional semiconductors and IC devices are typically formed on a substrate using photolithography. The substrate may be a silicon wafer. Multiple IC devices are typically formed on a single wafer and then the wafer is cut into die. The IC devices are typically packaged in a variety of ways to provide redistribution from the terminals on the die to a spacing that is conducive to cost effective printed circuit board (PCB) fabrication techniques. The package also serves to protect the fragile silicon or provide additional functions such as thermal management or near device decoupling. In many cases, the size and distance between die terminals is so small that the IC device cannot be connected to the final PCB without some sort of re-routing interface. In such cases, the package can provide the re-routing interface.

[0003] Most IC devices are produced with terminals in either a peripheral pattern that runs along the edges of the IC device or an area array pattern that spans across the surface of the IC device. A main method for attachment when the terminals are in an area array pattern is to connect the terminals with solder. Basically, the package has an array of terminals that correspond to the IC device terminals. Solder is applied to the terminals on the IC device and/or the package and reflowed to create the mechanical and electrical connection in a process commonly called flip chip attachment. In a flip chip attachment the IC device is flipped over to mate the terminals on the die to the terminals on the IC package substrate.

[0004] After an IC device is positioned in this type of package and attached to the package terminals, the package is often under filled with an epoxy of some type to provide support and strength to the solder joints. The epoxy protects the solder joints from thermal expansion, miss-match and/or shock during use. Regardless of whether a package is under filled with epoxy, the connection of the IC device to the

package is generally not reworkable after packaging, and if there is a missing or broken connection it is difficult to repair.

[0005] Once the IC devices are packaged, the IC devices are usually tested in a variety of ways to determine the reliability and performance of the IC devices in the package. The IC devices may be tested as they would be used in a final application. In many cases, the functional performance of the IC device is not known prior to placing it into the package. If the packaged IC device fails testing then the cost of the package and manufacturing process is lost.

[0006] Area array packaging has been utilized for many years, and provides a method for interconnecting IC devices with larger terminal counts than peripheral lead packaging. In general, the area array packaging is more expensive due to the larger pin counts and more sophisticated substrates required. The limitations for area array packaging include the terminal pitch, thermal management, cost, ability to rework faulty IC devices and reliability of the solder joints.

[0007] There also has been advancements in recent years in both area array packaging and peripheral lead packaging where multiple IC devices are placed in the same package, creating what has been nicknamed SiP for "system in package." Placing multiple IC devices in a single package further complicates the problems discussed above.

Brief Summary of the Invention

[0008] The present application relates to a compliant array IC device package (IC package). The present IC package is inexpensive to produce, has relative long life and provides excellent electrical performance.

[0009] The present disclosure can leverage the capabilities of the additive printing process to provide a high performance IC package capable of interconnecting a single device or multiple IC devices, while providing at or near terminal compliance to increase interconnect reliability. The unique nature of the additive printing process allows for a direct writing of circuitry and dielectrics, with the added benefit of stress decoupling at the terminal joints as well as embedded function not seen in traditional IC packaging. The additive printing process allows for packaging that provides very high frequency performance, as well as the addition of on-board electrical devices and circuitry planes that are not available with other IC packages.

[0010] The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and circuit fabrication methods take sheets of material

and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0011] The production cost for the IC packages in accordance with the present disclosure can be a fraction the cost of producing existing IC packages. The use of additive printing processes, such as for example to print electrical features, can reduce capital cost and lead time for building the present IC packages. The additive printing processes also increase production yields over conventional IC packages that rely on conventional lithography tools and masks.

[0012] Internal compliance of the interconnect assembly in the present IC package can greatly increase performance over conventional IC packages. The ability to build multi-layer structures over a relatively large area permits terminal pitch on the IC devices to be reduced. The addition of circuitry planes and electrical devices in the present IC package provides performance enhancements not available with current IC packages. The ability to add electrical devices, such as transistors and memory, to the present IC package provides the opportunity to incorporate intelligence directly into the package.

[0013] One embodiment of the present disclosure is directed to an IC package for an IC device. The IC package can include an interconnect assembly with at least one printed compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of printed conductive traces electrically coupling a plurality of the first and second contact members. The compliant layer can be positioned to bias at least the first contact members against terminals on the IC device. Packaging may substantially surround the IC device and the interconnect assembly. The second contact members are accessible from outside the packaging.

[0014] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to recesses or cavities in one or more previously applied layers. The use of additive printing

processes permit conductive material, non-conductive material, and semi-conductive material to be located on a single layer.

[0015] In one embodiment, pre-formed conductive trace materials are positioned in the cavities. The cavities are than plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the cavities. The conductive foil is sheared along edges of the cavities. The excess conductive foil not positioned in the cavities is removed and the cavities are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0016] The interconnect assembly can typically include a plurality of printed dielectric layers. The interconnect assembly can optionally include at least one additional circuitry plane. The additional circuitry plane can be one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, or a flexible circuit. The contact members may typically be made from one of a curable conductive material, sintered conductive particles, or a platable material.

[0017] In one embodiment, the interconnect assembly extends beyond a perimeter edge of the IC package. In another embodiment, a flexible circuit member is electrically coupled to the interconnect assembly and extends beyond a perimeter edge of the IC package.

[0018] At least one electrical device can be optionally printed on the interconnect assembly and electrically coupled to one or more of the conductive traces. The electrical device can be selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded ICs, RF antennae, and the like. In another embodiment, at least one electrical device can be printed on the packaging.

[0019] The packaging can include one or more of a preformed package, an encapsulating material, or a combination thereof.

[0020] The present disclosure is also directed to an IC package, including an interconnect assembly in accordance with one of the embodiments of the present disclosure. Terminals on at least one IC device can be compressively engaged with the first contact members so the compliant layer biases the first contact members against the terminals on the IC device. Packaging substantially surrounds the IC device and the interconnect assembly so the second contact members can be accessible from outside the packaging.

[0021] In one embodiment, a plurality of IC devices are electrically coupled to the interconnect assembly. In another embodiment, a plurality of interconnect assemblies can be electrically coupled to one or more of the second contact members and a plurality of IC devices are each electrically coupled to one of the interconnect assemblies.

[0022] The present disclosure is also directed to an electrical system including an IC package in accordance with one of the embodiments of the present disclosure and a PCB electrically coupled with the second contact members.

[0023] The present disclosure is also directed to a method of making an IC package. An interconnect assembly can be formed by printing at least one dielectric layer onto a surface of a fixture, depositing a conductive material comprising first contact members, printing a compliant layer along at least the first contact members, and printing a plurality of conductive traces electrically coupled with one or more of the first contact members. A plurality of second contact members can be formed along a second major surface of the interconnect assembly. The interconnect assembly can be removed from the fixture. Terminals on at least one IC device can be compressively engaged with the first contact members. The compliant layer can bias the first contact members against the terminals on the IC device. The IC device and the interconnect assembly can be substantially surrounded by packaging. The second contact members can be accessible from outside the packaging.

[0024] In one embodiment, conductive material can be deposited into a plurality of the cavities in the fixture. The conductive material can be deposited using for example inkjet printing technology, aerosol printing technology, and other maskless deposition techniques. The conductive material can be processed to form the plurality of contact members along the first and second major surfaces of the interconnect assembly.

[0025] In another embodiment, a second base layer of a dielectric material can be printed onto a surface of a fixture using for example inkjet printing technology, aerosol printing technology, and other maskless deposition techniques. A conductive material can be deposited into a plurality of the cavities in the fixture. The conductive material can be processed to form a plurality of second contact members. The second contact members can be electrically coupled with the conductive traces on the interconnect assembly so the second contact members extend along the second major surface of the interconnect assembly.

[0026] The method can include forming at least one additional circuitry plane in the interconnect assembly. The method can optionally include electrically coupling a flexible circuit member to the interconnect assembly and extending the flexible circuit member beyond a perimeter edge of the packaging. At least one electrical devices can be optionally printed on the interconnect assembly.

[0027] The present method is also directed to making an electrical assembly comprising the step of electrically coupling the second contact members on an IC package according to the present disclosure with a PCB.

Brief Description of the Several Views of the Drawing

[0028] Figure 1 is a cross-sectional view of a fixture for making an IC package in accordance with an embodiment of the present disclosure.

[0029] Figure 2 is a cross-sectional view of an IC package in accordance with an embodiment of the present disclosure.

[0030] Figure 3A is a cross-sectional view of an IC package with a ball grid array (BGA) interface in accordance with an embodiment of the present disclosure.

[0031] Figure 3B is a cross-sectional view of an IC package printed directly on another circuit member in accordance with an embodiment of the present disclosure.

[0032] Figure 4 is a cross-sectional view of an alternate fixture for making an IC package in accordance with an embodiment of the present disclosure.

[0033] Figure 5A is a cross-sectional view of an IC package in accordance with an embodiment of the present disclosure.

[0034] Figure 5B is a cross-sectional view of a solderless IC package in accordance with an embodiment of the present disclosure.

[0035] Figure 6 is a cross-sectional view of an alternate IC package with additional electrical functionality in accordance with an embodiment of the present disclosure.

[0036] Figures 7 and 8 are IC packages with additional compliance in accordance with an embodiment of the present disclosure.

[0037] Figures 9 and 10 are IC packages with terminal pad extensions in accordance with an embodiment of the present disclosure.

[0038] Figure 11 is an IC package with multiple IC devices in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0039] The present disclosure is directed to a compliant array IC package that is inexpensive to produce, has relative long life and provides excellent electrical performance. An IC package according to the present disclosure can be formed by an additive printing process to provide a high performance IC package capable of interconnecting a single device or multiple IC devices, while providing at or near terminal compliance to increase interconnect reliability. The unique nature of the additive printing process can allow direct writing of circuitry and dielectrics, while also allowing stress decoupling at the terminal joints as well as embedded function not seen in traditional IC packaging.

[0040] Printable silicon inks provide the ability to print electrical devices. Exemplary embodiments of printable silicone inks are disclosed, for example, in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. For example, conductive material can be deposited in the cavities using printing technology.

[0041] Printing process can preferably be used to fabricate various functional structures, such as conductive paths and electrical devices without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0042] U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated herein by reference, teach using inkjet printing to make various electrical devices, such as resistors, capacitors, diodes, inductors (or elements which can be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical

elements, transistors (including, light emitting, light sensing or solar cell elements, field effect transistors, top gate structures), and the like.

[0043] U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference, teach using aerosol printing to create various electrical devices and features.

[0044] Printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semiconductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0045] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or teflon.

[0046] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0047] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from Dupont located in Wilminton, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0048] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also

include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0049] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0050] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181 (Bridenbaugh et al.), which is incorporated herein by reference.

[0051] A protective layer can optionally be printed onto the electrical devices and features. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0052] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having

properties similar to those described above can be used in accordance with the present invention.

[0053] An inkjet print head, or other print head, preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0054] Alternatively, a separate print head can be used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0055] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electropneumatic, electrostatic, rapid ink heating, magnetohydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0056] The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0057] While inkjet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: premetered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure

coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; aerosol printing processes; and other similar techniques.

[0058] The additive printing process allows for packaging that provides very high frequency performance, as well as the addition of on-board electrical devices and circuitry planes that are not available with other IC packages.

[0059] An IC package according to the present disclosure can be used with IC devices having contact-to-contact spacing (pitch) on the order of less than about 1.0 millimeter (1×10^{-3} meters), and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter.

[0060] Figure 1 is a side cross-sectional view of a fixture 50 useful in making an IC package in accordance with an embodiment of the present disclosure. Metalized terminal pads 52 and a dielectric layer 54A can be preferably printed on surface 56 of the fixture 50 using for example inkjet printing technology, aerosol printing technology, and other maskless deposition techniques. The fixture 50 can be constructed from a variety of materials, such as for example metal, plastic, ceramics, and composites thereof. The surface 56 can be optionally coated with a material to facilitate release of the layer 54A and the terminal pads 52.

[0061] Although the terminal pads 52 are configured for use in a land grid array interface, the present printing process permits the terminal pads 52 to be configured to electrically couple with a wide variety of circuit members, including for example a flexible circuit, a ribbon connector, a cable, a printed circuit board (PCB), a ball grid array (BGA), a land grid array (LGA), a plastic leaded chip carrier (PLCC), a pin grid array (PGA), a small outline integrated circuit (SOIC), a dual in-line package (DIP), a quad flat package (QFP), a leadless chip carrier (LCC), a chip scale package (CSP), or packaged or unpackaged integrated circuits. See for example the fixture 100 in Figure 4.

[0062] Figure 2 is a cross-sectional view of an IC package 62, according to one embodiment of the present disclosure. As shown in Figure 2, additional dielectric layers 54B, 54C, 54D, 54E, 54F (collectively "54") can be printed on the fixture 50 along with conductive material 64 forming contact members 66A, 66B, 66C (collectively "66") to complete interconnect assembly 78. In one embodiment, the dielectric layers 54 are printed to create cavities 76 or recesses at the desired locations for depositing conductive material 64. The conductive material 64 may be,

for example, a metallic powder that can be sintered to create contact members 66 or a flowable, curable conductive material.

[0063] The conductive material 64 is preferably deposited in a first state and then processed to create a second more permanent state. For example, metallic powder can be deposited in the cavities 76 and subsequently sintered, or curable conductive material can flow into the cavities 76 and subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. The term "curable" refers to a characteristic of a material having the potential to be cured, such as for example by the application of a suitable energy source.

[0064] In the illustrated embodiment, conductive traces 68A, 68B route the contact members 66A and 66B to correspond to the terminals 70 on the IC device 72. The terminal pads 52 are arranged in an array that corresponds to contact pads 58 on a circuit member 60 to which the IC package 62 will be attached (see e.g., Figure 3A). Various methods for deposition of electronic materials may also be used to deposit the conductive material 64 in the cavities 76 or to print the dielectric layers 54, such as for example, screen printing, printing through a stencil, flexo-gravure printing, offset printing, inkjet printing, and aerosol printing as previously explained.

[0065] The cavities 76 in the layers 54 permit control of the location, cross section, material content, and aspect ratio of the contact members 66 and the conductive traces 68. Maintaining the conductive traces 68 with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the cavities 76 to control the aspect ratio of the conductive traces 68 can result in a more rectangular or square cross-section of the conductive traces, and a corresponding improvement in signal integrity.

[0066] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to recesses or trenches in the layers 54. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in

the recesses. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses.

[0067] In another embodiment, a thin conductive foil is pressed into the recesses, and the edges of the recesses acts to cut or shear the conductive foil. The process positions a portion of the conductive foil in the recesses, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses for easy removal. Again, the foil in the recesses are preferably post plated to add material to increase the thickness of the conductive traces and to fill any voids left between the conductive foil and the recesses.

[0068] In one embodiment, some or all of the dielectric layers 54 are a compliant material that provides the contact members 66 with a degree of compliance. In one embodiment, solder balls 70 are coupled to the IC device, but are not reflowed, and an electrical connection is formed by compressive forces. The compliant layers 54 bias the contact members 66 into engagement with the solder balls 70.

[0069] The interconnect assembly 78 and the IC device 72 are then enclosed in packaging 80. The packaging 80 can be a preformed structure, such as for example a plastic or ceramic substrate, an encapsulating material, or a combination thereof. In one embodiment, the packaging 80 is a curable material printed using the printing technology discussed herein. In another embodiment, the interconnect assembly 78 and IC device 72 are encapsulated in an epoxy material. The packaging 80 can be completed before or after the interconnect assembly 78 is removed from the fixture 50.

[0070] Figure 3A is a cross-sectional view of an IC package with a BGA interface in accordance with an embodiment of the present disclosure. Figure 3A illustrates the IC package 62 removed from the fixture 50 (shown in Figure 2). In the illustrated embodiment, solder balls 82 are attached to terminal pads 52. The solder 82 is preferably reflowed to electrically couple with contact pads 58 on a circuit member 60. The circuit member 60 can be another packaged integrated circuit device, an unpackaged integrated circuit device, a printed circuit board, a flexible circuit, a bare-die device, an organic or inorganic substrate, a rigid circuit, or any other device

capable of carrying electrical current. In another embodiment, the solder balls 82 are omitted and the IC package 62 is used in an LGA configuration.

[0071] Figure 3B is a cross-sectional view of an IC package printed directly on another circuit member in accordance with an embodiment of the present disclosure As shown in Figure 3B, a circuit member 60 can be substituted for fixture 50 during the process of forming the IC package. The interconnect assembly 78 can be formed directly on the circuit member 60, such as for example a PCB. The terminal pads 52 can be formed directly on the contact pads 58. The packaging 80 can be applied directly to the interconnect assembly 78 and IC device 72, sealing and attaching the interconnect assembly 78 directly to the printed circuit board 60. In one embodiment, the functionality of the IC device 72 may be tested before the packaging 80 is applied.

[0072] Figure 4 is a cross-sectional view of an alternate fixture 100 for making an IC package in accordance with an embodiment of the present disclosure. Conductive material 102 can be deposited in cavities 104 or recesses either before or after application of a dielectric layer 106A. The cavities 104 can be formed using a variety of techniques, such as molding, machining, printing, imprinting, embossing, etching, coining, and the like. Although the cavities 104 are illustrated as truncated cones or pyramids, a variety of other shapes can be used, such as for example, cones, hemispherical shapes, and the like.

[0073] In one embodiment, the dielectric layer 106A is printed onto surface 108, while leaving the cavities 104 exposed. In another embodiment, the dielectric layer 106A is applied to the surface 108 before the cavities 104 are formed, and the cavities 104 are formed through the dielectric layer 106A. In yet another embodiment, the dielectric layer 106A extends along the surfaces 110 of the cavities 104. The dielectric layer 106A facilitates removal of the interconnect assembly 112 (shown in Figure 5A) from the fixture 100.

[0074] Figure 5A is a cross-sectional view of an IC package 118 in accordance with an embodiment of the present disclosure. The completed interconnect assembly 112 is shown removed from the fixture 100 and sealed in packaging 114 with an IC device 116 to form the IC package 118. The IC device 116 includes solder balls 120 that are preferably reflowed to electrically couple with contact members 122A, 122B, 122C (collectively “122”) on the interconnect assembly 112. The contact members 124 were formed by processing a conductive material. The

contact members 124 provide an IC package 118 that is compatible with various sockets. The configuration of the contact members 124 can permit the IC package 118 to be coupled with a socket in a solderless configuration.

[0075] Figure 5B is a cross-sectional view of alternate solderless IC package 130 in accordance with an embodiment of the present disclosure. Rather than having to reflow solder, contact members 132 formed on the interconnect assembly 134 compressively engage with terminals 136 on the IC device 138. Compliant layers 140 bias the contact members 132 into engagement with the terminal 136. The compliant layers 140 also permit the contact members 132 to deflect and compensate for non-planarity of the terminals 136.

[0076] Figure 6 is a cross-sectional view of an alternate IC package 150 with additional functionality built into the interconnect assembly 152 in accordance with an embodiment of the present disclosure. One or more of the layers 154A, 154B, 154C, 154D, 154E, 154F (collectively "154") can include additional functionality, such as for example, specialty dielectrics, ground planes, power planes, shielding layers, stiffening layers, capacitive coupling features, circuitry layers, and the like. The close proximity of the layers 154 to the IC device 156 can improve electrical performance.

[0077] The additional functionality can also be provided by additional electrical devices 160A, 160B, and 160C (collectively "160"). The additional electrical devices 160 can be shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC, RF antennae, and the like. The electrical devices 160 can include passive or active functional elements. Passive functional elements may refer to structures having a desired electrical magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0078] The electrical devices 160 can be added as discrete components or printed onto one of the layers 154. In a preferred embodiment, the electrical devices 160 can be printed onto the interconnect assembly 152. As previously described, the availability of printable inks containing silicon and/or carbon nanotubes provides the ability to print electrical devices 160. Electrical devices that are typically located on a separate IC device or the circuit member 170 can be incorporated into the IC package 150, thereby improving electrical performance.

[0079] In the illustrated embodiment, the interconnect assembly 152 extends beyond the packaging 162. Conductive traces 164 permit and extension 166 to connect to other electrical devices, such as for example an external power source, another IC device, a test station, and the like. In the illustrated embodiment, terminal pads 158 form an LGA configuration with contact pads 168 on circuit member 170.

[0080] Figure 7 is an alternate IC package 200 with additional compliance built into the interconnect assembly 218 in accordance with an embodiment of the present disclosure. Compliant material 206 can be printed around terminal pads 202 and compliant material 208 can be printed around terminal pads 204. The additional compliance can assist with decoupling stress at interface 210 with a PCB 214 and the interface 212 with an IC device 216. Figure 8 is an IC package 240 configured as a variation of the IC package 200 of Figure 7. In the IC package 240 compliant material 242 extends into the first two layers 244, 246 of the interconnect assembly 248, providing a higher degree of compliance around terminal pads 250.

[0081] Figure 9 is an alternate IC package 260 with terminal pads 262A, 262B, 262C (collectively "262") that create a standoff with a circuit member 264 in accordance with an embodiment of the present disclosure. The terminal pads 262 can extend beyond the packaging 266 and maintain a gap 268 between the packaging 266 and the circuit member 264. The various dielectric layers 270 provide a degree of compliance, especially for the terminal pads 262A and 262B, which are coupled to the conductive traces 272 to create an offset relative to the terminal pads 274A, 274B. In one embodiment, the IC package 260 is electrically coupled with contact pads 276 on circuit member 264 without solder.

[0082] Figure 10 is an alternate IC package 300 with terminal pads 302A, 302B, 302C (collectively "302"), which also create a standoff with a circuit member 304 in accordance with an embodiment of the present disclosure. Compliant material 306 can be printed to the interconnect assembly 308 around orthogonally oriented conductive traces 310 to promote compliance of the terminal pads 302. The compliant material 306 near the terminals 302 can provide stress decoupling. The geometry of the terminals 302 can provide a more reliable connection than a solder ball when plugged into a solderless socket. In one embodiment, the IC package 300 can be electrically coupled with contact pads 312 on the circuit member 304 without solder.

[0083] Figure 11 is an IC package 350 with multiple IC devices 352, 354, also known as a system in package, in accordance with an embodiment of the present disclosure. Interconnect assembly 356 can be electrically coupled with interconnect assembly 360 via extension 358, such as for example, a flexible circuit member. Both IC devices 352, 354 and the interconnect assemblies 356, 360 are contained within packaging 362. Terminal pads 364 can provide a connection to circuit member 366.

[0084] The IC package 350 can include a plurality of electrical devices 370A, 370B, 370C printed on the interconnect assembly 356. Additional electrical devices 368 can be optionally printed on or integrally with the packaging 362.

[0085] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the invention. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the invention.

[0086] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0087] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the embodiments of the present invention are not entitled to antedate such publication by virtue of prior invention. Further, the dates of

publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0088] Other embodiments of the invention are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the invention. Thus, it is intended that the scope of at least some of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above.

[0089] Thus the scope of this invention should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. An integrated circuit (IC) package for an IC device, the IC package comprising:

an interconnect assembly including at least one printed compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of printed conductive traces electrically coupling a plurality of the first and second contact members, the compliant layer positioned to bias the first contact members against terminals on the IC device; and

packaging substantially surrounding the IC device and the interconnect assembly, wherein the second contact members are accessible from outside the packaging.

2. The IC package of claim 1, wherein the conductive traces in the interconnect assembly comprise substantially rectangular cross-sectional shapes.

3. The IC package of claim 1, wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer.

4. The IC package of claim 1, wherein the interconnect assembly comprises a plurality of printed dielectric layers.

5. The IC package of claim 1, wherein the interconnect assembly comprises at least one additional circuitry plane.

6. The IC package of claim 5, wherein the at least one additional circuitry plane comprises one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, and a flexible circuit.

7. The IC package of claim 1, wherein the contact members comprise one of a curable conductive material, sintered conductive particles, or a platable material.

8. The IC package of claim 1, wherein the interconnect assembly extends beyond a perimeter edge of the IC package.

9. The IC package of claim 8, further comprising a flexible circuit member electrically coupled to the interconnect assembly that extends beyond a perimeter edge of the IC package.

10. The IC package of claim 1, further comprising at least one electrical device printed on the interconnect assembly and electrically coupled to one or more of the conductive traces.

11. The IC package of claim 10, wherein the electrical device is selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC, RF antennae, and the like.

12. The IC package of claim 1, further comprising at least one electrical device printed on the packaging.

13. The IC package of claim 1, wherein the packaging comprises one or more of a preformed package, an encapsulating material, or a combination thereof.

14. An integrated circuit (IC) package comprising:

an interconnect assembly including at least one printed compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of printed conductive traces electrically coupling a plurality of the first and second contact members, the compliant layer positioned to bias the first contact members against terminals on the IC device;

at least one IC device with terminals compressively engaged with the first contact members, the compliant layer biasing the first contact members against the terminals on the IC device; and

packaging substantially surrounding the IC device and the interconnect assembly, the second contact members accessible from outside the packaging.

15. The IC package of claim 14, wherein the conductive traces in the interconnect assembly comprise substantially rectangular cross-sectional shapes.

16. The IC package of claim 14, wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer.

17. The IC package of claim 14, further comprising a plurality of IC devices electrically coupled to the interconnect assembly.

18. The IC package of claim 14, further comprising:

a plurality of interconnect assemblies electrically coupled to one or more of the second contact members; and

a plurality of IC devices each electrically coupled to one of the interconnect assemblies.

19. The IC package of claim 14, further comprising a plurality of electrical devices printed on the interconnect assembly and electrically coupled to one or more of the conductive traces.

20. An electrical system comprising:

the IC package of claim 14; and

a printed circuit board electrically coupled with the second contact members.

21. A method of making an IC package comprising the steps of:

forming an interconnect assembly by

printing at least one dielectric layer onto a surface of a fixture,

depositing a conductive material comprising first contact members,

printing a compliant layer along at least the first contact members,

printing a plurality of conductive traces electrically coupled with one or more of the first contact members,

forming a plurality of second contact members along a second major surface of the interconnect assembly, and

removing the interconnect assembly from the fixture;

compressively engaging terminals on at least one IC device with the first contact members, the compliant layer biasing the first contact members against the terminals on the IC device; and

substantially surrounding the IC device and the interconnect assembly with packaging, the second contact members accessible from outside the packaging.

22. The method of claim 21, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.

23. The method of claim 21, further comprising printing a conductive material, a non-conductive material, and a semi-conductive material on a single layer.

24. The method of claim 21, wherein the step of forming an interconnect assembly further comprises:

depositing the conductive material into a plurality of the cavities in the fixture; and

processing the conductive material to form the plurality of contact members along the first and second major surfaces of the interconnect assembly.

25. The method of claim 21, wherein the step of forming an interconnect assembly further comprises:

printing a second base layer of a dielectric material onto a surface of a fixture;

depositing a conductive material into a plurality of the cavities in the fixture;

processing the conductive material to form a plurality of second contact members; and

coupling the second contact members with the conductive traces on the interconnect assembly so the second contact members extend along the second major surface of the interconnect assembly.

26. The method of claim 21, wherein the step of forming an interconnect assembly further comprises forming at least one additional circuitry plane in the interconnect assembly.

27. The method of claim 21, further comprising electrically coupling a flexible circuit member to the interconnect assembly and extending the flexible circuit member beyond a perimeter edge of the packaging.

28. The method of claim 21, wherein the step of forming an interconnect assembly further comprises:

printing at least one electrical devices on the interconnect assembly; and

electrically coupling the electrical device to at least one contact member.

29. The method of claim 21, wherein the step of forming an interconnect assembly further comprises processing the conductive material, wherein processing comprises one of sintering, plating, or curing.

30. A method of making an electrical assembly comprising:

electrically coupling the second contact members on the IC package of claim 1 with a printed circuit board.

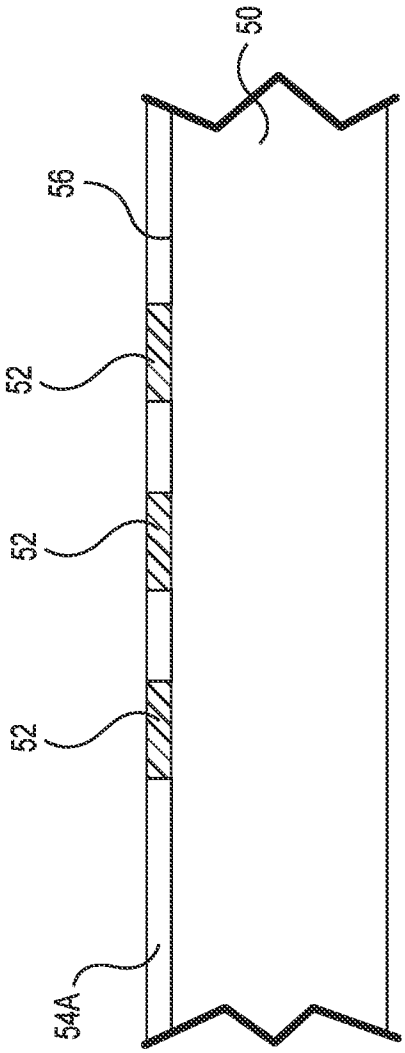

Fig. 1

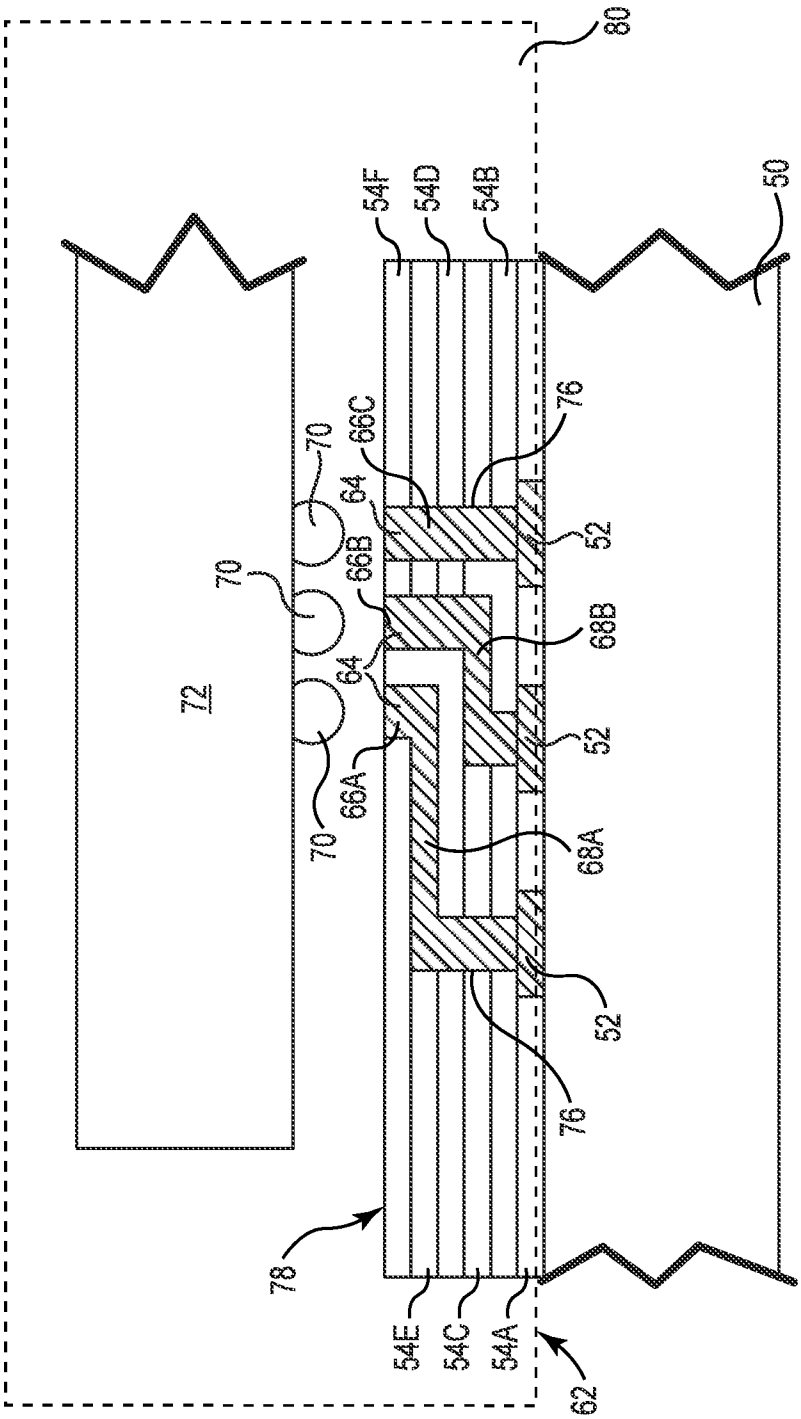
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Fig. 2

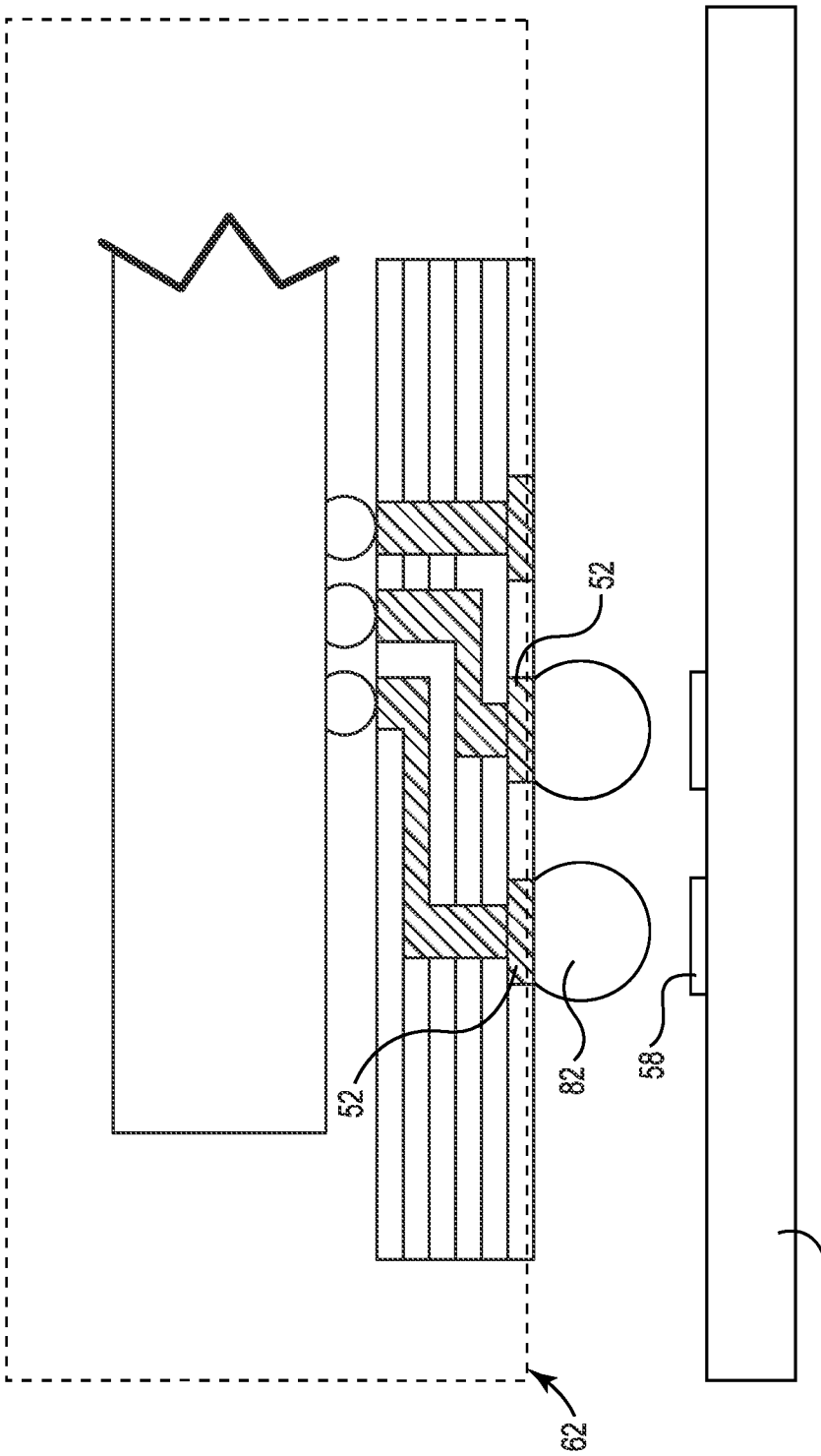

Fig. 3A

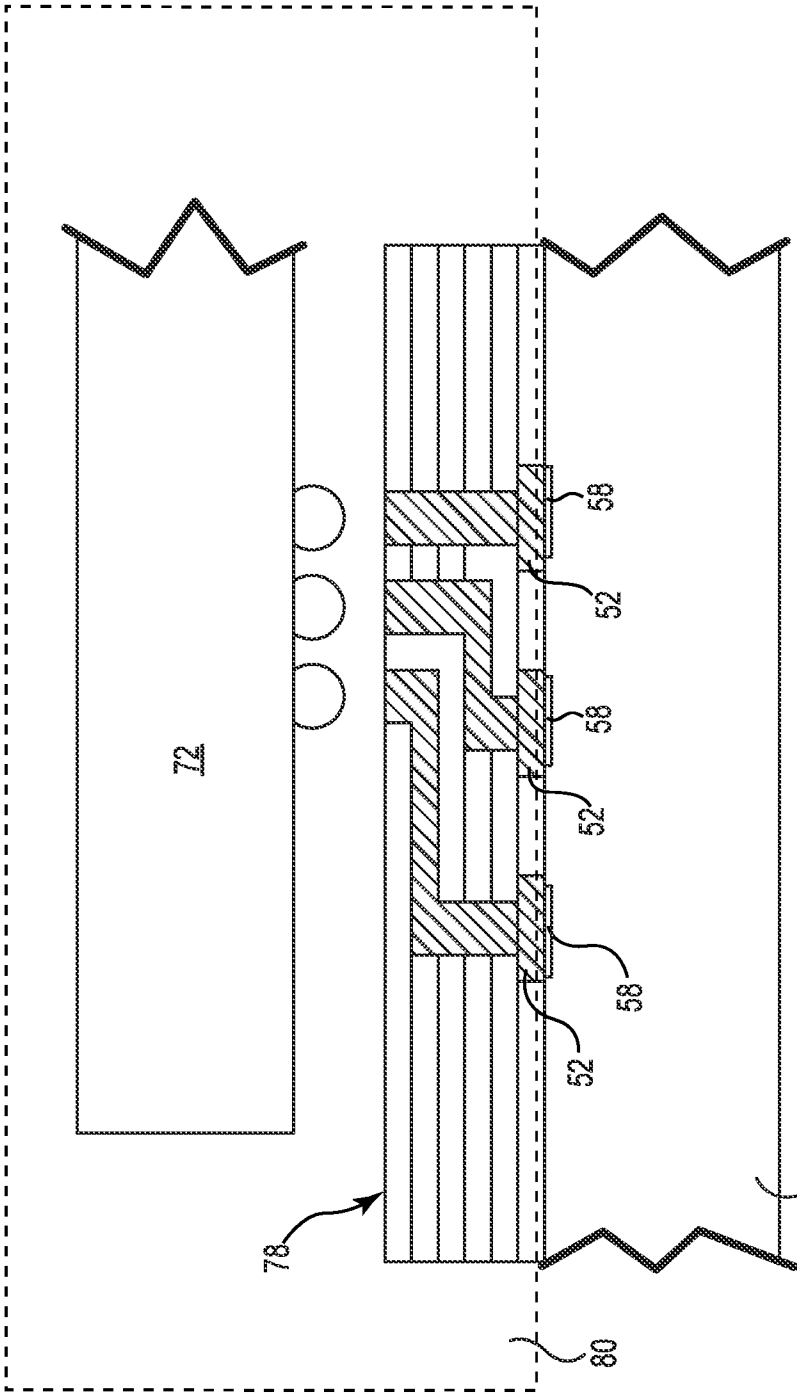

Fig. 3B

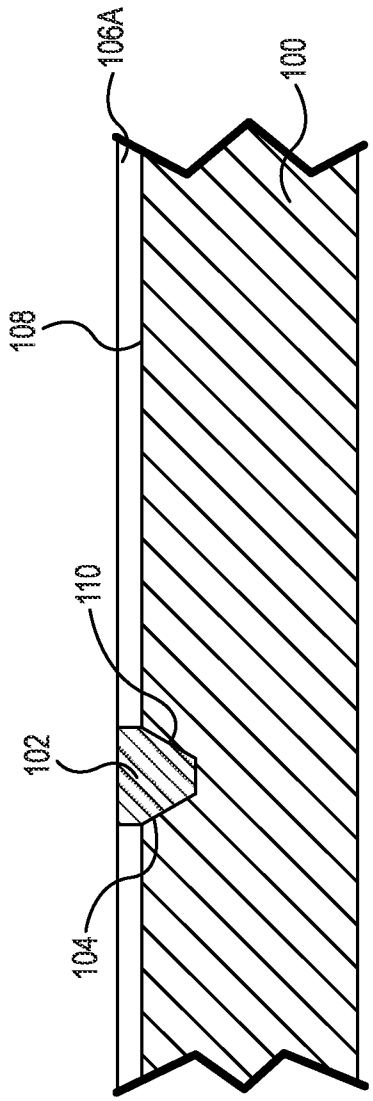

Fig. 4

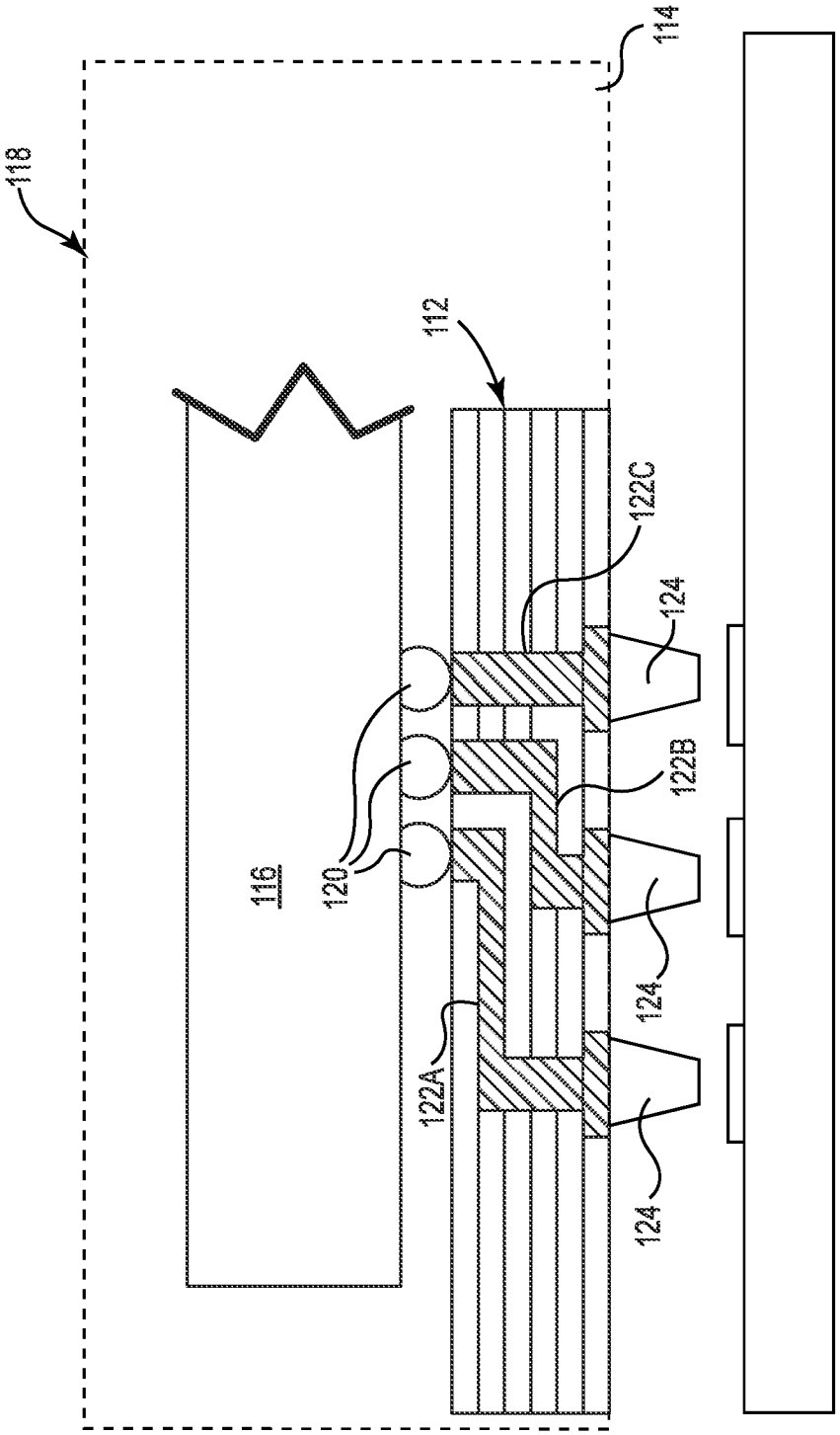

Fig. 5A

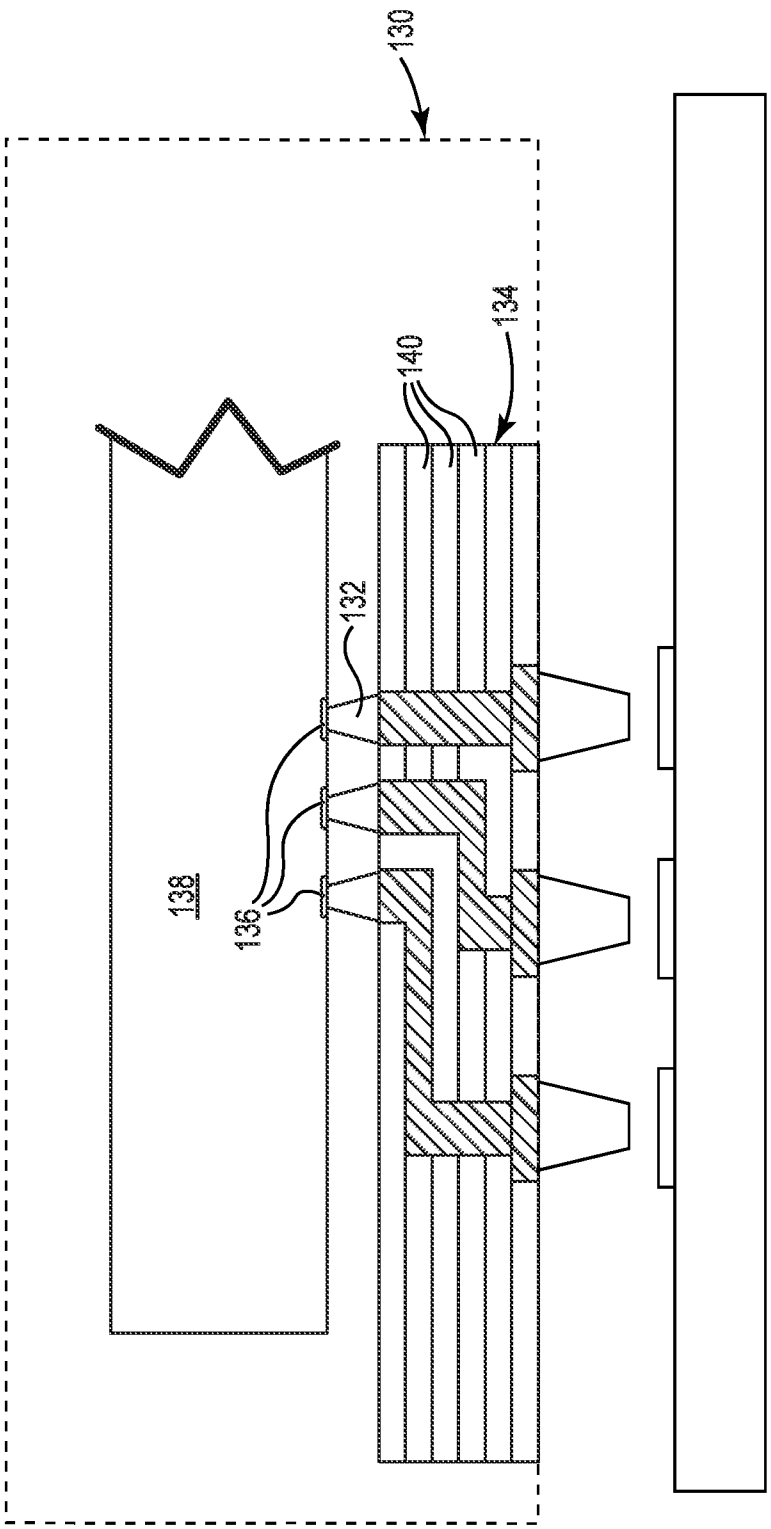

Fig. 5B

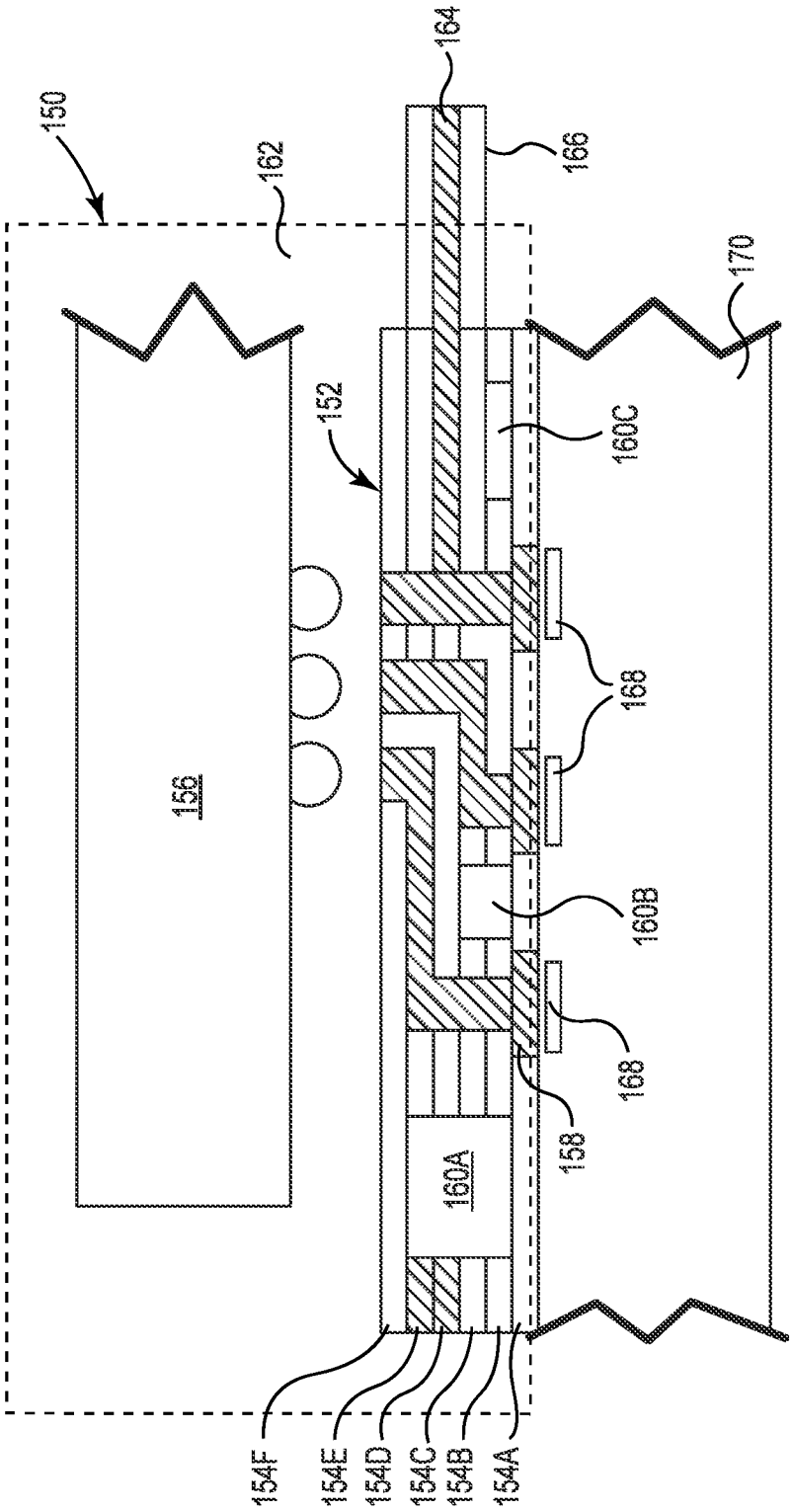
150
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Fig. 6

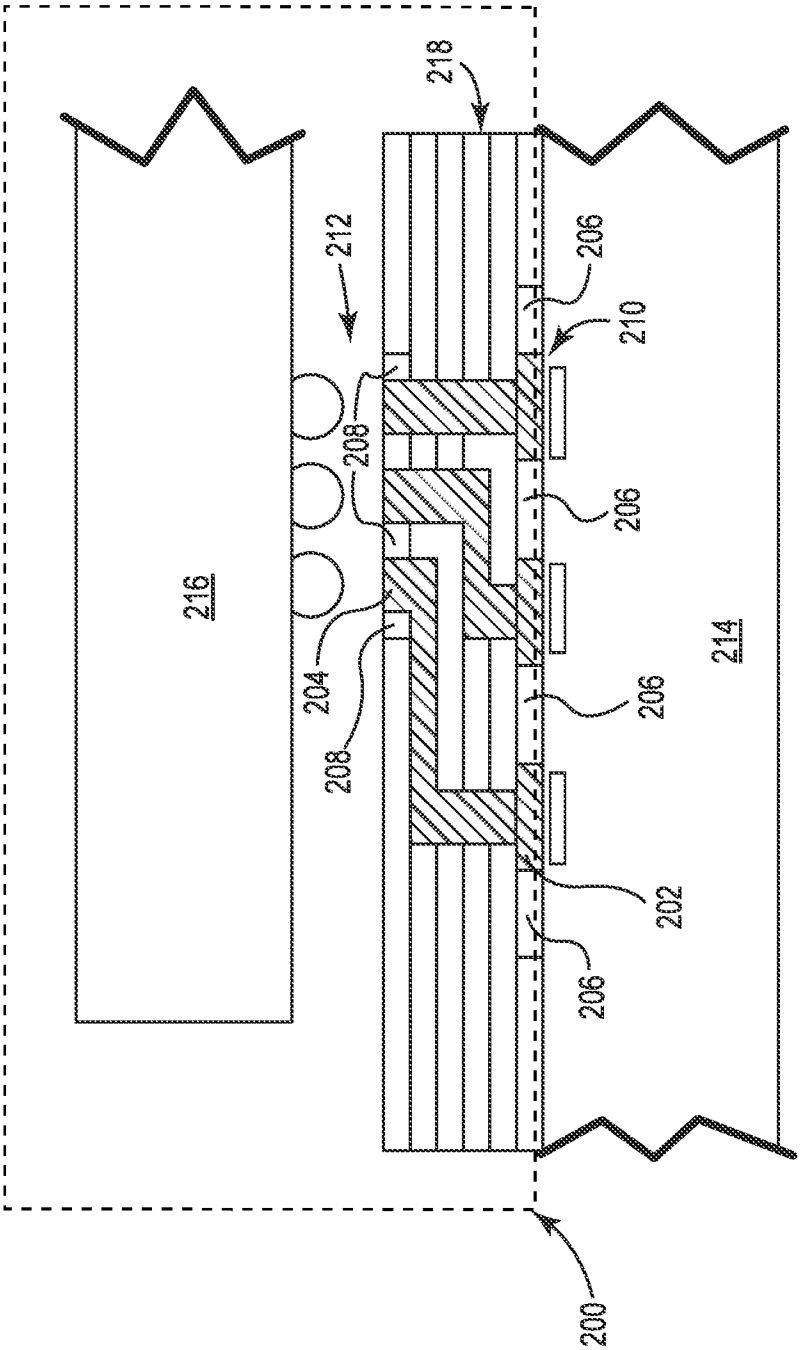

Fig. 7

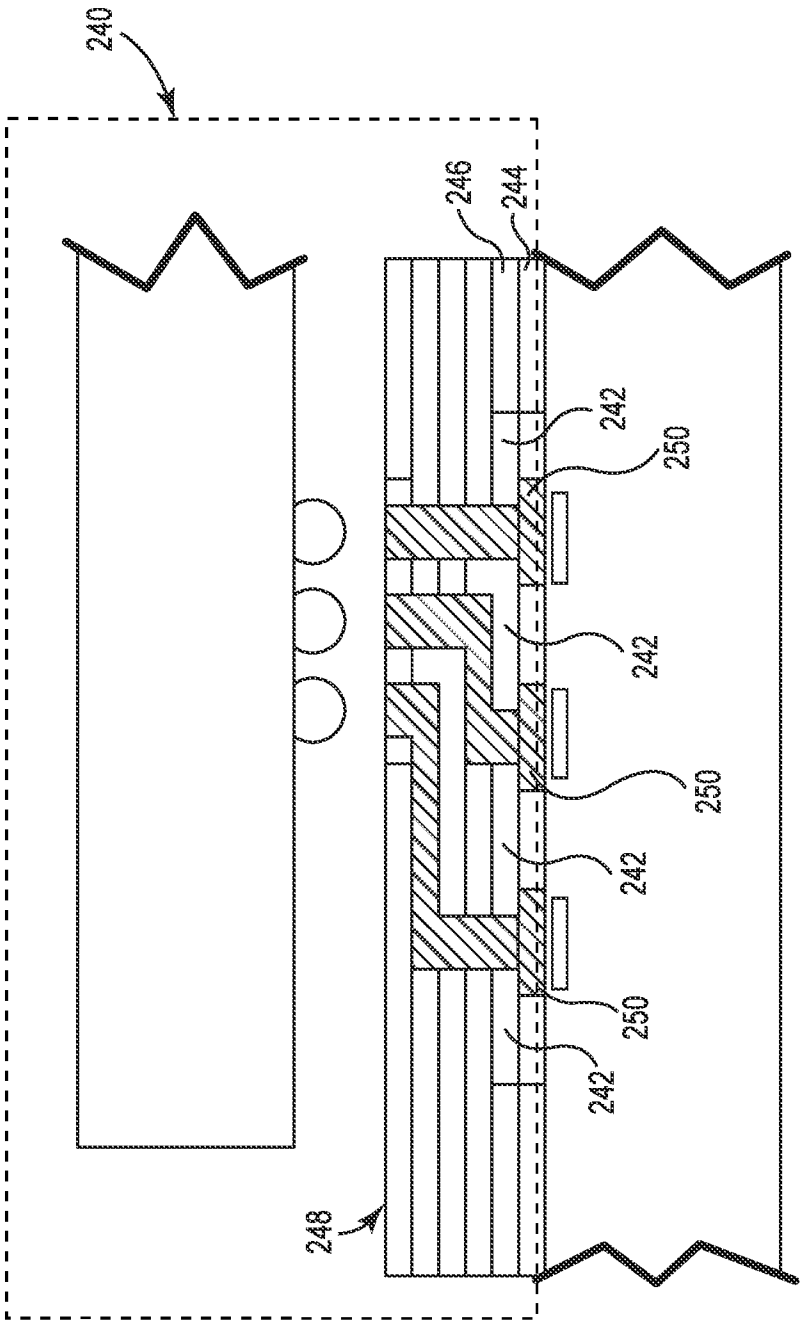

Fig. 8

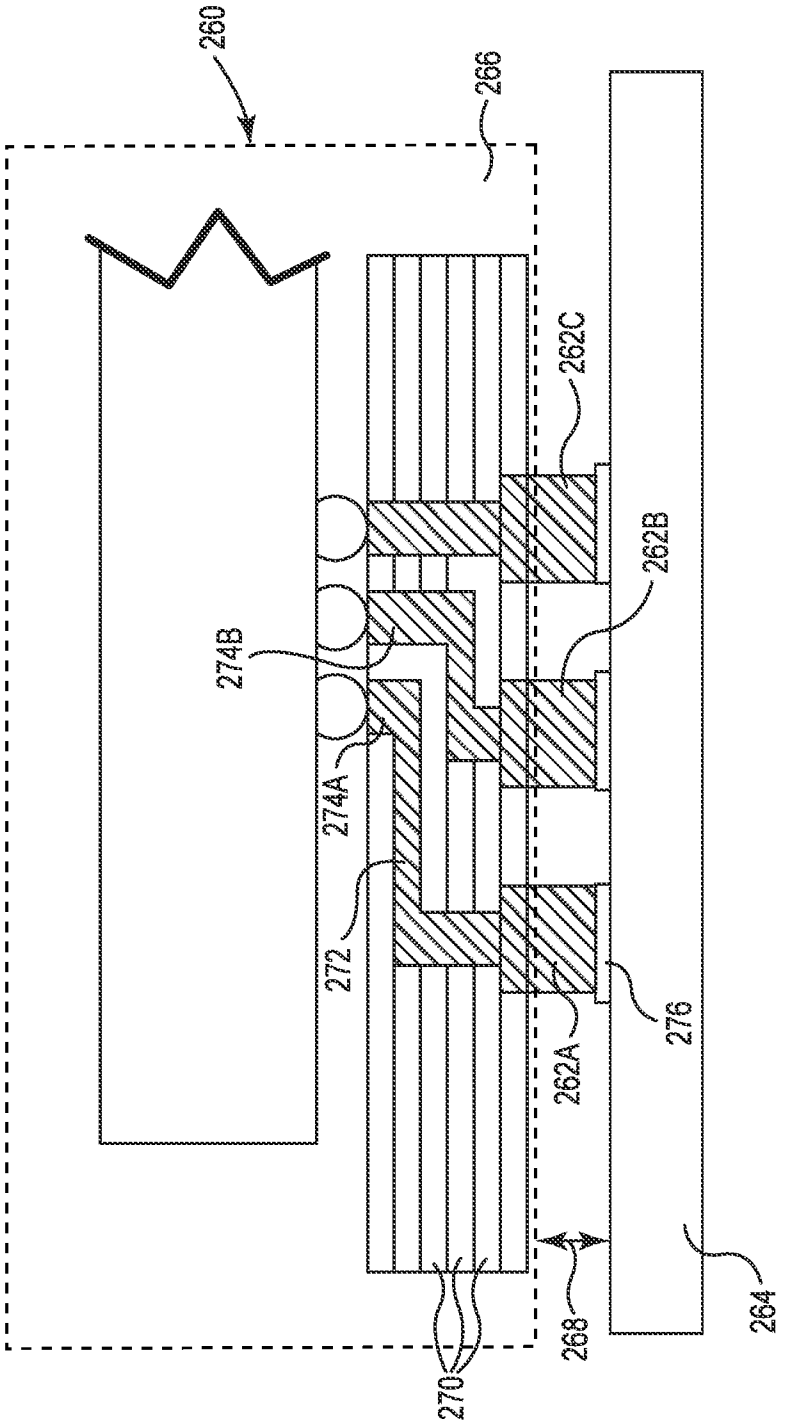

Fig. 9

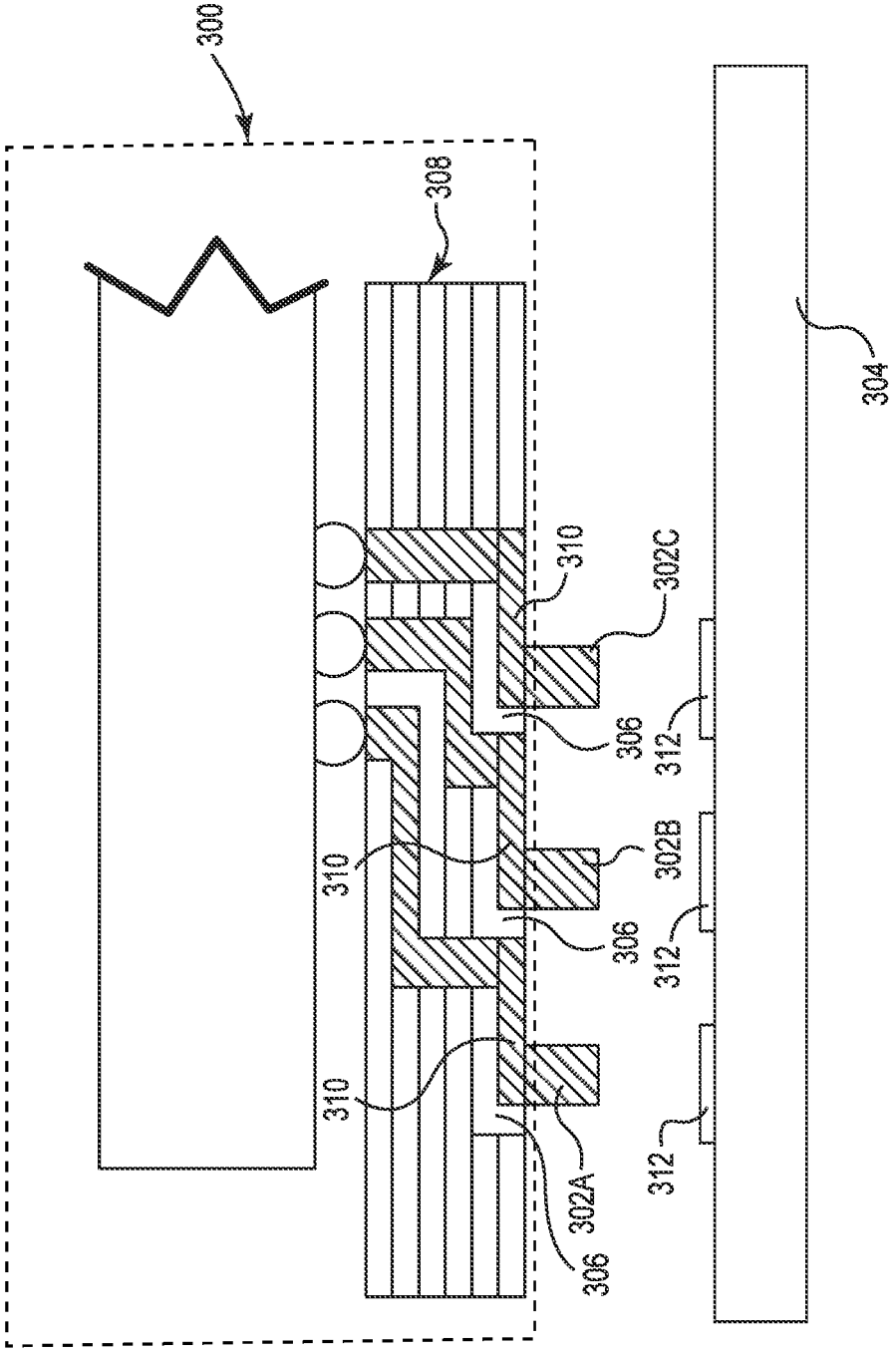

Fig. 10

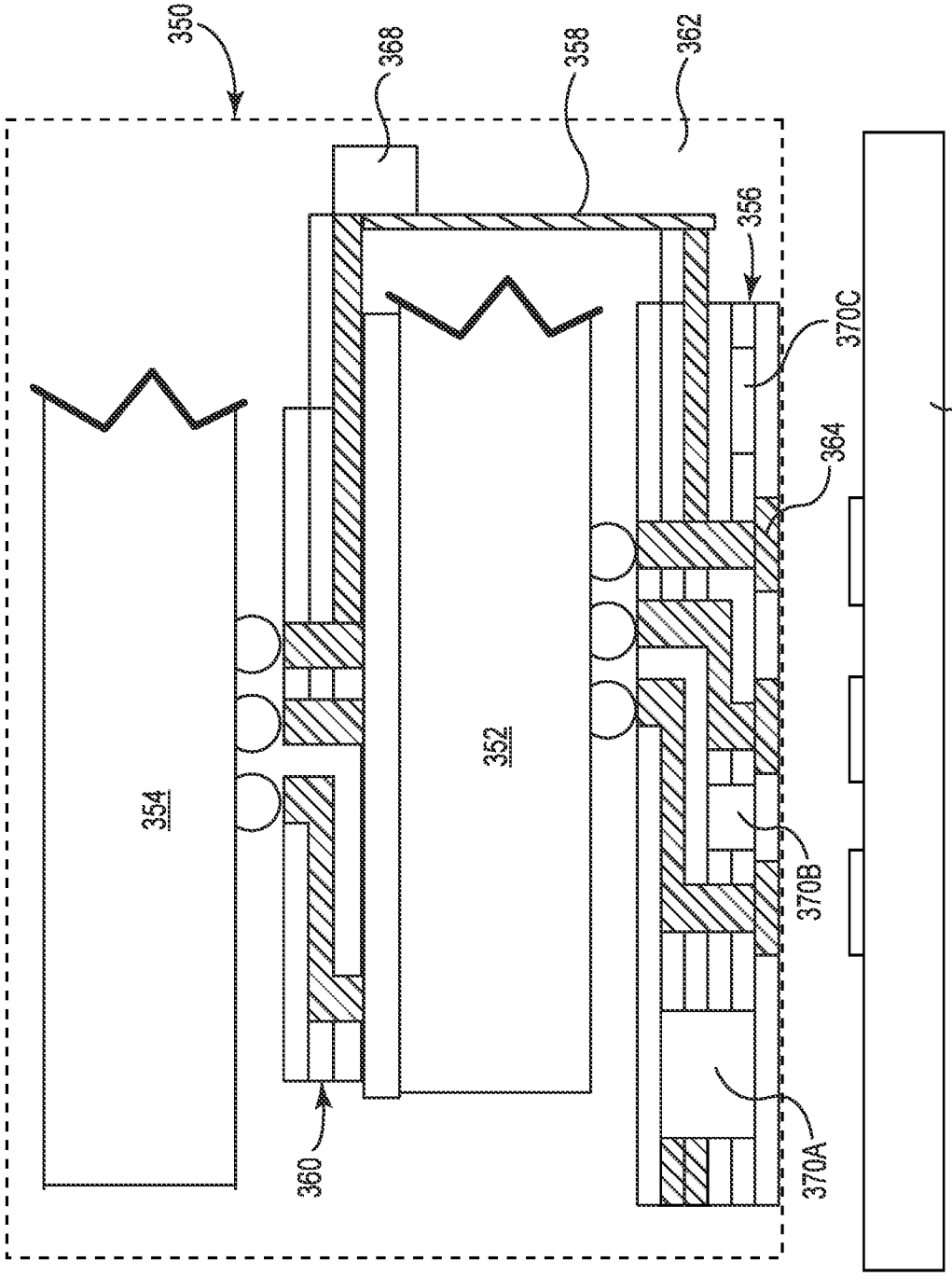

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 10/36363

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 23/485; H01L 21/00 (2010.01)
USPC - 174/260; 174/255; 257/787
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 23/485; H01L 21/00 (2010.01)
USPC - 174/260; 174/255; 257/787

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 174/260; 174/255; 257/787 (keyword search)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST, WIPO, DialogWeb (command search), Web: Google, Google Scholar, Google Patents
Search Terms Used: package, IC, interconnect, assembly, compliant, contact, conductive trace, printed, dielectric, circuit, device, preformed, encapsulate, printed circuit board, PCB, printing, cavity, recess, etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7,121,839 B2 (Rathburn) 17 October 2006 (17.10.2006), Entire document, especially: abstract; Figs 1-4, 10E, 12C, 14B, 15A, 16, 25-27; col 3, ln 10-13, 37-45, 62-66; col 4, ln 24-27; col 6, ln 41-46, 61-64; col 7, ln 10-12, 17-18, 35-39; col 9, ln 37-42; col 10, ln 3-7, 49-60; col 13, ln 61-63; col 14, ln 20-25, 34-51; col 15, ln 13-24, 42-44; col 15, ln 59 through col 16, ln 15; col 17, ln 21-22, 41-47, 58-64; col 18, ln 19-22, 29-38, 53-63; also see claims 7, 30	1-30
Y	US 2008/0246136 A1 (Haba et al.) 09 October 2008 (09.10.2008), Entire document, especially: abstract; para [0009], [0010], [0012], [0014], [0063], [0067], [0090]	1-30
Y	US 2007/0148822 A1 (Haba et al.) 28 June 2007 (28.06.2007), Entire document, especially: Figs 1, 2; para [0081], [0101], [0102]	2, 3, 15, 16, 22, 23
Y	US 7,326,064 B2 (Rathburn et al.) 05 February 2008 (05.02.2008), Entire document, especially: Fig 33; col 15, ln 46-50, 66-67	24, 25
A	US 6,313,528 B1 (Solberg) 06 November 2001 (06.11.2001), Entire document	1-30
A	US 7,114,960 B2 (Rathburn) 03 October 2006 (03.10.2006), Entire document	1-30

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2010 (22.07.2010)	28 JUL 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)