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[54] **CONSTANT CURRENT SOURCE**

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[58] **Field of Search** 328/176, 182–185; 307/228, 296, 297; 323/1

[56] **References Cited**

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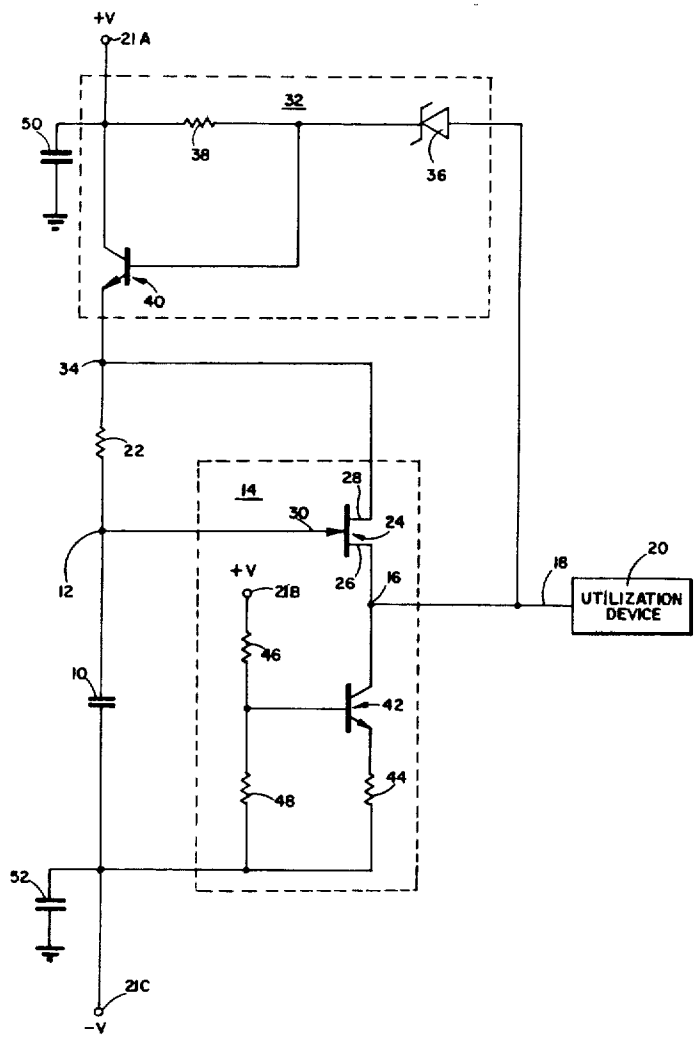
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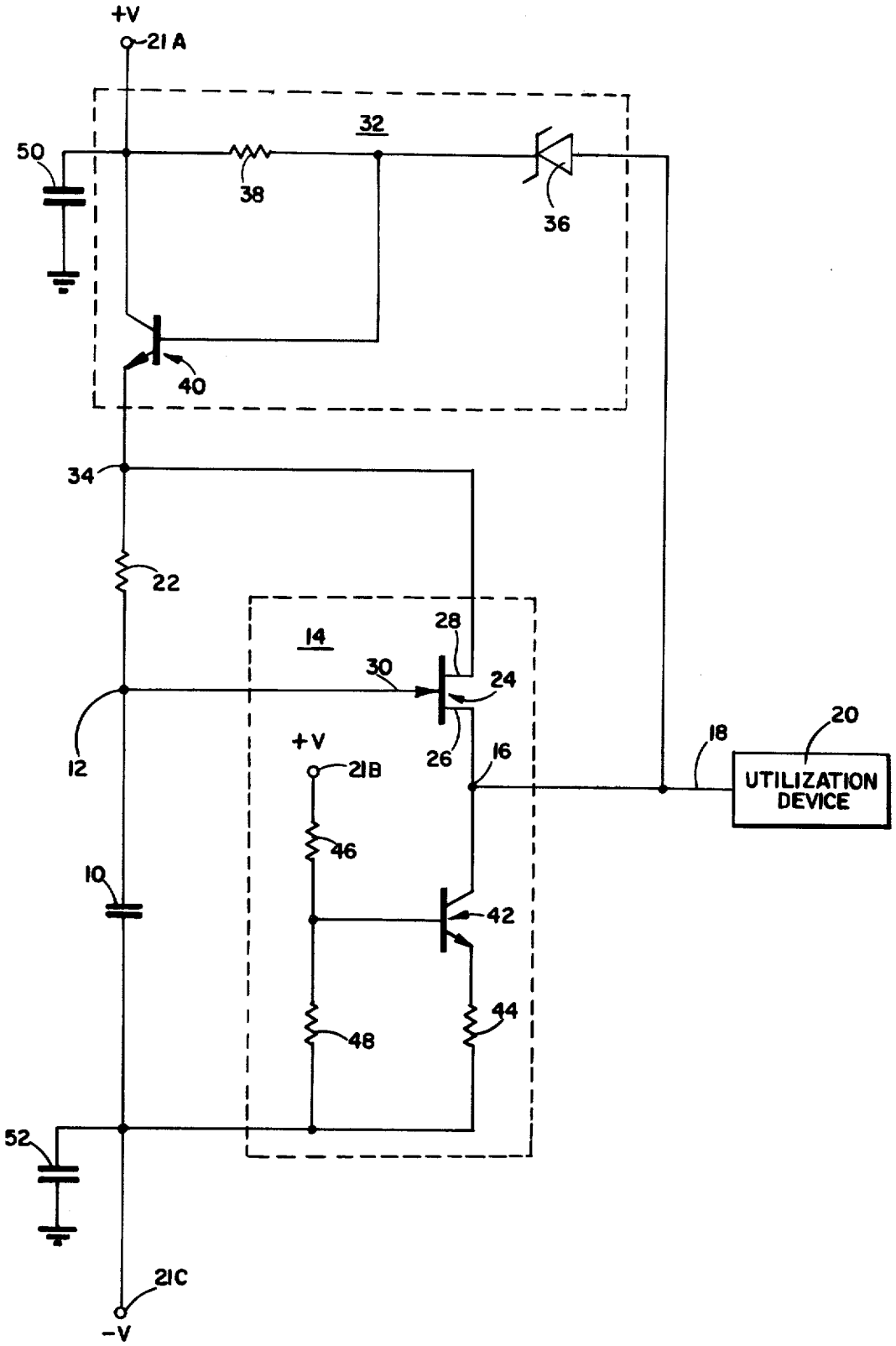
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[57] **ABSTRACT**

A current source for supplying constant, low level currents includes a high input impedance voltage follower, a voltage source connected to the voltage follower output terminal and, through an impedance, to the voltage follower input terminal.

6 Claims, 1 Drawing Figure




+V
21A
32
50
38
36
40
34
22
14
28
30
24
12
26
16
18
20
UTILIZATION DEVICE
+V
21B
46
10
42
44
48
52
21C
-V

CONSTANT CURRENT SOURCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to current supply systems and, more particularly, to a constant current source useful in the generation of voltage ramps for electronic timing purposes and the like.

2. Description of the Prior Art

Electronic timing circuits presently exist in many forms. One well known circuit employs a series connected resistor-capacitor (RC) combination in which the capacitor is charged from a source of constant voltage supplied through the resistor. With this arrangement, the output voltage across the capacitor approaches the supply voltage in a non-linear fashion. This arrangement is generally undesirable, especially for relatively long timing intervals, e.g. ten seconds or more, since the slope of the output voltage waveform steadily decreases as does the accuracy of the timing function.

As a result, other timing circuits have been developed to provide output voltage waveforms which vary substantially linearly with respect to time. Typically, such linear circuits employ a constant current source to charge the capacitor. For example, it is known to replace the resistor of the previously mentioned series resistor-capacitor combination with a device drawing constant current such as an appropriately connected field effect transistor or pentode vacuum tube. In another approach the resistor has been connected in the emitter circuit of a current controlling bipolar transistor with a zener diode connected across the transistor base-emitter junction and the resistor. This results in a current sensing and feedback arrangement which maintains the voltage across the resistor and, thus, the charging current therethrough, substantially constant.

Unfortunately, the above current supply circuits have not proved entirely satisfactory from a stability and/or cost standpoint, particularly for circuits requiring low current levels (e.g., in the microampere range and below). Low current values are desirable in various applications, including electronic timing circuits for generating relatively long voltage ramps for establishing extended timing intervals. The high quality timing capacitors required for such circuits (typically of the plastic film type exhibiting low leakage and low voltage dependence) are presently desirable from a cost and size standpoint only at values up to about one microfarad. As a result, with such capacitors it is necessary to employ currents of one microampere and below to generate a long output voltage ramp and establish a timing interval of ten seconds or more.

SUMMARY OF THE INVENTION

Briefly, and in general terms, the present invention provides a new and improved current supply system which overcomes the disadvantages and limitations of the prior art and which provides constant current levels in the microampere range and below using conventional components.

More specifically, and by way of example, the present invention comprises a voltage follower exhibiting high input impedance and a series connected voltage source and resistor connected between the follower output and input terminals. A constant, low level current is supplied through the resistor to the follower

input terminal dependent in value upon the resistance, the source voltage level, and any offset voltage across the follower. For timing applications, a capacitor load is connected to the follower input terminal and is charged by the current. An output voltage ramp corresponding to the capacitor voltage waveform is translated to the voltage follower output terminal and is isolated from the capacitor by the voltage follower.

In one embodiment, the follower may comprise a field effect transistor and the voltage source may comprise a combined bipolar transistor-zener diode voltage regulator. By connecting the regulator as a voltage supply source to the follower field effect transistor as well as to the charging resistor, the follower operates over a voltage range exceeding the voltage ratings of the field effect transistor.

BRIEF DESCRIPTION OF THE DRAWING

The sole FIGURE is an electrical schematic diagram of a preferred embodiment of a current supply system constructed in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in the drawing, for purposes of illustration, the invention is embodied in a current supply system which provides a substantially constant current to a load, such as a capacitor **10**, connected to an input terminal **12** of a voltage follower **14**. The voltage developed across capacitor **10** is translated via the voltage follower **14** to an output terminal **16** thereof and is supplied as an output ramp voltage over line **18** to an appropriate utilization device **20**. For a timing application, the utilization device may be a threshold detector, for example, actuated when the ramp voltage reaches a given level corresponding to a prescribed time interval.

Operating voltages for the system are provided by appropriate positive and negative voltage sources (not shown) connected to supply a relatively positive voltage level (+V) at circuit terminals **21A** and **21B** and to supply a relatively negative voltage level (−V) at terminal **21C**. Typically, these voltage levels may be +35 and −35 volts, respectively. Capacitor 10 is connected between negative terminal 21C and input terminal 12. A current path for charging capacitor 10 is provided through a resistor 22 connected to input terminal 12 in series with the capacitor 10.

Voltage follower **14** is a circuit exhibiting high input impedance and low output impedance and includes an N-channel junction field effect transistor (FET) **24** having source, drain, and gate electrodes identified, respectively, by reference numerals **26, 28** and **30**. Gate electrode **30** is connected to the input terminal **12** to receive the voltage signal across capacitor **10** as an electrical input to voltage follower **14**. Source electrode **26** is connected to output terminal **16** to provide an output voltage waveform thereat corresponding to the voltage signal across capacitor **10**. Because of its characteristic high gate resistance, the field effect transistor draws negligible gate current and, as a result, substantially all of the current supplied through resistor **22** is employed to charge the capacitor **10**.

A voltage regulator circuit **32** is connected in feedback relation from the output terminal **16** to a circuit terminal **34** common to the resistor **22** and to the drain electrode **28** of FET **24**. The regulator circuit includes

a zener diode 36 having the anode thereof connected to output terminal 16 and having its cathode connected through a resistor 38 to the positive terminal 21A. In addition, an NPN bipolar transistor 40 has the collector-base circuit thereof connected across the resistor 38 and the emitter electrode thereof connected to terminal 34 to supply a regulated voltage to resistor 22 and to the FET drain electrode 28. With this arrangement the voltage across the resistor 22 and, thus, the current therethrough is maintained substantially constant. In effect, the regulator circuit provides a source of constant voltage connected between output terminal 16 and resistor 22, and the resistor current is established by this voltage together with any offset voltage across the gate-source junction of FET 24.

A constant current load circuit is provided for the FET 24 and includes an NPN bipolar transistor 42 having the collector electrode thereof connected to source electrode 26 and the emitter electrode thereof connected through resistor 44 to the negative terminal 21C. The base bias for transistor 42 is established at a fixed level by potential divider resistors 46 and 48 connected in series between the positive and negative terminals 21B and 21C. With this biasing arrangement, transistor 42 provides current regulation to help establish constant operating conditions for FET24 over a wide swing in the output voltage delivered at terminal 16.

Capacitors 50 and 52 are connected between the respective positive and negative terminals 21A and 21C and ground level to shunt to ground any high frequency signals at the terminals.

In operation, at the beginning of a timing interval the positive and negative supply voltages +V and −V are applied to the circuit by closing appropriate switches (not shown) connected between the voltage sources and the circuit. Capacitor 10 is not charged at this time, and application of the supply voltages biases transistor 40 into conduction to provide a path therethrough for supplying charging current through resistor 22 to the capacitor 10. As the capacitor begins to charge, the voltage at input terminal 12 begins to increase substantially linearly in a positive direction from an initial value of approximately −V (−35 volts). This increasing voltage is supplied to the gate electrode 30 of the FET. The voltage at FET source electrode 26 increases at substantially the same slope as the gate voltage but is typically several volts more positive than the gate voltage. Similarly, the voltage at FET drain electrode 28 increases linearly in the positive direction at substantially the same rate as the gate and source voltages (due to the action of voltage regulator 32), with the drain voltage being more positive than either the gate or source electrode voltages. For the specific circuit illustrated, the source electrode 26 might be two volts positive with respect to the gate electrode 30 and the drain electrode 28 approximately eight and one-half volts more positive than the source electrode. As a result, a total and substantially constant voltage drop of about ten and one-half volts is established across resistor 22 for the duration of the timing interval. As a result, for the specific component values listed below, there is a substantially constant current of approximately one-half microampere through the resistor 22. Since any FET gate current is negligible by comparison, all current through the resistor is used in charging capacitor 10.

The FET load circuit establishes a constant current sink of approximately two and one-half milliamperes through load transistor 42 to establish the relative values of current through the FET 24 and the zener diode 36. At the beginning of the timing interval when the output voltage ramp at terminal 16 is at more negative levels, most of the constant load current through transistor 42 is provided through the zener diode. As the output voltage increases positively, the zener diode current decreases and the current through FET 24 correspondingly increases. Since load transistor 42 is a constant current sink, the sum of the currents through the zener diode 36 and FET 24 is held substantially constant to maintain the linearity and full voltage swing of the output voltage waveform at terminal 16.

After a timing interval is completed, the positive and negative voltage sources are disconnected from terminals 21A-21C in order to discharge capacitor 10 prior to a subsequent interval. This action can be effected by opening a power switch (not shown) between the sources and an additional portion of the circuit (not shown) to be powered from terminal 21A and 21C as a function of the operation of utilization device 20. A discharge path for positive current then exists from the capacitor 10 forward through the gate-source junction of FET 24, forward through zener diode 36, and forward through the collector-base junction of transistor 40 to terminal 21A.

The output voltage ramp at output terminal 16 will swing linearly in the neighborhood of fifty volts or more from roughly −35 volts to about +20 volts over a timing interval of about 95 seconds. By virtue of the regulated voltage supplied to the FET drain 28 by voltage regulator circuit together with the load current control by transistor 42, the maximum voltage across any two FET electrodes is never more than about twelve volts, despite the fact that the output voltage swings more than four times that amount.

From the above it is evident that the present invention provides a constant current supply circuit in the sub-microampere range which may be employed to charge a capacitor 10 to generate an output voltage ramp for timing purposes and the like as well as for other applications requiring low level current sources. The circuit provides a stable, linear, accurately timed, long duration output voltage ramp without the need for any special or unusual components. Moreover, the output voltage is buffered from the input by the voltage follower.

While the voltage regulator 32 supplies a regulated output voltage to both resistor 22 and FET drain electrode 28, it should be pointed out that, in accordance with the invention, the drain electrode could have a separate potential source connected thereto in lieu of the regulator 32, if the resulting increased maximum voltage seen across the FET terminals was tolerable. Similarly, the load transistor 42 could be replaced by a resistor, with a corresponding sacrifice in the total output voltage swing. Moreover, the invention in a simpler form contemplates connection of a voltage source such as a simple battery between the output terminal 16 and the resistor 22 in lieu of regulator 32. In fact, by making a direct feedback connection from output terminal 16 to resistor 22, the resistor voltage could be provided solely by the offset voltage across the voltage follower 14 (i.e. across the gate-source junction of FET 24) in some cases. It should also be noted that junction

FET 24 could be replaced by a MOS FET with a gate resistance several orders of magnitude higher in order to establish an even lower level constant current at input terminal 12. In addition, in some cases it would be advantageous to employ a voltage regulator 32 in integrated circuit form as well as an integrated circuit amplifier or the like for voltage follower 14.

Typical components and values for the circuit illustrated are:

	CAPACITORS
10	0.68 microfarads
50	0.01 microfarads
52	0.01 microfarads
	RESISTORS
22	22 megohms
38	30 kilohms
44	1.8 kilohms
46	62 kilohms
48	4.7 kilohms
	ZENER DIODE
36	IN 757A, 9.1 volts
	NPN TRANSISTORS
40	2N 3440
42	2N 3440
	JUNCTION FET
24	2N 5361

It will be apparent from the foregoing that, while particular forms of the invention have been illustrated and described, various modifications may be made without departing from the spirit and scope of the invention.

I claim:

1. In combination:

high input impedance voltage follower means having an input terminal connected to a load and having an output terminal isolated from said input terminal, said voltage follower means comprising a field effect transistor having a source, drain, and gate electrodes, said gate electrode connected to said input terminal and said source electrode connected to said output terminal;

impedance means connected to said input terminal;

a voltage source, said voltage source comprising a voltage regulator having a first terminal thereof connected to said voltage follower output terminal and having a second terminal thereof connected to a point common with said impedance means and said drain electrode of said field effect transistor in order to supply thereto a voltage signal regulated with respect to the voltage at said output terminal; and

means connecting said voltage source between said output terminal and said impedance means, whereby a substantially constant voltage is developed across said impedance means for establishing a substantially constant current therethrough to said load.

2. The combination of claim 1 including:

current regulating transistor means connected to said source electrode of said field effect transistor, said output terminal being located at a common point between said source electrode and said transistor means.

3. The combination of claim 1 wherein said load includes capacitance means connected to said input terminal and adapted to be charged by current supplied through said impedance means, the voltage across said capacitance means being translated to said output terminal to provide an output ramp voltage signal thereat.

4. In combination,

impedance means,

voltage regulator means,

voltage follower means exhibiting high imput impedance and low output impedance and having at least an input terminal and an output terminal, said voltage follower means comprising a field effect transistor having source, drain, and gate electrodes, said gate electrode connected to the input terminal of said voltage follower means, said source electrode connected to the output terminal of said voltage follower means, and said drain electrode connected to a common junction with a first terminal of said impedance means and said voltage regulator means in order to receive a voltage signal therefrom,

load means having a first terminal thereof connected to a common junction with a second terminal of said impedance means and said input terminal of said voltage follower means,

said voltage regulator means connected from said output terminal of said voltage follower means to said first terminal of said impedance means, and

constant current source means connected from said output terminal of said voltage follower means to a second terminal of said load means.

5. The combination of claim 4, wherein said voltage regulator means comprises a diode means and a transistor means having collector, base and emitter electrodes,

a first terminal of said diode means connected to said output terminal of said voltage follower means and a second terminal of said diode means connected at a common junction with the base electrode of said transistor means,

the emitter electrode of said transistor means connected at a common junction with the first terminal of said impedance means and the drain electrode of said field effect transistor.

6. The combination of claim 4, wherein said load means is a capacitive means,

said capacitive load means electrically connected in series with said impedance means,

said voltage follower means connected to said capacitive load means at said common junction to detect a voltage across said load means and to produce an output signal representative of said voltage, and

said voltage regulator means connected to receive said output signal from said voltage follower means and to supply a corresponding voltage signal to said impedance means at said first terminal thereof.

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