



(51) International Patent Classification:

C25D 11/06 (2006.01) *C25D 17/06* (2006.01)
C25D 11/12 (2006.01) *H01L 21/306* (2006.01)

(21) International Application Number:

PCT/AU2014/000307

(22) International Filing Date:

24 March 2014 (24.03.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2013901031 25 March 2013 (25.03.2013) AU

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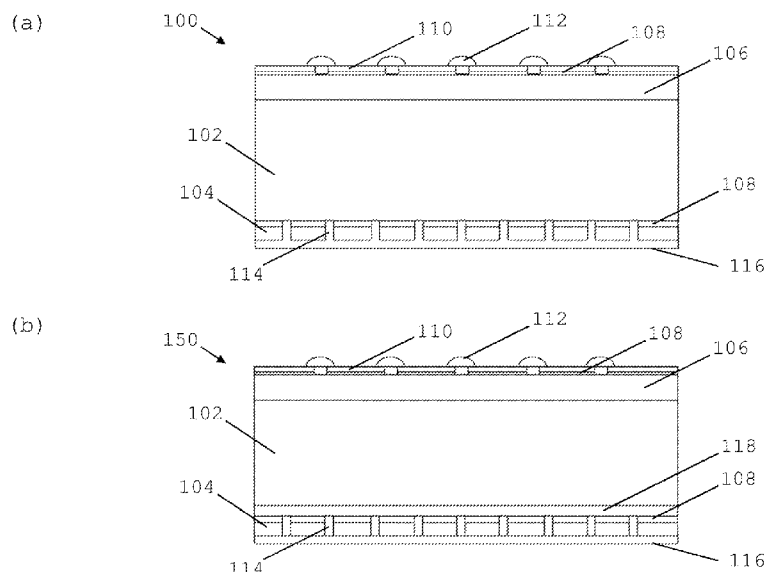
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: A METHOD OF ANODISING A SURFACE OF A SEMICONDUCTOR DEVICE



(57) Abstract: The present disclosure provides a method of anodising a surface of a semiconductor device comprising a p-n junction. The method comprises exposing a first surface portion of the semiconductor device to an electrolytic solution that is suitable for anodising the first surface portion when an electrical current is directed through a region at the first surface portion. Further, the method comprises exposing a portion of the semiconductor device to electromagnetic radiation in a manner such that the electromagnetic radiation induces the electrical current and the first surface portion anodises.

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A METHOD OF ANODISING A SURFACE OF A SEMICONDUCTOR DEVICE

Technical Field of the Invention

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The present invention relates generally to the field of semiconductor device fabrication and, in particular, to a method of anodising a surface of a semiconductor device.

10 Background of the Invention

Silicon solar cells require effective surface passivation to ensure high operating voltages and therefore high energy conversion efficiencies. Surface passivation is usually achieved by depositing or thermally growing a dielectric layer which can either reduce the density of defect states at the surface or largely repel electrical carriers of one polarity from the surface to decrease the probability of carrier recombination at the semiconductor surface.

Thermally-grown layers of silicon dioxide and silicon nitride, the latter deposited by plasma enhanced chemical vapour deposition (PECVD), are commonly-used in solar cell manufacturing as passivation dielectrics. These layers can improve the surface passivation of n-type silicon by storing positive charges, which induce accumulation layers of majority carrier electrons at the semiconductor surface.

Similarly, aluminium oxide layers which can be deposited using either PECVD or atomic layer deposition (ALD), can contain stored negative charges which can effectively passivate p-type silicon surfaces by inducing an accumulation layer of majority carriers.

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However, the deposition processes of the abovementioned dielectrics generally require high temperature furnaces or

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vacuum chambers, which involve a high thermal budget and/or long processing periods. Further, chemical and physical vapour deposition processes usually consume source materials that can be hazardous, are expensive
5 and/or toxic and consequently may create environmental problems.

Dielectric layers can be formed on silicon surfaces by anodisation of metal precursor layers in a solution-based
10 electrochemical reaction. The anodisation process has advantages over thermal growth and chemical or physical deposition processes. Typically, the reaction takes place in an electrolytic solution using inexpensive chemicals at room temperature and under atmospheric pressure.
15 Furthermore, the electrochemical bath can be maintained in such a way as to support an inline process with controlled dosing and bleeding of electrolyte to ensure electrolyte stability with time. Quality passivation, however, requires uniform and complete anodisation of the surface
20 layer. Unfortunately, the majority of previously proposed methods for anodising surface layers on semiconductor wafer require the application of a voltage to the layer being anodised whilst the wafer is immersed in an electrolytic solution. This voltage is typically applied
25 using a conductive clip. The voltage is applied to generate an electric field horizontally across the wafer and a lateral current flow through the layer to be anodised. The lateral current can result in a non-uniform anodisation and non-optimal passivation of the device
30 surface. Furthermore, the resistance to the lateral current flow increases with the thickness of the anodised layer, decreasing the anodisation current and increasing processing time.

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Summary of the Invention

In accordance with a first aspect, the present invention provides a method of anodising a surface of a

5 semiconductor device comprising a p-n junction, the method comprising the steps of:

exposing a first surface portion of the semiconductor device to an electrolytic solution that is suitable for anodising the first surface portion when an electrical
10 current is directed through a region of the semiconductor device at the first surface portion; and

exposing a portion of the semiconductor device to electromagnetic radiation in a manner such that the electromagnetic radiation induces the electrical current
15 and the first surface portion anodises.

In one embodiment the step of exposing a portion of the semiconductor device to electromagnetic radiation comprises exposing a second surface portion to the
20 electromagnetic radiation, the second surface portion being a surface portion that is different to the first surface portion. For example, the first and second surface portion may be at opposite sides of the semiconductor device.

25 The method may further comprise the step of applying a biasing voltage to generate a biasing electrical current to supplement the electrical current that is induced by the electromagnetic radiation. The semiconductor device
30 may comprise an electrode element and the method may comprise applying the biasing voltage via the electrode element. The electrode element may be semi-transparent or substantially transparent to the electromagnetic radiation. The electrode element may comprise at least one
35 of: a conductive oxide, a conductive polymer and graphite.

Embodiments of the method further comprise the step of

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selecting a property of the electrolytic solution to influence a property of the first surface portion after anodising.

- 5 The method may also comprise the step of selecting the biasing voltage to influence a property of the first surface portion after anodizing.

In another embodiment, the method comprises the step of
10 patterning the first surface portion after anodising to influence a property of the first surface portion after anodising. The step of patterning may comprise chemical etching or inkjet printing. The property of the anodised first surface portion may relate to a diameter or a
15 spacing of pores formed in the anodised first surface portion.

In some embodiments of the invention the first surface portion comprises a p-type region of the p-n junction or a
20 surface layer deposited on a p-type surface portion of the semiconductor device.

The method may be conducted such that the radiation-induced current flows transversally to the first surface
25 portion of the semiconductor device.

The electrolytic solution may be one or a combination of: sulphuric acid, phosphoric acid, oxalic acid, boric acid and nitric acid.

30 The semiconductor device may be arranged to form a solar cell, such as a silicon solar cell.

In accordance with a second aspect, the present invention
35 provides an apparatus for anodising a semiconductor device comprising a p-n junction, the semiconductor device having a first side portion and a second side portion, the

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apparatus comprising:

a radiation source arranged to illuminate the second side portion of the semiconductor device;

a container for containing an electrolytic solution;

5 a cathode element positioned for contacting the electrolytic solution; and

a support arranged to support the semiconductor device such that in use the first side portion of the semiconductor device is exposed to the electrolytic
10 solution when the container is charged with the electrolytic solution and the second side region is illuminated by radiation from the radiation source in a manner such that a radiation-induced current is generated to anodise the second side portion.

15

The apparatus may further comprise a voltage source arranged to apply a biasing voltage between the second side region of the semiconductor device and the cathode element.

20

In accordance with a third aspect, the present invention provides a solar cell device comprising an anodised dielectric layer formed by the method in accordance with the first aspect.

25

The anodised dielectric layer may be an oxide layer that may be porous. Further, the anodised dielectric layer may be a surface layer and may comprise aluminium or titanium. Additionally or alternatively, the anodised dielectric
30 layer may be patterned. The anodised dielectric layer may be patterned such that the anodised dielectric layer comprises pits with a diameter between 50 and 200 micrometers.

35 In embodiments of the invention the first surface portion comprises a surface layer that comprises aluminium and/or titanium. The first surface portion may be a surface

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portion of a p-type region of the p-n junction or a may be
a surface portion of a layer deposited on a p-type surface
portion of the semiconductor device. Alternatively, the
first surface portion may be a surface portion of an n-
5 type region of the p-n junction or may be a surface
portion of a layer deposited on an n-type region of the
semiconductor device.

In accordance with a second aspect, the present invention
10 provides a method of anodising a dielectric layer of a
solar cell device comprising use of the apparatus of the
second aspect of the present invention.

In specific embodiments the solar cell comprises silicon.
15

Brief Description of the Drawings

The embodiments of the invention will now be described, by
way of example, with reference to the accompanying
20 drawings in which:

Figure 1 is a schematic illustration of solar cell
devices that have anodised layers;

Figure 2 is a flow chart of a solar cell fabrication
process that includes the formation of an anodised layer
25 on the rear surface of the device;

Figure 3 is a flow chart of a light-induced
anodisation process;

Figures 4 to 7 are schematic representations of light-
induced anodisation apparatuses in accordance with
30 embodiments of the present invention;

Figure 8 is an equivalent circuit diagram of a light-
induced anodisation process;

Figure 9 is a schematic illustration of a close-up
cross-sectional view of an anodic aluminium oxide layer;

35 Figure 10 shows a scanning electron microscope image
of a patterned anodic aluminium oxide layer;

Figure 11 shows a schematic illustration and a

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scanning electron microscope image of a cross-section of a p-type back contact;

Figure 12 shows a scanning electron microscope comparison between anodic aluminium oxide layers formed by radiation-induced anodisation and a clip-based
5 anodisation; and

Figure 13 shows a comparison of implied open circuit voltages of solar cells with surfaces electronically passivated by anodic aluminium oxide layers formed by radiation-induced anodisation and a clip-based
10 anodisation.

Detailed Description of Embodiments

15 Embodiments of the present invention relate to a method and an apparatus for anodising a surface layer of a semiconductor device comprising a p-n junction, such as a solar cell. The surface of the semiconductor device being anodised is in contact with an electrolytic solution
20 containing oxygen. The anodisation is realised by illuminating a region of the semiconductor device and thus inducing a current in the device which circulates in the electrochemical circuit constituted by the device, the electrolytic solution, a cathode exposed to the
25 electrolytic solution, and an anode which is in electrical contact with a region of the semiconductor device. The radiation-induced current forward biases the semiconductor device generating a source of electrons at the n-type surface and a source of holes at the p-type surface of the
30 device. Embodiments of the method can be used to anodise a p-type surface of the semiconductor device to form, for example, a silicon dioxide layer or a dielectric layer comprising elements other than those of the semiconductor device.

35 Unlike other methods of anodising, which require a direct electrical contact to the material being anodised, the

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method and apparatus disclosed herein do not require that the surface to be anodised is directly contacted. In addition, the anodisation current is not required to flow laterally through the surface layer to be anodised.

5 Instead the radiation-induced current of the semiconductor device directs the current perpendicular to the surface therefore enabling uniform anodisation.

Referring now to figure 1(a), there is shown a silicon
10 solar cell 100 formed on a p-type wafer 102 with an anodised layer 104 formed as rear surface dielectric layer. The solar cell 100 has an n-type emitter layer 106 formed by way of phosphorus diffusion or ion implantation, which forms a p-n junction with the p-type wafer 102. A silicon
15 dioxide layer 108, which typically has a thickness between 5 nm and 20 nm, is formed on both n-type and p-type surfaces of the device to minimise the semiconductor defects at the surface and thus reduce recombination. A dielectric layer, such as silicon nitride or silicon oxy-
20 nitride 110, which typically has a thickness around 75 nm, is then usually formed over the oxide layer on the n-type surface of the device to act as an antireflection coating. The anodised dielectric layer 104 is then formed using an anodisation technique. Metal contacts 112 to the device
25 can be formed on the n-type surface using either a chemical etching process or a laser structuring process followed by metal plating or screen printing of metal pastes. Electrical contact can then be enabled to the p-type surface of the device by forming openings 114 in the anodised layer 104 and alloying a layer of metal 116, such
30 as aluminium, through these openings to form Ohmic contacts to the device. The openings may be formed using a patterning process that exploits the porous nature of the anodised layer 104. The anodised dielectric layer 104
35 therefore simultaneously passivates the device and enables fine-scale metal contacts to be formed to a surface of the device. The passivation provided by the anodised layer 104

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is due in part to the electrical charge stored in the layer and in part to the passivation of traps at the silicon/silicon dioxide interface. The thin oxide layer 108 formed on the p-type surface ensures the quality of
5 passivation and can provide a barrier to prevent anodisation extending in the semiconductor device. Thick silicon oxide layers 108 can also be used. However, to decrease the overall resistance during the anodisation process, the thickness of the oxide layer 108 is typically
10 limited to 30 nm.

Figure 1(b) shows a variation 150 of the solar cell 100 of figure 1(a), where a heavily-doped p-type layer 118 is formed on the p-type surface of the p-type silicon wafer
15 102. This layer can be formed using a solid state diffusion process or ion implantation and is typically very thin (i.e., less than 1 micrometre). Due to the high concentration of p-type atoms at the surface, a metal layer 116, for example a nickel layer, can be directly
20 plated through the openings of the anodised layer 104. Alternatively, a metal layer 116, such as aluminium, can be deposited by thermal evaporation, e-beam evaporation or sputtering onto the surface of the anodised layer 104 to form p-type metal contacts to the device. The advantage of
25 the structure 150 of figure 1(b) is that the fabrication process does not require a high temperature alloying step to form the Ohmic metal contacts through the anodised layer 104. The heavily-doped p-type layer 118 also provides a reduction of the lateral series resistance
30 associated with current being collected in the small area metal contacts which are made through the anodised layer 104.

Devices similar to the solar cells represented in figure 1
35 can be realised using an n-type wafer with a diffused p-type emitter. An anodised layer can be used in these devices in a similar manner as is illustrated in figure 1.

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Referring now to figure 2, there is shown a flow chart 200 with the fabrication process steps of the solar cell 100 of figure 1(a). An analogous process can be used to
5 fabricate the solar cell 150 of figure 1(b). In step 205, p-type mono-crystalline silicon wafers are textured, preferably using an alkaline texturing process, to reduce the reflection from the front surface. A phosphorus-doped emitter 106 is then formed in step 210.

10

After the emitter formation, the phosphosilicate glass is removed and the rear surface is etched to remove any residual phosphorus and isolate the emitter regions. A thin silicon dioxide layer 108 is formed on both surfaces
15 of the wafer in a thermal oxidation step, 215. In step 220, a dielectric layer, such as silicon nitride 110, is formed using plasma-enhanced chemical vapour deposition (PECVD) on the front surface of the device. Openings are then formed in the front surface in step 225 providing
20 electrical access to the n-type surface of the solar cell. The openings can be formed by chemical etching or laser doping. Typically the openings are linear such that they can be subsequently metallised by metal plating to form n-type electrical contacts to the solar cell.

25

A layer of metal, usually aluminium, with a thickness between 25 nm and 800 nm, such as with a thickness between 300 nm to 500 nm is formed over the rear thin oxide 108 on the p-type surface of the device in step 230. This layer
30 can be formed by thermal evaporation, e-beam evaporation or sputtering. The aluminium layer is optionally sintered at 350-400 °C for about 15 minutes to increase its grain size and improve uniformity of the pores.

35 In step 235 the metal layer formed on the solar cell is anodised using an anodisation technique such as the method disclosed herein. The effective minority carrier lifetime

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can be measured for the solar cell after step 235. The lifetime value may not have increased over the value measured before the aluminium evaporation, step 230. This can be due to electrical damage, or defects, caused by the current tunnelling through the thin oxide 108 of the solar cell. A subsequent annealing step 240 after anodisation is performed to passivate defects that may have been introduced during the anodisation step 235 and serves to increase the effective minority carrier lifetime of the solar cell. The improved lifetime is due to hydrogen-containing species within the anodised layer 104, such as retained water, releasing hydrogen into the silicon interface where it can passivate trap states which would otherwise result in carrier recombination. The parameters of the annealing step are related to the properties of the anodised layer and consequentially to the properties of the electrolytic solution and the magnitude of the voltage/current used during the anodisation process. Typically annealing temperatures between 300°C and 500°C provide effective passivation of the solar cell.

The rear anodised dielectric layer 104 is patterned in a further step, 245. The patterning can be realised using chemical etching techniques or by using an inkjet printing apparatus. A metal layer, such as aluminium, is deposited in step 250 on the rear surface of the cell on top of the patterned anodised layer 104 and alloyed in a high temperature firing process in step 255 to form localised heavily-doped regions that enable Ohmic contact to the solar cell and reduce the recombination at the contact regions by forming a high-low junction below the metal. Alternatively a low temperature annealing process can be performed, at temperatures between 300°C and 500°C, to facilitate formation of Ohmic contacts. Finally, metal contacts 112 are formed on the front surface, in step 260. Alternatively metal paste can be screen printed over the patterned openings.

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Referring now to figure 3, there is shown a flow chart 300 illustrating steps to anodise the surface of a semiconductor device comprising a p-n junction according to an embodiment of the present invention. In relation to the fabrication of a silicon solar cell, as in figure 2, the flow chart 300 corresponds to the step numbered as 235. The method 300 of figure 3 may be advantageously used to form a dielectric layer on a surface of a solar cell.

In step 305 the surface portion which needs to be anodised is exposed to an electrolytic solution containing a source of oxygen. The oxygen source can be water or provided by an oxidising electrolyte such as sulphuric acid, nitric acid, phosphoric acid or oxalic acid. To realise porous aluminium oxide layers, electrolytic solutions such as sulphuric acid, phosphoric acid and chromic acid may be advantageously used. Different electrolytic solutions will result in different pore sizes and spacing between pores.

A second portion of the semiconductor device is exposed to suitable radiation, such as visible light. The radiation is absorbed by the semiconductor resulting in the generation of electron and hole charge carriers which are separated by the p-n junction to generate a radiation-induced current. The radiation-induced current is proportional to the intensity of the incident electromagnetic radiation and therefore higher anodisation currents can be achieved using stronger illumination intensities. In some embodiments, the light intensity incident on the front surface of the solar cell is greater than the 0.005 W/cm^2 to sustain the anodisation reaction, and more preferably between 0.01 and 0.1 W/cm^2 . Although higher light intensities can result in larger currents, they can cause undesired variations of the temperature of the electrolytic solution.

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The radiation-induced current flows in the electrochemical circuit constituted by the semiconductor device, the electrolytic solution, a cathode exposed to the electrolytic solution, and an anode which is in electrical
5 contact with a surface portion of the device. In this case, the radiation-induced current and the oxygen contained in the electrolytic solution act together to anodise a surface portion of the semiconductor device.

10 However, often the radiation-induced current of the semiconductor device is insufficient to drive a sustained anodisation reaction on the surface of the semiconductor device as the current must be able to tunnel through the forming dielectric layer which presents a significant
15 resistance to the current flow in the circuit. The overall resistance of the electrochemical circuit, constituted by the surface being anodised, the wiring, the electrolytic solution and the interface between the solution and the surface being anodised, may be too high to allow a
20 sustained current. To overcome this problem, in some embodiments of the invention, a bias voltage is applied to the device to offset the circuit resistance, in step 315. In these embodiments the device is illuminated whilst a biasing voltage is applied to the illuminated surface. The
25 biasing voltage can be applied to a surface portion of the semiconductor device using an electrode element connected to the voltage source which acts as an anode for the electrochemical circuit. In an alternative embodiment the voltage source is replaced by a current generator, step
30 320.

An anodisation current can be observed in the electrochemical circuit as anodisation proceeds in step 325. When this current drops below a certain threshold
35 (typically less than 1 mA), the anodisation process is considered complete. The semiconductor device is removed from the anodisation apparatus in step 330 and then rinsed

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in deionised water to remove traces of electrolyte and dried in step 335.

Referring now to figure 4, there is shown a simplified
5 schematic of a light-induced anodisation apparatus 400 in accordance with an embodiment of the present invention. In the example of figure 4, the device is a single junction silicon solar cell 401 that comprises a p-type silicon wafer. The p-type surface of the solar cell 401 comprises
10 a thin oxide 403 and a metallic layer 405, such as an aluminium layer, and is exposed to the electrolytic solution. The apparatus comprises a container 402 for containing an electrolytic solution 404, a cathode element 406, a light source 408 arranged to illuminate the top
15 surface of the solar cell and a support 410 which supports the solar cell such to expose the bottom surface of the cell to the electrolytic solution and the top surface to the incoming light 412.

20 In the embodiment of figure 4 the system has a voltage source 414 which applies a biasing voltage between an electrode 416 on the top surface of the solar cell and the cathode element 406. The electrode 416 is a transparent or semi-transparent electrode which allows the incoming light
25 412 to reach the active area of the solar cell 401 to induce a current in the device. The cathode element 406 is at least partially exposed to the electrolytic solution 404. The light-induced current flows in the electrochemical circuit comprising the solar cell 401, the
30 anode 416, the voltage source 414, the cathode element 406 and the electrolytic solution 404, allowing the anodisation of the surface material at the bottom surface (rear) of the solar cell 401.

35 The electrode 416 may comprise a transparent conductive polymer layer formed on glass, or alternatively a conductive film deposited on a transparent substrate such

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as, an indium tin oxide (ITO) coated glass or plastic and fluorine doped tin oxide (FTO) coated glass or plastic.

The chemical solution 404 is typically an electrolytic
5 solution containing an oxygen source. The chemical
solution 404 may for example comprise an electrolyte with
0.5 M sulphuric acid. However, concentrations in the range
of 0.2 M and 2.0 M can also be used. Sulphuric acid is
known to result in fast anodisation compared to other
10 electrolytes (i.e., phosphoric acid and oxalic acid).

Referring now to figure 5, there is shown a simplified
schematic of a light-induced anodisation apparatus 500 in
accordance with another embodiment of the present
15 invention. In the example of figure 5, the device is a
silicon wafer 530 comprising a p-n junction. The wafer 530
is held by conductive vacuum wafer holder 510 with the n-
type surface facing up. Light sources 520, built into the
vacuum wafer holder 510, provide illumination during the
20 anodisation process. The p-type surface 540 of the wafer
may comprise a metallic layer, such as an aluminium layer,
and is exposed to the electrolytic solution. An underlying
nozzle 580 facilitates the initial contact with the
electrolytic solution by 'wetting' the surface 540. A
25 biasing voltage 505 is applied across the top side of the
wafer and the cathode element 560 in the p-n junction
reverse bias direction but without driving the junction in
the reverse bias region. The top surface of the wafer is
electrically connected to the anode of the voltage source
30 505 by the conductive vacuum holder 510. A filter 550 is
placed between the wafer 530 and the cathode element 560
to minimise the impact of bubbles from evolved hydrogen on
the cathode during anodisation.

35 Referring now to figure 6(a), there is shown a variation
600 of the light-induced anodisation apparatus 500 of
figure 5. In this embodiment the wafer 530 comprises a

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transparent electrode 610. An array of light sources 605 is placed above the transparent electrode 610 to provide illumination.

5 Referring now to Figure 6(b), there is shown a further variation 615 of the light-induced anodisation apparatus. In the embodiment of figure 6(b) the electrode element 620 is a patterned flexible electrode and does not require being transparent. Illumination provided by the light
10 sources array 605 is conveyed through the patterned electrode 620 to the top active surface of the wafer 530. The patterned flexible electrode may comprise a conductive gel formed on rubber, a conductive rubber or a graphite mat.

15 Referring now to figure 7(a), there is shown a schematic of an in-line light-induced anodisation apparatus 700 in accordance with another embodiment of the present invention. The apparatus consists of multiple vacuum wafer
20 holders 720, nozzles 580 and a larger electrolytic solution container. Wafer holders 720 are connected in parallel to the voltage source 505 to ensure consistent voltage bias. The electrolytic solution concentration and temperature is maintained by circulating the electrolytic
25 solution through an inlet 730 and an outlet 740 of the container.

Referring now to figure 7(b), there is shown a variation
715 of the apparatus of figure 7(a). The apparatus 715
30 consists of a set of conductive rollers 750 contacting the top side of solar cell whilst another set of non-conductive rollers 760 support wafers from the bottom side. An array of light sources 605 is above the conductive rollers 760 to provide illumination through the
35 gaps between rollers. The moving rollers will guide the wafer which moves laterally through the electrolytic solution container while being anodised.

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Referring now to figure 7(c), there is shown a variation 725 of the apparatus of figure 7(b) where the conductive rollers 750 are replaced by a conductive conveyer belt 770 which contacts the top side of solar cell. The use of a conveyer belt 770 allows continuous contact between the bias voltage source 505 and the top side of the solar cells.

10 In the embodiments of the radiation-induced anodisation apparatus disclosed herein, such as the examples illustrated in figures 4 to 7(c), the temperature of the electrolytic solution is maintained at a constant value to ensure a consistent anodisation reaction and to control
15 any electrolytic solution heating effects that may result from illumination. The temperature may be set at a value between 0 °C and 80 °C. The anodisation reaction is faster at higher temperature and the electrical and morphological properties of the porous oxide are related to the
20 anodisation temperature.

The method shown in figure 3 and the apparatus of figures 4 to 7(c) can be used to anodise a surface layer of a semiconductor device. The physical properties of the
25 anodised layer are related to the type of material being anodised, the type of electrolytic solution and the anodisation conditions. For example, a compact barrier oxide layer may be formed or a porous oxide layer may be formed depending on the solubility of the oxide in the
30 electrolytic solution. Aluminium, for example, can form a porous oxide layer because aluminium oxide has significant solubility in the commonly-used electrolytes of sulphuric acid, phosphoric acid, oxalic acid, and mixtures thereof. Nevertheless, aluminium forms a barrier oxide layer if it
35 is anodised in a solution such as boric acid wherein the aluminium oxide is less soluble. Porous anodic oxides can reach thicknesses of several micrometers. The pores in

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fact enable a sustained oxidation reaction to occur providing the electrolytic solution with access to the unreacted metal or semiconductor.

5 More generally, the physical properties of the anodised layer can be modified by changing the chemical properties of the electrolytic solution, the intensity of the radiation and the biasing voltage or current in the circuit. For example, in the anodisation process of
10 aluminium, a sulphuric acid electrolyte can be used to obtain pore sizes between 12 nm and 100 nm, with 12 nm pores being typical when a 0.5 M sulphuric acid electrolyte is used. Alternatively, phosphoric acid and oxalic acid may be used to obtain larger pore sizes, with
15 pore diameters between 30 nm and 235 nm being able to be achieved using phosphoric acid.

Advantageous embodiments of the present invention can be used to anodise the rear surface of a solar cell, or a
20 layer of material formed on a surface of a solar cell, such as a layer of aluminium or titanium on the p-type surface of a silicon solar cell. Figure 4 shows an embodiment of a light-induced anodisation apparatus where the rear surface of a silicon solar cell is anodised. The
25 p-type surface of the silicon solar cell 401 is in contact with the electrolyte 404, whilst the n-type surface is contacted by the electrode element 416 and illuminated by radiation 412 generated by the biasing light source 408. The oxide layer forms at the silicon/electrolyte interface
30 and grows inwards towards the silicon substrate. The anodisation process is sustained by the supply of electrons which tunnel through the formed oxide at the surface. As the oxide grows thicker, the amount of electrons which can tunnel through it decreases. The
35 anodisation reaction proceeds until the current ceases to flow or reduces below a threshold. The thickness of the anodised layer may be varied by modifying the voltage

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bias. In fact, a higher bias, thus a stronger electric field, allows electrons to tunnel through thicker oxide layers.

5 The bias voltage is operated in a manner to avoid reverse biasing of the p-n junction to maintain uniform current flow through the surface being anodised. Reverse bias of the junction may cause breakdown which may lead to non-uniform currents. Reduced sources of recombination in the
10 solar cell increase the radiation-induced potential of the cell and may increase the thickness of the formed oxide layer.

Suitable electrolytic solutions for the formation of
15 silicon oxide layers are nitric acid and sulphuric acid, with acid concentrations of 0.1 M to 5 M. These provide silicon oxide layers with high electrical quality.

The properties of the surface portion exposed to the
20 electrolytic solution also affect the anodisation process. For example, a hydrophobic surface is difficult to 'wet' uniformly in the electrolytic solution. Non-uniform anodisation may occur in localised regions where the surface is not as hydrophobic. Uniform anodisation
25 requires a clean and hydrophobic surface that aids 'uniform wetting' by the electrolytic solution, assuring effective surface passivation. In some instances, a clean and hydrophobic surface is formed by removing the native oxide in a 2.5% (w/v) hydrofluoric acid solution and
30 rinsing in deionised water for at least 10 minutes to grow another clean thin native oxide. The native oxide is densified and incorporated into the anodic oxide that forms during the anodisation process. In other instances, for example radiation-induced anodisation of silicon, the
35 anodisation process may be started on the hydrophobic surface of a silicon substrate directly after hydrofluoric acid solution and a seed oxide layer is not essential.

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The electronic passivation of the formed anodised layer may be improved by performing an annealing step (see figure 2, step 240). For example, anodised silicon dioxide layers can be annealed in an oxygen ambient at 400 °C for at least 15 minutes and then in forming gas (Ar/H₂) at the same temperature for additional, at least, 15 minutes. The oxygen anneal facilitates the completion of the oxide formation. The forming gas provides a source of hydrogen that can penetrate the anodic oxide and passivate defect states that may have formed at the silicon interface with the formed silicon dioxide layer. Unlike the anodisation process of a metal layer, such as aluminium, where water vapour and other hydrogen-containing species can become trapped within the porous structure and provide a source of hydrogen. Barrier silicon dioxide layers have limited ability to store hydrogen sources from the electrolytic solution and consequently are more dependent on external sources of hydrogen such as forming gas for passivation of the interfacial defect states.

In order to further understand the mechanisms which regulate the light-induced anodisation process, the apparatus illustrated in Figure 4 can be represented in terms of an equivalent electrochemical circuit 800 as shown in figure 8. The solar cell can be represented as a single junction device, which comprises a current generator 805 representing the light-induced current, the p-n junction 810, the shunt resistance 860 and a series resistance 820. A capacitor in parallel with a resistor 830 represents the electrochemical surface potential between the material to be anodised and the electrolytic solution. The Ohmic resistance in the electrochemical circuit is represented by a resistor 840. This resistance includes contributions from the electrolytic solution and the wires, whilst another resistor 870 represents the contact resistance between the electrode element and the

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electrically contacted surface of the solar cell. The electrochemical surface potential between the cathode and the electrolytic solution is represented by a capacitor in parallel with a resistor 880.

5

The biasing voltage 850 is applied across the electrode element and the cathode in a polarity such as to reverse bias the p-n junction 810 and thus effectively offset the resistance of the two resistors 840, 870 in the circuit.

10 If resistance is high then the load experienced by the solar cell will exceed the open circuit voltage and there will be no light-induced current, thus no anodisation will occur. To give a term of comparison, the resistances associated with the anodisation electrochemical circuit
15 are much larger, for example, than the resistances of a metal plating electrochemical circuit. This is due to the tunnelling current through the dielectric layer. In one embodiment a thin oxide layer 108 is realised on the surface of the solar cell to prevent damage of the silicon
20 and provide a barrier layer for the aluminium oxide.

In the embodiments represented in figures 4 to 7, the light-induced current flows through the solar cell towards the p-type surface in a direction that is transversal to
25 the surface being anodised. This is substantially different to other anodising systems where current extends over the surface exposed to the electrolytic solution from a contact point or region of an anode. The fact that the current is uniformly delivered to the entire surface to be
30 anodised means that very uniform oxides can be formed.

The bias voltage should be selected such that the illuminated current-voltage curve of the device operates closer to the short circuit current position to maximise
35 the light-induced current and avoid reverse bias. It is important not to reverse-bias the device being anodised to avoid non-uniform current flow. For example, if laser-

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doped openings are being used to enable the bias voltage to be applied to one side of the device and the device is forced into reverse bias, the regions of the junction may enter electrical breakdown at different voltage levels and
5 a non-uniform current may flow through the device. In severe cases of reverse-biasing a solar cell's operating voltage may be reduced.

The electrolytic solution for the anodisation process does
10 not require metal ions, thus the absorbance of the incident light by the solution is negligible, in contrast with light-induced plating processes. Consequently, a wide range of light sources can be used in a light-induced anodisation apparatus. In one specific arrangement,
15 compact fluorescent light sources are used. However, alternative variations can use other light sources such as high-power LEDs, neon light sources or halogen light sources.

20 Referring now to figure 9, there is shown a simplified diagram of a portion 900 of a device comprising a porous anodised aluminium oxide layer formed over an interfacial thin oxide layer 930 by anodising in an acid electrolytic solution in accordance with an embodiment of the present
25 invention. During the anodisation process small pores are initiated at the surface and grow inwards as the oxidation process attains equilibrium between dissolution and formation of the aluminium oxide. The pores 910 become transversally oriented with a barrier layer of aluminium
30 oxide 920. The thickness of the aluminium oxide 920 is determined principally by the anodisation voltage, which is related to the self-bias of the p-n junction in the device being anodised (light-induced voltage) and the applied bias voltage. Whilst unreacted aluminium remains
35 and the current can tunnel through the barrier layer 920 the anodisation process continues. The result of this process is a porous layer of anodised aluminium with an

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inner barrier layer of compact aluminium oxide. In the method described herein no regions of unreacted aluminium remain when the anodisation current drops below a certain threshold which indicates the end of the anodisation process. In some instances the threshold may be lower than the accuracy of the current-measuring instrument used to monitor the anodisation current. Furthermore, the light-induced anodisation process is not sensitive to the morphology of the surface being anodised and forms a uniform layer irrespective of whether the underlying surface of the semiconductor device is textured, planarised or polished.

In some embodiments, the light-induced anodisation method of the present invention is used to form barrier layer oxides. For example, layers of metals including, but not limited to, aluminium can be anodised in electrolytic solutions in which the formed oxide has a low solubility. The thickness of the dense oxide layer is limited by the voltage insisting on the anodised surface. Layers of an active device, for example a silicon layer of a silicon solar cell, may also be anodised to form compact barrier thin silicon dioxide layers. These thin oxide layers can contribute to surface passivation and also provide protection to potential-induced degradation. The thin oxides layers can be capped with other dielectric layers such as silicon nitride and form part of an antireflection coating of the solar cell.

After the light-induced anodisation process and successive annealing step, the anodised layer may be patterned to enable further processing, for example, the formation of metal contacts to one surface of a silicon solar cell. In an embodiment, the patterning step is realised using an inkjet printing apparatus which is arranged to selectively etch areas of the anodised layer. Well-resolved arrays of holes in the both the thin oxide and anodised layer, with

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a diameter as small as 20 micrometers to 40 micrometers can be formed by inkjet printing 50% (w/w) H_3PO_4 onto the surface of an anodised aluminium layer. The printing process may be performed using a substrate temperature
5 within the range of 30 °C to 75 °C, such as around 60 °C. The ambient relative humidity may be in the range of 20% to 80%. After the ink-jet printing is performed, wafers are transferred to a heated plate with a temperature in the range of 60 °C to 250 °C to accelerate the etching. The
10 residue acid is then rinsed off in deionised water.

Referring now to Figure 10, there is shown a microscopic image of an array of etched holes 160 spaced 250 micrometers apart formed in an anodised aluminium layer
15 with an initial thickness of 600 nm. The aluminium layer, deposited on a planar wafer, was anodised using a light-induced anodisation method in accordance with an embodiment of the present invention and it was patterned by inkjet patterning. When the anodised aluminium layer is
20 used on the p-type rear surface of a silicon solar cell to form an effective contact to the solar cell, an additional capping layer of aluminium may be deposited on the anodised layer. The additional layer may be deposited by thermal evaporation, e-beam evaporation or sputtering onto
25 the patterned anodised aluminium surface. This additional aluminium layer is then alloyed with silicon through the fine scale patterned holes 160 by annealing the solar cell at temperatures above the eutectic temperature of the aluminium-silicon binary alloying system. The result of
30 this process is schematically represented in figure 11(a) and a cross sectional scanning electron microscope image is shown in figure 11(b).

Figure 11(a) shows a portion 165 of a solar cell
35 comprising an aluminium-doped silicon layer 175 at the interface of a p-type silicon substrate and the eutectic region 170. The local back surface electric field (BSF)

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created by the aluminium-doped p-type region 175 provides shielding of the minority carriers from the high surface recombination velocity area at the metal-silicon interface. Figure 11(b) shows a cross sectional scanning electron microscope image 180 of a point contact and local BSF formed by the aluminium alloying step. The local BSF regions were exposed for imaging purposes by laser cleaving from the front (i.e., non-aluminium) surface and etched for 20 seconds in an $\text{CH}_3\text{COOH}:\text{HNO}_3:\text{HF}$ (6:3:1) solution which etches heavily-doped p-type silicon at a faster rate than moderately-doped silicon.

Referring now to figure 12, there is shown a comparison of scanning electron microscope images of an aluminium layer 191 anodised using a light-induced anodisation method in accordance with an embodiment of the present invention and an aluminium layer 192 anodised using the clip-based anodisation common in the prior art. The cross sectional image 194 shows the porous structure of the light-induced anodised aluminium layer 191. Both surfaces show the porous structures, although small differences in pore spacing exists, the size of the pores formed through the use of the light-induced anodisation method is very similar to those formed using the clip-based method.

Referring now to figure 13, there is shown a plot 195 of implied open circuit voltages (iVoc) of solar cell devices as a function of processing steps. The iVoc can be computed from photo-conductance measurements and is representative of the effective minority carrier lifetime of the device. The plot compares the iVoc values of solar cells with anodised layers formed using a light-induced anodisation method in accordance with an embodiment of the present invention (left columns - LIA) and the clip based method common in the prior art (right columns - CLIP). The iVoc were measured at each step of the fabrication process and compared. Figure 13 highlights the variations of iVoc

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throughout the process, with the error bars showing the standard deviation of 5 samples. Solar cells in both groups started with comparable iVoc values, however the cells in the LIA group were affected by laser induced damage during the required laser doping step. After anodisation, an average increase of 10 mV in iVoc was observed in the CLIP group, while only marginal increase occurred in the LIA group. A significant improvement of the cells in the LIA group was observed after the annealing process. The iVoc of the LIA cells increased from 640 mV to an average of 670 mV, whilst the iVoc of the CLIP group increased only slightly in average. The anneal process effectively passivates the damage induced by the light induced anodisation process and increases the iVoc. On the contrary, the susceptible non-uniform and incomplete anodisation of the clip-based method introduces variations between wafers, which result in inconsistent results after heat treatment and poorer final passivation properties.

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

Throughout this specification the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

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The Claims:

1. A method of anodising a surface of a semiconductor device comprising a p-n junction, the method comprising
5 the steps of:
 exposing a first surface portion of the semiconductor device to an electrolytic solution that is suitable for anodising the first surface portion when an electrical current is directed through a region of the semiconductor
10 device at the first surface portion; and
 exposing a portion of the semiconductor device to electromagnetic radiation in a manner such that the electromagnetic radiation induces the electrical current and the first surface portion anodises.
15
2. The method of claim 1 wherein the step of exposing a portion of the semiconductor device to electromagnetic radiation comprises exposing a second surface portion to the electromagnetic radiation, the second surface portion
20 being a surface portion that is different to the first surface portion.
3. The method of claim 2 wherein the first and second surface portion are at opposite sides of the semiconductor
25 device.
4. The method of any one of the preceding claims further comprising the step of selecting a property of the electrolytic solution to influence a property of the first
30 surface portion after anodising.
5. The method of any one of the preceding claims comprising the step of patterning the first surface portion after anodising to influence a property of the
35 first surface portion after anodising.
6. The method of any one of the preceding claims wherein

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the method is conducted such that the radiation-induced current flows transversally to the first surface portion of the semiconductor device.

5 7. The method of any one of the preceding claims wherein semiconductor device is a silicon solar cell.

8. The method of any one of the preceding claims comprising the step of applying a biasing voltage to
10 generate a biasing electrical current to supplement the electrical current that is induced by the electromagnetic radiation.

9. The method of claim 8 wherein the semiconductor
15 device comprises an electrode element that is at least semi-transparent to the electromagnetic radiation and wherein the biasing voltage is applied via the electrode element.

20 10. The method of claims 8 or 9 further comprising the step of selecting the biasing voltage to influence a property of the first surface portion after anodizing.

11. An apparatus for anodising a semiconductor device
25 comprising a p-n junction, the semiconductor device having a first side portion and a second side portion, the apparatus comprising:

a radiation source arranged to illuminate the second side portion of the semiconductor device;

30 a container for containing an electrolytic solution;

a cathode element positioned for contacting the electrolytic solution; and

a support arranged to support the semiconductor device such that in use the first side portion of the
35 semiconductor device is exposed to the electrolytic solution when the container is charged with the electrolytic solution and the second side portion is

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illuminated by radiation from the radiation source in a manner such that a radiation-induced current is generated to anodise the second side portion.

5 12. The apparatus of claim 11 further comprising a voltage source arranged to apply a biasing voltage between the second side portion of the semiconductor device and the cathode element.

10 13. A solar cell device comprising an anodised dielectric layer formed by the method in accordance with any one of claims 1 to 10.

14. The solar cell device of claim 13 wherein the
15 anodised dielectric layer is an oxide layer.

15. The solar cell device of claim 13 wherein the anodised dielectric layer comprises aluminium and/or titanium.

20 16. The solar cell device of any one of claims 13 to 15 wherein the anodised dielectric layer is patterned.

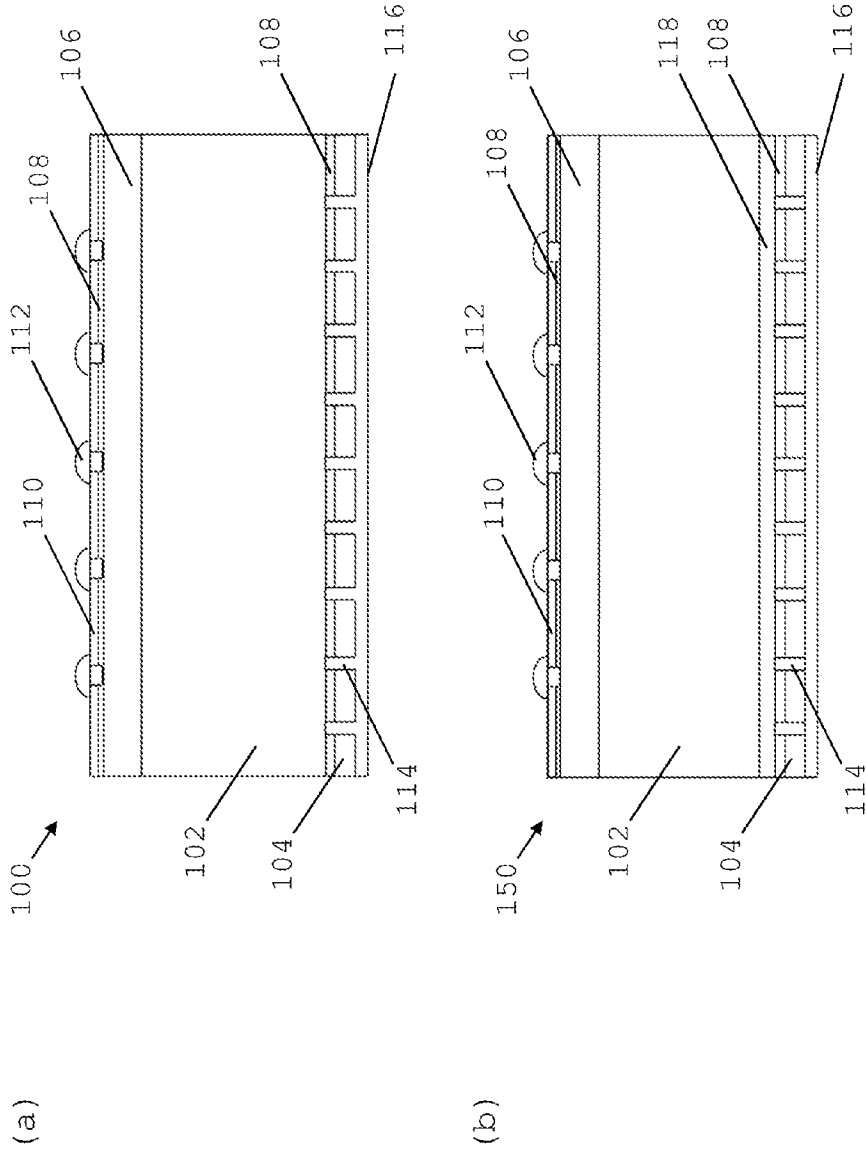
17. The solar cell of claim 16 wherein the anodised
25 dielectric layer is patterned such that the anodised dielectric layer comprises pits with a diameter between 50 and 200 micrometers.

18. The solar cell of any one of claims 13 to 17 wherein
30 the first surface portion is a surface portion of a p-type or n-type region of the p-n junction.

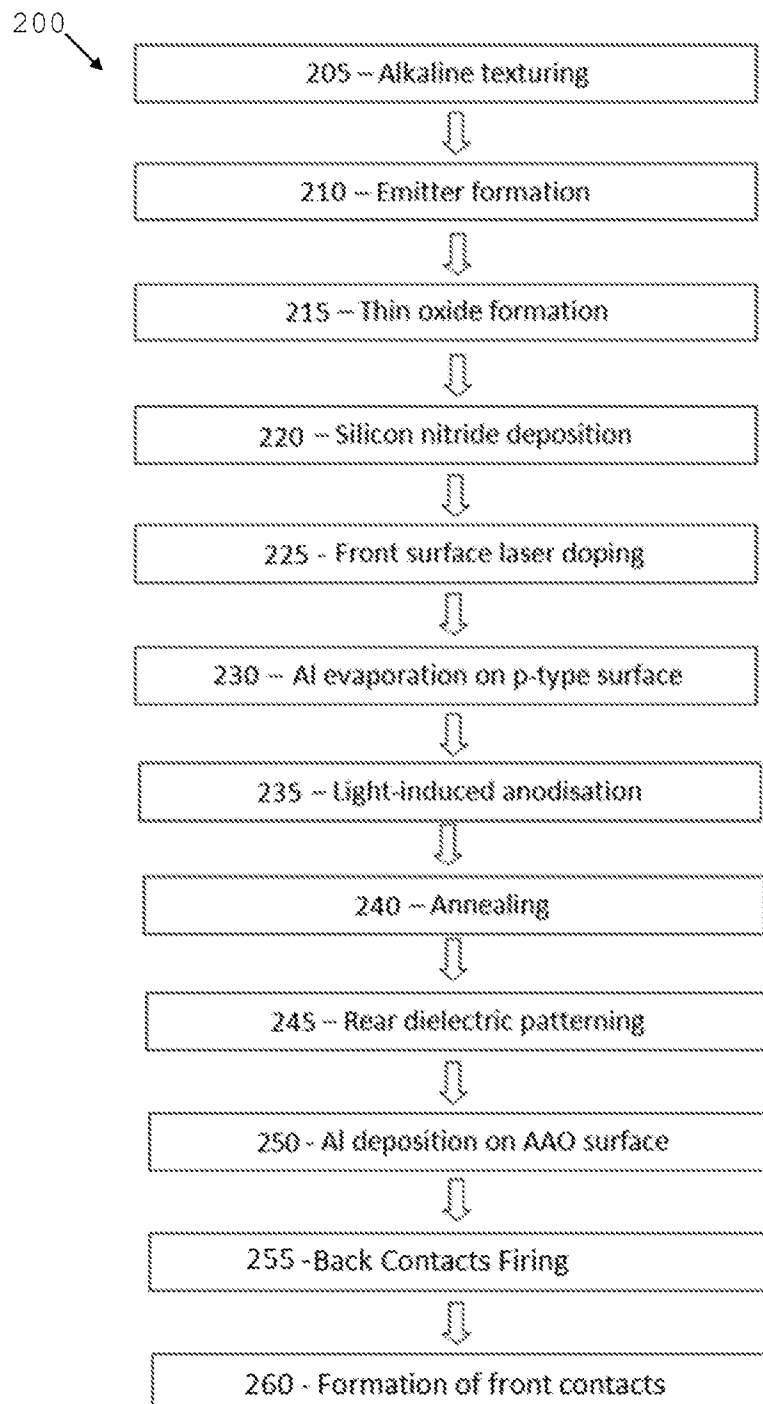
19. The solar cell of any one of claims 13 to 17 wherein
the first surface portion is a surface portion of a layer
35 deposited on a p-type or n-type surface portion of the semiconductor device.

- 30 -

20. A method of anodising a dielectric layer of a solar cell device comprising use of the apparatus of claim 11 or 12.



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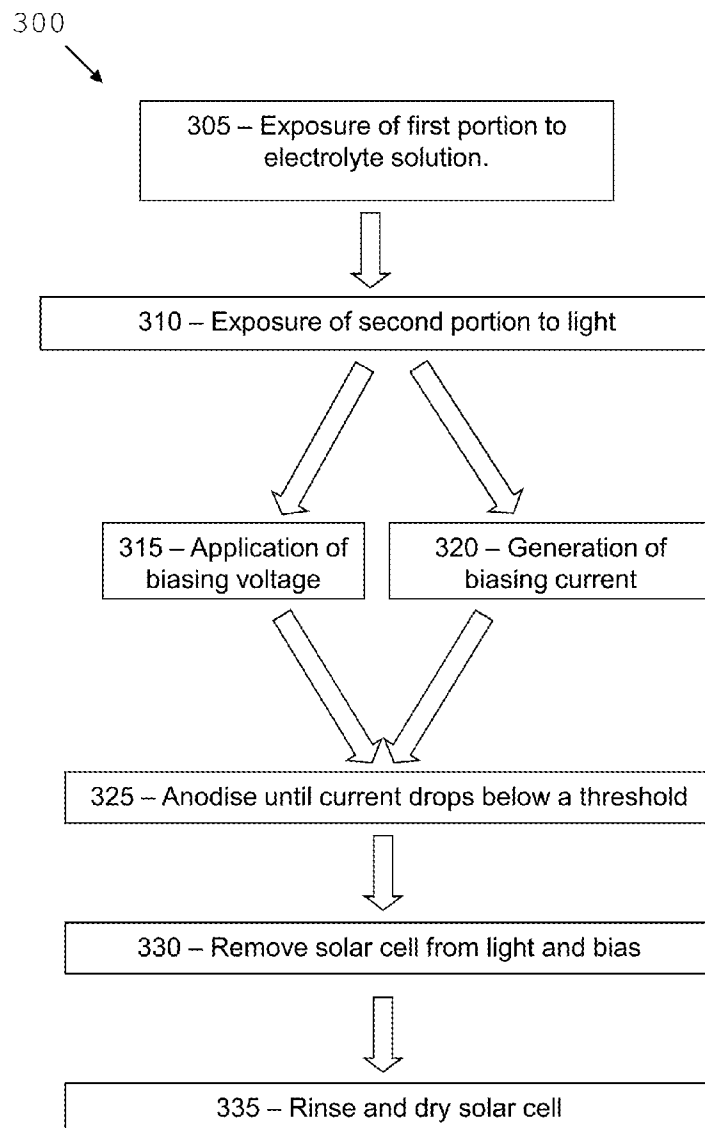


FIGURE 3

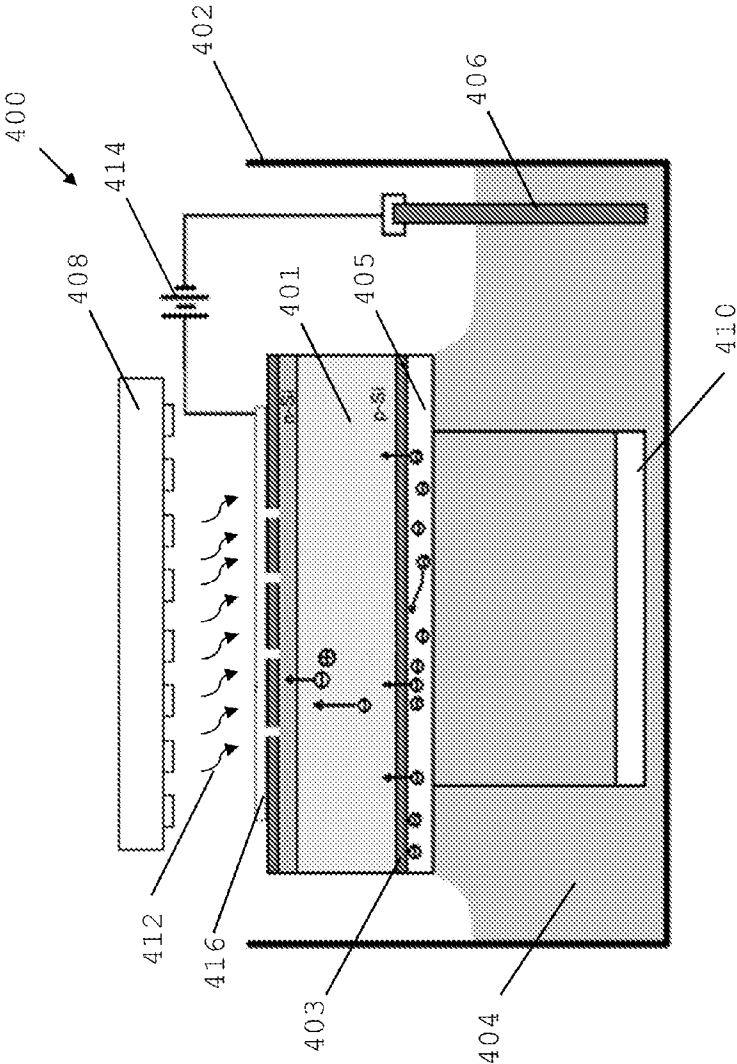


FIGURE 4

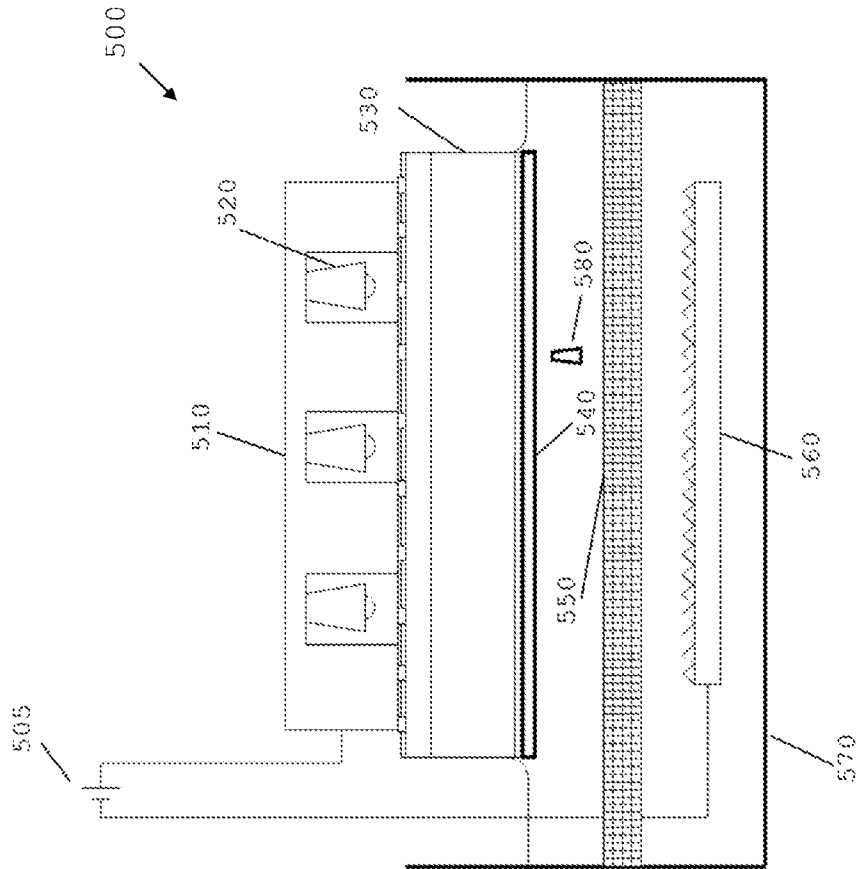


FIGURE 5

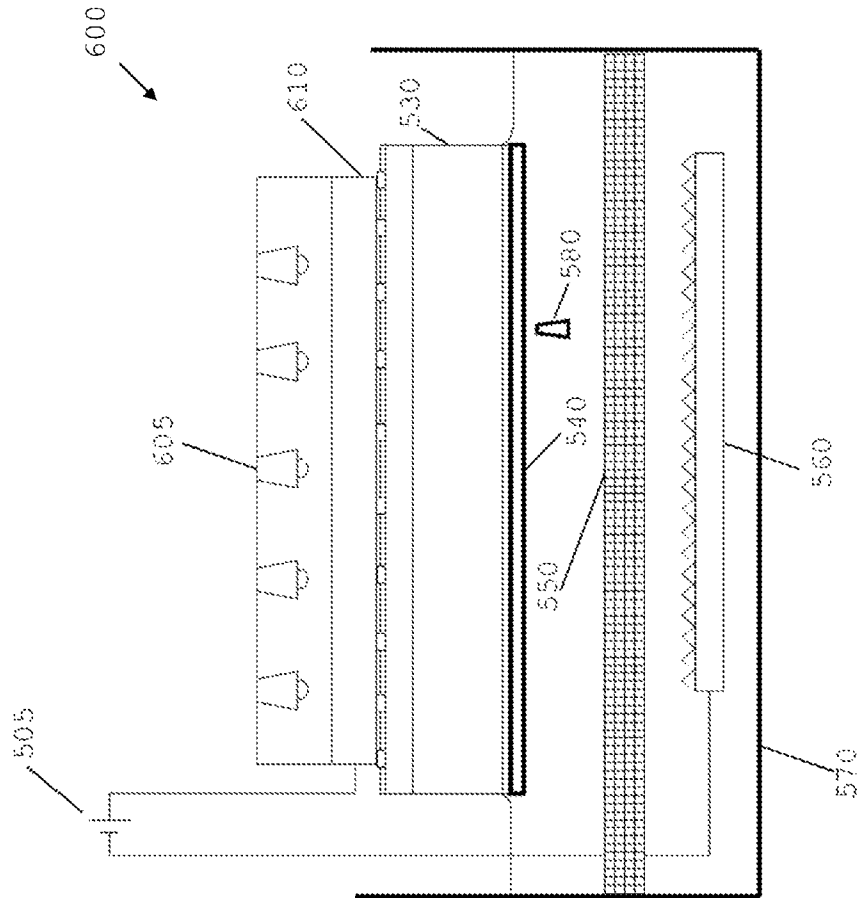


FIGURE 6 (a)

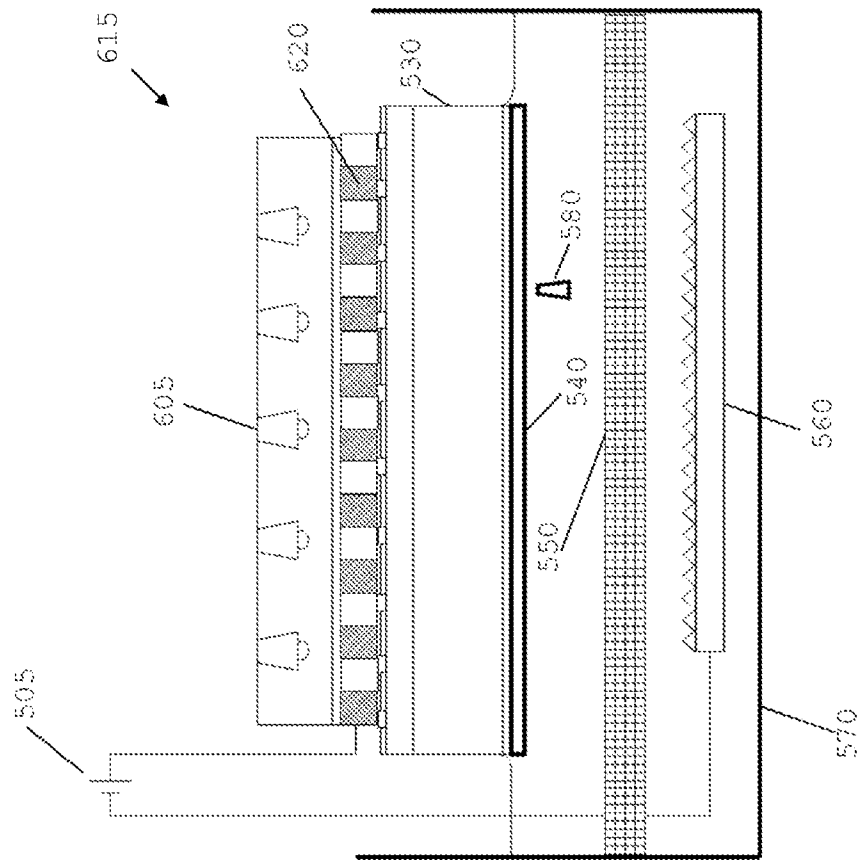


FIGURE 6(b)

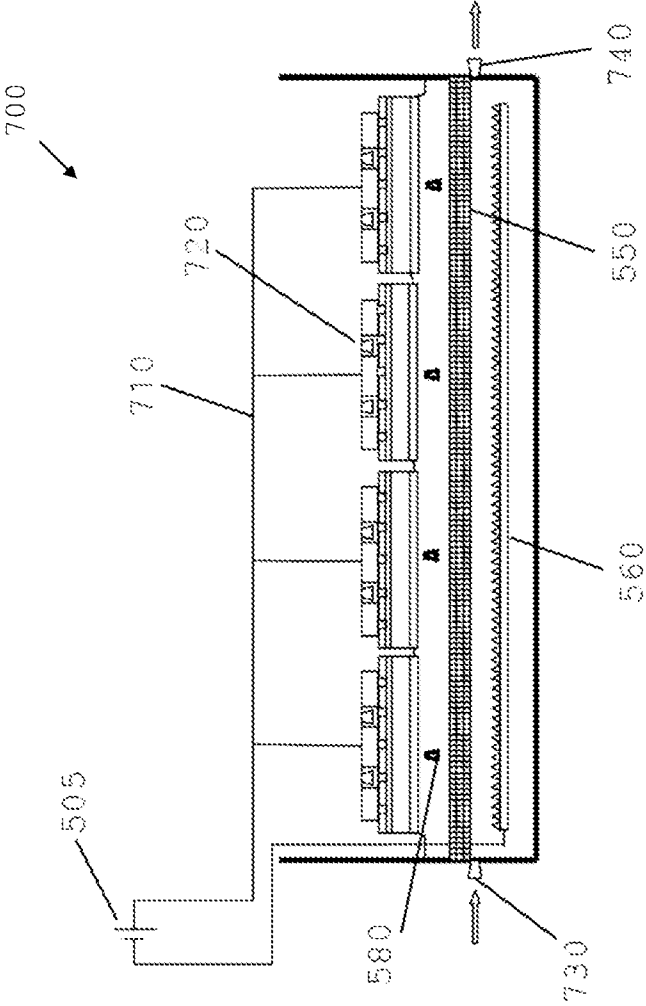


FIGURE 7(a)

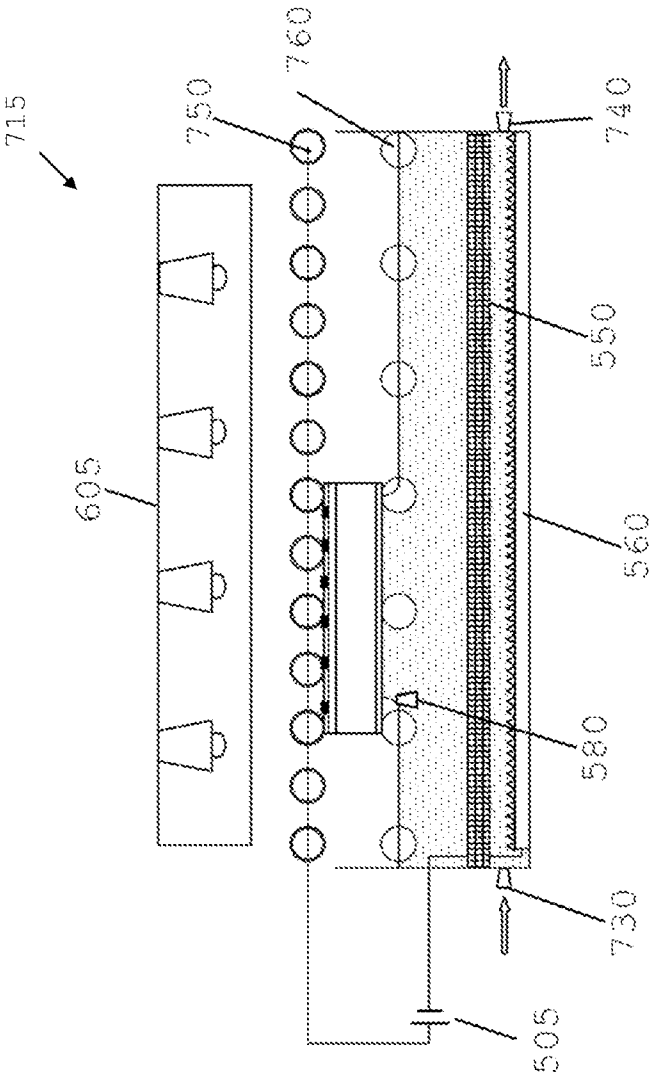


FIGURE 7(b)

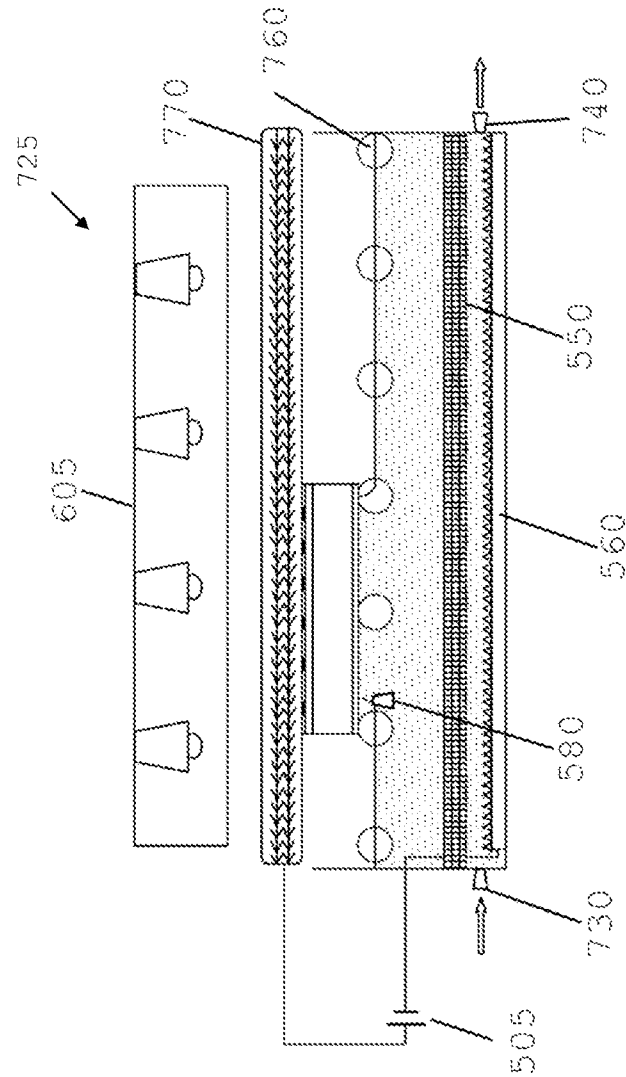


FIGURE 7(c)

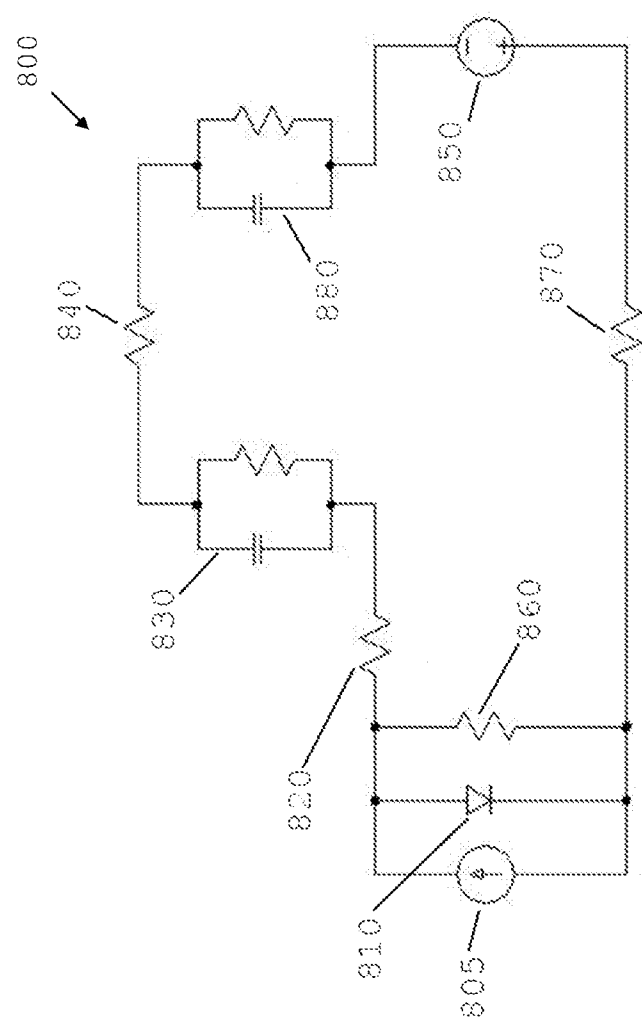


FIGURE 8

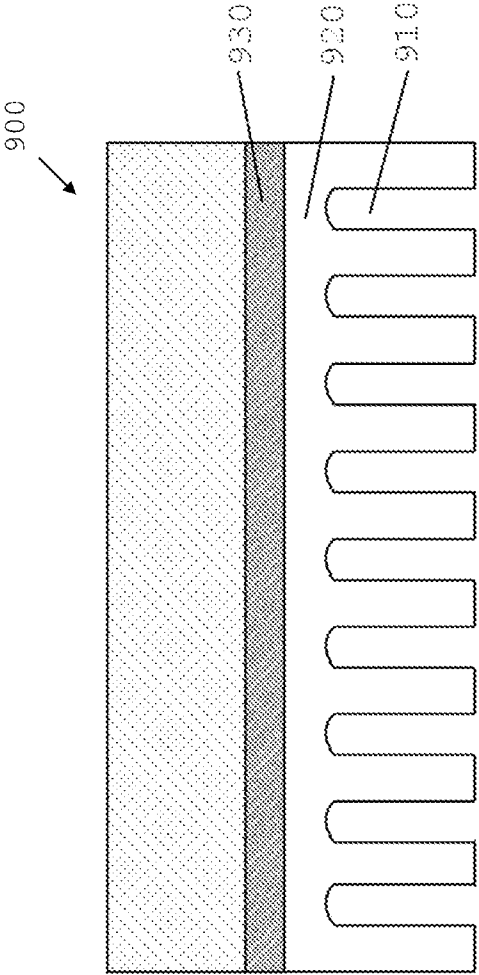


FIGURE 9

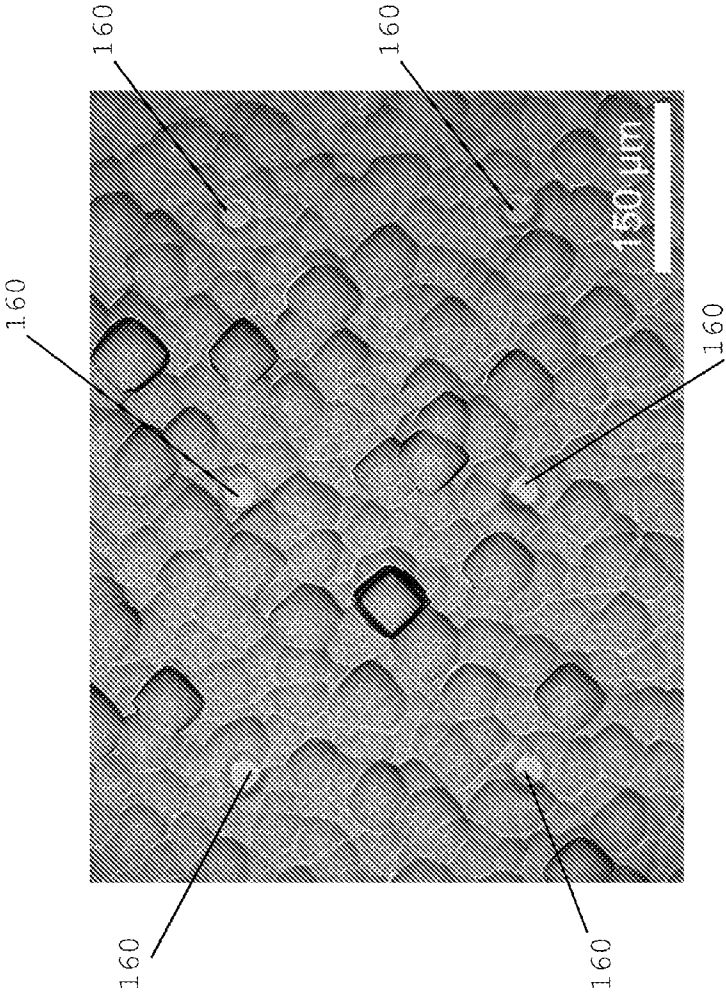


FIGURE 10

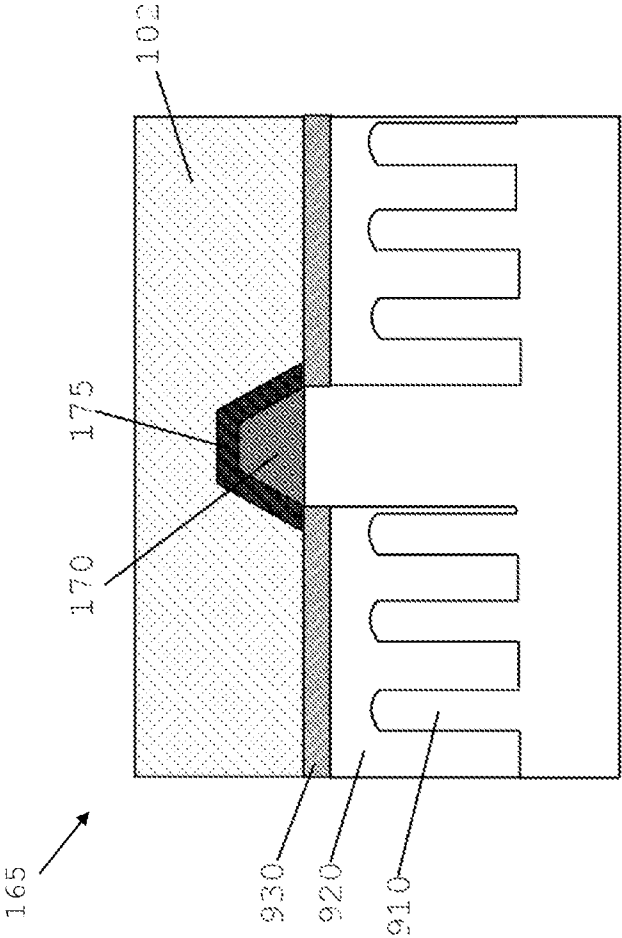


FIGURE 11(a)

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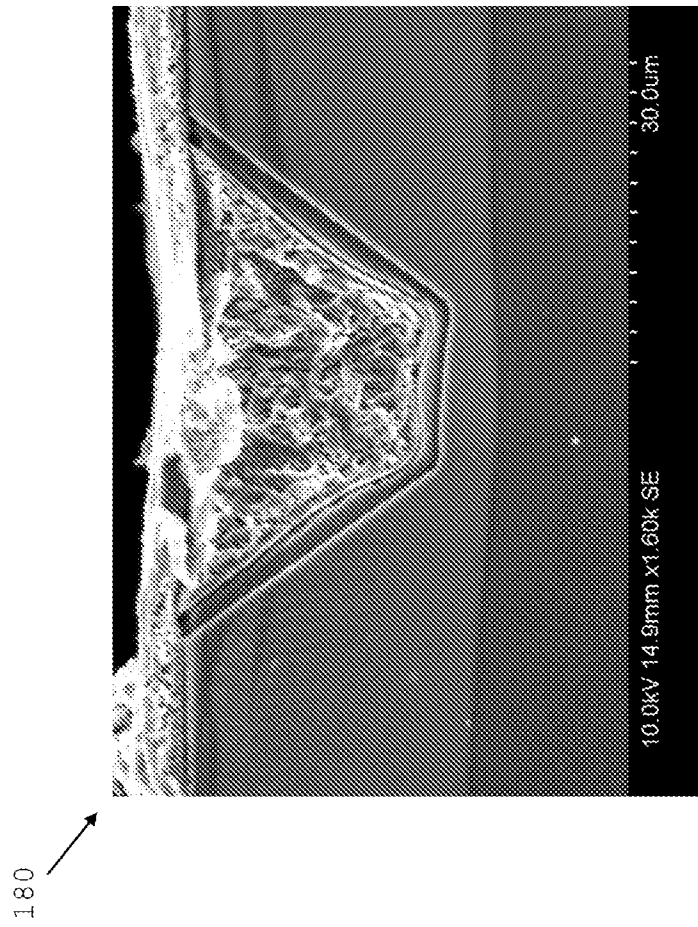


FIGURE 11(b)

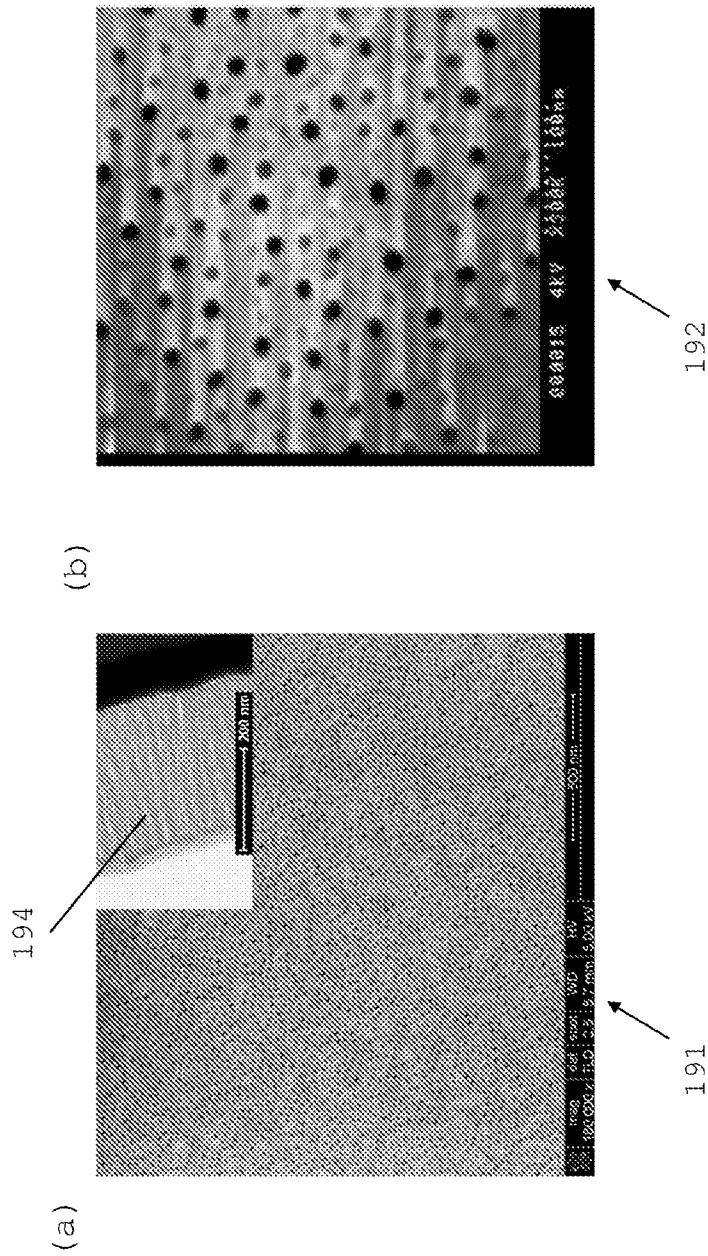


FIGURE 12

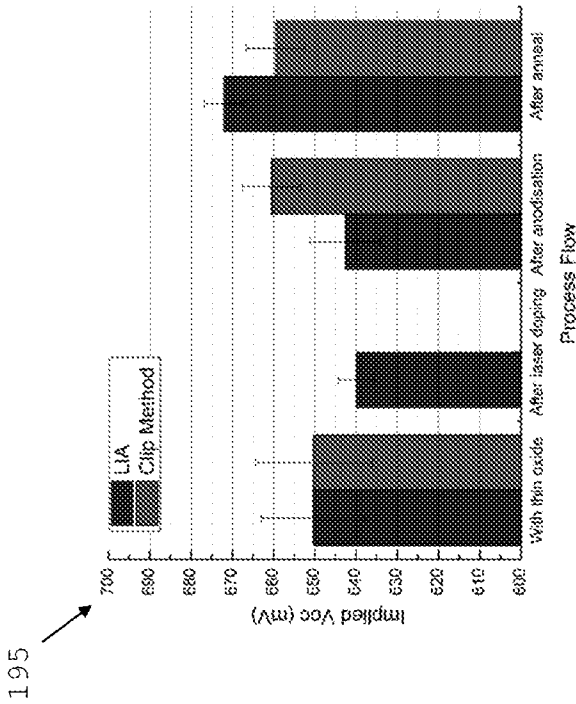


FIGURE 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/AU2014/000307**A. CLASSIFICATION OF SUBJECT MATTER****C25D 11/06 (2006.01) C25D 11/12 (2006.01) C25D 17/06 (2006.01) H01L 21/306 (2006.01)**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: GOOGLE PATENTS, GOOGLE SCHOLAR, ESPACENET, WPI, EPODOC, INSPEC, English fulltext cluster (TXTUS5, TXTUS4, TXTUS3, TXTUS2, TXTUS1, TXTUS0, TXTEP1, TXTGB1, TXTWO1, TXTAU1, TXTCA1, TXTSG1)**Keywords:** Anodising, P-N Junction, Semiconductor, Solar, Substrate, Passivation, Dielectric, Layer, Coating, Film, EMR, Electromagnetic, Radiation, Bias, Voltage, Current, Radiation Induced, Light Induced and similar terms.**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search
20 May 2014Date of mailing of the international search report
20 May 2014**Name and mailing address of the ISA/AU**AUSTRALIAN PATENT OFFICE
PO BOX 200, WODEN ACT 2606, AUSTRALIA
Email address: pct@ipaustalia.gov.au
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Telephone No. 0262832814

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/AU2014/000307
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Yoshida, T. et al., "Photo-Induced Preferential Anodization for Fabrication of Monocrystalline Micromechanical Structures", Micro Electro Mechanical Systems, 4 - 7 February 1992, Travemünde, Germany, Pages 56 - 61 Abstract, Pages 56, 57 & 59, Figures 1 & 8	1 - 7, 11, 13 - 20
A	US 2694040 A (DAVIS et al.) 09 November 1954 Whole Document	1 - 20
A	GB 1058689 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) 15 February 1967 Whole Document	1 - 20
A	EP 2565299 A1 (SHARP KABUSHIKI KAISHA) 06 March 2013 Whole Document	1 - 20

Form PCT/ISA/210 (fifth sheet) (July 2009)

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/AU2014/000307	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2694040 A	09 Nov 1954	None	
GB 1058689 A	15 Feb 1967	DE 1489019 A1	19 Jun 1969
		DE 1489019 B2	30 Mar 1972
EP 2565299 A1	06 Mar 2013	CN 102869813 A	09 Jan 2013
		WO 2011136229 A1	03 Nov 2011
		US 2013037412 A1	14 Feb 2013
End of Annex			