

[54] VARIABLE INTERVAL TIMER CIRCUIT
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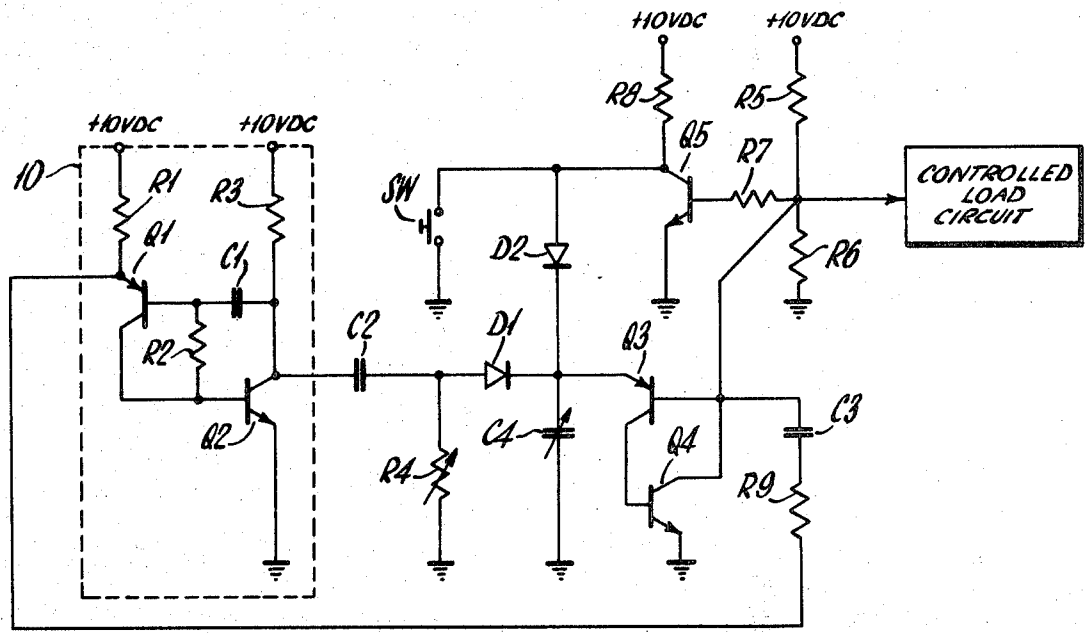
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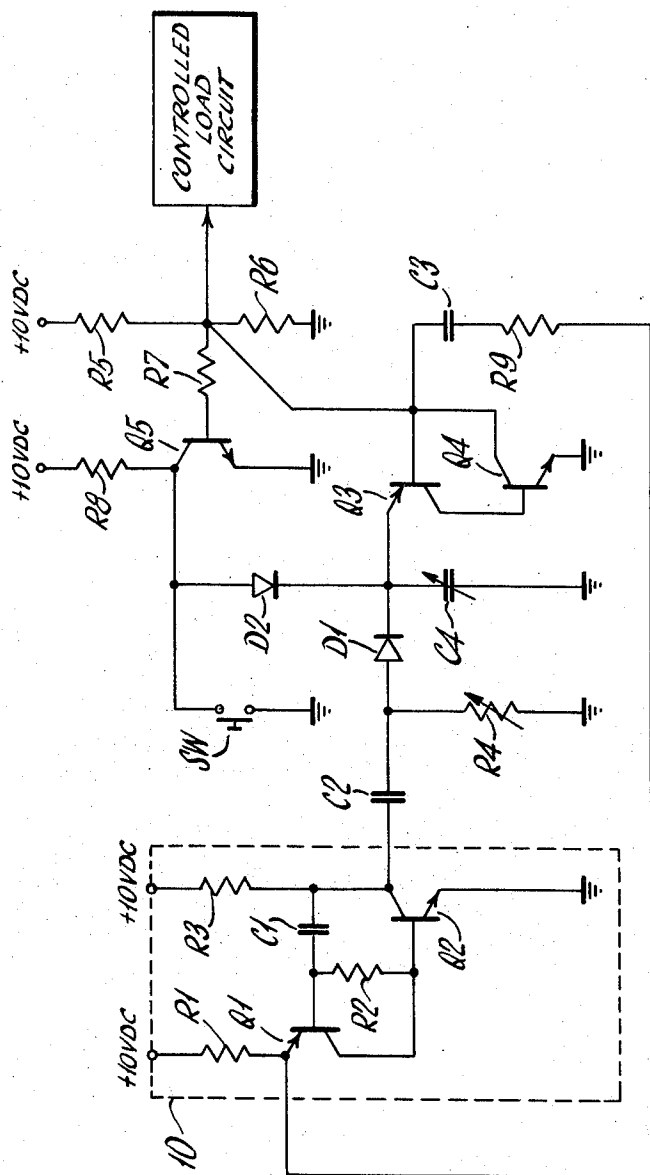
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[57] ABSTRACT

A circuit employing relatively small capacitances to provide an output signal for a predetermined, variable time period measured from the closing of a control switch.

9 Claims, 1 Drawing Figure





VARIABLE INTERVAL TIMER CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION

The present invention advantageously incorporates a pulse generator of the type disclosed and claimed in co-pending U.S. Pat. application Ser. No. 255,155 for ELECTRONIC TIMING CIRCUITS filed on May 19, 1972 in the name of Paul A. Carlson.

BACKGROUND OF THE INVENTION

Numerous prior art circuits have been devised to carry out the function of providing an output signal, which may be utilized for control purposes, for a predetermined, variable time period from the application of an input signal. The input signal may comprise a change in a voltage or current level, or the opening or closing of a switch. Typically, when long time periods on the order of several minutes are desired, such prior art circuits would employ very large capacitors in an RC charging or discharging circuit. Such capacitors are expensive, bulky and usually exhibit a high degree of sensitivity to variations in ambient temperatures. In addition, many prior art circuits employ semiconductor devices which are variably conductive during the timing operation, thereby making the circuit unstable due to variations in leakage currents and other temperature-dependent characteristics.

SUMMARY OF THE INVENTION

The present invention is embodied in and carried out by a circuit which is operative to provide an output signal for a predetermined, variable time period measured from the initiation of application of an input signal. The circuit embodying the present invention employs relatively small, non-electrolytic capacitors, thereby keeping component size and cost low and reliability high. In addition, the semiconductor devices employed in the timing portion of applicant's circuit are normally in a saturated or cut-off condition during the timing operation, so that circuit functioning is not adversely affected by fluctuations in ambient temperature.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be better understood by reading the written description thereof with reference to the accompanying drawing, which is a schematic circuit diagram of the preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawing, the circuit incorporates a pulse generator 10 which is operative to provide substantially rectangular output pulses of brief duration and having a relatively low frequency, e.g., approximately 1 hertz. In the pulse generator which is preferred in the present application, such pulses may be derived, as shown, from both the emitter of transistor Q1 and the collector of transistor Q2. The pulse trains derived at these two points in the pulse generator 10 are in synchronization with one another. This pulse generator is part of the subject matter of the cross-referenced application.

When the circuit shown in the drawing is energized by a +10 volt source as indicated, the pulse generator 10 will continually generate the aforementioned syn-

chronous pulse trains. The transistor switch formed by the complementary transistor pair Q3-Q4 connected in the regenerative feedback configuration is maintained conductive by sustaining current passing through resistance R8, diode D2 and the switch Q3-Q4. Transistor Q5 is normally non-conductive, since the bias voltage provided by voltage divider R5 and R6 is too low because R6 is connected in parallel with the conductive transistor switch Q3-Q4. This same shunt path diverts the pulses fed to timing capacitance C4 through diode D1, leaving C4 uncharged.

The timing function is initiated by momentarily closing the normally open switch SW. This has the effect of diverting sustaining current from transistor switch Q3-Q4, causing that switch to become non-conductive. Simultaneously, the voltage at the junction of R5 and R6 rises to a value which energizes the controlled load circuit and biases transistor Q5 conductive through resistance R7. Thus, when switch SW is re-opened, the capacitance C4 cannot be charged through diode D2 since the current which would normally follow that path is diverted by the now-conductive transistor Q5.

Consequently, charging of C4 is initiated. The pulses derived at the collector of transistor Q2 are differentiated by C2 and R4, at the junction of which appear pulses in the form of spikes, having alternately positive and negative polarities. Only the positive pulses thus developed will pass through diode D1 to charge C4. Thus, the combination of C2, R4 and D1 operates as a frequency divider by halving the number of pulses which are produced by pulse generator 10, and reduces the amount of charge placed on C4 by each of those pulses.

The voltage on C4 will subsequently rise at a relatively slow rate. Because the transistor switch Q3-Q4 responds more predictably to sudden changes in voltage rather than a slow-rising voltage, it has been found to be advantageous to feed the synchronous pulse train derived at the emitter of transistor Q1 through series-connected resistance R9 and capacitance C3 to the base of transistor Q3. Thus, after each increment of charge has been added to capacitance C4 by the pulses passing through diode D1, thereby raising the voltage at the emitter of transistor Q3, this increase is immediately followed by a sharp decrease in the voltage at the base of Q3, thereby facilitating turn-on of the transistor switch Q3-Q4 when C4 has become sufficiently charged.

Once the transistor switch Q3-Q4 has again been rendered conductive after the passage of the time period determined by the charging of capacitance C4, the voltage at the junction of resistance R5 and R6 again goes low since R6 is again shunted by the conductor transistor switch, thereby de-energizing the controlled load circuit. The charge on memory capacitance C4 now discharges through the transistor switch Q3-Q4, which is again provided with sustaining current through resistance R8 and diode D2 due to transistor Q5 again being rendered non-conductive as a result of the decrease in bias voltage at its base. Because the circuit returns to its normal condition virtually instantaneously, it may be restarted at the end of each cycle without hesitation.

In the disclosed circuit forming the preferred embodiment of the present invention, the values of the various components are as follows:

Resistances

R1 — 10K
 R2 — 22 meg
 R3 — 1K
 R4 — 330K
 R5 — 5.1K
 R6 — 3.3K
 R7 — 5.1K
 R8 — 10K
 R9 — 10K

Capacitances

C1 — 0.22 μ f
 C2 — 0.0033 μ f
 C3 — 0.1 μ f
 C4 — 0.33 μ f

Transistors

Q1 — 2N5139
 Q2 — 2N5132
 Q3 — 2N5139
 Q4 — 2N5132
 Q5 — 2N5132

Diodes

D1 — 1N914
 D2 — 1N914

The controlled load circuit connected to the junction of resistances R5 and R6 may consist of a variety of circuits, including variations of the pulse generator 10 which is capable of operating as a flasher in automotive lighting circuits. The duration of the time period may be controlled in a number of ways, such as by varying resistance R4 or capacitance C4, or by varying the frequency of the pulse generator 10, or the width of its output pulses, or by eliminating the frequency divider circuit. Alternate methods of initiating the timing operation may be employed. For example, switch SW could be normally closed and connected in series with diode D2, or in either connection it could be replaced by a transistor which is controlled by an associated circuit. The circuit embodying the present invention may find numerous applications. For example, it could be employed to actuate a warning signal for a predetermined period of time if a driver leaves his automobile with the keys in the ignition.

The advantages of the present invention, as well as certain changes and modifications of the disclosed embodiment thereof, will be readily apparent to those skilled in the art. It is the applicant's intention to cover all those changes and modifications which could be made to the embodiment of the invention herein chosen for the purposes of the disclosure without departing from the spirit and scope of the invention.

What is claimed is:

1. A variable-interval timer circuit comprising:

1. pulse-generating means operative to produce, in synchronization, first and second trains of low-frequency pulses;
2. timing means comprising:
 - a. a timing capacitance connected to said pulse generating means to receive and store said first train of low-frequency pulses; and
 - b. switching means normally operative to shunt said first train of low-frequency pulses from said timing capacitance, and to receive said second

train of low-frequency pulses to facilitate turn-on of said switching means;

3. control means coupled to said timing means and operative normally to prevent said timing capacitance from storing said first train of low-frequency pulses; and
4. starting means coupled to said control means and operative upon actuation to enable said timing capacitance to store said first train of low-frequency pulses and, cooperatively with said control means, to produce an output signal for a predetermined period of time after actuation of said starting means.
2. A variable-interval timer circuit according to claim 1 wherein said switching means is biased by both the voltage on said timing capacitance and said second train of low-frequency pulses produced by said pulse-generating means.
3. A variable-interval timer circuit according to claim 2 wherein said switching means is connected to receive said second train of low-frequency pulses from said pulse-generating means through a coupling circuit.
4. A variable-interval timer circuit according to claim 3 wherein said coupling circuit comprises a resistance and a capacitance connected in series between said pulse-generating means and said switching means.
5. A variable-interval timer circuit according to claim 1 wherein said switching means is maintained normally conductive by sustaining current provided by said control means.
6. A variable-interval timer circuit according to claim 5 wherein said control means comprises:
 1. transistor means normally operative to provide said sustaining current to said switching means via a diode, said starting means being operative, when actuated, to prevent flow of said sustaining current to said switching means; and
 2. bias circuit means connected to the input terminal of said transistor means, and normally partially shunted by said switching means.
7. A variable-interval timer circuit according to claim 6 wherein said starting means comprises a normally open switch connected across the output terminals of said transistor means.
8. A variable-interval timer circuit according to claim 6 wherein said bias circuit means comprises a voltage divider formed by a pair of resistances connected in series, and a resistance connected between the junction of said voltage divider resistances and the input terminal of said transistor means.
9. A variable-interval timer circuit according to claim 8 wherein one voltage divider resistance is connected in parallel with said switching means.

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