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(54) Title: METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (MOSFET) AND METHOD FOR FABRICATING THE SAME

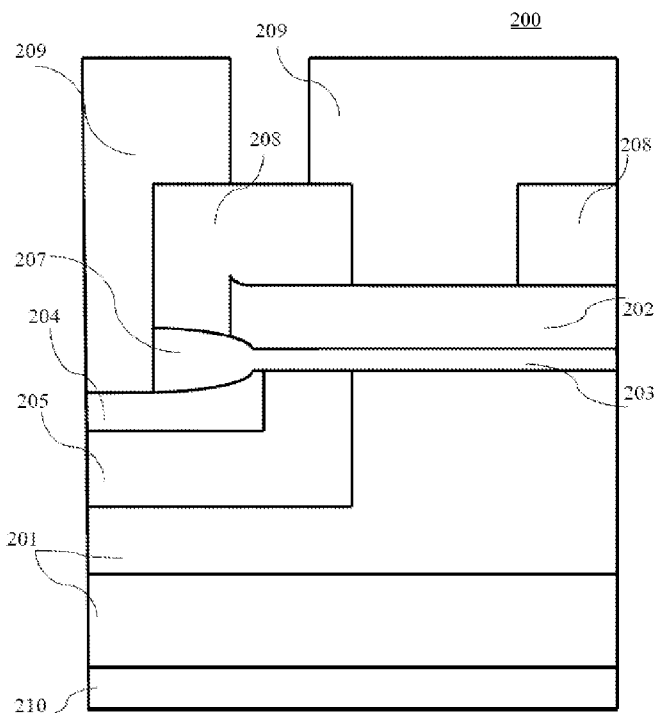


FIG. 3

(57) Abstract: A method is provided for fabricating a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET, 200) on a semiconductor wafer. The method includes providing a substrate containing an epitaxial layer (201), forming a gate oxide layer (203) on a surface of the epitaxial layer (201) by a first oxidization process, forming a polysilicon gate (202) on the gate oxide layer (203) within a gate region, forming a body region (205) in the epitaxial layer (201), forming a source region (204) in the body region (205) of the epitaxial layer (201), and oxidizing the source region (204) to form oxide (207) in a gap between the polysilicon gate (202) and the source region (204) on a surface of the source region (204) by a second oxidization process.



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**METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (MOSFET)
AND METHOD FOR FABRICATING THE SAME**

5 CROSS REFERENCE TO RELATED ART

[0001] This application claims the priority of Chinese patent application no. 201010564084.3, filed on November 29, 2010, the entire contents of which are incorporated herein by reference.

10

FIELD OF THE INVENTION

[0002] The present invention generally relates to the field of semiconductor manufacturing, and more particularly, to the Metal-Oxide-Semiconductor Field-Effect
15 Transistor (MOSFET) technologies.

BACKGROUND OF THE INVENTION

[0003] With the fast development of semiconductor manufacturing technologies and the
20 demands for faster computing speed, larger data storage, and more functions of semiconductor devices, semiconductor wafer is developed to have higher component density and higher integration degrees. This further creates higher and higher requirements for the physical structures and manufacture processes of the semiconductor wafer.

25 [0004] For example, to make a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), the conventional manufacturing process generally includes the followings: forming a gate oxide layer on the surface of an epitaxial layer of a semiconductor wafer

and a subsequent polysilicon layer on the gate oxide layer; forming a gate region pattern on the surface of the polysilicon layer by sequentially performing: coating a photoresist on the polysilicon layer, marking a gate region pattern in the photoresist, etching a polysilicon gate and removing the photoresist and so on; forming a body region by means of ion
5 implantation and impurity driving-in; forming a source region in the body region; growing a dielectric layer; forming a contact hole leading to the gate region and the source region in the dielectric layer; and interconnecting metal wires to complete metallization.

[0005] However, the higher and higher requirements for the physical structures and manufacturing processes of the MOSFET make the above conventional manufacturing
10 process less ideal. The disclosed methods and systems are directed to solve one or more problems set forth above and other problems.

SUMMARY OF THE INVENTION

[0006] One aspect of the present disclosure includes a method for fabricating a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) on a semiconductor wafer. The method includes providing a substrate containing an epitaxial layer, forming a gate oxide layer on a surface of the epitaxial layer by a first oxidization process, and forming a polysilicon gate on the gate oxide layer within a gate region. The method also includes
15 forming a body region in the epitaxial layer, forming a source region in the body region of the epitaxial layer, and oxidizing the source region to form oxide in a gap between the polysilicon gate and the source region on a surface of the source region by a second oxidization process.
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[0007] Another aspect of the present disclosure includes a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The MOSFET includes a substrate containing an epitaxial layer, a gate oxide layer formed on a surface of the epitaxial layer by a first oxidization process, and a polysilicon gate formed on the gate oxide layer within a gate region. The MOSFET also includes a body region formed in the epitaxial layer and a source region formed in the body region of the epitaxial layer. Further, the source region
25

is oxidized to form oxide in a gap between the polysilicon gate and the source region on a surface of the source region by a second oxidization process.

[0008] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

5

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 shows a partial structural schematic diagram of a MOSFET by a conventional manufacturing process;

10 [0010] Figure 2 illustrates an exemplary MOSFET by a manufacturing process consistent with the disclosed embodiments; and

[0011] Figure 3 illustrates an exemplary MOSFET by a manufacturing process consistent with the disclosed embodiments.

15 DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0012] Reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

20 [0013] Figure 1 shows a partial structural schematic diagram of a conventional MOSFET 100 fabricated by a conventional manufacturing process. As shown in Figure 1, the conventional MOSFET 100 includes an epitaxial layer 101, a polysilicon gate 102, a gate oxide layer 103, a source region 104, and a body region 105.

25 [0014] Due to corrosion of gate oxide layer 103, a gap 106 may be present between the polysilicon gate 102 and the source region 104 at the edge of the gate region, where ideally the gate oxide layer 103 should be present instead. In a subsequent vapor deposition process, the gap 106 acts as a dielectric film and is filled with dielectric oxide generated in

the vapor deposition process. Because the conductivity of the dielectric oxide filled in the gap 106 in the vapor deposition process is much worse than that of the gate oxide generated by thermal oxidation in the gate oxide layer 103, the gate oxide layer 103 at the edge of the gate region may be prone to gate oxide breakdown, leading to malfunction of the MOSFET 100.

[0015] Figure 2 illustrates a MOSFET 200 fabricated by a manufacturing process consistent with the disclosed embodiments. To make MOSFET 200, a substrate (not shown) is first provided on a semiconductor wafer. The substrate may include any appropriate material for making double-gate structures. For example, the substrate may include a semiconductor structure, e.g., silicon, silicon germanium (SiGe) with a monocrystalline, polycrystalline, or amorphous structure. The substrate may also include a hybrid semiconductor structure, e.g., carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide or gallium antimonide, alloy semiconductor, or a combination thereof. Further, the substrate may include a silicon-on-insulator (SOI) structure. In addition, the substrate may also include other materials, such as a multi-layered structure of epitaxial layer or buried layer. Other materials may also be used.

[0016] The substrate includes an epitaxial layer 201 in any appropriate structure. For example, the epitaxial layer 201 may be an N^-N^+ structure formed on the substrate in the semiconductor wafer. The thickness of the epitaxial layer 201 may be determined according to the specific application of the device (i.e., MOSFET 200); and the epitaxial layer 201 may be formed on the front surface or the back surface of the substrate.

[0017] After the substrate is provided and prepared, a gate oxide layer and a polysilicon gate are formed on a surface of the epitaxial layer 201. Figure 2 shows a gate oxide layer 203 formed on the epitaxial layer 201 and a polysilicon gate 202 formed on the gate oxide layer 203. The gate oxide layer 203 may be formed by certain processes. For example, the gate oxide layer 203 may be formed on the surface of the epitaxial layer 201 by a thermal oxidation process. The formed gate oxide layer 203 may include at least silicon oxide and may have a thickness of approximately 20-50 Angstrom.

[0018] After forming the gate oxide layer 203, a polysilicon layer (e.g., the polysilicon gate 202) may be formed by certain processes, such as placing the substrate with the gate oxide layer 203 into a low pressure chemical vapor deposition (CVD) equipment, inletting silane into a process chamber of the CVD equipment; and depositing a polysilicon layer in a thickness of approximately 5000 Angstrom on the surface of the gate oxide layer 203 after the decomposition of the silane. The polysilicon may also be doped after the deposition of the polysilicon.

[0019] Further, a photoresist layer may be formed on the polysilicon layer and a pattern of a gate region may be formed in the photoresist layer by exposure and development. The gate region (e.g., the polysilicon gate 202) is then formed by etching a portion of the gate oxide layer and a portion of the polysilicon layer outside the pattern of the gate region using the photoresist layer as a mask. For example, the polysilicon gate 202 may be formed by an isotropic plasma etching process or a wet chemical corrosion process.

[0020] A body region 205 may be formed in the epitaxial layer 201 by ion implantation or other appropriate processes. More particularly, the body region 205 may be formed on a side of the polysilicon gate 202 by ion implantation and impurity driving-in. For example, the body region 205 may be formed on each of two sides of the polysilicon gate by ion implantation and impurity driving-in using the polysilicon gate as a mask.

[0021] After forming the body region 205, a source region 204 may be formed in the body region 205. For example, the source region 204 may be formed by implanting impurity into the body region 205. In certain embodiments, the epitaxial layer 201 may be in an N^-N^+ doped structure, the source region 204 may be N^+ -doped, and the body region 205 may be P^- -doped. The P^- doped body region 205 may be formed using the pattern of the gate region as a mask to implant boron ions and drive-in impurity. Other configurations may also be used.

[0022] Further, after the source region 204 is formed (or after the polysilicon gate 202 is formed), the semiconductor wafer is annealed. A nitrogen annealing process may be employed for annealing the semiconductor wafer in an annealing furnace by inletting nitrogen into the annealing furnace. The specific parameters for the annealing may be

configured as: the temperature being about 800-900°C and the duration of the annealing being about 14-16 minutes. A preferred approach is to anneal at a temperature of about 850°C for a duration of about 15 minutes.

5 [0023] As previously explained, a gap may appear between the source region 204 and the polysilicon gate 202 along the edge of the gate oxide layer 203. To eliminate the potential impact of the gap, the source region 204 is oxidized to form oxide 207 in the gap between the polysilicon gate 202 and the source region 204 on the surface of the source region 204.

10 [0024] As previously described, the gate oxide layer 203 is formed by a thermal oxide growth process. Thus, in order to ensure or maintain approximate electric properties between the oxide 207 formed on the source region 204 and the gate oxide layer 203, the thermal oxide growth process (i.e., the same type of oxidization process forming the gate oxide layer 203) is also used to oxidize the source region 204. More specifically, hydrogen and oxygen may be inlet into an oxidation chamber for about 14-16 minutes, preferably about 15 minutes. In certain embodiments, the oxide 207 formed on the surface of the source region may be 1-3 times as thick as the gate oxide layer 203, and the thickness of the oxide 207 may also be controlled by controlling the doping concentration of the source region 204.

20 [0025] That is, as shown in Figure 2, the gap between the edge of the polysilicon gate 202 and the source region 204 is filled with the oxide 207 formed on the surface of the source region 204, and the thickness of the gate oxide layer 203 at the edge of the gate region is increased, so that the possibility of the breakdown of the gate oxide layer 203 at the edge of the gate region is reduced, and the service life of the MOSFET 200 may be extended.

25 [0026] Additionally or optionally, before forming the gate oxide layer 203 and the polysilicon layer 202, a conduction protective region for device protection and isolation may be formed in the substrate or the semiconductor wafer. To form the conduction protective region, an oxide protective layer may be first formed on the surface of the epitaxial layer 201 of the semiconductor wafer substrate. A pattern of the conduction

protective region may then be formed in the oxide protective layer by photolithography. Further, a well region (i.e., the conduction protective region) is formed by performing ion implantation and impurity driving-in in the epitaxial layer 201 using the conduction protective layer (the conduction protective region pattern) as a mask. Afterwards, the oxide protective layer is removed.

[0027] The oxide protective layer may be obtained through oxidation reaction of silicon by inletting oxygen into a high-temperature process chamber to let the oxygen react with silicon. The oxide protective layer mainly acts as an oxide-shielding layer to control the scope and depth for implanting the impurity during the ion implantation, to prevent the surface of the epitaxial layer 201 from being contaminated, and to prevent the semiconductor wafer or substrate from excessive damage during the ion implantation.

[0028] Further, after removing the oxide protective layer and before forming the gate oxide layer and the polysilicon layer, a plurality of active regions may be defined in the substrate to form a plurality of semiconductor devices. To define the plurality of active regions, the surface of the epitaxial layer 201 of the substrate may be first oxidized to form an oxide layer on the surface of the epitaxial layer 201. A pattern of the active regions may then be formed in the oxide layer on the surface of the epitaxial layer 201 by photolithography, and the plurality of active regions may be formed using the pattern of the active regions as a mask. Afterwards, the oxide layer is removed by corrosion. Other steps may also be included.

[0029] Further, after forming the source region 204 and the oxide 207, other structures may also be formed to complete fabricating the MOSFET 200. Figure 3 illustrates an exemplary MOSFET 200 after additional structures are fabricated consistent with the disclosed embodiments.

[0030] More specifically, as shown in Figure 3, a dielectric layer 208 may be first formed on the surface of the epitaxial layer 201 of the semiconductor wafer substrate. Further, contact holes 209 may be formed in the dielectric layer 208 and the contact holes 209 may respectively lead to the gate region 202 and the source region 204. The contact holes are then metalized (e.g., filled with metal material) to obtain a gate (or gate electrode)

and a source (or source electrode) of the MOSFET 200. A drain (or drain electrode) 210 is also formed on the back surface of the semiconductor wafer substrate to form the MOSFET 200. Other structures may also be included.

5 [0031] By using the disclosed methods and devices/systems, the gap between the edge of the polysilicon gate and the source region is filled with the oxide formed on the surface of the source region. The thickness of the gate oxide layer at the edge of the gate region is increased, so that the possibility of the breakdown of the gate oxide layer at the edge of the gate region is reduced and the service life of the formed MOSFET is extended.

10 [0032] It is understood that the disclosed embodiments may be applied to any appropriate semiconductor device manufacturing processes and can also be extended to the manufacturing of multi-gate structures or multi-device chips. Various alternations, modifications, or equivalents to the technical solutions of the disclosed embodiments can be obvious to those skilled in the art.

CLAIMS:

1. A method for fabricating a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) on a semiconductor wafer, comprising:

- 5 providing a substrate containing an epitaxial layer;
- forming a gate oxide layer on a surface of the epitaxial layer by a first oxidization process;
- forming a polysilicon gate on the gate oxide layer within a gate region;
- forming a body region in the epitaxial layer;
- 10 forming a source region in the body region of the epitaxial layer; and
- oxidizing the source region to form oxide in a gap between the polysilicon gate and the source region on a surface of the source region by a second oxidization process.

2. The method according to claim1, wherein, after forming the source region and
- 15 before oxidizing the source region, the method further includes:
- annealing the semiconductor wafer.

3. The method according to claim 2, wherein the annealing includes:
- annealing the semiconductor wafer at an annealing temperature of about
- 20 800°C-900°C for an annealing duration of about 14-16 minutes.

4. The method according to claim1, wherein:
- the first oxidization process and the second oxidization process are of a same type to maintain approximate electric properties between the formed oxide on the source region
- 25 and the gate oxide layer.

5. The method according to claim 4, wherein:

the formed oxide on the surface of the source region is 1-3 times as thick as the gate oxide layer such that a thickness of the gate oxide layer at an edge of the gate region is increased.

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6. The method according to claim 4, wherein:

the second oxidization process is a thermal oxide growth process with a duration of 14-16 minutes.

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7. The method according to claim 1, wherein:

the body region is formed on each of two sides of the polysilicon gate by ion implantation and impurity driving-in before forming the source region.

8. The method according to claim 1, before forming the gate oxide layer and the polysilicon gate, further including:

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forming an oxide protective layer on the surface of the epitaxial layer of the semiconductor wafer;

forming a pattern of a conduction protective region in the oxide protective layer by photolithography;

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forming a well region as the conduction protective region by performing ion implantation and impurity driving-in using the pattern of the conduction protective region as a mask; and

removing the oxide protective layer.

25

9. The method according to claim 8, further including:

oxidizing the surface of the epitaxial layer to form an oxide layer;

forming a pattern of a plurality of active regions in the oxide layer on the surface of the epitaxial layer by photolithography;

forming the plurality of active regions for forming a plurality of semiconductor devices using the pattern of the plurality of active regions as a mask; and

5 removing the oxide layer by corrosion.

10. The method according to claim 1, further including:

forming a dielectric layer on the surface of the epitaxial layer;

forming contact holes in the dielectric layer respectively leading to the gate region
10 and the source region;

metalizing the contact holes to obtain a gate and a source; and

forming a drain on a back surface of the semiconductor wafer.

11. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET),
15 comprising:

a substrate containing an epitaxial layer;

a gate oxide layer formed on a surface of the epitaxial layer by a first oxidization process;

a polysilicon gate formed on the gate oxide layer within a gate region;

20 a body region formed in the epitaxial layer; and

a source region formed in the body region of the epitaxial layer,

wherein the source region is oxidized to form oxide in a gap between the polysilicon gate and the source region on a surface of the source region by a second oxidization process.

25

12. The MOSFET according to claim 11, wherein:

the first oxidization process and the second oxidization process are of a same type to maintain approximate electric properties between the formed oxide on the source region and the gate oxide layer.

5

13. The MOSFET according to claim 12, wherein:

the formed oxide on the surface of the source region is 1-3 times as thick as the gate oxide layer such that a thickness of the gate oxide layer at an edge of the gate region is increased.

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14. The MOSFET according to claim 12, wherein:

the second oxidization process is a thermal oxide growth process with a duration of 14-16 minutes.

15

15. The MOSFET according to claim 11, wherein:

the body region is formed on each of two sides of the polysilicon gate by ion implantation and impurity driving-in before forming the source region.

20

16. The MOSFET according to claim 11, further including:

a dielectric layer formed on the surface of the epitaxial layer;

contact holes formed in the dielectric layer respectively leading to the gate region and the source region;

a gate and a source obtained by metalizing the contact holes; and

a drain formed on a back surface of the semiconductor wafer.

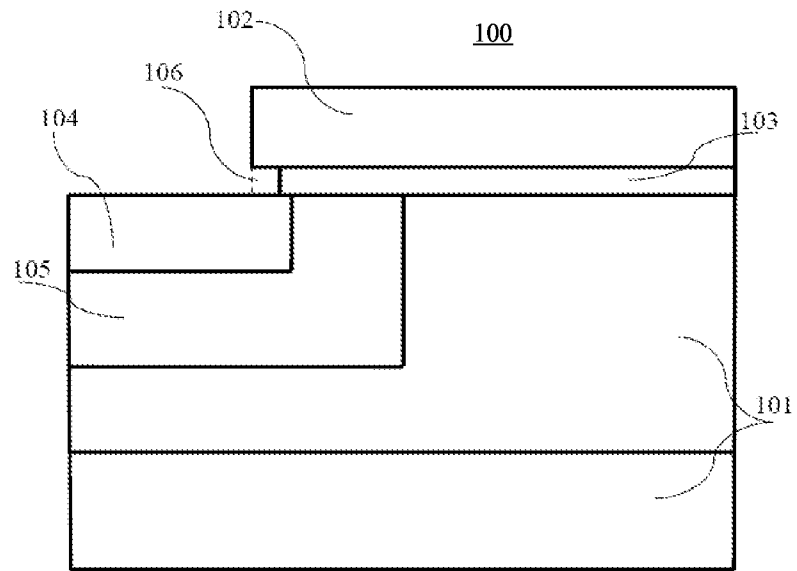


FIG. 1 (Prior Art)

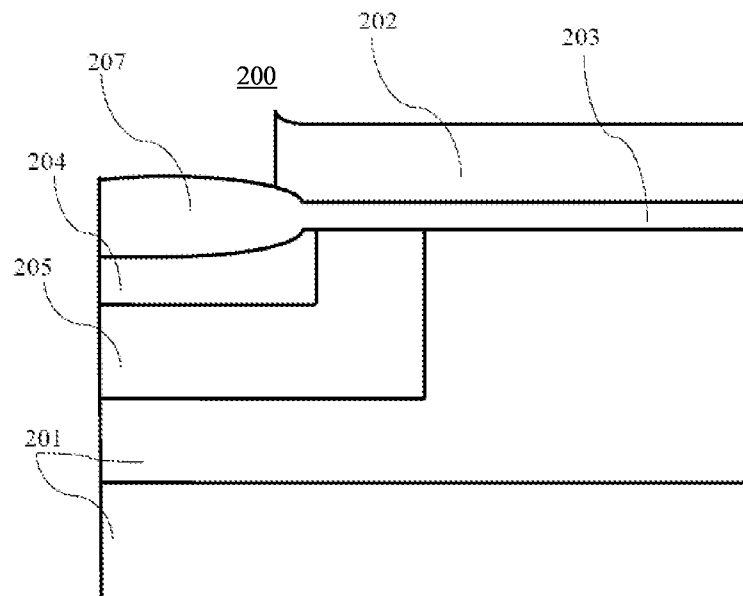


FIG. 2

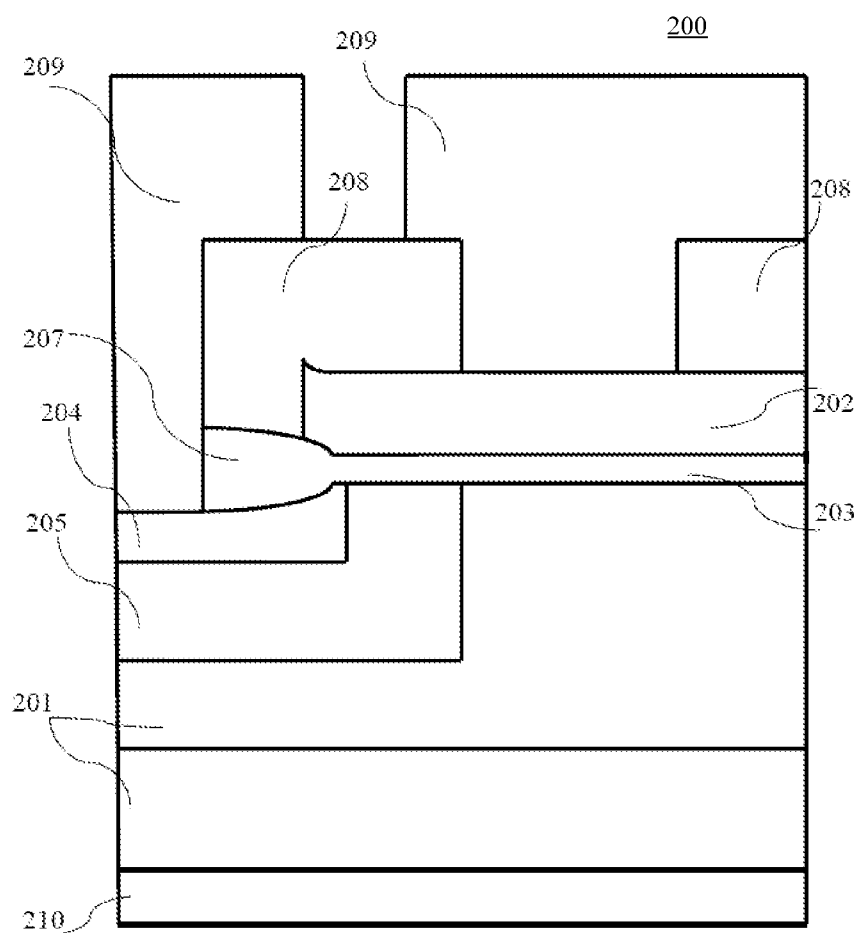


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/083107

A. CLASSIFICATION OF SUBJECT MATTER

See the extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: VDMOS, MOSFET, gate, oxide, thickness, source, epitaxial, dielectric, insulate, breakdown, short circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2009072306A1, (ROHM CO LTD), 19 March 2009(19.03.2009), paragraphs [0148]-[0175] of the description; figures 5,6	1-16
A	WO2010119789A1, (ROHM CO LTD), 21 October 2010(21.10.2010), the whole document	1-16
A	JP2009070849A, (ROHM CO LTD), 02 April 2009(02.04.2009), the whole document	1-16

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&”document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 20 February 2012(20.02.2012)	Date of mailing of the international search report 08 Mar. 2012 (08.03.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer XU, Ying Telephone No. (86-10)62412106

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Form PCT/ISA /210 (patent family annex) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.

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Continuation of classification of subject matter:

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H01L29/78(2006.01)i

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