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(54) **Method of encapsulating a semiconductor device.**

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Description

This invention relates to a method of manufacturing a semiconductor device.

There are a number of known manners of manufacturing a semiconductor device, in which a semiconductor chip is sealed in a resin package. Figure 4 of the accompanying drawings shows a known "die pad" construction in which a chip c is bonded to a die-pad a by a bonding material d, such as a silver paste or a gold-silicon eutectic alloy. The die-pad a is connected to a peripheral portion of a lead frame by connecting fingers a'. A plurality of lead fingers b project from the peripheral portion of the lead frame, and each lead finger b is connected to a respective electrode of the chip c by a respective bonding wire e. The chip c, die-pad a, bonding wires e and inner ends of the fingers a', b are then placed in a moulding die and sealed in a resin package.

Another known "chip-on-lead" type of construction is shown in Figure 5. In this case, an insulator f, such as a polyimide sheet, is placed on the inner ends of lead fingers b, a semiconductor chip c is placed on the insulator f and the electrodes of the semiconductor chip c are connected to respective inner ends of the lead fingers b by respective bonding wires e. Again, the assembly is then sealed in a resin package.

A further known "lead-on-chip" type of construction is shown in Figure 6. In this case, a surface of a semiconductor chip c, excluding the electrodes thereon, is covered with an insulator f, lead fingers b are placed on the insulator f, and the lead fingers b are connected to respective electrodes by respective bonding wires e. Once again, the assembly is then sealed in a resin package.

Lastly, Figure 7 shows a known "directly connected" form of construction, in which electrode pads g of a semiconductor chip c project upwardly from the upper surface of the chip c, and the inner ends of lead fingers b are directly connected to the electrode pads g. The assembly is then sealed in a resin package.

It is desirable that the height of the semiconductor device is as small as possible. However, in the die pad construction described above, the thickness of the die pad a and bonding material d add to the height of the package. In the chip-on-lead and lead-on-chip forms of construction described above, the thickness of the insulators f and the lead fingers b add to the height of the package. In the directly connected form of construction described above, the thickness of the lead fingers b and the height of the electrode pads g add to the overall height of the semiconductor package. Also, the die pad construction suffers from the problem that thermal stress is induced in the device due to differences in the coefficients of thermal expansion of the die pad a, the semiconductor chip c and the resin of the package, which can cause a breakdown in bonding between the chip c and the die pad a, between the die pad a and the resin package, or between the chip c and the resin package.

The problems with which the present invention are concerned are: to enable a semiconductor device to be produced which has a decreased height; to alleviate thermal stresses in the semiconductor package; and/or to enable the semiconductor device to be produced reliably, such that there is a small risk of the bonding wires being broken or short circuited while the resin package is being formed around the assembly of the chip, bonding wires and lead fingers.

The Patent Abstracts of Japan abstract of Patent Application JP-A-60-037754 and Patent Application EP-A-0 366 386 each show a chip package with no die pad, and with bonding wires extending between the lead fingers and electrode pads, but do not address the problem of the bonding wires being broken or short-circuited while the plastics package is being formed.

The Patent Abstracts of Japan abstract of Patent Application JP-A-01-262115 shows a lead on chip construction and a mould which has sliding pins which engage the leads on top of the chip and the underside of the chip during plastics injection to hold the chip.

In accordance with the present invention, there is provided a method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip, the semiconductor chip having an upper surface and a lower surface and having a plurality of electrodes formed on said upper surface;

providing a lead frame having no die pad, the lead frame comprising a peripheral portion surrounding a region for receiving the chip and a plurality of lead finger portions and movement restricting finger portions projecting from the peripheral portion towards said region and terminating outside said region;

placing the chip in said region such that said lead finger portions and said movement restricting finger portions do not contact said chip;

connecting each of the electrodes to a respective one of the lead finger portions with a respective bonding wire;

providing a mould having a mould cavity and at least one projection projecting into said cavity;

placing said chip in said mould cavity such that said projection projects towards but does not contact said upper or lower surfaces of said chip;

injecting resin into said mould cavity, thereby sealing the chip and bonding wires in a resin package such that the lead finger portions project out of the package and such that the resin package directly contacts both the upper surface and the lower surface of the chip; and

severing each of the lead finger portions from

the peripheral portion of the frame.

There follows a description of a preferred embodiment and example of the present invention with reference to the accompanying drawings, in which:

Fig. 1 is a partial perspective view of a lead frame to which are connected a pair of semiconductor chips;

Fig. 2 is a sectional view of a moulding die loaded with a lead frame and a semiconductor chip;

Fig. 3 is a sectional view of a resin package as formed by the moulding die of Fig. 2;

Fig. 4 is a sectional view of a known die pad form of assembly of a lead frame and semiconductor chip;

Fig. 5 is a perspective view of a known chip-on-lead form of assembly of semiconductor chip and lead frame;

Fig. 6 is a perspective view of a known lead-on-chip form of assembly of a semiconductor chip and lead frame; and

Fig. 7 is a sectional view of a known direct connection form of assembly of a semiconductor chip and lead frame.

Referring to Figures 1 to 3, a lead frame 1 for manufacturing a plurality of semiconductor devices has apertures 2 for receiving semiconductor chips 7 in a longitudinal arrangement at regular intervals. The apertures 2 are provided instead of the die pads in the known die pad form of construction. Each aperture 2 is of a size such that the respective chip 7 could be passed through the aperture.

The lead frame 1 has peripheral frame members 5 surrounding each aperture 2, tie bars 4 connecting portions of the lead frame for each chip, lead fingers 3 projecting towards each aperture 2 and horizontal movement restricting fingers 6 projecting inwardly from the side portions of the frame members 5 towards the apertures 2.

Each semiconductor chip 7 is placed in the respective aperture 2. The size of the aperture 2 (defined by inner ends of the lead fingers 3 and movement restricting fingers 6) is such that the lead fingers 3 and the movement restricting fingers 6 do not contact the chip 7.

Each chip 7 has a plurality of electrodes 9, and each electrode is connected to the inner end of a respective one of the lead fingers 3 by a respective bonding wire 8. Thus, each semiconductor chip 7 is connected to the lead frame 1 solely by the bonding wires 8.

Then, the lead frame 1, with the chips 7 connected thereto, is placed in a moulding die, as shown in Figure 2. The moulding die comprises a lower die part 10 and a complementary upper die part 11, and the lead fingers and movement restricting fingers pass through channels 14 between the die parts 10,11. Both die parts 10,11 are provided with vertical movement restricting pins 12, which project towards the chip 7, but which are slightly separated from the upper and lower surfaces of the chip 7. After the chip 7 has been placed in the moulding die, supported solely by the lead frame 1 and the bonding wires 8, resin is injected into the mould cavity of the moulding die to seal the semiconductor chip, the bonding wires 8, and the inner ends of the lead fingers 3 within a resin package 13 as shown in Figure 3.

Although the resin has a sufficiently low viscosity in the initial stage of injection of resin into the mould cavity, the resin tends to urge the chip 7 vertically either towards the lower die part 10 or the upper die part 11, due to slight differences in resistance against the flow of the resin between the upper and lower surfaces of the semiconductor chip 7. However, vertical movement of the chip 7 is restricted by the vertical movement restricting projections 12, so that the chip 7 cannot significantly move towards the lower die part 10 or upper die part 11. As injection progresses, the resin becomes distributed uniformly within the mould cavity, and the resin tends to fill the gaps between the tips of the vertical movement restricting projections 12 and the upper and lower surfaces of the chip 7. Once injection of the resin has been completed, the chip 7 tends to return to its original position within the moulding die, and therefore partial exposure of the chip 7 at the locations of the movement restricting projections 12 is unlikely to occur. The viscosity of the resin being injected may also tend to urge the chip sideways in the mould cavity. However, sideways movement of the chip is restricted not only by the bonding wires 8, but also by the horizontal movement restricting fingers 6. Even if the tip of one or more of the horizontal movement restricting fingers 6 possibly remains in contact with a side surface of the chip 7 after the resin has hardened, no problem arises because the portions of the horizontal movement restricting projections which project outside the resin package 13 are subsequently cut off.

After the resin has hardened, the lower and upper die parts 10,11 are separated, and the lead frame with the packages moulded thereon are removed. Then, the horizontal movement restricting portions 6 are cut off flush with the side of each package 13, and the lead fingers 3 are severed each at a location spaced from the resin package so as to form individual connecting leads for the chips.

Claims

1. A method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip (7), the semiconductor chip having an upper surface and a lower surface and having a plurality of electrodes (9) formed on said upper surface;

providing a lead frame (1) having no die

pad, the lead frame comprising a peripheral portion (5) surrounding a region for receiving the chip and a plurality of lead finger portions (3) and movement restricting finger portions (6) projecting from the peripheral portion towards said region and terminating outside said region;

placing the chip in said region such that said lead finger portions (3) and said movement restricting finger portions (6) do not contact said chip (7);

connecting each of the electrodes to a respective one of the lead finger portions with a respective bonding wire (8);

providing a mould (10, 11) having a mould cavity and at least one projection (12) projecting into said cavity;

placing said chip in said mould cavity such that said projection (12) projects towards but does not contact said upper or lower surfaces of said chip;

injecting resin into said mould cavity, thereby sealing the chip and bonding wires in a resin package (13) such that the lead finger portions project out of the package and such that the resin package directly contacts both the upper surface and the lower surface of the chip; and

severing each of the lead finger portions from the peripheral portion of the frame.

2. A method as claimed in claim 1, wherein immediately prior to said injecting step the chip is mechanically connected to the peripheral portion solely by the bonding wires and the lead finger portions.

3. A method as claimed in claim 1 or 2, wherein the mould has a plurality of such projections (12) which project towards but do not contact said upper and lower surfaces of the chip when the chip is placed in the mould cavity.

Patentansprüche

1. Verfahren zur Herstellung einer Halbleitereinrichtung, das folgende Schritte aufweist:

Bereitstellen eines Halbleiterchips (7), wobei der Halbleiterchip eine obere Oberfläche und eine untere Oberfläche hat und eine Vielzahl von Elektroden (9), die auf der oberen Oberfläche gebildet sind;

Bereitstellen eines Systemträgers (1), der keinen Kontaktfleck hat, wobei der Systemträger einen peripheren Bereich (5) aufweist, der einen Bereich zur Aufnahme des Chips und einer Vielzahl von Leiterbahnfingerbereichen (3) und Bewegungsbeschränkungsfingerbereichen (6) umgibt, die sich vom peripheren Bereich in Richtung auf diesen Bereich erstrecken und an der Außenseite dieses Bereichs enden;

Anordnen des Chips in diesem Bereich so, daß die Leiterbahnfingerbereiche (3) und die Bewegungsbeschränkungsfingerbereiche (6) nicht den Chip (7) berühren;

Kontaktieren jeder der Elektroden mit einem entsprechenden der Leiterbahnfingerbereiche mit einem entsprechenden Bonddraht (8);

Bereitstellen einer Form (10, 11) mit einer Formmulde und zumindest einem Ansatz (12), der in die Mulde hineinragt;

Anordnen des Chips in dieser Formmulde, so daß dieser Ansatz (12) sich in Richtung auf den Chip erstreckt, jedoch nicht die obere oder untere Oberfläche des Chips berührt;

Einspritzen von Kunststoff in die Formmulde, wodurch der Chip und die Bonddrähte zu einem Kunststoffgehäuse (13) vergossen werden, so daß die Leiterbahnfingerbereiche aus dem Gehäuse herausragen und das Kunststoffgehäuse unmittelbar sowohl die obere Oberfläche als auch die untere Oberfläche des Chips berührt, und

Abtrennen eines jeden der Leiterbahnfingerbereiche vom peripheren Bereich des Rahmens.

2. Verfahren nach Anspruch 1, wobei unmittelbar vor dem Einspritzungsschritt der Chip mechanisch mit dem peripheren Bereich lediglich durch die Bonddrähte und die Leiterbahnfingerbereiche kontaktiert wird.

3. Verfahren nach Anspruch 1 oder 2, wobei die Form eine Vielzahl von Ansätzen (12) aufweist, die sich in Richtung auf den Chip erstrecken, jedoch nicht die obere und untere Oberfläche des Chips berühren, wenn der Chip in der Formmulde angeordnet wird.

Revendications

1. Procédé de fabrication d'un dispositif à semiconducteur, comportant les étapes consistant à :

prévoir une plaquette semi-conductrice (7), la plaquette semi-conductrice ayant une surface supérieure et une surface inférieure et ayant plusieurs électrodes (9) formées sur ladite surface supérieure;

prévoir un cadre de connexion (1) n'ayant pas de support, le cadre de connexion comportant une partie périphérique (5) qui entoure une zone destinée à recevoir la plaquette et plusieurs parties de patte de connexion (3) et parties de patte de limitation de mouvement (6) qui dépassent de la partie périphérique en direction de la-

dite zone et se terminent à l'extérieur de ladite zone;

placer la plaquette dans ladite zone de telle sorte que lesdites parties de patte de connexion (3) et lesdites parties de patte de limitation de mouvement (6) ne viennent pas en contact avec ladite plaquette (7);

relier chacune des électrodes à une partie respective desdites parties de patte de connexion avec un fil de liaison respectif (8);

prévoir un moule (10, 11) ayant une cavité de moule et au moins une saillie (12) qui dépasse dans ladite cavité;

placer ladite plaquette dans ladite cavité de moule de telle sorte que ladite saillie (12) dépasse vers mais ne vient pas en contact avec lesdites surfaces supérieure ou inférieure de ladite plaquette;

injecter de la résine dans ladite cavité de moule, scellant ainsi la plaquette et les fils de liaison dans un boîtier en résine (13) de telle sorte que les parties de patte de connexion dépassent du boîtier et de telle sorte que le boîtier en résine vient directement en contact avec la surface supérieure et la surface inférieure de la plaquette; et

sectionner chacune des parties de patte de connexion de la partie périphérique du cadre.

2. Procédé selon la revendication 1, dans lequel, immédiatement avant ladite étape d'injection, la plaquette est mécaniquement reliée à la partie périphérique uniquement par les fils de liaison et les parties de patte de connexion.

3. Procédé selon la revendication 1 ou 2, dans lequel le moule possède plusieurs saillies (12) qui dépassent vers mais ne viennent pas en contact avec lesdites surfaces supérieureet inférieure de la plaquette lorsque la plaquette est placée dans la cavité de moule.

FIG. 1

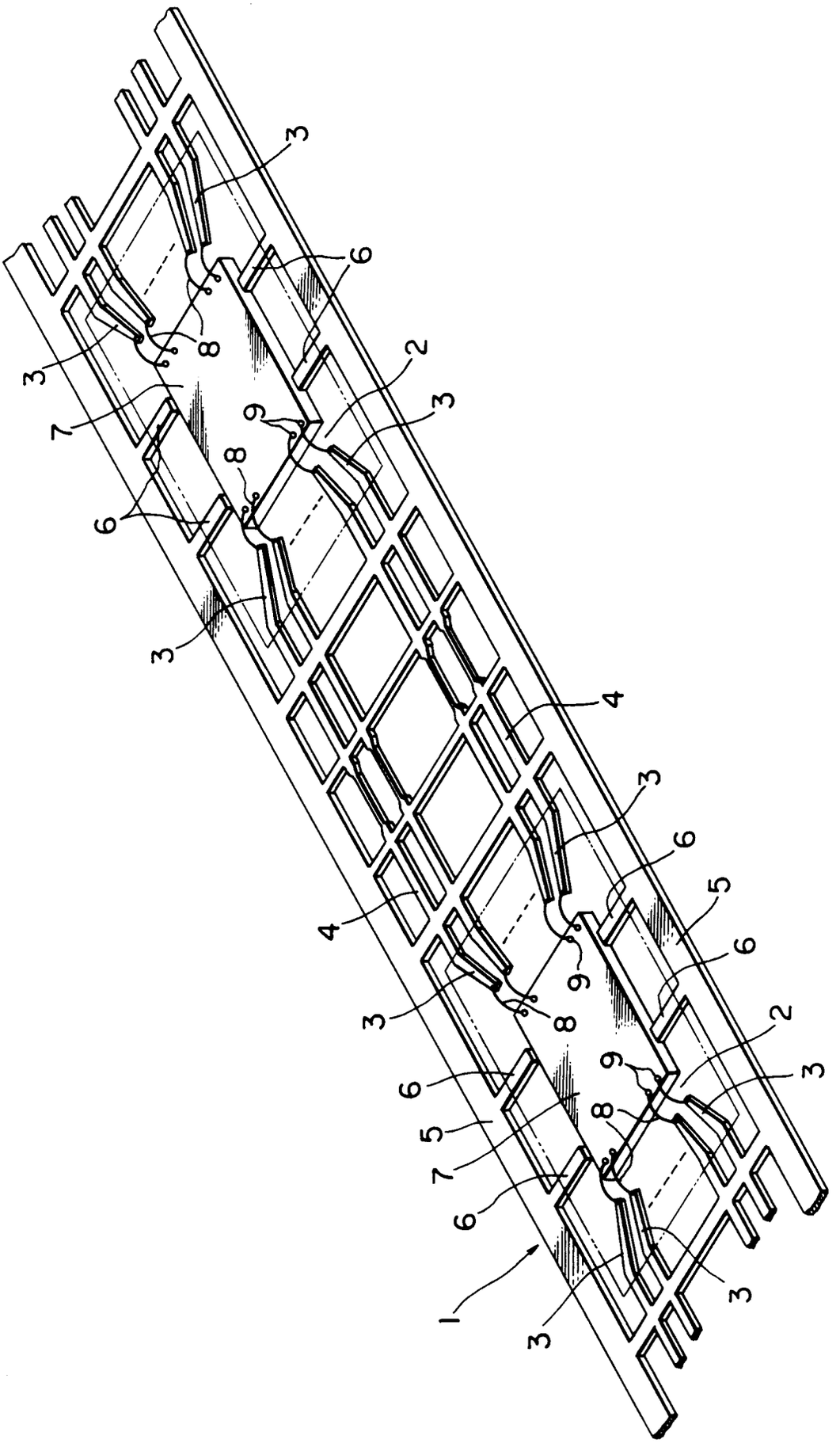

FIG. 2

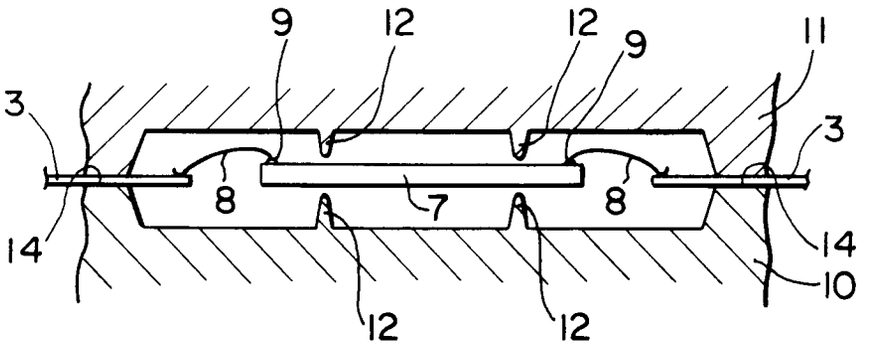

FIG. 3

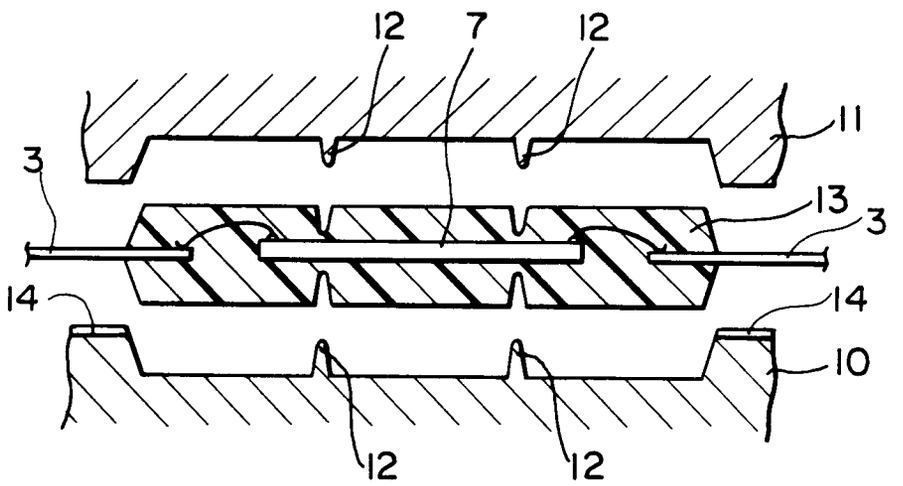

FIG. 4

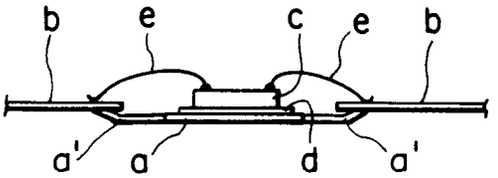

FIG. 5

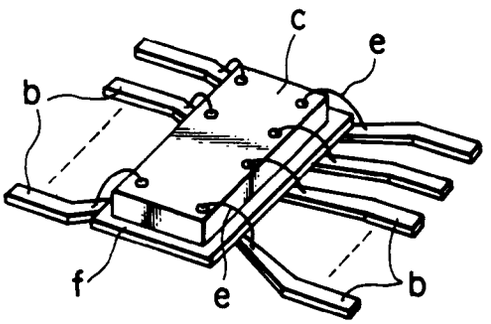

FIG. 6

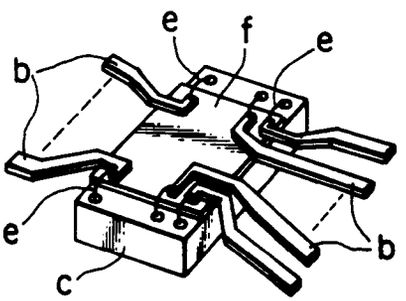

FIG. 7