United States Patent

Ritzenthaler

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[54] SERIES TRANSISTOR POWER SUPPLY REGULATOR

[72] Inventor: **Jean Ritzenthaler,** Geneva, Switzerland

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[21] Appl. No.: **176,957**

[52] **U.S. Cl.**.....**323/9,** 321/18, 323/22 T, 307/297

[51] **Int. Cl.**.....**G05f 1/64,** H02m 7/24

[58] **Field of Search**.....323/22 R, 22 T, 4, 9, 20; 321/18, 27 R; 307/296, 297

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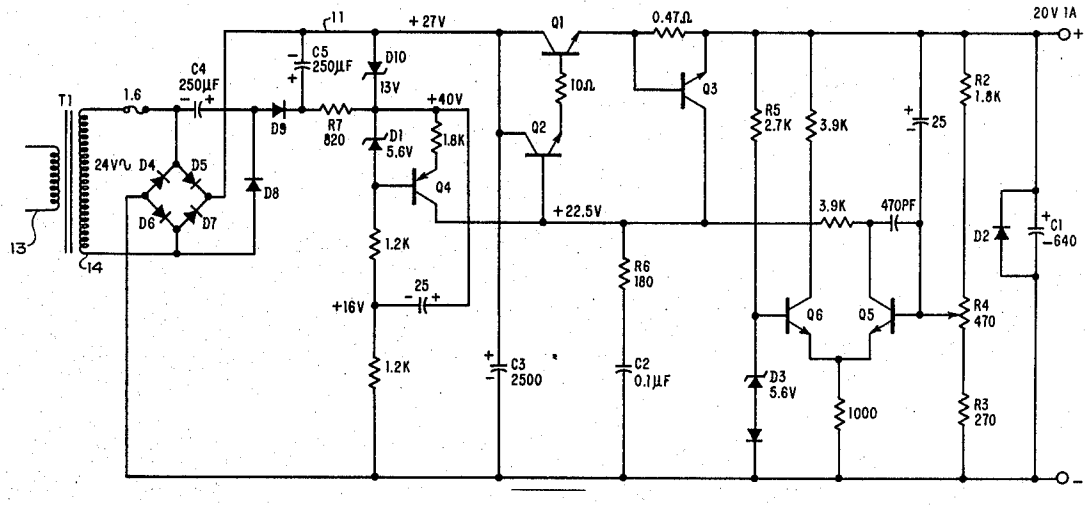
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[57] **ABSTRACT**

A power supply regulator of the series transistor type employing a current limiter transistor circuit coupled to the output of the series transistor and a constant current supply comprising a transistor and Zener diode for supplying current to the current limiter transistor circuit, and a voltage multiplier circuit coupled to the rectifier circuit input of the regulator circuit, said constant current supply being coupled to said voltage multiplier circuit.

4 Claims, 2 Drawing Figures



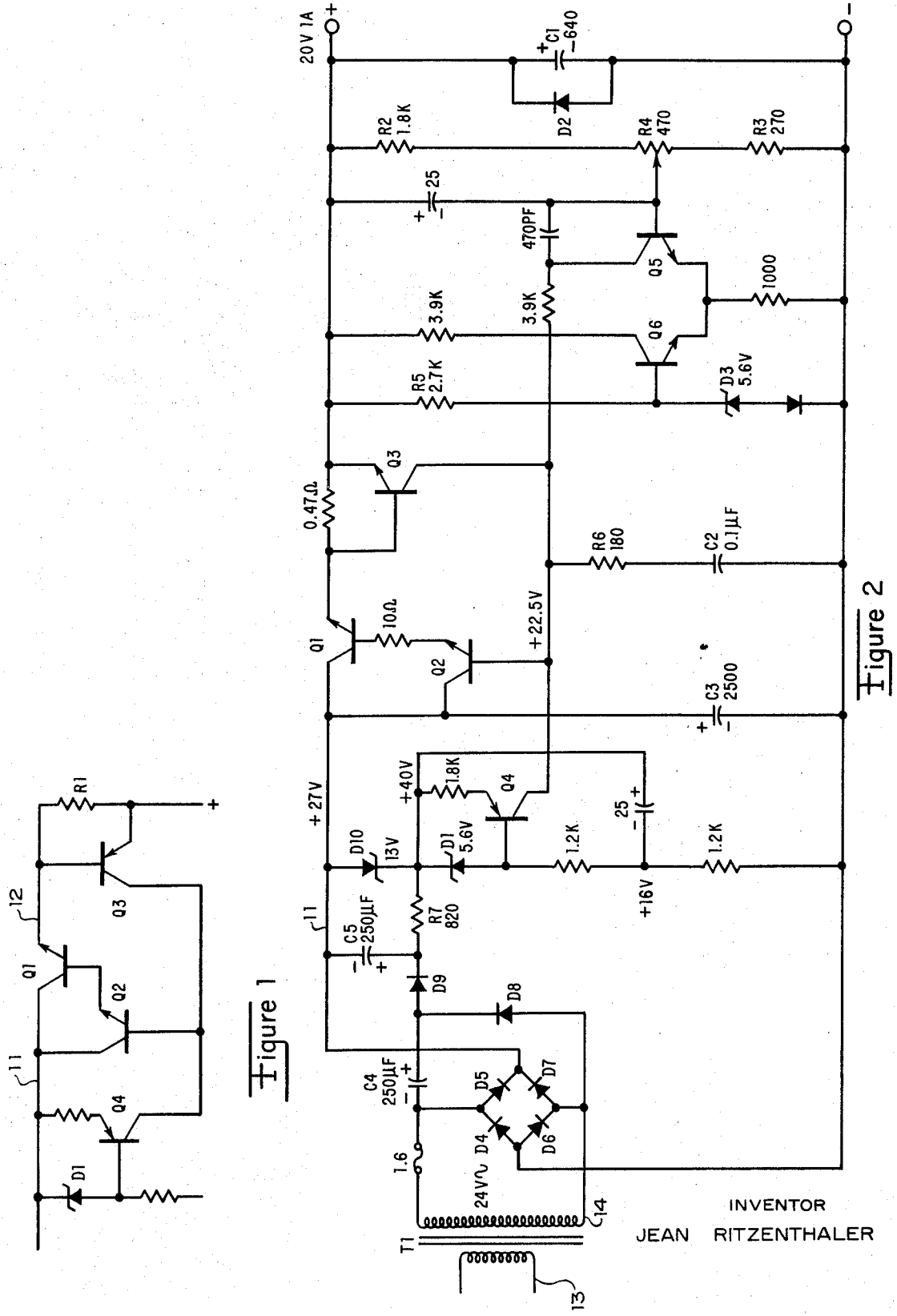


Figure 1

Figure 2

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SERIES TRANSISTOR POWER SUPPLY REGULATOR

BACKGROUND OF THE INVENTION

Regulated power supplies of the series transistor type often employ a current limiter transistor in the output circuit of the series transistor for limiting the current in the output to a selected value. This current limiting transistor requires a constant current supply for its collector-emitter circuit and, for good regulation, this constant current supply takes the form of a transistor coupled between the incoming line to the series transistor and the collector-emitter circuit of the current limiter combined with a Zener diode coupling the base of the current supply transistor to the incoming line. A Zener diode is employed because of the sharp knee characteristic and thus the good regulation achieved.

A Zener diode with good regulating characteristics at modest current requirements requires an operating voltage of about 5.6 volts and, since this order of magnitude of voltage will also appear across the series transistor circuit located between the constant current source circuit and the current limiter circuit, a rather high series transistor power dissipation results.

In addition, the existence of this substantial value of voltage across the series transistor circuit reduces the degree of excursion permitted the incoming line voltage. For example, with a 20 volt output level and a 7 volt drop across the switching transistor, the input voltage to the switching transistor may not fall below 27 volts.

BRIEF SUMMARY OF THE PRESENT INVENTION

In the present invention, a voltage doubler circuit is employed coupled to the full wave rectifier input circuit of the series regulator, and the constant current supply circuit is coupled to this voltage doubler rather than to the input of the series transistor circuit. This voltage doubler circuit therefore provides the desired high voltage to the current supply circuit, and a lower input voltage may be applied to the series transistor circuit.

The reduced voltage across the series transistor circuit results in lower power dissipation, and the regulator will tolerate larger excursion of the incoming line voltage.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a portion of the series regulator circuit of a typical form of known voltage regulator.

FIG. 2 is a schematic diagram of the series voltage regulator incorporating the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, there is shown a series transistor Q1 in a Darlington configuration with Q2 which forms the current regulation circuit between the input line 11 and the output line 12 in a typical type of series voltage regulator.

A current limiter transistor Q3 is provided to sense the value of the output current through the resistor R1 in the output line, this transistor Q3 turning on as the current in R1 rises to draw current from the base circuit of Q2, reducing the current flow through Q1 and thus limiting the current in the output to a desired maximum level.

For proper operation, the current limiter transistor Q3 requires a constant current source for its collector-emitter circuit, and often times this is provided by the transistor Q4 in combination with the Zener diode D1 coupled between the incoming line 11 and the collector of Q3 and base of Q2. A Zener diode with good regulating characteristics at modest current levels requires a relatively high voltage, for example, 5.6 volts. Thus, the voltage drop across D1 and the V_{BC} of Q4 results in a voltage drop greater than 5.6 volts across the Darlington circuit from the collector of Q1 to the base of Q2. The voltage across the series transistor Q1 is greater than this voltage by the V_{BE} of both Q1 and Q2, and thus the voltage across Q1 is substantial, resulting in a significant power dissipation in the series transistor.

Since this substantial voltage difference must be maintained between incoming line 11 and output line 12, the amount of voltage excursion allowed on incoming line 11 is limited. For example, with a 20 volt output and a voltage drop of 7 volts across Q1, the voltage on the input line 11 may not drop below 27 volts.

Referring now to FIG. 2 , there is shown a series regulator circuit incorporating the present invention which results in a substantial decrease in the voltage across the series transistor Q1.

As with standard voltage regulators, the regulated voltage output appears across the output circuit comprising capacitor C1 and diode D2, which, in this illustration, is 20 volts at 1 amp. A voltage divider comprising resistors R2, R3 and potentiometer R4 is coupled across the output, the tap on the potentiometer being coupled to the base of one transistor Q5 in the differential pair Q5 and Q6. A fixed reference voltage is provided at the base of Q6 by the circuit comprising resistor R5 and Zener diode D3. Should the output voltage tend to rise, the voltage on the base of Q5 tends to increase relative to the reference voltage on the base of Q6, and current tends to flow in Q5, this current being drawn from the base circuit of Q2. The current through Q1 tends to decrease, reducing the output voltage, resulting in a tendency to decrease the voltage on the base of Q5 and reduce the current drawn from the base of Q2. This differential pair thus serves to control the series transistor Q1 and maintain a constant output voltage.

The circuit comprising resistor R6 and capacitor C2 reduces the gain of the circuit to prevent oscillations.

The input to this voltage regulator circuit comprises the input transformer T1 with is primary winding 13 coupled to the source of AC and with its secondary winding 14 coupled across the full wave rectifier bridge comprising diodes D4, D5, D6 and D7. The main filter circuit comprising capacitor C3 is coupled across the bridge and serves as the input to the series transistor circuit.

In the present invention, rather than coupling the constant current source comprising transistor Q4 and Zener diode D1 to the incoming line at the collector of Q1, a voltage multiplier circuit is provided which serves to produce an elevated voltage from the input, and provides this elevated voltage to the current source. This elevated voltage serves the high voltage requirements of the Zener diode D1 in the constant current supply, and frees the input to the switching transistor Q1 from the duty of supplying this voltage.

One preferred form of voltage doubler circuit comprises the two diodes D8 and D9, the two capacitors C4 and C5, the resistor R7 and Zener diode D10. In operation, during the negative half cycle of the incoming waveform, current flows from the secondary winding through D8 and capacitor C4, charging up this capacitor to a substantial voltage level, for example, 30 volts. During the positive half cycle, diode D5 forms a low impedance path between C4 and C5 and C4 shares its charge with capacitor C5, raising the junction of C5 and diode D9 to a high voltage relative to the junction of C5 and the input line 11. A voltage substantially higher than that on line 11 appears at the junction of resistor R7 and Zener diode D10 in the constant current supply.

The voltage across the switching transistor Q1 may now be lowered substantially, thus reducing the power dissipation in Q1. This input voltage may also reach lower levels with the circuit of FIG. 1, thus permitting a greater input voltage excursion while maintaining the desired output voltage level.

It should be understood that this particular form of voltage doubler or multiplier is illustrative only and that other known forms of voltage multiplier may be employed.

A voltage substantially higher than that on line 11 appears at the junction of resistor R7 and Zener diode D10, and this elevated voltage is utilized as the operating voltage for the Zener diode D1 in the constant current supply.

The voltage across the switching transistor Q1 may now be lowered substantially, thus reducing the power dissipation in Q1. This input voltage may also reach lower levels than the voltage levels with the circuit of FIG. 1, thus permitting a

greater input voltage excursion while maintaining the desired output voltage level.

It should be understood that this particular form of voltage doubler or multiplier is illustrative only and that other known forms of voltage multiplier may be employed.

I Claim:

1. A series regulator circuit comprising a full wave rectifier circuit coupled to the AC input, an output line, a current regulating transistor coupled in series between said rectifier circuit and said output line; a current transistor circuit coupled between said series regulating transistor and said output line, and a constant current supply including a transistor and Zener diode coupled to said rectifier circuit for supplying current to the collector-emitter circuit of said current limiter transistor, the improvement comprising a voltage multiplier circuit coupled to said full wave rectifier circuit for producing a voltage higher than that coupled to said series transistor, the elevated voltage output of said voltage doubler circuit being coupled to said constant current supply.

2. A series regulator circuit as claimed in claim 1 wherein the collector-emitter circuit of said series regulator transistor is coupled in series between said rectifier circuit and said output line, a second transistor having its collector-emitter circuit coupled across the collector-base circuit of said series regulator transistor, the collector-emitter circuit of said current limiter transistor being coupled to the base of said second transistor to control the current flow through said second transistor and thus the current flow through said series regulator transistor.

3. A series regulator as claimed in claim 1 wherein said full wave rectifier circuit includes the secondary winding of an input transformer, said voltage doubler circuit comprising a first capacitor and first diode connected in series across said secondary winding, and a second capacitor and second diode connected in series between the junction of said first capacitor and said first diode and the high side of said rectifier circuit.

4. A series regulator circuit as claimed in claim 3 including a Zener diode and a resistor connected in series across said second capacitor, said constant current supply circuit being coupled to the junction between said Zener diode and resistor.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,671,852 Dated June 20, 1972

Inventor(s) Jean Ritzenthaler, Geneva, Switzerland

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 10, after "current" insert -- limiter --.

Signed and Sealed this

Nineteenth Day of October 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

UNITED STATES PATENT OFFICE

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