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(71) Applicant: MARTIN MARIETTA CORPORATION [US/US]; 6801 Rockledge Drive, Bethesda, MD 20817 (US).

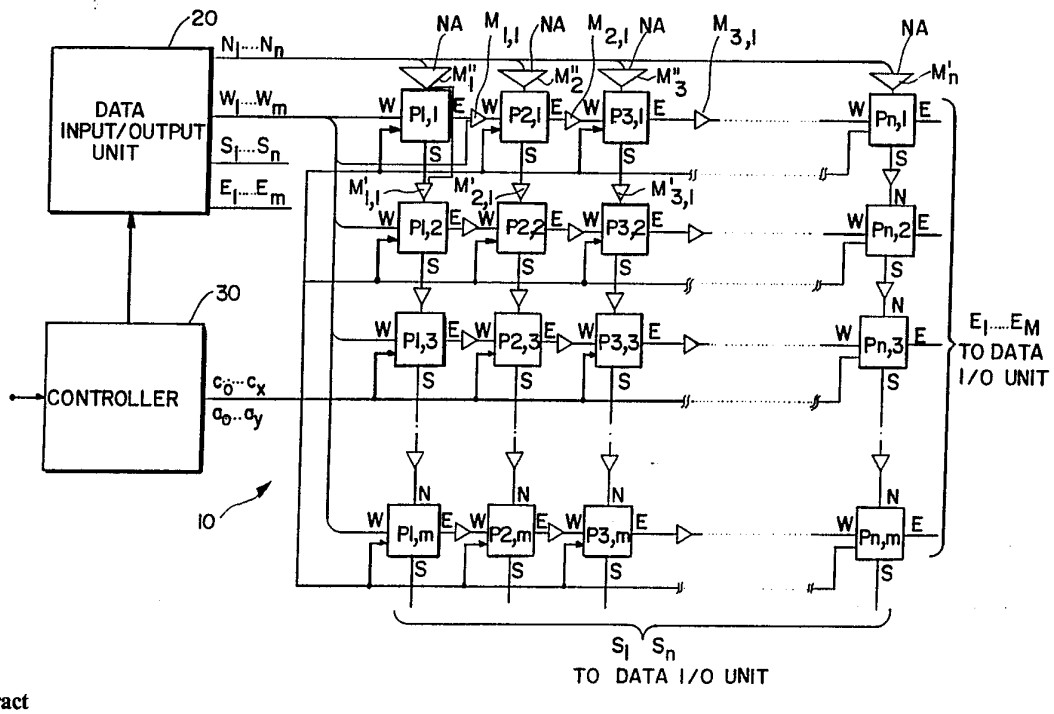
(72) Inventors: HOLSZTYNSKI, Wlodzimierz ; 707 Continental Circle, Apartment 1831, Mountainview, CA 94040 (US). BENTON, Richard, W. ; 775 Little Wekiva Circle, Altamonte Springs, FL 32714 (US). JOHNSON, W., Keith ; 6012 Paseo Palmilla, Goleta, CA 93117 (US). MCNAMARA, Robert, A. ; 5709 Rockwood Avenue, Orlando, FL 32809 (US). NAEYAERT, Roger, S. ; 2500 Cobre Valle, Plano, TX 75023 (US). NODEN, Douglas, A. ; 1516 Montcalm Street, Orlando, FL 32806 (US). SCHOOMAKER, Ronald, W. ; 9220 Buttonwood Street, Orlando, FL 32825 (US).

(74) Agents: CHIN, Gay; Martin Marietta Corporation, 6801 Rockledge Drive, Bethesda, MD 20817 (US) et al.

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(54) Title: PARALLEL DATA PROCESSOR



(57) Abstract

A parallel data processor comprised of an array of identical cells concurrently performing identical operations under the direction of a central controller, and incorporating one or more of a special cell architecture including a segmented memory, conditional logic for preliminary processing, and circuitry for indicating when the cell is active, and programmable cell interconnection including cell bypass and alternate connection of edge cells.

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PARALLEL DATA PROCESSOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a high speed parallel data processing system and, more particularly, to a parallel data processing system comprised of an array of identical interconnected cells operating under the control of a master controller to operate on single bits of data. Even more particularly, the invention pertains to the architecture of the cells and to specific patterns of interconnection.

2. Background Art

Certain data processing tasks require that substantially identical logical or arithmetic operations be performed on large amounts of data. One approach to carrying out such tasks which is drawing increasing attention is parallel processing. In parallel processing, each element or cell of an array processor made up of such cells processes its own bit of data at the same time as all other cells of the array processor perform the same process on their own bit of data. Such machines are referred to by several names, including Single Instruction-Multiple Data (SIMD) machines.

A common arrangement for such a machine is as a rectangular array of cells, with each interior cell

connected to its four nearest neighboring cells and each edge cell connected to a data input/output device. Each cell is connected as well to a master controller which coordinates the movement of data through the array by providing appropriate instructions to the processing elements. Such an array proves useful, for example, in high resolution image processing. The image pixels comprise a data matrix which can be loaded into and processed quickly and efficiently by the processor array.

Although all may be based upon the same generic concept of an array of cells all performing the same function in unison, parallel processors vary in details of cell design. For example, U.S. Patent No. 4,215,401 to Holsztynski et al discloses a cell which includes a random access memory (RAM), a single bit accumulator, and a simple logical gate. The disclosed cell is extremely simple and, hence, inexpensive and easily fabricated. A negative consequence of this simplicity, however, is that some computational algorithms are quite cumbersome so that it may require many instructions to perform a simple and often repeated task.

U.S. Patent No. 4,739,474, to Holsztynski et al, represents a higher level of complexity, in which the logic gate is replaced by a full adder capable of performing both arithmetic and logical functions. Pressing the full adder into dual service creates an

efficiency which more than offsets the added complexity and cost incurred by including a full adder in each cell.

It is important to note that the substitution of a full adder for a logic gate, while superficially simple, is in reality a change of major consequence. The cell structure cannot be allowed to become too complex. This is because in a typical array the cell will be repeated dozens if not hundreds of times. The cost of each additional element in terms of money and space on a VLSI chip is therefore multiplied many times. It is therefore no simple matter to identify those functions which are sufficiently useful, to justify their incorporation into the cell. It is similarly no simple matter to implement those functions so that their incorporation is not realized at too high a cost.

Parallel processors may also vary in the manner of cell interconnection. As mentioned above, cells are typically connected to their nearest physical neighbors. All cells except those at the edge of the entire array are connected to four neighbors. It has not heretofore been completely appreciated, however, that significant benefits may flow from providing for alternate paths of interconnection and, specifically, in providing programmable, flexible interconnection between cells.

SUMMARY OF THE INVENTION

There is thus a continuing need to identify and implement variations in cell architecture which result in a maximal increase in cell efficiency with a minimal increase in cell complexity. This need is addressed in the present invention through the provision in each cell of a segmented random access memory to permit the performance of more than one read/write operation per clock cycle. It is further addressed through the provision of circuitry ahead of the main processing element for conditionally processing data prior to processing in the main processing element. It is further addressed through the provision of circuitry in the cell by which the master controller can deactivate or activate the cell, or by which the cell can provide indication of whether the cell has activated or deactivated itself. This permits independent conditional operations for each individual cell.

The present invention not only exploits variations in cell architecture, but also in cell interconnection. In one enhancement, at least one bypass network is intermeshed with the array for bypassing cells as needed or desired. In another embodiment, in which the cells are arranged in an n x m array, cells on at least one edge are arranged to be connectable to either an external device or to another cell in the array, thus creating the

ability to reshape the virtual configuration of the array.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features of the present invention will become apparent to one of ordinary skill in the art to which the invention pertains from the following detailed description when read in conjunction with the drawings, in which:

Figure 1 is a block diagram of a preferred embodiment of a processor array according to the invention;

Figure 2 is a schematic diagram of a second preferred embodiment of a processor array according to the invention;

Figures 3(a), 3(b), and 3(c) are block diagrams showing alternate array interconnection according to a preferred embodiment of the invention;

Figure 4 is a schematic diagram of a preferred embodiment of a cell according to the invention;

Figure 5 is a schematic diagram of a preferred embodiment of a segmented memory according to the invention;

Figure 6 is a schematic diagram of a preferred embodiment of a conditional logic unit according to the invention; and

Figure 7 is a block diagram of a typical application for a processor array according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

General details concerning the arrangement of parallel processors as an array of identical cells are available from aforementioned U.S. Patent No. 4,739,474 to Holsztynski et al, the specification of which is hereby incorporated by reference. As shown in that patent and in Figure 1 herein, an array 10 may comprise n rows and m columns of identical processors or cells $P_{o,o}$ through $P_{n,m}$ to form an n x m rectangular network or matrix (the subscripts "n" and "m" representing variables which may assume any positive integral value). There are thus cells having four nearest neighbors (interior cells) and cells having less than four nearest neighbors (edge cells). For uniform orientation, the directions north, south, east, and west are used to reference up, down, right, and left, respectively, in the drawing, so that the nearest neighbors will be referred to as N, S, E, and W, respectively.

The edge cells of the array 10 are connected to a data input/output unit 20 as illustrated. Every cell receives command and address signals Co - Cx and Ao - Ay, respectively, from a controller 30. In addition, clock

signals may be provided by the controller 30 to each cell, and the data input/output unit 20 may also be controlled by the controller 30. These and other details are available from the Holsztynski et al '474 patent.

Figure 1 also shows two multiplexer networks intermeshed with the cell array. The first multiplexer network is made up of multiplexers $M_{1,1}$ through $M_{n,m}$ and $M_{1,1}'$ through $M_{n,m}'$ ("n" and "m" here and elsewhere assuming values not necessarily related to those assumed in connection with labelling the cells unless otherwise specified). As will be developed below, this network is used for selective bypass of cells on an individual, row, column, or block basis.

The second multiplexer network is made up of multiplexers M_1'' through M_n'', and is used for selectively altering the connection of the north edge cells to either the data input/output unit 20 or to another cell in the array. An array may be made up of several interlinked chips, each supplying its own section or subarray of the main array. The second multiplexer network provides a capability of changing the virtual configuration of the array.

All of the multiplexers are responsive to the controller 30 through connections which have been omitted for clarity. It should be noted that the communication paths provided by the multiplexers are bidirectional, so

that the multiplexers should be regarded as multiplexer/demultiplexers. It should also be noted that the term multiplexer is used herein generically to encompass any device for performing the functions ascribed to these elements, i.e., line selection based on a control input. Thus, simple switches may be multiplexers to the extent they are provided to perform such a function.

Figure 2 is a more detailed rendering of an array 10 according to the present invention, in this case an 8 x 16 array of 128 identical cells $P_{1,1}$ - $P_{8,16}$. Peripheral equipment such as controller 30 and connections thereto have been omitted for clarity, but it will be understood that such connections are present. The embodiment of Figure 2 has a multiplexer bypass network with members arranged between selected cells thus bypassing intervening cells. As can be seen, it is not necessary that there be a multiplexer between every cell and its nearest neighbors in order to bypass entire rows, columns, or blocks and so, in effect, alter the virtual dimensions of the array to suit a particular application. In the embodiment shown, there is one set of eight multiplexers per column and one set of four per row. Thus, in general, it is necessary only to have half as many multiplexers as cells in any row or column. Of course, if there is an alternate communication path,

(such as the CM path described below) it may be desirable to provide that path with a multiplexer network as well.

When cell bypass is invoked, cell-to-cell communication is based on the value of a latched bypass control word which continuously drives the row and column multiplexer select lines. If it were desired to bypass the first column, for example, the westernmost I/O pins become logically connected to the west port of the cells in the second column.

Row and column bypass can be separately controlled so that all possible virtual array sizes, such as 7 x 12, 4 x 10, 1 x 16, or even 1 x 1, can be obtained. The embodiment of Figure 2, however, is designed so that it is not possible to bypass the array 10 entirely. The cells in the easternmost column are always connected to the east I/O pins so that data must always pass through the easternmost column of cells. Similarly, the cells in the southernmost row are always connected to the south I/O pins so that data must always pass through the southernmost row of cells. There is therefore a minimum 1 x 1 configuration.

The benefits of the cell bypass network are well exemplified in operations such as parallel data summation, also known as an array sum. An array sum is a summation of the same data type variable in each cell throughout the entire array. With programmable bypass,

this summation may be achieved using the following algorithm:

(1) program the cell bypass network to full 8 x 16 configuration;

(2) command each cell to shift its variable to its eastern neighbor;

(3) command each cell to add the received variable to its resident value (which results in cells in columns 2, 4, 6, and 8 containing a non-overlapping set of sums);

(4) program the cell bypass network to a 4 x 16 configuration logically interconnecting columns 2, 4, 6, and 8;

(5) repeat steps (2) and (3) (which results in cells in columns 4 and 8 containing a non-overlapping set of sums);

(6) program the cell bypass network to a 2 x 16 configuration logically interconnecting cells in column 4 to cells in column 8;

(7) repeat step 5 (which results in cells in column 8 containing the sums for the entire array from west to east); and

(8) repeat the algorithm north to south to sum cells in column 8, halving the row configuration after each shift and add until the entire array sum resides in the cell at the southeastern corner of the array.

Without the cell bypass network, many additional clock cycles would be required to shift the data through the non-participating cells to the ultimate destination when performing the partial array summations. The cell bypass network allows direct cell communication for a minimal overhead of 2 cycles for array reconfiguration.

The other multiplexer network comprises bidirectional semiconductor switches or multiplexers M_0'' through M_7'' on the eight north edge cells. These allow selection of either a "normal" north data path (to data input/output unit 20) or an "alternate" north data path (to another cell on the same or a different chip). The array 10 is thus no longer limited to north, south, east, west connectivity. For example, consider a 32 x 32 array made up of 4 x 4 subarrays of 64 cells each, with the north edge cells of each subarray being provided with a switchable north alternate connection as shown in Figure 3(a). Each subarray may, for example, be on a separate semiconductor chip. By appropriate interconnection of north and north alternate inputs, the array can be reconfigured as two 16 x 32 arrays (Figure 3(b)) or as one 1024 x 1 array (Figure 3(c)). Thus, the second multiplexer network has great utility in varying connection of multiple-chip arrays.

The north alternate connector may also be connected to a memory device to extend logically the memory

capability of each cell and to allow data operands to be rolled in and rolled out as necessary. It also provides a port which can be connected to an I/O device or other processing cells in the array to allow for corner turn operations.

A preferred embodiment according to the present invention may also include one or more enhancements in the architecture of the individual cells. As can be seen in Figure 4, the cell may include a group of registers, namely, a north-south (NS) register 40, an east-west (EW) register 50, a carry (C) register 60, and a communication (CM) register 70. It also includes a group of corresponding multiplexers, namely, an NS multiplexer 45, an EW multiplexer 55, a C multiplexer 65, and a CM multiplexer 75.

The registers are single bit and provide working storage and communications functions for the cell. The NS and CM registers are sources or destinations for data flowing north or south. Thus, the NS register 40 can communicate bidirectionally with the NS registers of its north and south neighboring cells. The CM register provides I/O communications to each cell bidirectionally along the north-south axis. The difference between these two is that operation of the CM register 70 does not influence operation of an arithmetic logic unit (ALU) 110 also incorporated into the cell. As a consequence, the

CM register 70 can perform input/output functions without interfering with the ALU 110 which allows I/O to occur without interfering with normal processing. The EW registers 50 are the sources and destinations of data flowing east or west. Each multiplexer controls data flow from various sources to its respective register under control signals originating from a master controller such as controller 30 of Figure 1.

The cell may incorporate various additional elements, which will be described below in detail. These include a memory 100, which, as will be described below, is segmented to provide flexibility in data storage and retrieval. It also includes a conditional logic unit (CLU) 120 which, as will be developed below, simplifies and accelerates data processing according to certain algorithms. The cell may also incorporate AF logic circuitry 130, which includes a single-bit register AF register 140. This circuitry defines two states, activated and deactivated. Also included is Global OR (GLOR) circuitry 150, which is used in forming a signal which is a logical "or" of all active cells in the array. The signal is the product of "anding" the output of the C register 60 with that of the AF register 140.

The various functions of these circuits will now be described in greater detail.

Arithmetic functions within the cell are performed by the ALU 110 which operates on data presented to it under the control of the master controller 30. The inputs to the ALU 110 are the C register 60 and the outputs from a conditional logic circuit 120 described below, which obtains its data from the NS register 40 and the EW register 50. The ALU 110 may send its output to any of these registers or to the memory 100. Specifically, when the ALU 110 is a single bit full adder, the SUM output can be written to a memory 100 and the CARRY and BORROW outputs can be used as inputs to the C register 60. Multi-bit operations such as addition are carried out by adding the operands on a bit-by-bit basis, while propagating the resultant carry into the next higher-order addition.

All multi-bit operands must be stored in the memory 100. Thus, performance of almost all operations is highly dependent on the capabilities of memory 100. For example, in an architecture where the memory has only a single port, and so can perform only a single read or write per clock cycle, an n-bit operation would require 2n cycles for reading two operands, n cycles for writing each partial sum, and one cycle for writing the final carry value, for a total of 3n+1 clock cycles. Thus, a memory which permits only a single read or a single write

per cycle is a bottleneck for computationally intensive algorithms.

Due to the great dependence of cell efficiency on the memory 100, it is preferred in the present invention to use a segmented RAM as the memory 100. "Segmented" herein refers to a virtual or logical division of the RAM into at least semi-independently operable blocks. In a preferred implementation shown in Figure 5, the memory 100 is 128 bits divided into four contiguous blocks BLK0 through BLK3, of 32 bits each. Each block is preferably a separate, single-ported memory, that can perform either a single read, or a single write, in one clock cycle. It will be appreciated in the embodiment described, however, that there can be no more than one write to the entire RAM per clock cycle. It will also be appreciated that each block may be a multi-ported memory, if such would provide advantages for a given application. Servicing the blocks BLK0 through BLK3 are three read ports, ARAM, BRAM, and BRAM*, and one write port ARAM*. Two address busses service these ports. The first, AADR or A0 through A6, sources the address for operations on the ARAM and ARAM* ports. The second, BADR or B0-B5, sources the address for operations on the BRAM and BRAM* ports. Memory address decode logic circuits 160 and 170 use selected address bits, for example, the upper address bits, to select which port is to be connected to which

block. The decode logic is provided to ensure that only one port is allocated to each block for a given address on the busses. The signal WE* is an internally generated write enable signal.

The provision of 2 address busses, 3 read ports, and 1 write port creates a pseudo multi-port capability. Addressing options allow for either 1, 2, or 3 reads per clock cycle. The inclusion of simultaneous read/write capability means that n-bit operations such as addition can now be performed in n+2 clock signals, instead of 3n+1. This is a net improvement of 2.5 to 1 in the case of an 8-bit add.

The memory 100 may be loaded from the C register 60, the CM register 70, an AF register 140, or the SUM output of the ALU 110. The outputs of memory 100 may be loaded into the NS register 40, EW register 50, C register 60, CM register 70, a D register 190, or the AF register 140.

The cell is also naturally very dependent on the capabilities of ALU 110. To enhance the capabilities of this element, it is preferred to include in the cell a conditional logic unit (CLU) 120, as shown in Figure 6. The CLU 120 includes an input multiplexer 180 with inputs connected to the output of C multiplexer 65 and to the output of a D register 190. The input multiplexer 180 is controlled by an appropriate control signal. Its output is connected to the input of the D register 190. The

output of the D register 190 is also connected to a first logic gate 200 and a second logic gate 210. In the embodiment of Figure 6, these are AND gates. One input of the first logic gate 200 is connected to the NS register 40; the other input is connected to the D register 190 and, in the embodiment of Figure 6, is an inverting input. One input of the second logic 210 is also connected to the input of D register 190. The other input is connected to the EW register 50.

The CLU 120 also includes a first output multiplexer 220 and a second output multiplexer 230. The inputs for the first multiplexer 220 are the outputs of the NS register 40 and the first logic gate 200. The inputs for second output multiplexer 230 are the outputs of the EW register 50 and the second logic gate 210.

The CLU 120 allows both conditional arithmetic operation and conditional selection operation on the operands of the NS register 40 and the EW register 50 based on the contents of the D register 190. This leads to great simplification of operations such as multiplication. For example, without conditional logic, the algorithm for multiplication of two multi-bit numbers involved a reiterative process of "anding" the first bit of the multiplier with the multiplicand to form a first partial sum, and then "anding" the second bit of the multiplier with the multiplicand and adding the result to

the first partial sum to form a second partial sum, continuing for each successive bit until the product is formed.

The following example is indicative, with the usual right justification on bit placement:

```
     101   (Multiplicand)
     011   (Multiplier)
  000101   (1st Partial Sum)
+  101
  001111   (2nd Partial Sum)
+  000
  001111   (Product)
```

The CLU 120 eliminates the requirement for "anding" by providing a conditional summation capability. This allows the partial sum to be conditionally added to the multiplicand based on the present multiplier-bit value. If the multiplier bit is 0, then the next partial sum is the present partial sum since 0*x=0. If the multiplier bit is 1, the next partial sum is the sum of the present sum and the multiplicand. Right justification in bit placement is accomplished by incrementing the starting address of the partial sum operand by one after each iteration.

In the context of the device shown in Figure 6, multiplication would be carried out by loading a zero into the NS register 40, the multiplicand into the EW register 60, and the least significant multiplier bit into the D register 190. The CLU 120 then selects the multiplicand if the contents of the D register 190 is

"1". The partial sum is then loaded into the NS register 40, the multiplicand into the EW register 60, and the next significant multiplier bit into the D register 190. The multiplicand is added to the partial sum if the contents of the D register 190 is "1". The process is repeated as necessary to derive the final product.

The cell also preferably includes "Activity Flag" (AF) logic or circuitry 130. This circuitry is used to place the cell in one of two states - activated or deactivated. An activated cell participates in algorithm execution. A deactivated cell does not. The state is determined by the contents of the AF register 140. For example, a set register may indicate activated cell, so that a reset register would then indicate a deactivated cell.

The contents of the AF register 140 may be generated either internally, for example, through the C multiplexer 65 as shown, as a result of internal algorithm execution. This would provide an indication of status of internal algorithm execution. Alternatively, however, the contents of the AF register 140 may originate externally and be directed to the cell as a result of decoding by an AF logic unit 240. The AF logic unit may decode an address appearing, for example, on address bus AADR as shown. This permits a row, column, or individual cell to

be uniquely selected. The AF logic unit 240 may also be responsive to two select lines X and Y. These lines are used in a multi-chip array to select a particular chip, row of chips, or column of chips.

The AF logic unit 240 generates a value (cell enable) applied to an AF multiplexer 250 to in turn determine the value of the AF register 140 if that value is to be determined externally.

As an example of how such a system would work in practice, consider the system of Figure 4 where the AF logic unit 240 is responsive to the AADR address bus, to control signals on two lines of the BADR address bus, and to control signals designated C17 and C18. The signals on the AADR address bus select the row, column, or individual cell. The X and Y select lines select chips in a multi-chip array. The control signals BADR1, BADR0, C17, and C18 can then be used to select whether the value of the AF register 140 at the address indicated is internally derived, whether the cell (or the row or column containing it) should be externally activated or deactivated. When a cell is active, its "Global" output contributes to the overall GLOR output signal and writes to the cell's memory 100 are enabled. A deactivated cell's "Global" output cannot contribute to the overall GLOR output signal and writes to the cell's memory 100 are inhibited.

The AF circuitry 130 address decoding logic thus provides a means to obtain information concerning algorithm execution by a cell through use of the GLOR output signal. For example, if an array sum as previously described were being carried out, the final sum could be obtained through the GLOR output if all other cells except that at the southeastern corner were inactive.

As another example of the usefulness of the GLOR output in combination with the AF logic circuitry 130, consider the performance of a content addressable memory function. After all cells concurrently search, the combination of GLOR with the AF logic circuitry could be used to determine not only whether any cell uncovered a match, but also the location of the cell.

Figure 7 depicts schematically a concrete application for a parallel data processor according to the present invention, as a component of a infrared image processing system. Such a system typically requires a resolution of 512 x 512 pixels per frame, 8-bits per pixel, and a frame update rate of 30Hz. With these characteristics, a real-time pixel processor must maintain an average throughput rate of 262,144 pixels every 33.33 ms. The parallel processor of the present invention is ideally suited to perform a two-dimensional data processing problem of this type. The theoretical

ideal would be one processor per pixel, or, in other words, a 512 x 512 array of cells. At a clock rate of 20 MHz, this would permit execution of nearly 666,666 instructions every 33.33 ms. Usually, however, a smaller array is used, with the image being processed as a series of overlapping sub-images.

In addition to the array 10 and array controller 30, the system includes an IR sensor 260, a sensor interface/control 270, and a host CPU 280. A data input buffer/formatter 290 and a data output buffer/formatter 300 together perform the functions ascribed to data input/output circuit 20 of Figure 1.

The IR sensor 260 and sensor interface 270 are front-end modules common to most applications of this type. The IR energy received by IR sensor 260 is converted to digital data by sensor interface 270. The digital data must then be transposed from a data word stream to a data bit plane format to enable transfer to the array 10 for processing. A bit plane is a two-dimensional plane (i.e., array or matrix) of data bits of common significance, of the same size as the array 10. This transposition, called pixel to plane conversion, is carried out by input buffer/formatter 290. The output buffer/formatter 300 performs the inverse operation, to make the output comprehensible to the host CPU 280. The array controller 30 coordinates program execution with

the bit-plane I/O. It is similar in design to controllers found in most bit-slice systems.

Other system embellishments are possible. For example, logic can be incorporated to selectively enable, disable or modify functions to make the cells or array compatible with other parallel data processors. Such a scheme is implemented in the embodiment of Figure 4 through the provision of a series of multiplexers 310 and gates 320 connected as shown to operate in response to, for example, a "mode" command, to disable the segmented RAM and AF logic enhancements, or at least to prevent those enhancements from interfering with cell operation.

The invention has been described above in terms of specific embodiments merely for the sake of elucidation. No statement above is intended to imply that the above embodiments are the only fashion in which the invention may be embodied or practiced, and no statement above should be so construed. To the contrary, it will be readily apparent to one of ordinary skill in the art that it is possible to conceive of many embodiments not described above which nevertheless embody the principles and teachings of the invention. The invention should therefore not be limited to what is described above, but instead should be regarded as being fully commensurate in scope with the following claims.

CLAIMS

1. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said identical cells being connected to at least one neighboring cell and responsive to said controller, and adapted to process data from said at least one neighboring cell in accordance with said control signals, said cell including a memory segmented into at least two blocks to be able to perform more than one read/write operation per clock cycle at the direction of said controller.

2. A parallel data processor as claimed in claim 1, wherein said memory is a random access memory.

3. A parallel data processor as claimed in claim 2 wherein said random access memory is divided into four blocks and comprises at least two address busses, at least three read ports, and at least one write port.

4. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said identical cells being connected to at least one neighboring cell and responsive to said controller, and adapted to process data from said at least one neighboring cell in accordance with said control signals, said cell including a memory having at least two ports to be able to perform more than one read/write operation per clock cycle at the direction of said controller.

5. A parallel data processor as claimed in claim 4, wherein said memory is a random access memory.

6. A parallel data processor as claimed in claim 5 wherein said random access memory comprises at least three read ports and at least one write port.

7. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said identical cells being connected to at least one neighboring cell and responsive to said controller, and including:

first means, including a full adder, for performing logical and arithmetic operations, and

a plurality of memory means, connected to said controller and said first means, for selectively retaining digital data,

at least one of said memory means being segmented into at least two blocks for performing more than one read/write operation per clock cycle.

8. The parallel data processor of claim 7, wherein said segmented memory means comprises a random access memory.

9. A parallel data processor as claimed in claim 8, wherein said random access memory is divided into four blocks and comprises at least two address busses, at least three read ports, and at least one write port.

10. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said identical cells being connected to at least one neighboring cell and responsive to said controller, and including:

first means, including a full adder, for performing logical and arithmetic operations, and

a plurality of memory means, connected to said controller and said first means, for selectively retaining digital data,

at least one of said memory means having at least two ports for performing more than one read/write operation per clock cycle.

11. The parallel data processor of claim 10, wherein said at least one memory means comprises a random access memory.

12. A parallel data processor as claimed in claim 11, wherein said random access memory has at least three read ports and at least one write port.

13. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said cells being connected to at least one neighboring cell and responsive to said controller, and including:

first means for carrying out logical algorithms; and

second means, responsive to said controller, for selectively generating an indication of whether the said first means is currently engaged in carrying out said algorithms.

14. A parallel data processor as claimed in claim 13, wherein each cell further includes third means for generating a signal to be logically combined with similar signals from other cells to generate a global signal, and wherein said second means is further for selectively disabling said third means so that said cell does not contribute to said global signal.

15. A parallel data processor as claimed in claim 13, wherein each cell includes memory means for selectively retaining and retrieving digital data, and wherein said second means is further for selectively inhibiting storage in said memory means.

16. A parallel data processor as claimed in claim 13, wherein said second means is further responsive to said first means, and is further for generating said indication in response to a signal generated by either of said controller and said first means.

17. A parallel data processor as claimed in claim 13, wherein said second means is individually addressable by said controller.

18. A parallel data processor comprising:

a controller for generating control signals; and

a plurality of identical cells, each of said cells being connected to at least one neighboring cell and responsive to said controller, and including:

at least two data registers for storing digital data, and

first means, responsive to said data registers and said controller, for conditionally carrying out preliminary operations on digital data from said data registers, and

second means, responsive to said first means, for carrying out arithmetic and logical functions on digital data from said first means.

19. A parallel data processor as claimed in claim 18, wherein said second means comprises a full adder.

20. A parallel data processor as claimed in claim 18, wherein said at least two data registers comprise a first data register and a second data register, and wherein said first means includes:

a first logic gate having a first input terminal connected to said first data register;

a second logic gate having a first terminal connected to said second data register;

first selecting means, responsive to said controller, and connected to an output terminal of said first data register and said first logic gate, for selecting one of the output the first data register and the output of the first logic gate;

second selecting means, responsive to said controller, and connected to said second data register and to an output terminal of said second logic gate, for selecting one of the output of the second data register and the output of said second logic gate; and

means, connected to a second input terminal of said first logic gate and to a second input terminal of said second logic gate, for generating a control value.

21. A parallel data processor as claimed in claim 20, wherein said control value generating means comprises:

a third data register connected to said second input terminal of said first logic gate and said second input terminal of said second logic gate; and

third selecting means, responsive to said controller, for selecting as an output to said third data register one of an externally-applied signal and the contents of said third data register.

22. A parallel data processor as claimed in claim 21, wherein said second means comprises a full adder having first and second data input terminals, and wherein an output of said first selecting means is connected to said first data input terminal, and an output of said second selecting means is connected to said second data input terminal.

23. A parallel data processor comprising:

a controller for generating control signals;

an n x m array of identical cells, n and m being positive integers, each of said cells being connected to at least one neighboring cell; and

n selecting means, respectively connected and responsive to n edge cells of said n x m array, for selectively connecting an associated one of said edge cells to one of at least two external I/O devices in response to said control signals.

24. A parallel data processor comprising:

a controller for generating control signals;

a plurality of identical cells each responsive to said control and selectively interconnected to other cells of said plurality to form a cell array; and

bypass means responsive to said controller and interconnected between predetermined cells of said array

for selectively establishing data paths bypassing portions of said array.

25. A parallel data processor as claimed in claim 24, wherein said bypass means comprises a plurality of multiplexer/demultiplexers respectively connected between said portions of said array.

26. A parallel data processor as claimed in claim 24, wherein said array is arranged in rows and columns, and wherein said bypass means is arranged for selectively bypassing selected rows and columns.

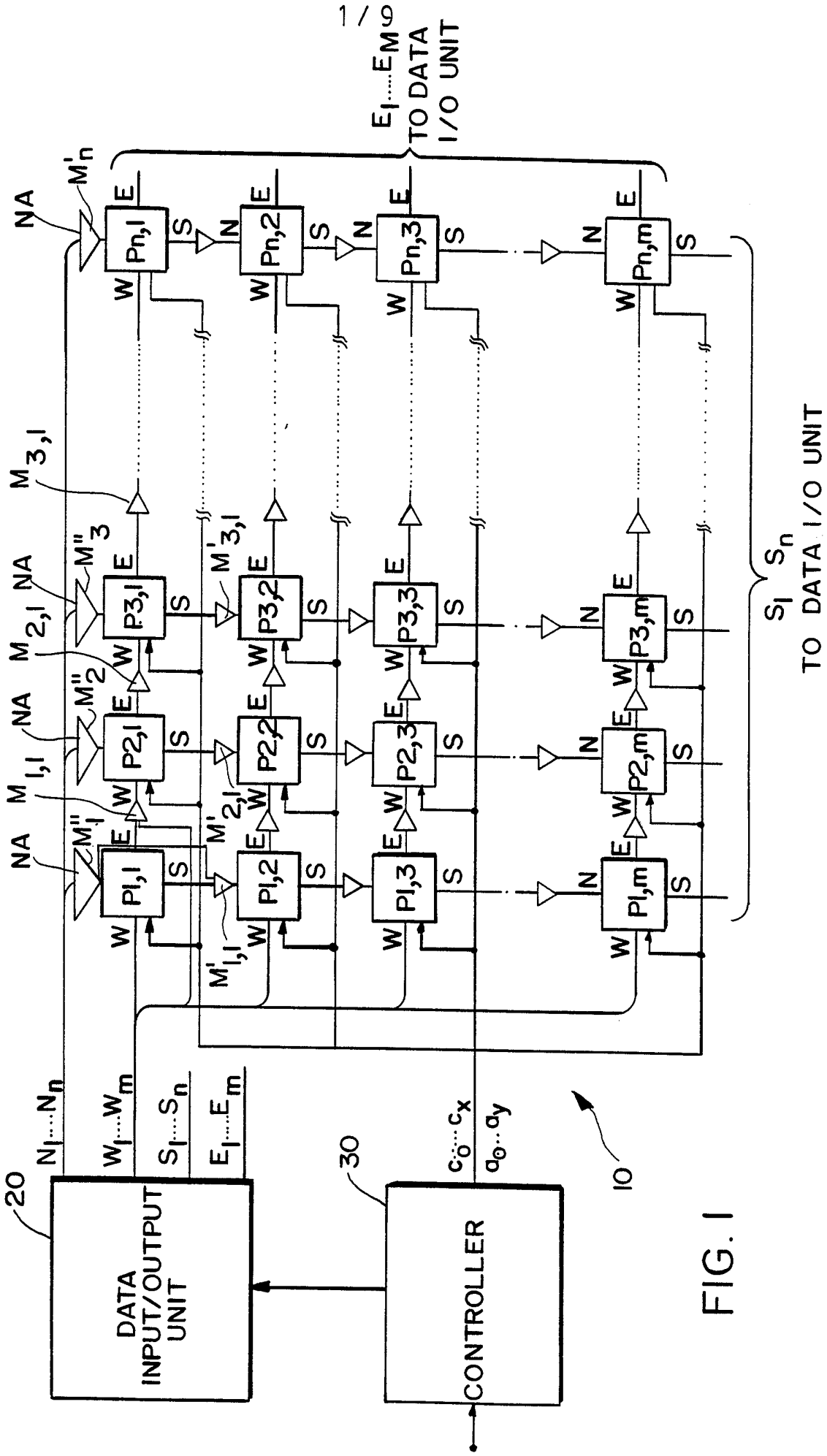

E1....EM
TO DATA I/O UNIT
NA
M'n
Pn,1
Pn,2
Pn,3
Pn,m
M3,1
M"3
M'3,1
P3,1
P3,2
P3,3
P3,m
M2,1
M"2
M'2,1
P2,1
P2,2
P2,3
P2,m
M1,1
M"1
M'1,1
P1,1
P1,2
P1,3
P1,m
E W N S
Sn
S1
TO DATA I/O UNIT
N1....Nn
W1....Wm
S1....Sn
E1....Em
c0....cx
a0....ay
20
30
10
DATA INPUT/OUTPUT UNIT
CONTROLLER

FIG. 1

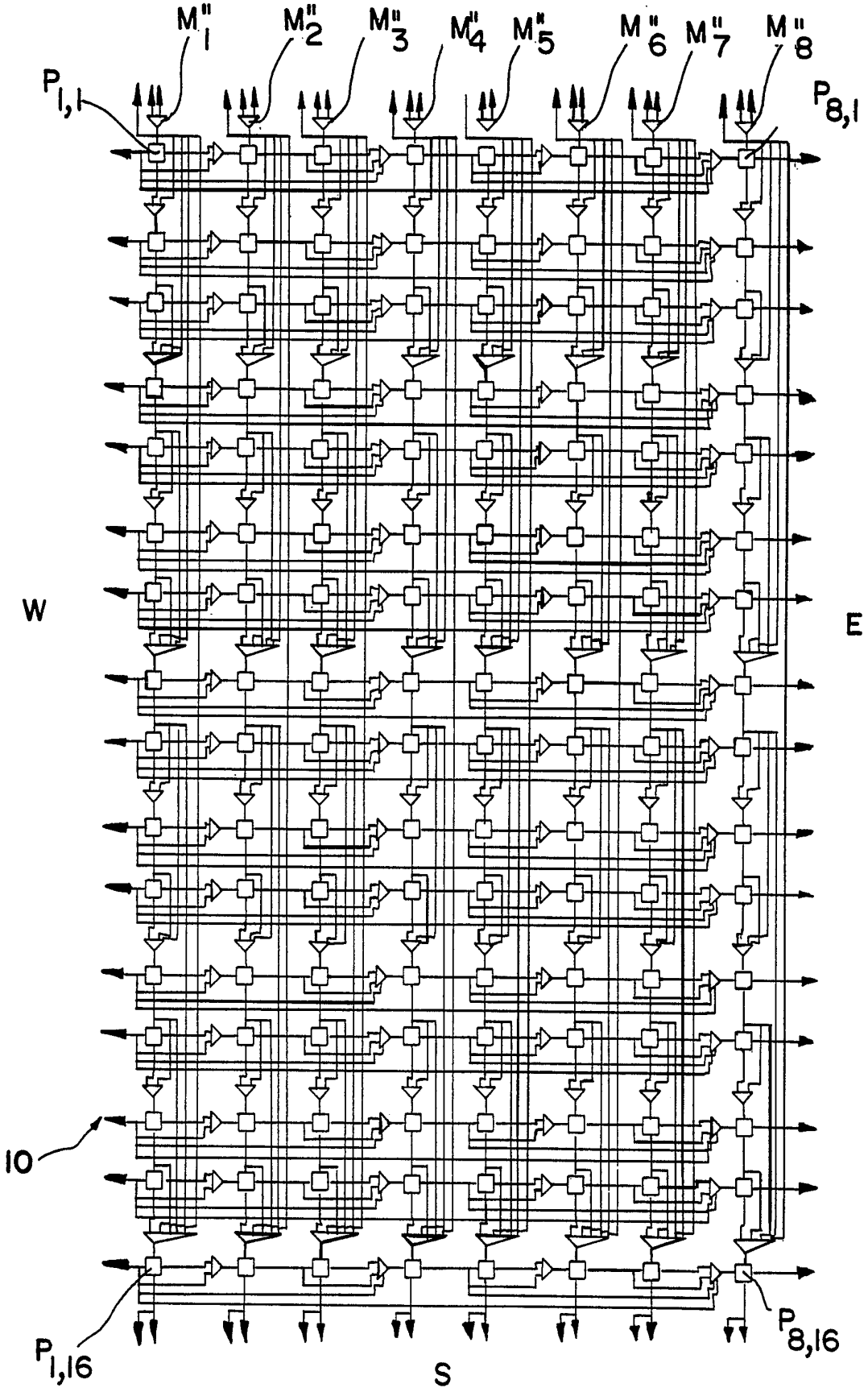


FIG. 2

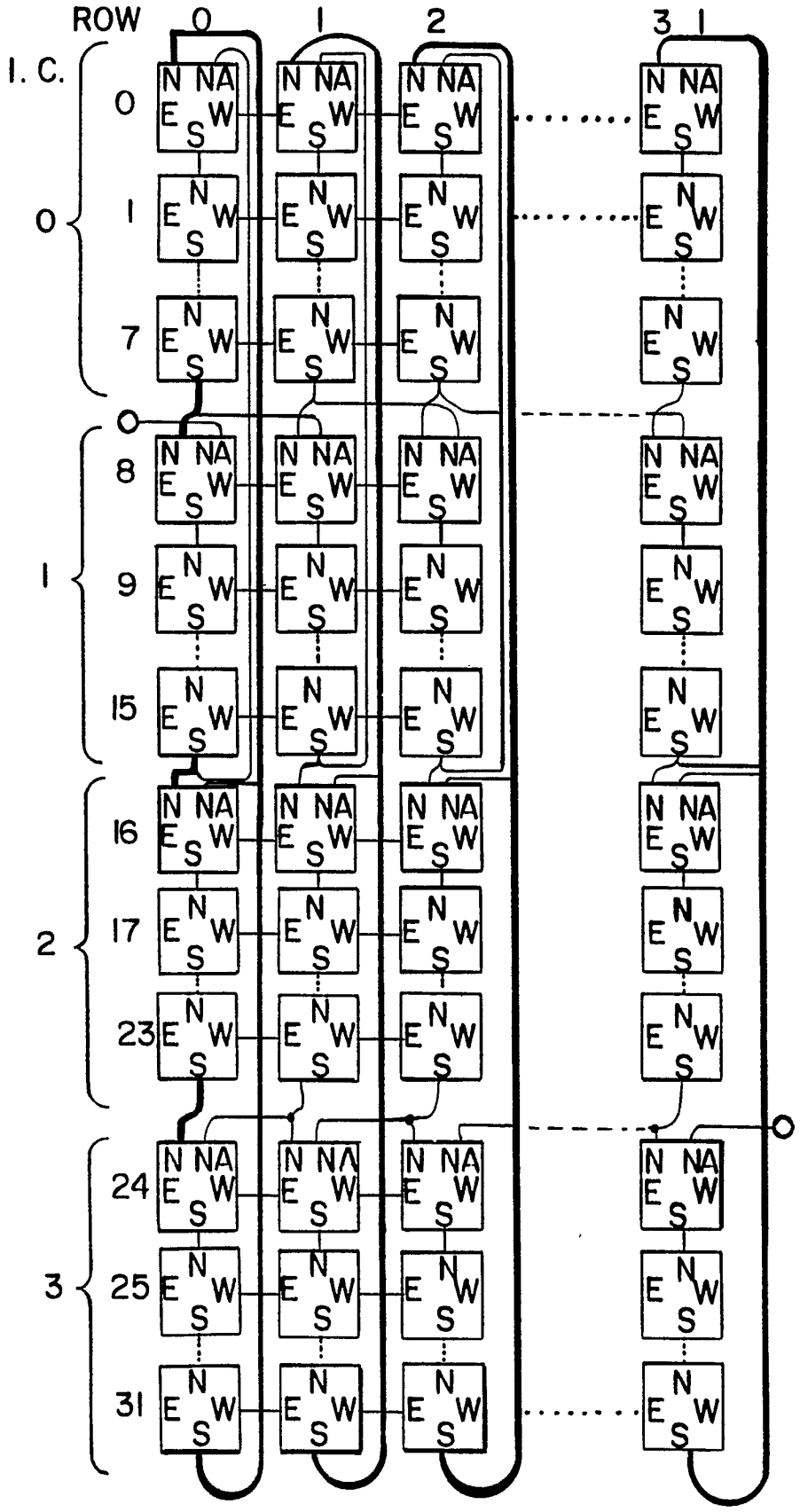


FIG. 3a

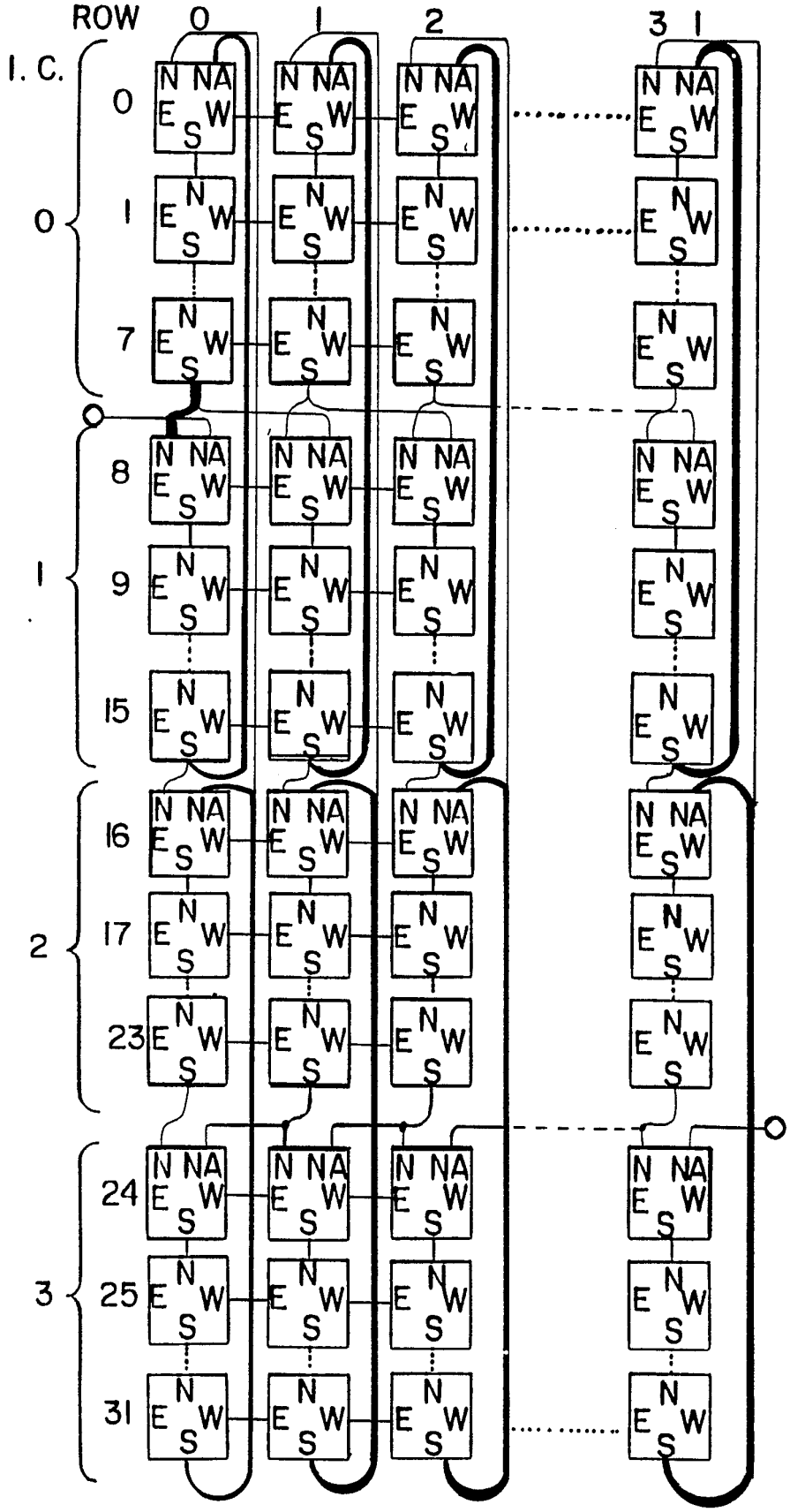


FIG. 3b

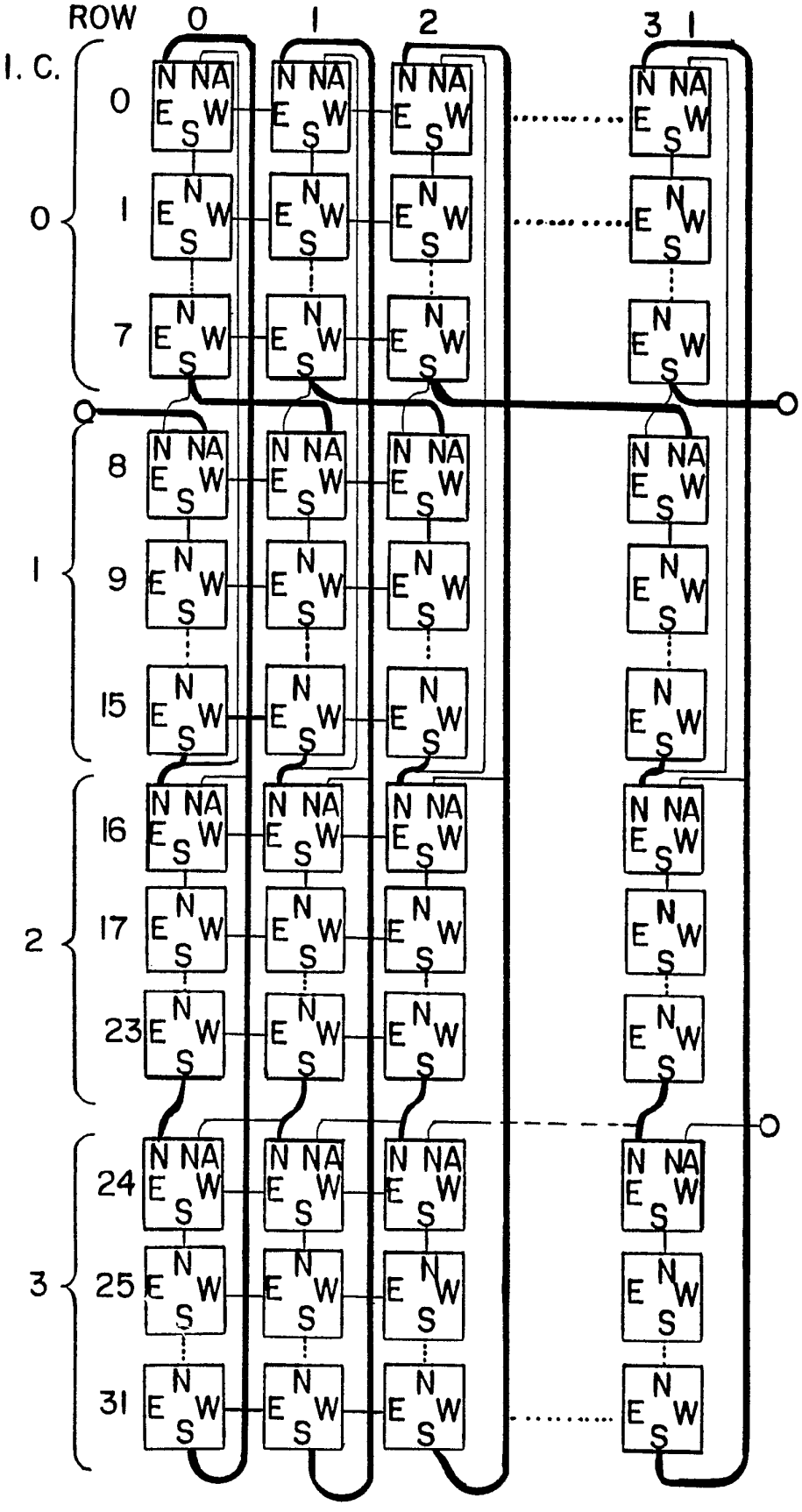


FIG. 3c

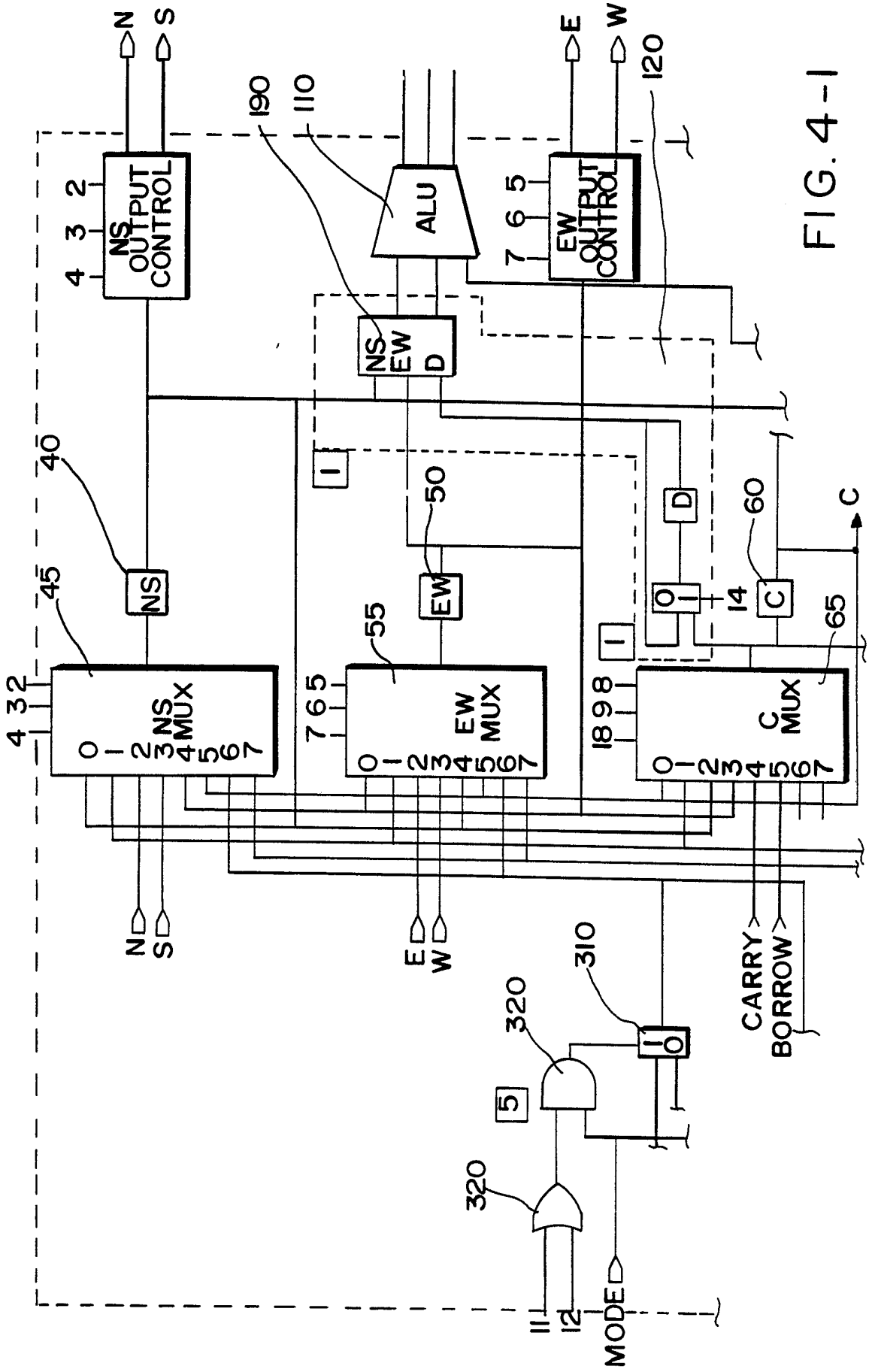

N
S
E
W
190
110
120
NS OUTPUT CONTROL
ALU
EW OUTPUT CONTROL
NS EW D
40
50
60
C
45
55
65
NS
EW
D
C
NS MUX
EW MUX
C MUX
14
N
S
E
W
CARRY
BORROW
310
320
320
5
11
12
MODE

FIG. 4-1

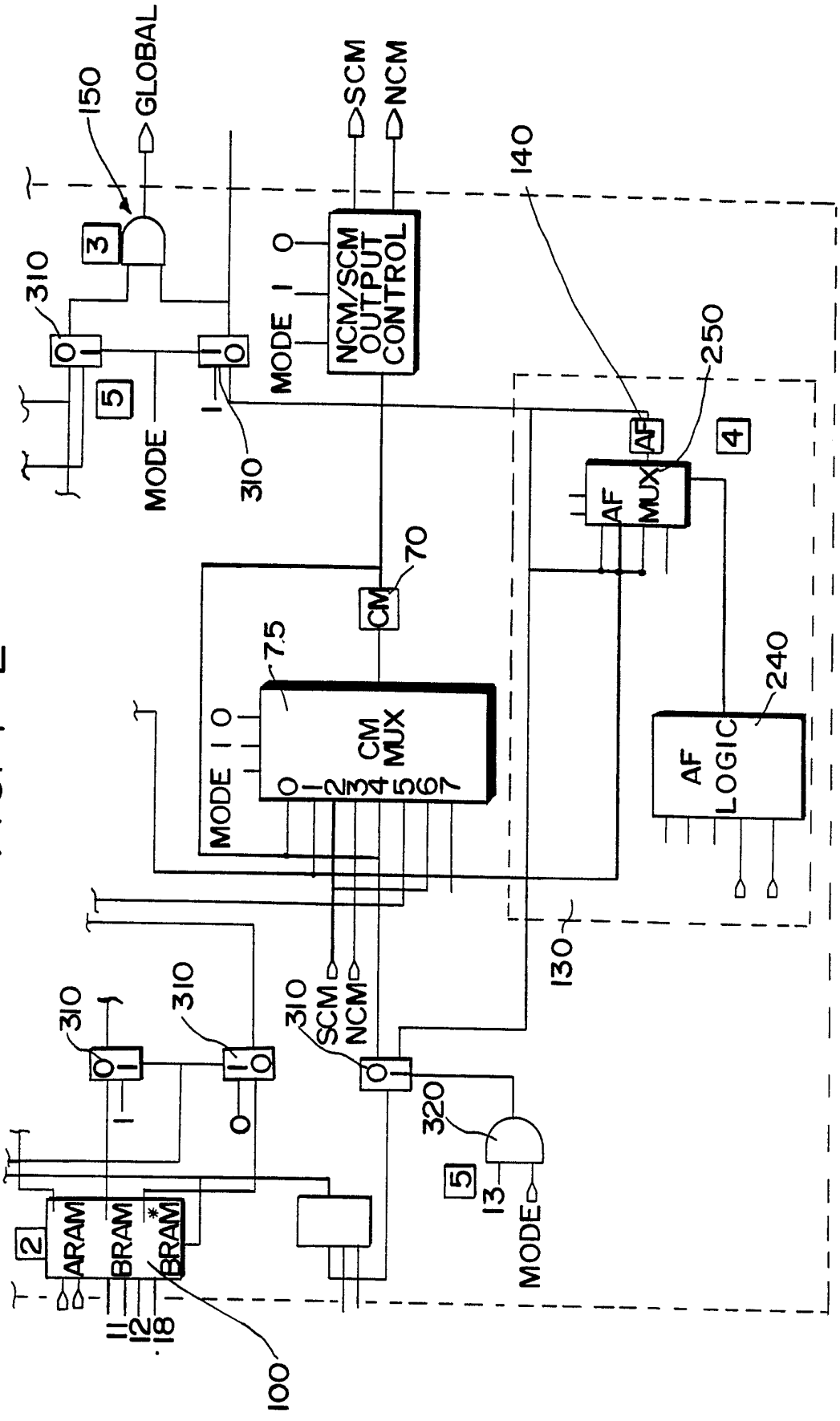

GLOBAL
150
SCM
NCM
140
NCM/SCM OUTPUT CONTROL
MODE 1 0
310
MODE
AF
250
AF MUX
4
CM
70
75
CM MUX
MODE 1 0
0 1 2 3 4 5 6 7
AF LOGIC
240
130
320
13
MODE
ARAM
BRAM
BRAM*
2
11
12
18
100

FIG. 4-2

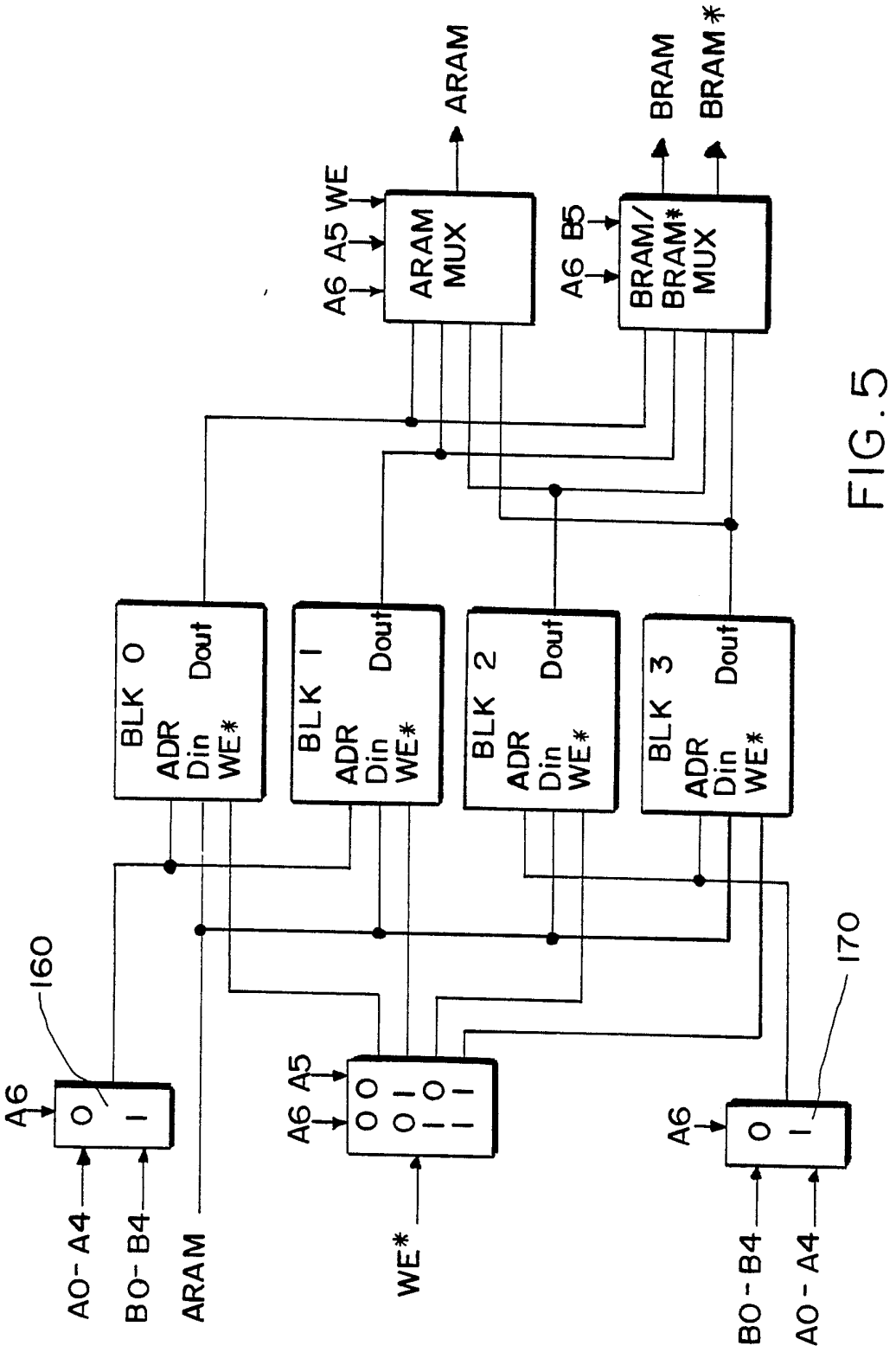

ARAM
BRAM
BRAM*
A6 A5 WE
ARAM MUX
A6 B5
BRAM/ BRAM* MUX
BLK 0
BLK 1
BLK 2
BLK 3
ADR
Din
WE*
Dout
160
170
A6
A5
A0- A4
B0- B4
ARAM
WE*
B0 - B4
A0 - A4

FIG. 5

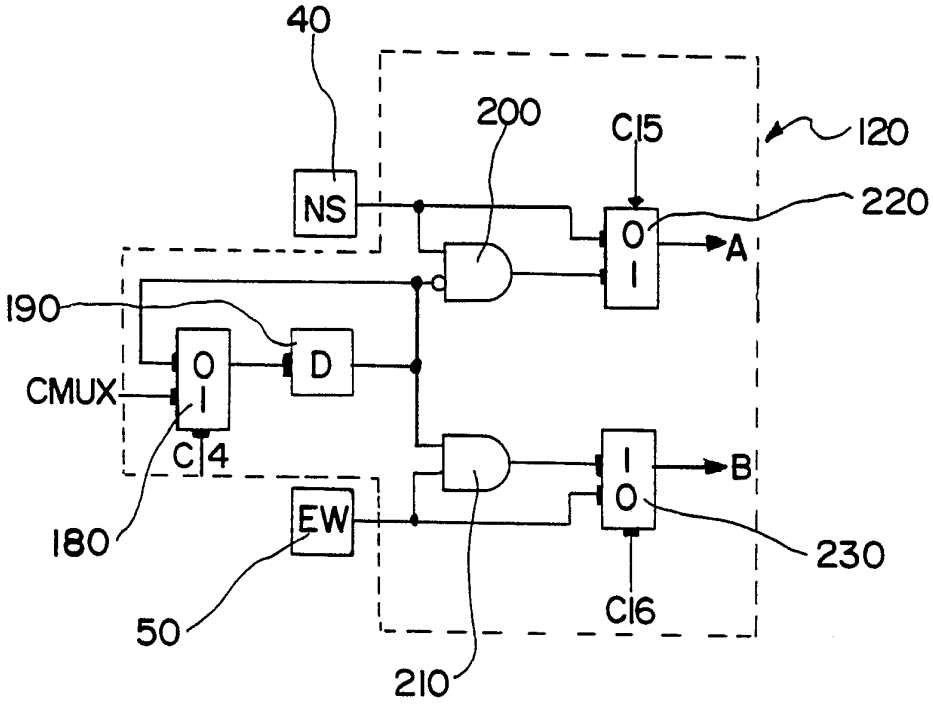

40
200
C15
120
NS
220
0
1
A
190
D
CMUX
0
1
C14
1
0
B
180
EW
230
50
C16
210

FIG. 6

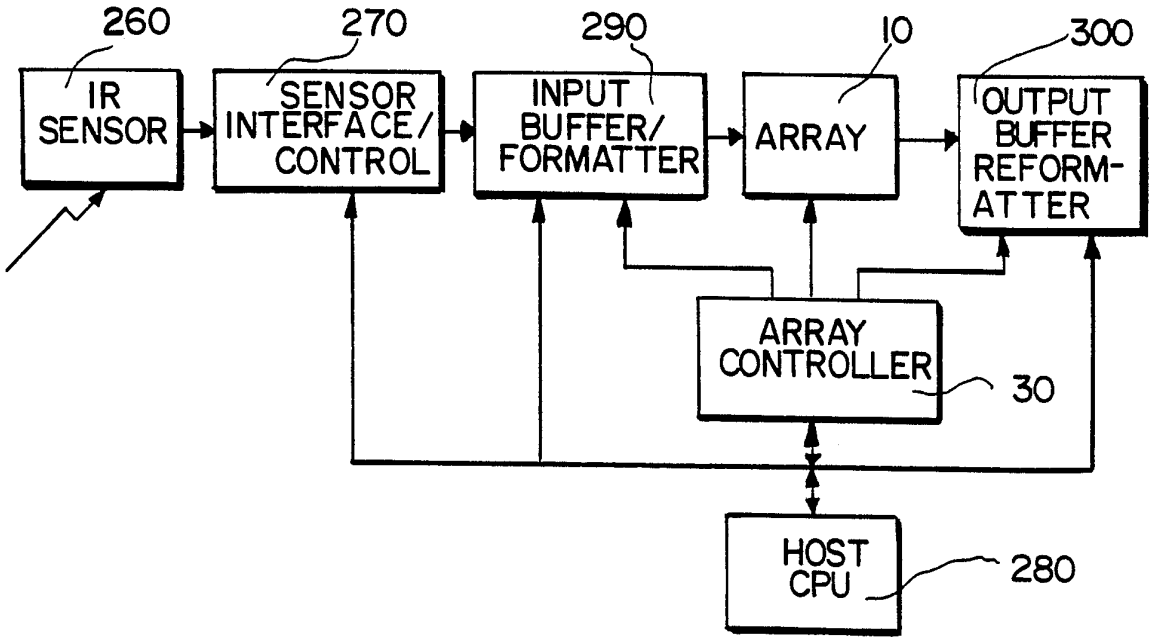

260
270
290
10
300
IR SENSOR
SENSOR INTERFACE/ CONTROL
INPUT BUFFER/ FORMATTER
ARRAY
OUTPUT BUFFER REFORM- ATTER
ARRAY CONTROLLER
30
HOST CPU
280

FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 89/04281

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: G 06 F 15/80

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	G 06 F 15

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	EP, A, 0223690 (INT. STANDARD ELECTRIC CORP.) 27 May 1987, see figures 1-4; page 1, line 1 - page 3, line 30; page 4, line 17 - page 5, line 27; page 7, line 16 - page 8, line 36; page 18, line 20 - page 19, line 27	1-13
Y		23-26
A		14-22
	--	
Y	Digital Processes, vol. 3, no. 2, 1977, Georg Publishing Company (CH) J. Rochez: "Calculateur cellulaire universel destiné à l'étude des structures cellulaires spécialisées" pages 121-138, see figure 4; page 127, lines 3-10	23
	--	
Y	Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers, 6-9 October 1986, New York, IEEE (New York, US)	24-26

./.

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22nd January 1990	21. 02. 90
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	T.K. WILLIS

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	P. Franzon: "Interconnect strategies for fault tolerant 2D VLSI arrays" pages 230-233, see figure 4; page 231, left-hand column, lines 7-37 --	
A	EP, A, 0237218 (THINKING MACHINES CORP.) 16 September 1987, see figures 1,2; page 3, line 15 - page 7, line 3 --	1-14
A	US, A, 3287703 (SLOTNICK) 22 November 1966, see figures 1-3; column 1, line 9 - column 4, line 38 --	1,7
A	WO, A, 86/03038 (HUGHES AIRCRAFT CO.) 22 May 1986, see figure 12; page 23, lines 6-31 --	3,6,9,12
A	US, A, 4314349 (BATCHER) 2 February 1982, see figures 1,2; column 3, line 15 - column 4, line 68	7,10,24

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8904281 SA 31861

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/02/90 The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0223690	27-05-87	AU-B- 588394	14-09-89
		AU-A- 6483486	21-05-87
		JP-A- 62119675	30-05-87
EP-A- 0237218	16-09-87	US-A- 4773038	20-09-88
		JP-A- 62264357	17-11-87
US-A- 327703		None	
WO-A- 8603038	22-05-86	EP-A- 0199757	05-11-86
		JP-T- 62500750	26-03-87
		US-A- 4837676	06-06-89
US-A- 4314349	02-02-82	CA-A- 1154168	20-09-83
		CA-A- 1165005	03-04-84
		DE-A,C 3049437	24-09-81
		FR-A- 2472784	03-07-81
		GB-A,B 2062915	28-05-81
		GB-A,B 2140589	28-11-84
		JP-A- 56101262	13-08-81