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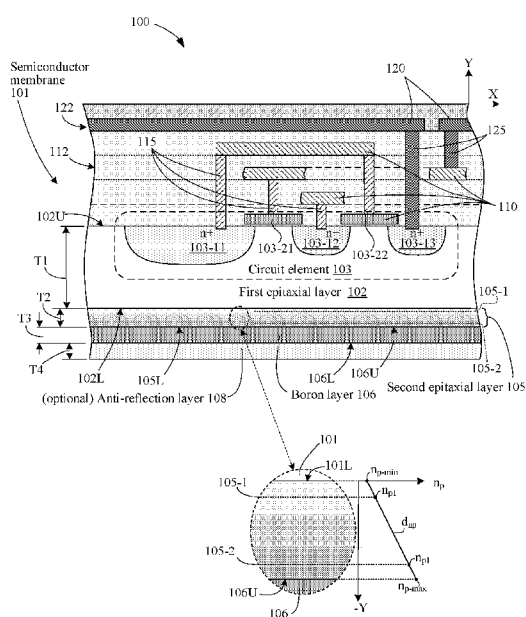


Figure 1

(57) Abstract: An image sensor utilizes a pure boron layer and a second epitaxial layer having a p-type dopant concentration gradient to enhance sensing DUV, VUV or EUV radiation. Sensing (circuit) elements and associated metal interconnects are fabricated on an upper surface of a first epitaxial layer, then the second epitaxial layer is formed on a lower surface of the first epitaxial layer, and then a pure boron layer is formed on the second epitaxial layer. The p-type dopant concentration gradient is generated by systematically increasing a concentration of p-type dopant in the gas used during deposition/growth of the second epitaxial layer such that a lowest p-type dopant concentration of the second epitaxial layer occurs immediately adjacent to the interface with the first epitaxial layer, and such that a highest p-type dopant concentration of the second epitaxial layer occurs immediately adjacent to the interface with pure boron layer.

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BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR

Related Applications/Patents

[0001] This application claims priority from U.S. Provisional Patent Application No. 62/778,445, entitled "BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR", which was filed on December 12, 2018, and is incorporated by reference herein. This application also is related to U.S. Patent Nos. 9,496,425, 9,818,887 and 10,121,914, all to Chern et al., and all entitled "Back-illuminated sensor with boron layer". These patents and applications are incorporated herein by reference.

Field of the Disclosure

[0002] The present application relates to image sensors suitable for sensing radiation in deep UV (DUV) and vacuum UV (VUV) wavelengths, and to methods for making such image sensors. These sensors are suitable for use in photomask, reticle, or wafer inspection systems and for other applications.

Related Art

[0003] The following description and examples are not admitted to be prior art by virtue of their inclusion in this section.

[0004] The integrated circuit industry requires inspection tools with increasingly higher resolution to resolve ever smaller features of integrated circuits, photomasks, reticles, solar cells, charge coupled devices etc., as well as detect defects whose sizes are of the order of, or smaller than, those feature sizes.

[0005] Inspection systems operating at short wavelengths, e.g. wavelengths shorter than about 250 nm, can provide such resolution in many cases. In particular for photomask or reticle inspection, it is desirable to inspect using a wavelength identical, or close, to the wavelength that will be used for lithography, i.e. close to 193.4 nm for current generation lithography and close to 13.5 nm for future EUV lithography, as the phase-shifts of the inspection light caused by the patterns will be identical or very similar to those caused during lithography. For inspecting semiconductor patterned wafers, inspection systems operating over a relatively broad range of wavelengths, such as a wavelength range that includes wavelengths in the near UV, DUV, and/or VUV ranges, can be advantageous because a broad range of wavelengths can reduce the sensitivity to small changes in layer thicknesses or pattern dimensions that can cause large changes in reflectivity at an individual wavelength.

[0006] In order to detect small defects or particles on photomasks, reticles, and semiconductor wafers, high signal-to-noise ratios are required. High photon flux densities are required to ensure high signal-to-noise ratios when inspecting at high speed because statistical fluctuations in the numbers of photons detected (Poisson noise) is a fundamental limit on the signal-to-noise ratio. In many cases, approximately 100,000 or more photons per pixel are needed. Because inspection systems are typically in use 24 hours per day with only short stoppages, the sensors are exposed to large doses of radiation after only a few months of operation.

[0007] A photon with a vacuum wavelength of 250 nm has energy of approximately 5 eV. The bandgap of silicon dioxide is about

10 eV. Although it may appear such wavelength photons cannot be absorbed by silicon dioxide, silicon dioxide as grown on a silicon surface must have some dangling bonds at the interface with the silicon because the silicon dioxide structure cannot perfectly match that of the silicon crystal. In addition, because the single dioxide is amorphous, there will be dangling bonds within the material. In practice, there will be a non-negligible density of defects and impurities within the oxide, as well as at the interface to underlying semiconductor, that can absorb photons with DUV wavelengths, particularly those shorter than about 220 nm in wavelength. Furthermore, under high radiation flux density, two high-energy photons may arrive near the same location within a very short time interval (nanoseconds or picoseconds), which can lead to electrons being excited to the conduction band of the silicon dioxide by two absorption events in rapid succession or by two-photon absorption.

[0008] A further requirement for sensors used for inspection, metrology and related applications is high sensitivity. As explained above, high signal-to-noise ratios are required. If the sensor does not convert a large fraction of the incident photons into signal, then a higher intensity light source would be required in order to maintain the same inspection or measurement speed compared with an inspection or metrology system with a more efficient sensor. A higher intensity light source would expose the instruments optics and the sample being inspected or measured to higher light intensities, possibly causing damage or degradation over time. A higher intensity light source would also be more expensive or, particularly at DUV and VUV wavelengths, may not be available. Silicon reflects a high percentage of DUV and VUV light incident on it. For example, near 193 nm in wavelength, silicon with a 2 nm oxide layer on its

surface (such as a native oxide layer) reflects approximately 65% of the light incident on it. Growing an oxide layer of about 21nm on the silicon surface reduces the reflectivity to close to 40% for wavelengths near 193 nm. A detector with 40% reflectivity is significantly more efficient than one with 65% reflectivity, but lower reflectivity, and hence higher efficiency, is desirable.

[0009] Anti-reflection coatings are commonly used on optical elements such as lenses and mirrors. However, many coating materials and processes commonly used for optical elements are often not compatible with silicon-based sensors. For example, electron and ion-assisted deposition techniques are commonly used for optical coatings. Such coating processes cannot generally be used to coat semiconductor devices because the electrons or ions can deposit sufficient charge on the surface of the semiconductor device to cause electrical breakdown resulting in damage to the circuits fabricated on the semiconductor.

[0010] DUV and VUV wavelengths are strongly absorbed by silicon. Such wavelengths may be mostly absorbed within about 10 nm or a few tens of nm of the surface of the silicon. The efficiency of a sensor operating at DUV or VUV wavelengths depends on how large a fraction of the electrons created by the absorbed photons can be collected before the electrons recombine. Silicon dioxide can form a high-quality interface with silicon with a low density of defects. Most other materials including many of those commonly used for anti-reflection coatings, if deposited directly on silicon, result in a very high density of electrical defects at the surface of silicon. A high density of electrical defects on the surface of silicon may not be an issue for a sensor intended to operate at visible wavelengths, as such wavelengths may typically travel about 100 nm or more into the

silicon before being absorbed and may, therefore, be little affected by electrical defects on the silicon surface. However, DUV and VUV wavelengths are absorbed so close to the silicon surface that electrical defects on the surface and/or trapped charged within the layer(s) on the surface can result in a significant fraction of the electrons created recombining at, or near, the silicon surface and being lost, resulting in a low efficiency sensor.

[0011] U.S. Patents 9,496,425, 9,818,887 and 10,121,914, all to Chern et al., describe image sensor structures and methods of making image sensors that include a boron layer deposited on, at least, an exposed back surface of the image sensor. Different ranges of temperature for deposition of the boron are disclosed, including a range of about 400-450°C and a range of about 700-800°C. The inventors have discovered that one advantage of a higher deposition temperature for the boron, such as a deposition temperature between about 600°C and about 900°C, is that at such temperatures boron diffuses into the silicon providing a very thin, heavily p-type doped silicon layer on the light-sensitive back surface. This p-type doped silicon layer is important for ensuring a high quantum efficiency to DUV and VUV radiation because it creates a static electric field near the surface that accelerates electrons away from the surface into the silicon layer. The p-type silicon also increases the conductivity of the back surface of the silicon, which is important for high-speed operation of an image sensor, since a return path is needed for ground currents induced by the switching of signals on electrodes on the front surface of the sensor.

[0012] However, processing temperatures higher than 450°C cannot be used on semiconductor wafers that include conventional

CMOS circuits because 450°C is close to the melting point metals such as aluminum and copper commonly used in fabricating CMOS devices. At high temperatures, such as those greater than 450°C, these metals expand, become soft and can delaminate. Furthermore, at high temperatures copper can easily diffuse through silicon which will modify the electrical properties of the CMOS circuits. Thinning a wafer before any metals are deposited on it allows a boron layer to be deposited on the back surface as described in the aforementioned patents at a temperature between 600 and 900°C enabling boron to diffuse into the surface during, or subsequent to, the deposition of the boron layer. Subsequently metal interconnects can be formed on the front surface. After the image sensor regions of the wafer have been thinned, for example to a thickness of about 25 μm or thinner, the thinned region can be significantly warped and may have peak-to-valley non-flatness of many tens of microns or more. So, it is necessary to use relatively wide metal interconnect lines and vias, such as multiple microns wide or more, to ensure that the lines and vias connect in spite of any misalignment caused by the non-flatness. Such wide metal interconnects and vias increase the capacitance per unit area associated with those lines and vias. Furthermore, wide interconnects and vias can make it difficult, or impossible, to interconnect all the signals on a large area sensor with about one million or more pixels. In some cases, polysilicon jumpers may be needed to connect together metal interconnects, but polysilicon has much higher resistivity than any metal, so the use of such jumpers can limit the maximum operating speed of a sensor.

[0013] US patent 5,376,810 to Hoenk et al. describes a delta-doping technique for image sensors that may be performed at a temperature of 450°C or lower. This technique includes a 1.5 nm

cap layer of nominally undoped silicon. This cap layer may be deliberately oxidized or may oxidize due to water and oxygen in the environment. This oxide layer will degrade under high intensity DUV, VUV, EUV or charged-particle radiation and can cause the sensor to degrade.

[0014] Therefore, a need arises for an image sensor capable of efficiently detecting high-energy photons without degrading yet overcoming some, or all, of the above disadvantages. In particular, a method of fabricating a back-thinned image sensor with a boron layer and boron doping on its back surface while allowing formation of metal interconnects on a relatively flat wafer (i.e. with a flatness of about 10 μm or less) would allow the use of finer design rules (such as the design rules corresponding to a 0.35 μm process or finer). Such a method would allow narrower metal lines connecting to critical features such as the floating diffusion, enabling smaller floating-diffusion capacitance and higher charge to voltage conversions ratios. Finer design rules also allow more interconnect lines per unit area of the sensor and allow more flexibility in connecting the circuits on the image sensor.

SUMMARY OF THE DISCLOSURE

[0015] Image sensors and methods of fabricating image sensors with high-quantum-efficiency for imaging DUV, VUV, EUV, X-rays and/or charged particles (such as electrons) are described. These image sensors are capable of long-life operation under high fluxes of radiation. These methods include process steps to form light sensitive active and/or passive circuit elements in a layer on a semiconductor (preferably silicon) wafer, as well as forming metal interconnections between the electrical elements of the sensor. These image sensors can include fine metal interconnects

and vias (such as those conforming to about 0.35 μm , or finer, design rules), while having a backside surface coated with an amorphous boron layer and having a highly doped p-type silicon layer immediately adjacent to the boron layer. The metal interconnections may comprise tungsten, aluminum, copper or other metals used in fabricating interconnects in known CMOS processes.

[0016] An exemplary method of fabricating an image sensor includes forming a first epitaxial silicon layer on a substrate, forming a gate layer on the first epitaxial silicon layer, the gate layer comprising one or more layers of dielectric materials such as silicon dioxide and silicon nitride, forming circuit elements on the gate layer comprising poly-silicon and dielectric materials, forming metal vias and metal interconnects to connect together at least some of those circuit elements, thinning the substrate to expose at least a portion of the first epitaxial silicon layer (the exposed first epitaxial silicon layer is referred to herein as a semiconductor membrane), growing a second epitaxial silicon layer directly on the exposed portions of the first epitaxial layer, the second epitaxial silicon layer incorporating a concentration gradient of a p-type dopant such as boron, forming an amorphous pure boron layer directly on the surface of the second epitaxial silicon layer, and optionally forming one, or more, anti-reflection layers directly on the surface of the amorphous boron layer. As used herein, the phrase "circuit elements" refers to light sensitive devices such as charge-coupled devices and photodiodes, other semiconductor devices such as transistors, diodes, resistors and capacitors, and electrical interconnections (often called metal interconnects or interconnects) between them. These circuit elements are formed using standard semiconductor manufacturing processes including, but not limited to, photolithography, deposition,

etching, ion implantation and annealing. The second epitaxial silicon layer may comprise an epitaxial silicon layer with a low concentration of the p-type dopant adjacent to the surface of the first epitaxial silicon layer and high concentration of the p-type dopant adjacent to the pure boron layer. The second epitaxial silicon layer may be formed by molecular-beam epitaxy (MBE). Thinning the substrate (e.g. a wafer) can be performed using reactive-ion etching, chemical etching and/or polishing. Notably, this thinning can increase the sensitivity of the image sensor to light impinging the back surface. An anti-reflection coating may be formed on the boron layer. Alternatively, a thin metal coating may be deposited on the boron layer. The thin metal coating may be particularly useful when the sensor is used to detect charged particles (such as electrons), EUV or X-rays. Such a thin metal coating may reduce to sensitivity of the sensor to stray light, may protect the surface of the sensor, and may facilitate **in-situ** cleaning of contaminants, such as carbon and organic molecules from the sensor surface.

[0017] Another method of fabricating an image sensor includes forming a first epitaxial silicon layer on a substrate, then forming circuit elements on the first epitaxial silicon layer. This step includes forming metal interconnects. The metal interconnects may comprise tungsten, molybdenum, aluminum, copper or another metal. A protective layer may be formed on the circuit elements. A handle wafer may be bonded to the surface that includes the circuit elements. The substrate is then thinned to expose, at least part of, the first epitaxial silicon layer. As indicated above, this thinning can increase the sensitivity of the image sensor to light impinging on the back surface. A second epitaxial silicon layer is grown on the exposed surface of the semiconductor membrane. The second

epitaxial layer is doped with a p-type dopant such as a boron. The second epitaxial silicon layer may be grown at a temperature less than or about 450°C. The p-type dopant may be incorporated into the second epitaxial silicon layer during growth of that layer by including a dopant (such as boron) or a dopant precursor (such as diborane) in a growth chamber during a growth process. The partial pressure of the dopant or dopant precursor may be increased over time as the second epitaxial silicon layer grows thereby forming a dopant concentration profile within the second epitaxial silicon layer that is highest at the outer surface of the second epitaxial silicon layer and lowest at surface immediately adjacent to the first epitaxial silicon layer. A pure boron layer is formed on the surface of the p-type doped epitaxial silicon layer. The pure boron layer may be deposited at a temperature between about 300°C and about 450°C. An anti-reflection coating may be formed on the boron layer. The anti-reflection coating may be formed by an atomic-layer deposition (ALD) or other process. Alternatively, a thin metal coating may be deposited on the boron layer. The thin metal coating may be particularly useful when the sensor is used to detect charged particles (such as electrons), EUV or X-rays. Such a thin metal coating may reduce to sensitivity of the sensor to stray light, may protect the surface of the sensor, and may facilitate **in-situ** cleaning of contaminants, such as carbon and organic molecules from the sensor surface.

[0018] Image sensors with high-quantum-efficiency and long-life operation for DUV, VUV, EUV and/or X-ray radiation are described. These image sensors are thinned from the back-side to expose at least a portion of a first epitaxial silicon layer so that they are highly sensitive to radiation impinging on the back-side of the image sensors (wherein these image sensors are

back-illuminated). A second epitaxial silicon layer is grown directly on the exposed back surface of the first epitaxial silicon layer. The second epitaxial silicon layer is **in-situ** doped with a p-type dopant such that the concentration of the p-type dopant increases away from the surface of the first epitaxial layer. A thin (e.g. between about 2 nm and about 20 nm thick), high-purity, amorphous boron layer is deposited on the second epitaxial silicon layer. In some embodiments, one or more additional layers of material may be coated on the boron. The thickness and material of each layer may be chosen to increase the transmission of a wavelength of interest into the image sensor, and/or to protect the boron layer from damage.

[0019] The image sensors described herein may be fabricated using CCD (charge coupled device) or CMOS (complementary metal oxide semiconductor) technology. The image sensors may be two-dimensional area sensors, or one-dimensional array sensors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Figure 1 is a cross-sectional view showing an exemplary image sensor produced in accordance with the present invention.

[0021] Figure 2 illustrates an exemplary technique for fabricating an image sensor.

[0022] Figures 3A, 3B and 3C illustrate an exemplary method for fabricating an image sensor.

[0023] Figures 4A, 4B, 4C, 4D, 4E, 4F, 4G and 4H illustrate exemplary cross-sections of a portion of a wafer subjected to the method described in reference to Figure 2.

[0024] Figure 5 illustrates an exemplary detector assembly incorporating an image sensor, a silicon interposer, and other electronics.

DETAILED DESCRIPTION OF THE DRAWINGS

[0025] Although claimed subject matter will be described in terms of certain embodiments, other embodiments, including embodiments that do not provide all of the benefits and features set forth herein, are also within the scope of this disclosure. Various structural, logical, process step, and electronic changes may be made without departing from the scope of the disclosure. Accordingly, the scope of the disclosure is defined only by reference to the appended claims.

[0026] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure as provided in the context of a particular application and its requirements. As used herein, directional terms such as "top," "bottom," "front," "back," "over," "under," "upper," "upward," "lower," "down," and "downward" are intended to provide relative positions for purposes of description, and are not intended to designate an absolute frame of reference. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present disclosure is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0027] Fig. 1 is a cross-sectional side view depicting a portion of an image sensor 100 configured to sense deep ultraviolet (DUV) radiation, vacuum ultraviolet (VUV) radiation, extreme ultraviolet (EUV) radiation or charged particles

according to an exemplary embodiment of the present invention. Image sensor 100 includes a semiconductor membrane 101 including a circuit element 103 formed on an upper (first) surface 102U of a first epitaxial layer and metal interconnects 110 and 120 formed over circuit element 103, a second epitaxial layer 105 disposed on a lower (second) surface 101L of first epitaxial layer 101, a pure boron layer 106 disposed on a lower surface 105L of second epitaxial layer 105, and an optional anti-reflection coating 108 disposed on a lower (outward-facing) surface 106L of pure boron layer 106.

[0028] In one embodiment, first epitaxial layer 101 comprises a layer of lightly p-doped epitaxial silicon having a thickness T1 in a range of 10 μm to 40 μm and a p-type (e.g., boron) dopant concentration in a range of about 10^{13} cm^{-3} to 10^{14} cm^{-3} .

[0029] Circuit element 103 includes a sensor device (e.g., a light sensitive device such as a photodiode) and associated control transistors that are formed on (i.e., into and over) an upper (first) surface 101U of first epitaxial layer 101 using known techniques. In the depicted exemplary embodiment, circuit element 103 includes spaced-apart n+ doped diffusion regions 103-11, 103-12 and 103-12 that extend from upper surface 101U into corresponding portions of epitaxial layer 101, and polycrystalline silicon (polysilicon) gate structures 103-21 and 103-22 that are respectively separated from upper surface 101U by intervening gate oxide layers. First metal interconnects 110 and second metal interconnects 120, along with corresponding first metal vias 115 and second metal vias 125, are formed over circuit element 113 and are operably electrically connected to associated regions of circuit element 113 using known techniques. First metal interconnects 110 are formed in or on one or more

dielectric layers 112 deposited over circuit element 113, and first metal vias 115 extend through dielectric layers 112 using known via formation techniques. Second metal interconnects 120 are formed in a second dielectric layer 122 that is disposed over first metal interconnects 110, and second metal vias 125 extend through one or both dielectric layers 112 and 122. In one embodiment, a protection layer (not shown in Fig. 1) is formed between first metal interconnects 110 and second metal interconnects 120, and all second metal vias 125 comprise at least one of aluminum and copper and extend through this protection layer. The exemplary diffusion regions and gate structures forming circuit element 103 depicted in Fig. 1, along with the exemplary metal interconnects 110 and 120 and metal vias 115 and 125, are arbitrarily configured for illustrative purposes and provided solely to for purposes of describing exemplary circuit element structures and is not intended to represent a functional sensor device or to limit the appended claims.

[0030] Second epitaxial layer 101 is disposed on lower surface 101L of first epitaxial layer 101 and has a thickness T_2 in the range of 1nm to 100nm, and more preferably in the range of about 2nm and about 20nm.

[0031] Referring to the bubble located at the bottom of Fig. 1, according to an aspect of the present invention, second epitaxial layer 105 is formed using processing techniques described below such that second epitaxial layer 105 has a p-type dopant concentration gradient d_{np} that systematically increases from a minimum (lowest) p-type doping concentration n_{p-min} at lower surface 102L to a maximum (highest) p-type doping concentration n_{p-max} at upper surface 106U. A benefit gained by simultaneously forming p-type dopant concentration gradient d_{np} and second

epitaxial layer 105 in this manner is the ability to create p-type dopant concentration gradient d_{np} at substantially lower processing temperatures (i.e., about 450°C or lower) than that required to form a similar p-type dopant concentration gradient within first epitaxial layer 101 (i.e., forming a similar gradient by diffusing a p-type dopant into first epitaxial layer 101 requires a processing temperature of at least 700°C, preferably about 800°C or higher), thereby preserving thermal budget and reducing total manufacturing costs by way of facilitating the use of low-cost metallization materials (e.g., aluminum and copper). In addition, forming p-type dopant concentration gradient d_{np} within second epitaxial layer 105 greatly enhances control over the rate at which the p-type dopant concentration changes within gradient d_{np} , which facilitates different gradient patterns (e.g., linear or parabolic) that may be used to further enhance the ability of image sensor (circuit element) 103 to efficiently detect high-energy photons. For example, the exemplary embodiment of Fig. 1 depicts the systematic increase of p-type dopant concentration gradient d_{np} as a continuous linear increase as a function of the negative-Y-axis direction. In other embodiments the gradual increase of p-type dopant concentration gradient d_{np} may be defined by any function of the thickness (negative-Y-axis) direction, such as a continuously curved increase (e.g., the change in doping concentration as a function of layer thickness follows a parabolic curve) or a discontinuous (step-wise) increase by way of varying the introduction of P-type dopant material during the second epitaxial layer formation process. In any case, first-to-be-formed layer portions (i.e., incremental layer portions generated during a given time period that occurs relatively early in the second epitaxial layer formation process) have a lower p-type doping concentration than at least one subsequently formed

layer portion. For example, a p-type dopant concentration n_{p1} of a (first) intermediate layer portion 105-1 of second epitaxial layer 105 is equal to or lower than a p-type dopant concentration n_{p2} of a (second) intermediate layer portion 105-1 of second epitaxial layer 105. When p-type dopant concentration gradient d_{np} varies in a continuously increasing manner relative to thickness (e.g., consistent with the linear function depicted in the example shown in Fig. 1, or based on a parabolically increasing rate), p-type dopant concentration n_{p1} of intermediate layer portion 105-1 is higher (greater) than minimum p-type doping concentration n_{p-min} and p-type dopant concentration n_{p2} of intermediate layer portion 105-2 is lower (less) than maximum p-type doping concentration n_{p-max} . However, when p-type dopant concentration gradient d_{np} varies in a step-wise increasing manner, a particular p-type dopant concentration may remain the same for thickness-wise regions of second epitaxial layer 105 (e.g., p-type dopant concentration n_{p1} of intermediate layer portion 105-1 may be equal to minimum p-type doping concentration n_{p-min}). In an exemplary embodiment, maximum p-type doping concentration n_{p-max} is approximately 10^{20} cm^{-3} , and minimum p-type doping concentration n_{p-min} is greater than or approximately equal to a dopant concentration of first epitaxial layer 101.

[0032] In one embodiment, pure boron layer 106 is formed using techniques described below such that pure boron layer 106 has a thickness T3 in the range of 2 nm and 10 nm. In one embodiment, pure boron layer 106 comprises a boron concentration of 80% or higher, with inter-diffused silicon atoms and oxygen atoms predominantly making up the remaining 20% or less.

[0033] In one specific embodiment, thickness T3 of pure boron layer 106 is in the range of 3 nm to 10 nm, and optional anti-

reflection coating 108 comprises a silicon dioxide layer deposited on a lower (outward-facing) surface 106L of pure boron layer 106.

[0034] Figure 2 illustrates an exemplary technique 200 for fabricating an image sensor. In this embodiment, the circuit elements can be created in step 201 using standard semiconductor processing steps including lithography, deposition, ion implantation, annealing, and etching. In one embodiment, CCD and/or CMOS sensor elements and devices may also be created in step 201. These circuit elements are created in a first epitaxial (epi) layer on the front-side surface of the wafer. In preferred embodiments, the first epitaxial layer is about 10 μm to 40 μm thick. The first epitaxial layer is lightly p (p-) doped. In one embodiment, the first epitaxial layer resistivity is between about 10 and 100 $\Omega\text{ cm}$. Metal interconnects are created in step 201 using any suitable metal including aluminum, copper, tungsten, molybdenum or cobalt. The use of refractory metals, such as tungsten or molybdenum to form first metal interconnects and associated metal vias may allow high temperatures (such as temperatures greater than about 600°C) in subsequent steps, in particular in steps 209 and/or 211. However, when the temperatures in subsequent steps are limited to about 450°C or lower, any convenient metal, including copper and aluminum may be used to form second metal interconnects and associated metal vias.

[0035] In step 203, the front-side surface of the wafer can be protected. This protection may include depositing one or more protective layers on top of the circuit elements formed during step 201. The one or more protective layers may comprise silicon dioxide, silicon nitride or other material. This protection may

include attaching the wafer to a handling wafer, such as a silicon wafer, a quartz wafer, or a wafer made of other material. The handling wafer may include through-wafer vias for connecting to the circuit elements.

[0036] Step 205 involves thinning the wafer from the back-side so as to expose the first epitaxial layer in, at least, the active sensor areas. This step may involve polishing, etching, or both. In some embodiments, the entire wafer is back-thinned. In other embodiments, only the active sensor areas are thinned all the way to the first epitaxial layer.

[0037] Step 207 includes cleaning and preparing the back-side surface prior to deposition of a second epitaxial layer. During this cleaning, the native oxide and any contaminants, including organics and metals, should be removed from the back-side surface. In one embodiment, this cleaning can be performed using a dilute HF solution or using an RCA clean process. After cleaning, the wafer can be dried using the Marangoni drying technique or a similar technique to leave the surface dry and free of water marks.

[0038] In preferred embodiments, the wafer is protected in a controlled environment between steps 207 and 208 (e.g. in a vacuum environment or in an environment purged with a dry, inert gas such as nitrogen) to minimize native oxide regrowth after the cleaning.

[0039] In step 208, a second epitaxial silicon layer is grown (deposited) on, at least, the exposed portion of the first epitaxial layer. In one embodiment the second epitaxial layer is grown by molecular-beam epitaxy (MBE) or other process at a temperature of about 350°C or lower. In another embodiment, the

second epitaxial layer is grown by a chemical vapor deposition (CVD) or plasma-enhanced CVD (PECVD) process at a temperature of about 450°C or lower. As depicted in Figs. 3A to 3C, second epitaxial layer 105A may be grown in a reaction chamber using a gas G containing both silicon and a p-type dopant such as boron, so as to create a p-doped epitaxial silicon layer. Referring to Fig. 3A, early in the deposition process gas G includes a relatively low amount P0 of p-type dopant, whereby a first layer portion 105A0 is formed such that a minimum p-type dopant concentration n_{p-min} is generated adjacent to surface 102L of first epi layer 102. As the deposition progresses, the amount (concentration) of the p-type dopant in gas G is increased according to a selected schedule while maintaining the same amount of silicon such that the p-type dopant concentration in the second epitaxial layer portions disposed further from the first epitaxial layer is increased. For example, as indicated in Fig. 3B, during an intermediate stage of the epitaxial deposition process the deposition process gas G includes an intermediate amount P1 of p-type dopant that is greater than amount P0 used at the point indicated in Fig. 3A, whereby an intermediate layer portion 105A1 is formed with an intermediate p-type dopant concentration n_{p-int} that is greater than minimum p-type dopant concentration n_{p-min} . Similarly, as indicated in Fig. 3C, during a final stage of the epitaxial deposition process the deposition process gas G includes a final amount P2 of p-type dopant that is greater than intermediate amount P1, whereby a final layer portion 105A2 is formed with maximum p-type dopant concentration n_{p-max} that is greater than intermediate p-type dopant concentration n_{p-int} . In alternative embodiments, gas G used to grow the second epitaxial layer may include silicon or boron in elemental form, or may include precursors such as silane for silicon or diborane for boron.

[0040] In step 209, boron is deposited on the surface of the second epitaxial layer. In one preferred embodiment, this deposition can be done using diborane, or a diborane-hydrogen mixture, diluted in nitrogen at a temperature between about 300°C and about 450°C, thereby creating a high-purity amorphous boron layer. In an alternative embodiment, the deposition may be done at a temperature lower than about 350°C, for example, by using a gas containing elemental boron. The thickness of the deposited boron layer depends on the intended application for the sensor. Typically, the boron layer thickness will be between about 2 nm and 20 nm, preferably between about 3 nm and 10 nm. The minimum thickness is set by the need for a pinhole-free uniform film, whereas the maximum thickness depends on the absorption of the photons or charged particles of interest by the boron, as well as the maximum length of time that the wafer can be kept at the deposition temperature.

[0041] More details on depositing boron from diborane gas can be found in "Chemical vapor deposition of a-boron layers on silicon for controlled nanometer-deep p⁺-n junction formation," Sarubbi et al., J. Electron. Material, vol. 39, pp. 162-173, 2010, which is incorporated by reference herein.

[0042] After step 209, other layers may be deposited on top of the boron layer. These other layers may include anti-reflection coatings comprised of one or more materials, such as silicon dioxide, silicon nitride, aluminum oxide, hafnium dioxide, magnesium fluoride, and lithium fluoride. These other layers may include a thin protective layer comprising a metal such as aluminum, ruthenium, tungsten or molybdenum. One or more of these other layers may be deposited using ALD. An advantage of using an ALD process for depositing these layers is that ALD

processes typically allow very precise (single monolayer) control of the thickness of the deposited layer(s). In an alternative embodiment, other layers may be deposited on top of the boron layer after step 213.

[0043] In one embodiment, the protective front-side layer may be removed in step 213. In another embodiment, in step 213, holes or vias can be opened or exposed in the handling wafer and/or protective front-side layer, or through-silicon vias around the edges of the device can be exposed, thereby allowing connection to the circuit elements.

[0044] In step 215, the resulting structure may be packed in a suitable package. The packing step may comprise flip-chip bonding or wire bonding of the device to a substrate. The package may include a window that transmits wavelengths of interest, or may comprise a flange or seal for interface to a vacuum seal.

[0045] Figures 4A-4G illustrate exemplary cross-sections of a wafer subjected to method 200 (Figure 2). Figure 4A illustrates a first epitaxial (epi) layer 402 formed on the front side of a substrate 401. First epi layer 402 is preferably a p- epi layer. In one embodiment, the first epi layer resistivity is between about 100 and 1000 Ω cm.

[0046] Figure 4B illustrates various circuit elements 403 including interconnects that can be formed on the first epi layer 402 as described in step 201 above). Because the interconnects are formed on the wafer while the substrate is still hundreds of microns thick and hence not severely warped, these interconnects can be formed using normal sub-micron CMOS processing techniques and may include multiple layers of high-density metal

interconnects. The metal interconnects comprise a metal such as copper, aluminum, tungsten, molybdenum or cobalt. In one embodiment, the metal interconnects consist entirely of refractory metals. In one embodiment, multiple through-silicon vias (TSV) 403A are created around one, or more, edges of the image sensor array in order to allow connection to the circuit elements 403.

[0047] Figure 4C illustrates a handling wafer 404 attached to the top surface of first epi layer 402 over circuit elements 403 (step 203). Note that the through-silicon vias are shown but not labeled so as not to overly complicate the drawings. In an alternative embodiment, a protective layer can be used instead of, or in addition to, handling wafer 404. In one embodiment (not shown), vias are formed in handling wafer 404 to allow connection to the circuit elements 403.

[0048] Figure 4D illustrates the wafer after the substrate (e.g., substrate 401 shown in Fig. 4C) is back-thinned to form the semiconductor membrane mentioned above or removed to expose a back-side (lower) surface 402L of first epi layer 402 (i.e., opposite to the surface on which circuit elements 403 are formed and to which handling wafer 404 is attached). As depicted in Figure 4D, a native oxide may form on back-side surface 402L, which is exposed by the back-thinning process.

[0049] Figure 4E illustrates the wafer after a cleaning and preparation of the back-side surface 402L is completed (step 207) to prepare first epi layer 402 for the formation of a second epitaxial (epi) layer.

[0050] Figure 4F illustrates the wafer after a second epi layer 405 is formed on back-side surface 402L of first epi layer

402, and a pure boron layer 406 is formed on a lower surface 405L of second epi layer 405are respectively (steps 208 and 209). In-situ p-type doping of the second epi layer 405 during growth (as described above for step 208) creates a dopant concentration profile that increases from the bottom (back-side) surface 402L of first epi layer 402 to lower surface 405L of pure boron layer 406.

[0051] Figure 4G illustrates one or more optional anti-reflection or protection layers 408 deposited bottom/lower surface 406L of pure boron layer 406. At least one of the layers may be deposited using an ALD process.

[0052] Figure 4H illustrates the wafer after etching and deposition steps create metal pads 407 so as to allow electrical connection to the TSVs 403A (step 213). Note that if vias are formed in handling wafer 404, then metal pad 407 should be formed on the top surface of handling wafer 404.

[0053] The above examples are not meant to limit the scope of the invention disclosed herein. They are meant merely as illustrations of how a p-type doped second epitaxial layer may be deposited on a back-side surface of a first epitaxial layer. The second epitaxial layer is subsequently coated with a boron layer on its photo-sensitive surface. Because the second epitaxial layer includes a concentration gradient of the p-type dopant which has its maximum value adjacent to the boron, the image sensor has high efficiency even for short-wavelength light, or low-energy charged particles, which may penetrate only a few nm, or a few tens of nm into the epitaxial layers.

[0054] Figure 5 illustrates an exemplary detector assembly 500 incorporating an image sensor 504, a silicon interposer 502 and

other electronics in accordance with certain embodiments of the present invention.

[0055] In one aspect of the present invention, the detector assembly 500 may include one or more light sensitive sensors 504 disposed on the surface of an interposer 502. In one embodiment, the one or more interposers 502 of the assembly 500 may include, but are not limited to, a silicon interposer. In a further aspect of the present invention, the one or more light sensitive sensors 504 of the assembly 500 are back-thinned and further configured for back-illumination including a boron layer and a p-type doped second epitaxial layer adjacent to the boron layer as described above.

[0056] In another aspect of the present invention, various circuit elements of the assembly 500 may be disposed on or built into the interposer 502. In one embodiment, one or more amplification circuits (e.g., charge conversion amplifier) (not shown) may be disposed on or built into the interposer 502. In another embodiment, one or more conversion circuits 508 (e.g., analog-to-digital conversion circuits, i.e. digitizers 508) may be disposed on or built into the interposer 502. In another embodiment, one or more driver circuits 506 may be disposed on or built into the interposer 502. For example, the one or more driver circuits 506 may include a timing/serial drive circuit. For instance, the one or more driver circuits 506 may include, but are not limited to, clock driver circuitry or reset driver circuitry. In another embodiment, one or more decoupling capacitors (not shown) may be disposed on or built into the interposer 502. In a further embodiment, one or more serial transmitters (not shown in Figure 5) maybe disposed on or built into the interposer 502. In another embodiment, one or more of amplification circuits, analog-to-digital converter circuits and

driver circuits may be included in light sensitive sensor 504, reducing the number of (or eliminating the need for) circuits such as 506 and 508.

[0057] In another aspect of the present invention, one or more support structures may be disposed between the bottom surface of the light sensitive array sensor 504 and the top surface of the interposer 502 in order to provide physical support to the sensor 504. In one embodiment, a plurality of solder balls 516 may be disposed between the bottom surface of the light sensitive array sensor 504 and the top surface of the interposer 502 in order to provide physical support to the sensor 504. It is recognized herein that while the imaging region of the sensor 504 might not include external electrical connections, the back-thinning of the sensor 504 causes the sensor 504 to become increasingly flexible. As such, solder balls 516 may be utilized to connect the sensor 504 to the interposer 502 in a manner that reinforces the imaging portion of the sensor 504. In an alternative embodiment, an underfill material may be disposed between the bottom surface of the light sensitive array sensor 504 and the top surface of the interposer 502 in order to provide physical support to the sensor 504. For example, an epoxy resin may be disposed between the bottom surface of the light sensitive array sensor 504 and the top surface of the interposer 502.

[0058] In another aspect of the present invention, the interposer 502 and the various additional circuitry (e.g., amplification circuit, driver circuits 506, digitizer circuits 508, and the like) are disposed on a surface of a substrate 510. In a further aspect, the substrate 510 includes a substrate having high thermal conductivity (e.g., ceramic substrate). In this regard, the substrate 510 is configured to provide physical support to the sensor 504/interposer 502 assembly, while also

providing a means for the assembly 500 to efficiently conduct heat away from the imaging sensor 504 and the various other circuitry (e.g., digitizer 506, driver circuitry 508, amplifier, and the like). It is recognized herein that the substrate may include any rigid highly heat conductive substrate material known in the art. For example, the substrate 510 may include, but is not limited to, a ceramic substrate. For instance, the substrate 510 may include, but is not limited to, aluminum nitride.

[0059] In another embodiment, the substrate 510 may be configured to provide an interface to a socket or an underlying printed circuit board (PCB). For example, as shown in Figure 5, the substrate 510 may provide interconnection between the interposer 502 and a socket or a PCB via interconnects 512. Those skilled in the art will recognize that the substrate 510 may be operatively coupled to an underlying PCB and further electrically coupled to a socket or PCB in a variety of ways, all of which are interpreted to be within the scope of the present invention.

[0060] The various embodiments of the structures and methods of this invention that are described above are illustrative only of the principles of this invention and are not intended to limit the scope of the invention to the particular embodiments described. For example, additional steps may be added to the flow chart depicted in Figure 2, or some of the steps shown may be done in different sequence than shown. Thus, the invention is limited only by the following claims and their equivalents.

CLAIMS

1. A method of fabricating an image sensor, the method comprising:

forming a first epitaxial layer on a substrate;

forming a circuit element first epitaxial layer;

thinning the substrate to generate a thinned substrate, the thinned substrate exposing at least a surface portion of the first epitaxial layer;

forming a second epitaxial layer on the exposed portion of the first epitaxial layer; and

forming a pure boron layer on the second epitaxial layer, wherein forming the second epitaxial layer includes generating a p-type dopant concentration gradient in the second epitaxial layer by gradually increasing a concentration of a p-type dopant used during formation of the second epitaxial layer such that a first layer portion of the second epitaxial layer has a lower p-type dopant concentration than a subsequently formed second layer portion of the second epitaxial layer, and a highest p-type dopant concentration of the second epitaxial layer is adjacent to the pure boron layer.

2. The method of claim 1, wherein the p-type dopant comprises boron.

3. The method of claim 1, wherein forming the second epitaxial layer comprises utilizing a gas containing elemental boron at a temperature lower than about 350°C.

4. The method of claim 3, wherein forming the second epitaxial layer comprises growing said second epitaxial layer using molecular-beam epitaxial growth.

5. The method of claim 1, wherein the method further comprises depositing an anti-reflection layer on a surface of the pure boron layer.

6. The method of claim 1, wherein the method further comprises depositing a metal protective layer on the surface of the pure boron layer.

7. The method of claim 1, wherein the method further comprises attaching a handling wafer to the first epitaxial layer over the circuit elements prior to thinning the substrate.

8. The method of claim 7, wherein the method further comprises forming vias in at least one of the first epitaxial layer and the handling wafer prior to thinning the substrate.

9. The method of claim 8, wherein the method further comprises exposing the vias after forming the pure boron layer.

10. The method of Claim 1, wherein forming the second epitaxial layer comprises utilizing a plasma-enhanced chemical vapor deposition process at a temperature lower than about 450°C.

11. An image sensor for sensing at least one of deep ultraviolet (DUV) radiation, vacuum ultraviolet (VUV) radiation, extreme ultraviolet (EUV) radiation, and charged particles, the image sensor comprising:

a semiconductor membrane comprising a first epitaxial layer and including circuit elements and metal interconnects formed on a first surface of the first epitaxial layer;

a second epitaxial layer formed on a second surface of the first epitaxial layer; and

a pure boron layer formed on the second epitaxial layer, wherein the second epitaxial layer includes a p-type dopant concentration gradient that has a minimum p-type doping concentration adjacent to the second surface of the first epitaxial layer and has a maximum p-type doping concentration immediately adjacent to the pure layer boron layer.

12. The image sensor of claim 11, wherein the first epitaxial layer has a thickness in the range of about 10 μm to about 40 μm .

13. The image sensor of claim 12, wherein the pure boron layer has a thickness in the range of 2 nm to 20 nm.

14. The image sensor of claim 11, further comprising an anti-reflection coating deposited on the pure boron layer.

15. The image sensor of claim 11, further comprising a handling wafer attached to the first epitaxial layer over the circuit elements.

16. The image sensor of claim 11, further comprising a protective layer formed on the first epitaxial layer over the circuit elements.

17. The image sensor of claim 11, wherein the p-type dopant comprises boron.

18. The image sensor of claim 13, wherein the image sensor comprises a charge-coupled device (CCD) or a CMOS device.

19. An image sensor for sensing at least one of deep ultraviolet (DUV) radiation, vacuum ultraviolet (VUV) radiation, extreme ultraviolet (EUV) radiation, and charged particles, the image sensor comprising:

a semiconductor membrane comprising a first epitaxial layer and including circuit elements formed on a first surface thereof, and metal interconnects connected to at least one of said circuit elements;

a second epitaxial layer formed on a second surface of the first epitaxial layer; and

a pure boron layer formed on the second epitaxial layer, wherein the second epitaxial layer includes a p-type dopant concentration gradient configured such that a first layer portion of the second epitaxial layer has a lower p-type dopant concentration than a second layer portion of the second epitaxial layer, and includes a p-type dopant maximum concentration immediately adjacent to the pure boron layer, said second epitaxial layer being disposed between said first layer portion and the pure boron layer.

20. The image sensor of Claim 19, wherein the pure boron layer has a thickness in the range of 2 nm to 20 nm, and

wherein the semiconductor membrane has a thickness in the range of 10 μm to 40 μm .

21. The image sensor of Claim 19, the image sensor further comprising one of an anti-reflection and a protective layer disposed on the pure boron layer, wherein the pure boron layer is between 3 nm and 10 nm thick.

22. The image sensor of Claim 19, wherein p-type dopant consists of boron.

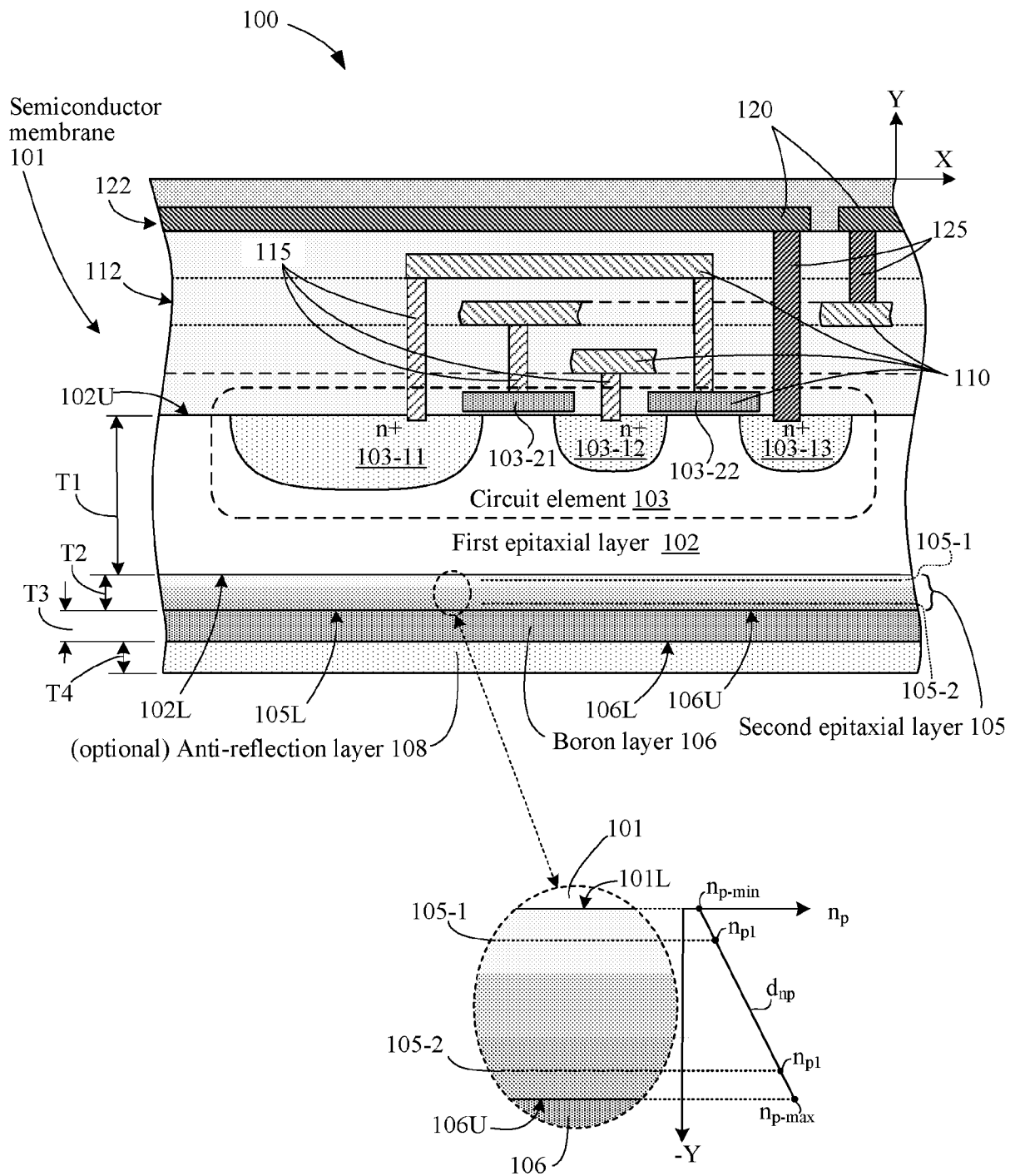


Figure 1

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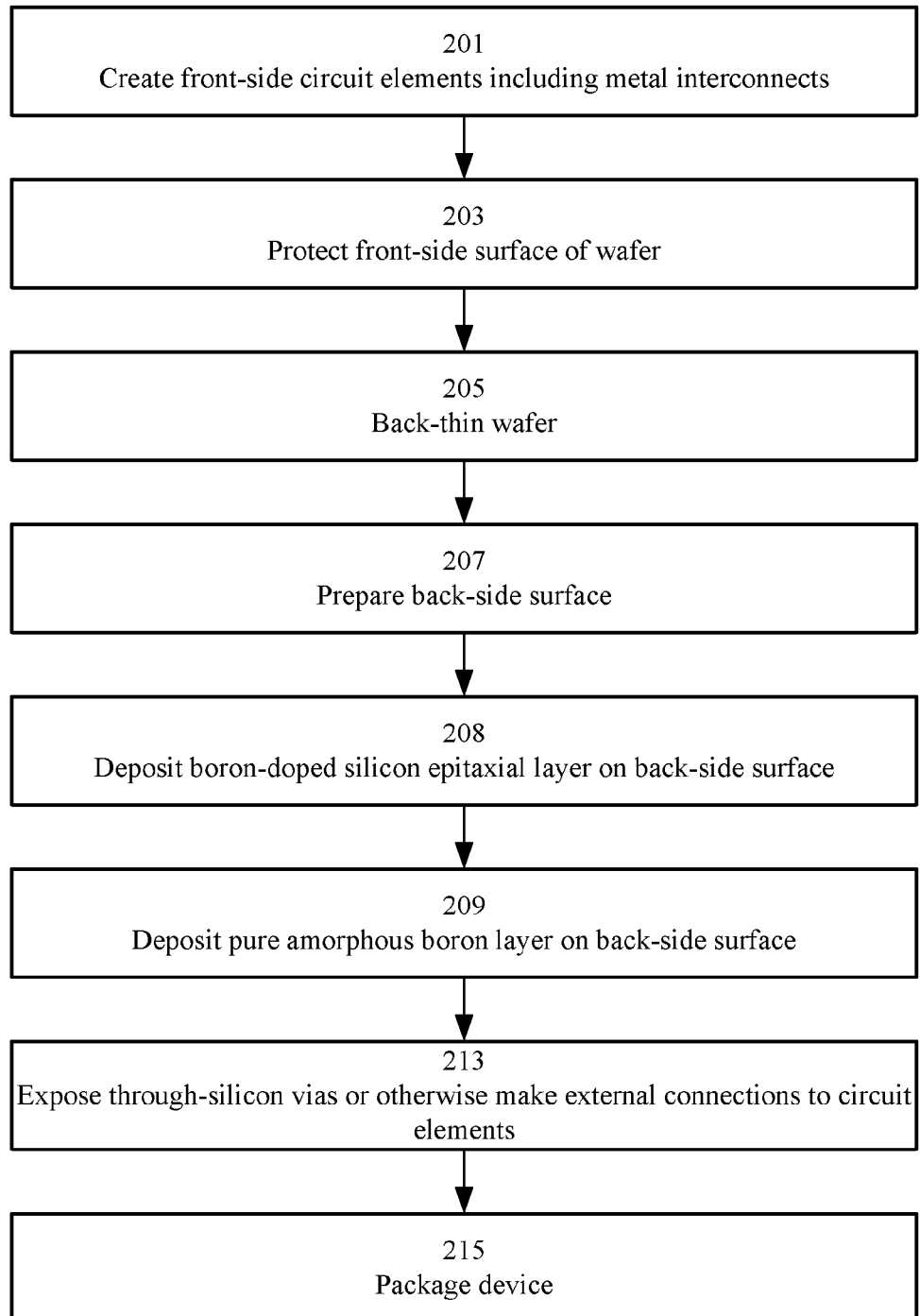
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Figure 2

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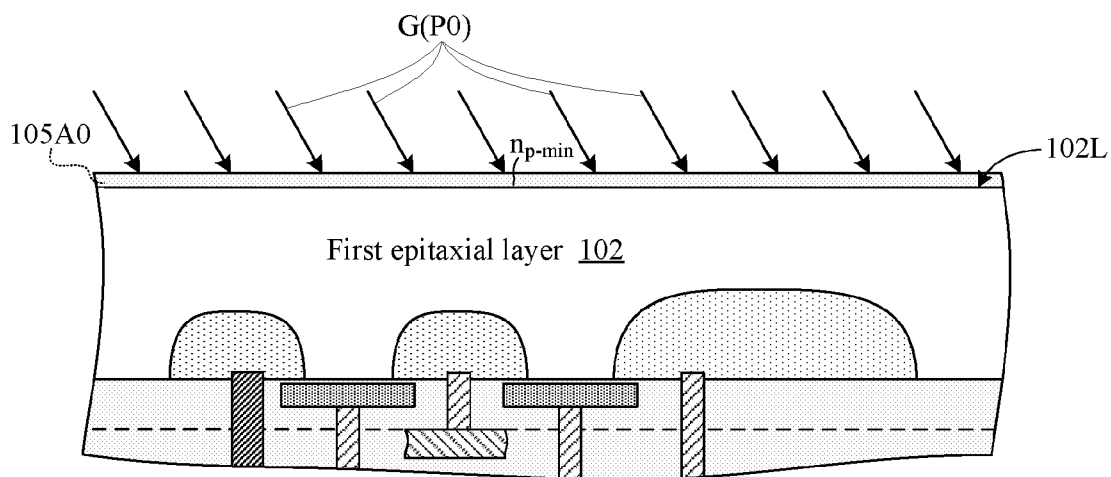


Figure 3A

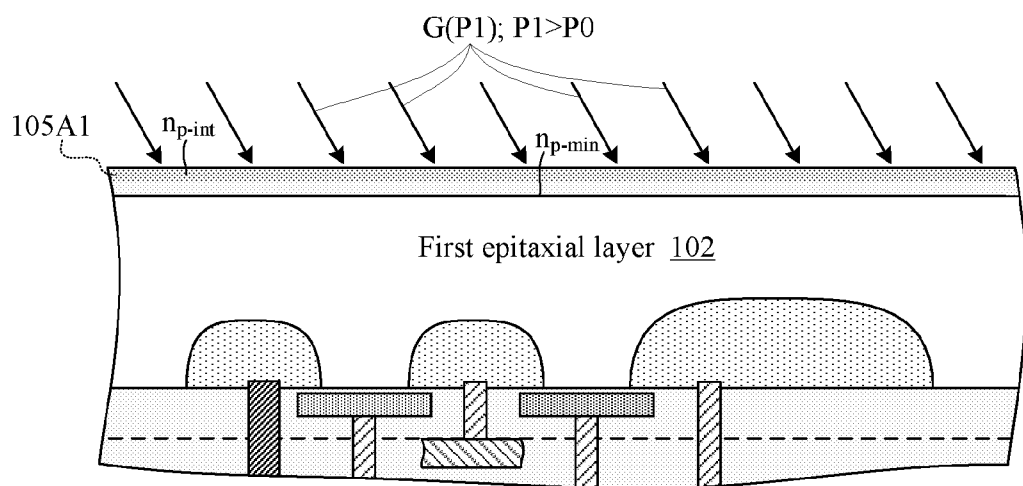


Figure 3B

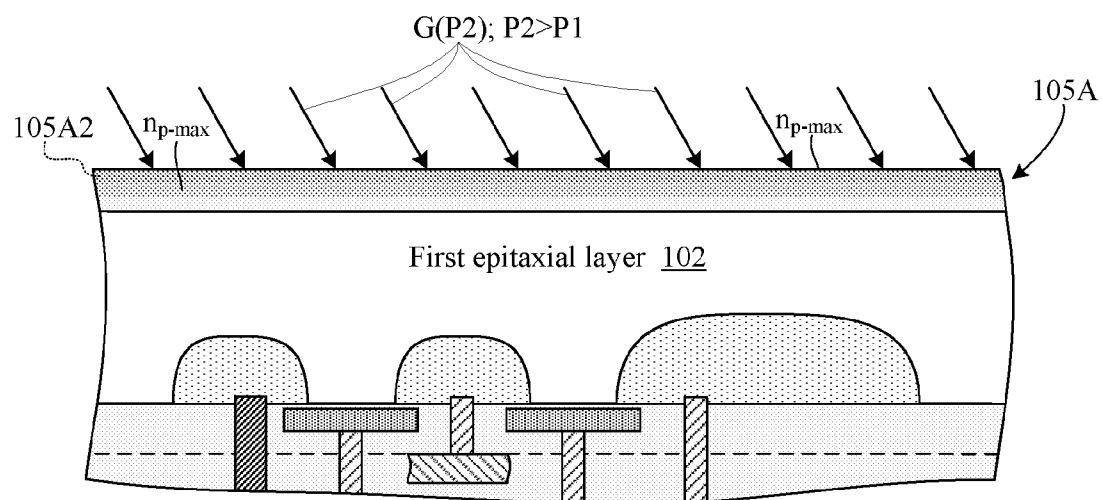


Figure 3C

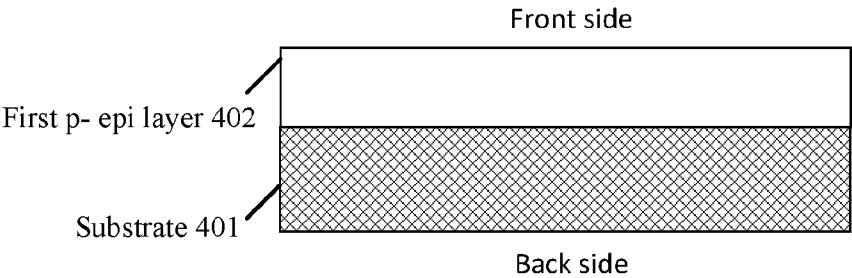


Figure 4A

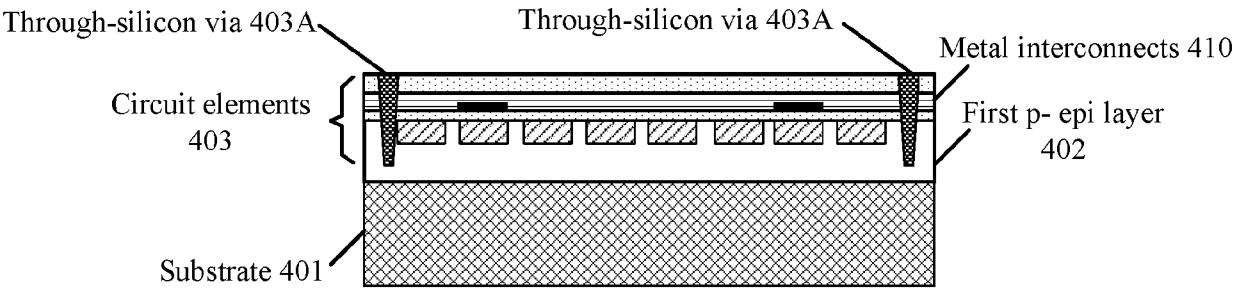


Figure 4B

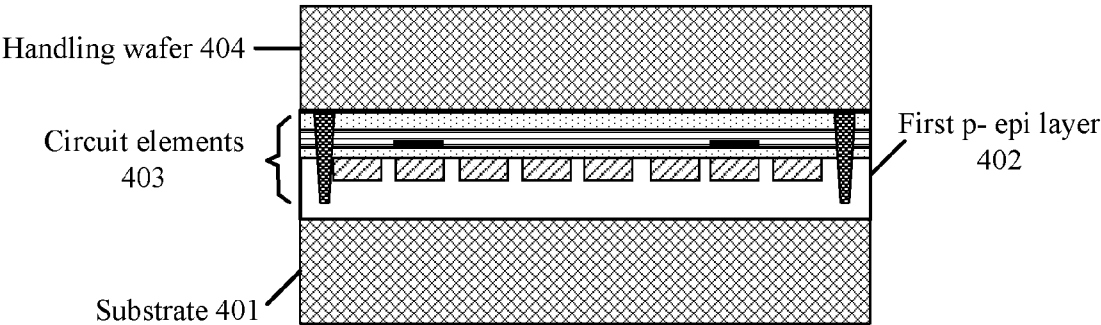
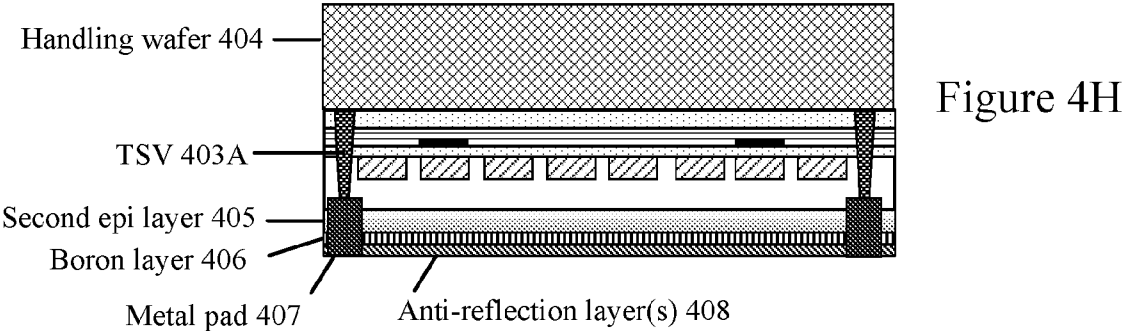
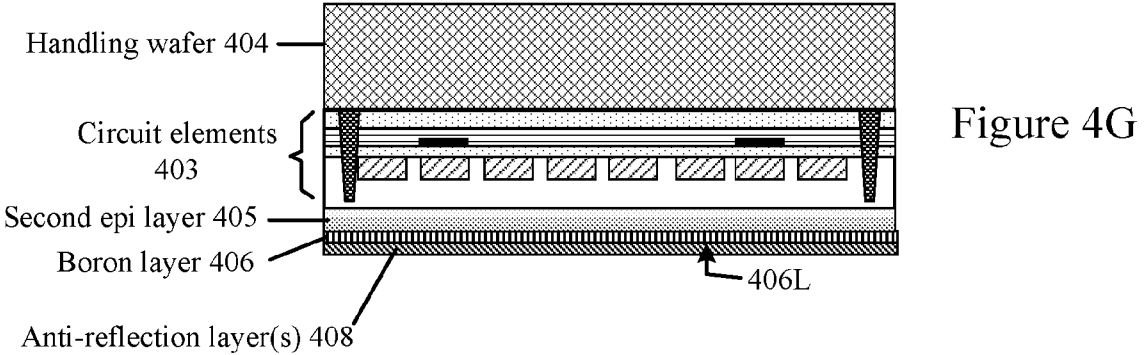
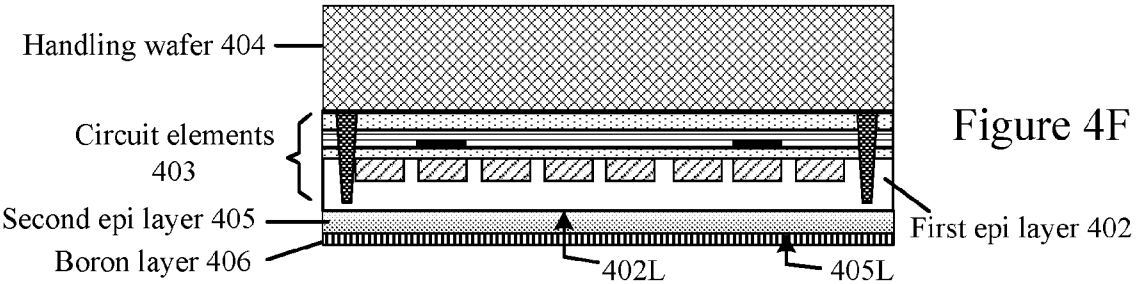
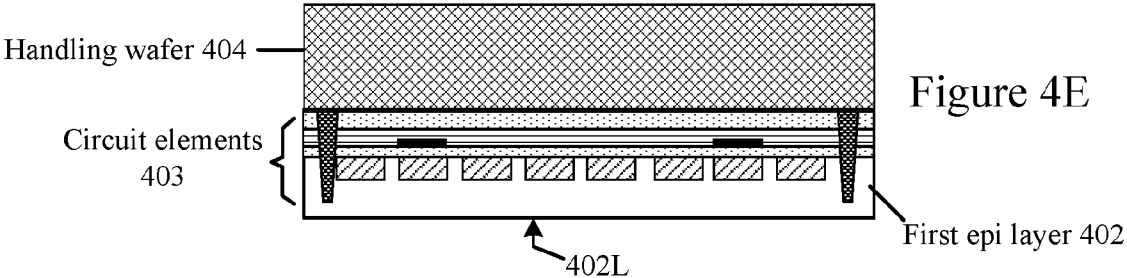
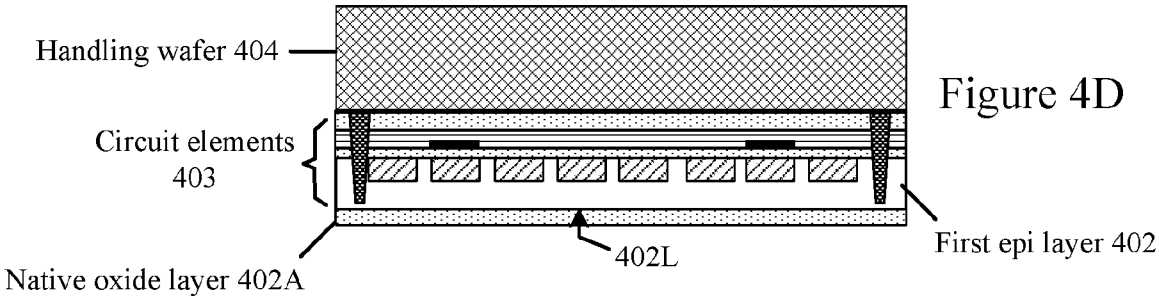


Figure 4C



500

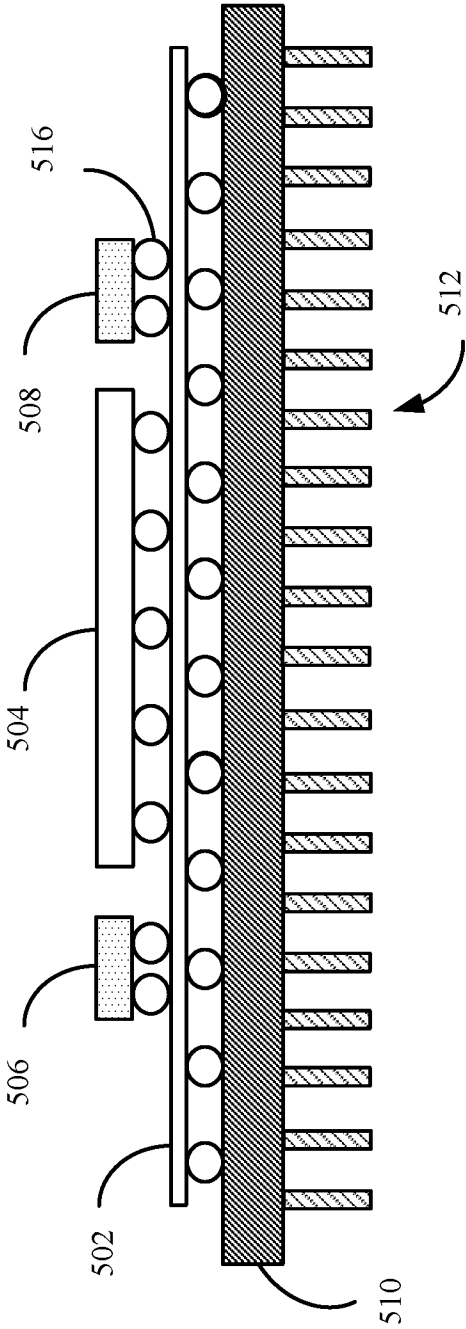


Figure 5

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/146(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/146; H01L 31/02; H01L 31/0232; H01L 31/18; H04N 5/361

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: image sensor, epitaxial layer, dopant, gradient

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015-0200216 A1 (KLA-TENCOR CORPORATION et al.) 16 July 2015 paragraphs [0024]-[0045], claims 1, 14 and figures 1-4H	1-22
A	US 2007-0235829 A1 (PETER ALAN LEVINE et al.) 11 October 2007 paragraphs [0020]-[0049] and figures 1A-8	1-22
A	US 2013-0334638 A1 (SZU-YING CHEN et al.) 19 December 2013 paragraphs [0031]-[0064] and figures 3-10	1-22
A	US 2014-0302630 A1 (SHANGHAI HUALI MICROELECTRONICS CORPORATION) 09 October 2014 paragraphs [0032]-[0037] and figures 3-6	1-22
A	US 2018-0061872 A1 (CANON KABUSHIKI KAISHA) 01 March 2018 paragraphs [0016]-[0065] and figures 1A-6B	1-22



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

08 April 2020 (08.04.2020)

Date of mailing of the international search report

08 April 2020 (08.04.2020)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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