(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 November 2005 (24.11.2005)

PCT

(10) International Publication Number
WO 2005/112105 A1

(51) International Patent Classification[7]: H01L 21/4763

(21) International Application Number: PCT/US2005/014645

(22) International Filing Date: 28 April 2005 (28.04.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/709,357 29 April 2004 (29.04.2004) US

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2005/112105 A1

(54) **Title:** METHOD FOR FORMING SUSPENDED TRANSMISSION LINE STRUCTURES IN BACK END OF LINE PROCESSING

(57) **Abstract:** A method for forming a transmission line structure (300) for a semiconductor device includes forming an interlevel dielectric layer over a first metallization level, removing a portion of the interlevel dielectric layer and forming a sacrificial material within one or more voids (308) created by the removal of the portion of the interlevel dielectric layer. A signal transmission line (302) is formed in a second metallization level formed over the interlevel dielectric layer, the signal transmission line (302) being disposed over the sacrificial material. A portion of dielectric material included within the second metallization level is removed so as to expose the sacrificial material, wherein a portion of the sacrificial material is exposed through a plurality of access holes (310) formed through the signal transmission line (302). The sacrificial material is removed so as to create an air gap beneath the signal transmission line (302).

METHOD FOR FORMING SUSPENDED TRANSMISSION LINE STRUCTURES IN BACK END OF LINE PROCESSING

TECHNICAL FIELD

The present invention relates generally to semiconductor manufacturing processes and, more particularly, to a method for forming suspended transmission line structures in back end of line (BEOL) processing of semiconductor devices.

BACKGROUND ART

Semiconductor integrated circuits typically are formed by MOS (metal oxide semiconductor) or by bipolar transistors that are integrated at a top planar major surface of a silicon chip. Electrical interconnections between various transistors, as well as between certain transistors and access pins located along the periphery of the chip, have typically taken the form of two (or more) "levels" of interconnections, i.e., electrically conducting lines in the form of metallization stripes running along two (or more) essentially planar surfaces that are oriented mutually parallel to, and are insulated from, both each other and the top planar surface of the chip by suitable insulating layers. Interconnection vias (windows) in the insulating layers are provided wherever needed in accordance with the desired circuit interconnections.

In particular, microstrip structures are used primarily in radio frequency (RF) CMOS/SiGe chips, where wiring is not dense. Generally, microstrip structures provide fairly good isolation of the signal from lossy substrate material underneath. As illustrated in Figure 1(a), a typical microstrip transmission line structure 10 includes a signal transmission line 12, an underlying ground plane 14 for shielding, and an interlayer dielectric material (ILD) 16 therebetween. Since the shielding 14 and signal transmission line 12 are fabricated as standard interconnect components, they are encapsulated by the dielectric material 16. Examples of such dielectric material include, for example, silicon dioxide (SiO_2), SiCOH, SiLK, FSG, USG, among others. The dielectric constant of such

materials generally ranges from about 2.5 to about 4.1.

On the other hand, coplanar waveguides are commonly used where wiring density is relatively high, such as in CMOS chips, for example, where it is difficult to create an explicit return path below the signal line. The only way to reliably return the signal is to also use the same routing metal level as the one used for the signal wire. Thus, as shown in Figure 1(b), a typical coplanar waveguide transmission line structure 20 includes a signal transmission line 22 and two adjacent shielding lines 24 disposed on the same wiring level as the transmission line 22. The coplanar waveguide structure 20 is at a fixed distance from the silicon substrate 26. A third structure referred to as a microstrip transmission line having side shielding (i.e., having characteristics of both microstrip and coplanar structures) has also been used in existing transmission line structures.

As shown in Figure 1(c), a typical microstrip transmission structure 30 with side shielding includes a signal transmission line 32, a ground plane 34 for shielding, and an interlayer dielectric material 36 therebetween. In addition, however, the shielding also includes shielding lines 38 disposed on the same wiring level as the signal transmission line 32. The shielding lines 38 are electrically contiguous with the ground plane 34 through conductively filled vias 40. As with the microstrip structure 10, the conventional coplanar elements are also surrounded by ILD material.

In each instance, the use of the ILD material as described above generates dielectric losses and reduces the Q-factor of the transmission lines in the BEOL interconnect. Accordingly, it would be desirable to create such shielded transmission line structures in conjunction with a lower dielectric material so as to improve the performance of the transmission lines.

Disclosure of the Invention

The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for forming a transmission line structure for a semiconductor

device. In an exemplary embodiment, the method includes forming an interlevel dielectric layer over a first metallization level, removing a portion of the interlevel dielectric layer and forming a sacrificial material within one or more voids created by the removal of the portion of the interlevel dielectric layer. A signal transmission line is formed in a second metallization level formed over the interlevel dielectric layer, the signal transmission line being disposed over the sacrificial material. A portion of dielectric material included within the second metallization level is removed so as to expose the sacrificial material, wherein a portion of the sacrificial material is exposed through a plurality of access holes formed through the signal transmission line. The sacrificial material is removed so as to create an air gap beneath the signal transmission line.

In another embodiment, a back end of line transmission line structure for a semiconductor device includes an interlevel dielectric layer formed over a first metallization level, and one or more voids formed in the interlevel dielectric layer. A signal transmission line is formed in a second metallization level, the signal transmission line being disposed over the one or more voids. The signal transmission line further includes a plurality of access holes formed therethrough to provide removal access to a sacrificial material used to define the one or more voids, wherein the one or more voids define an air gap beneath the signal transmission line.

In still another embodiment, a back end of line microstrip transmission line structure includes a signal transmission line formed on one metallization level and a ground plane formed on another metallization level. An air gap is disposed between the signal transmission line and the ground plane, the air gap formed within an interlevel dielectric layer. One of the signal transmission line and the ground plane further includes a plurality of access holes formed therethrough to provide removal access to a sacrificial material used to define the air gap.

In still another embodiment, a back end of line coplanar waveguide transmission

line structure includes a signal transmission line formed on a first metallization level, and a pair of coplanar shielding lines adjacent the signal transmission line in the first metallization level. An air gap is disposed beneath the signal transmission line, the air gap formed within an interlevel dielectric layer. The signal transmission line further includes a plurality of access holes formed therethrough to provide removal access to a sacrificial material used to define the air gap.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

Figure 1(a) is a cross-sectional view of a conventional microstrip transmission line structure;

Figure 1(b) is a cross-sectional view of a conventional coplanar waveguide transmission line structure;

Figure 1(c) is a cross-sectional view of a conventional microstrip transmission line structure with side shielding;

Figures 2(a) through 2(i) are a series of process flow diagrams illustrating a method for forming a suspended transmission line structure in back end of line (BEOL) processing, in accordance with an embodiment of the invention;

Figure 2(j) is a plan (top-down) view of the design and mask layout of the resulting suspended transmission line structure formed in Figures 2(a) through 2(i);

Figure 3 is a cross sectional view of a microstrip transmission line embodiment having an air gap dielectric;

Figure 4 is a cross sectional view of an inverted microstrip transmission line embodiment having an air gap dielectric;

Figure 5 is a cross sectional view of a coplanar transmission line embodiment having an air gap dielectric, and without a ground plane directly underneath the signal line;

Figure 6 is a cross sectional view of a coplanar waveguide transmission line embodiment having an air gap dielectric, and without any underlying ground plane;

Figures 7(a) through 7(g) are a series of process flow diagrams illustrating one possible method for encapsulating a suspended transmission line structure as formed in Figures 2(a) through 2(g), in accordance with an embodiment of the invention;

Figures 8(a) through 8(d) are a series of process flow diagrams illustrating an alternative method for encapsulating a suspended transmission line structure as formed in Figures 2(a) through 2(g), in accordance with an embodiment of the invention;

Figures 9(a) through 9(c) are a series of process flow diagrams illustrating the formation of a strip line transmission line embodiment having an air gap below the signal line, and with underlying and overlying ground planes; and

Figures 10(a) through 10(d) are graphs depicting various simulation results comparing a microstrip air gap transmission line structure (such as illustrated in Figure 3) with a conventional microstrip structure with an SiO_2 dielectric.

BEST MODE FOR CARRYING OUT THE INVENTION

Disclosed herein is a method for forming suspended transmission line structures in back end of line (BEOL) semiconductor processing, in which the integration scheme results in copper BEOL transmission line structures with lower dielectric losses. It will be appreciated, however, that the method embodiments described herein are not limited to copper BEOL as such, and can be extended to other interconnects fabricated using various materials including for example, but not limited to, aluminum, tungsten, gold. In one embodiment, the integration method results in the formation of an air gap between a

signal line and a ground plane so as to reduce the interconnect dielectric constant and thus the amount of capacitive cross-talk, which can be particularly high at microwave frequencies. Furthermore, the term "air gap" as used hereinafter is not necessarily limited to the presence of air between a signal line and ground plane, but is also intended to describe or refers to the presence of any gaseous phase material, or a vacuum.

Referring generally now to Figures 2(a) through 2(i), there is shown a series of process flow diagrams illustrating a method for forming a suspended transmission line structure in back end of line (BEOL) processing, in accordance with an embodiment of the invention. Beginning in Figure 2(a), a ground plane 102 is formed through single damascene processing techniques. In particular, a liner material 104 (e.g., tantalum nitride/tantalum) is deposited within an opening formed in an insulating layer 106, after which the BEOL metallization 108 (e.g., copper) is deposited over the liner material by (for example) electroplating, sputtering, etc., and thereafter planarized. As shown in Figure 2(b), the ground plane 102 is thereafter completely encapsulated by recess etching a portion of the BEOL metallization 108, depositing additional liner material and planarizing to form a top liner portion 110. Thus encapsulated, the ground plane 102 is resistant to diffusion of atoms of the metallization 108, as well as to oxidation from subsequent processing steps described hereinafter.

In an exemplary embodiment, the top surface of the wiring 108 is recessed with respect to the top layer of dielectric layer 106. One method for recessing the metal is to use a timed wet etch to achieve the desired depth. For example, a solution comprised of water, acetic acid and hydrogen peroxide (of an exemplary concentration of 3 liters, 15 ml, and 9 ml, respectively) is applied for about 2.5 minutes to achieve a depth of about 600 Angstroms (Å) to about 800 Å. The layer of barrier material 110 is then deposited, and is used to encapsulate the copper to protect it during subsequent processing. One particular embodiment incorporates a layer 100 Å thick of tantalum (Ta), followed by 400 Å of tantalum nitride (TaN). Alternatively, the barrier material 110 could also be made of a dielectric or any number of other suitable metallic barriers.

Still another method of encapsulating the metallization is to pattern the blanket barrier 110 using the same mask for defining the conductors, along with the opposite polarity photoresist and then etching the barrier layer from the upper most surface. Other materials that may be used for encapsulating the interconnects include cobalt-tungsten-phosphorus (CoWP) and Ni-Au alloys, which may be deposited by electroplating and electroless plating, among other methods.

Figure 2(c) illustrates the formation of vias 112 within an interlevel (ILD) layer 114, in accordance with a coplanar transmission line embodiment. The ILD layer 114 may include, for example, a silicon nitride (Si_3N_4) layer 116 followed by a thicker SiO_2 layer 118, which is thereafter lithographically patterned for via definition. Then, the liner and metallization materials are formed within the openings and planarized as known in the art to form the filled vias 112.

Referring to Figure 2(d), parallel trenches 120 are formed within the ILD layer 114 between vias 112. Alternatively, the original nitride layer 116 may be left at the bottom of the trenches 120 to seal and protect the ground plane as discussed above. The trenches are disposed so as to create an insulating support member 122 therebetween. The lithographic patterning in this step may be designed such that support member 122 is a continuous rail running the length of the ground plane 102 or, alternatively, such that support member is a plurality of individual posts disposed along the length of the ground plane 102. In other words, if a post configuration is desired for support member 122, then the trenches 120 are "connected" to one another at various locations along the length of the ground plane 102 (i.e., looking into the Figure). It should further be appreciated that the support member 122 may also be configured as two or more parallel rails or series of individual posts. Then, in Figure 2(e), a sacrificial material 124 is formed and planarized within the trenches. The sacrificial material 124 may be, for example, an organic low-k dielectric polymer, chosen so as to be subsequently selectively removable with respect to the ILD layers and the BEOL metallization material.

Some exemplary materials that may be used as the sacrificial material are SiLK®, diamond-like carbon (DLC) and polynorbornene (PNB). SiLK® is a semiconductor dielectric manufactured by Dow Chemical Corp., and is available under various formulations of the product, such as Porous SiLK®. This particular dielectric is a polymer resin comprised of gamma-butyrolactone, proprietary B-staged polymer and mesitylene. Another material which may be employed for this purpose is DLC, which is an amorphous carbon containing coating wherein a proportion of the carbon atoms are bonded in a manner that is similar to diamond. These materials may be removed by way of oxygen plasma exposure, so long as there is no oxidizable material that is exposed. If there is an oxidizable material that will be exposed during the removal of the organic material, a $H_2/CO_2/CO/N_2$ type plasma removal process could be used. These gas mixtures will be recognizable to practitioners skilled in the art of reactive ion etching. Polynorbornene is a sacrificial polymer that thermally decomposes at about 400 - 425°C. Hence, a simple thermal treatment may be employed to remove the sacrificial material.

Figure 2(f) illustrates the formation of the signal level metallization structures. As is shown, another dielectric layer 126 is formed over ILD layer 114, after which openings are defined therein for the formation of signal transmission line 128 and coplanar shielding lines 130. However, it can be seen that the patterning for the signal transmission line is implemented in a manner as to leave a plurality of plugs 132 of the dielectric layer 126. Thus, when the liner and metallization material is added for the coplanar shielding lines 130 and the signal transmission line 128, the resulting signal transmission line metallization is not completely continuous along the length thereof.

As was the case with the ground plane 102, a portion of the BEOL metallization for the signal transmission line 128 and coplanar shielding lines 132 is recessed etched in preparation for a top liner 134 formed thereover for encapsulating the signal level metallization structures. This is shown in Figure 2(g). In Figure 2(h), another patterning step is implemented in order to remove a portion of dielectric layer 126 adjacent each side of signal transmission line 128 so as to create voids 136 that expose the outer edges of the

sacrificial material 124. In addition, the dielectric plugs 132 left after the patterning of the signal transmission line 128 are now also removed so as to form access holes 138. The combination of voids 136 and access holes 138 at various points along the signal transmission line 128 allow for the release of the sacrificial material 124 (e.g., by an O_2 plasma etch), as shown in Figure 2(i).

When the selected sacrificial material is SiLK® or DLC, it is released by exposure to an oxygen or hydrogen plasma, which decomposes the material. Additional details regarding this process may be found in the publication by A. Joshi and R. Nimmagadda entitled "Erosion of diamond films and graphite in oxygen plasma", Journal of Material Research, Vol. 6, No. 7, p. 1484, 1996, published by the Materials Research Society, the contents of which are incorporated by reference herein in their entirety. For polynorbornene, a thermal treatment at 425°C may be carried out to release the signal line. Additional details of this release process may be found in the paper by Dhananjay Bhusari et al., entitled "Fabrication of Air-Channel Structures for Microfluidic, Microelectromechanical, and Microelectronic Applications", Journal of Microelectromechanical Systems, Vol. 10, No.3, p. 400, 2001, the contents of which are incorporated by reference herein in their entirety. The resulting transmission line structure thus includes a low dielectric constant (air) gap 140 both underneath the signal transmission line 128 in the ILD 114 level, as well as adjacent the signal transmission line 128 in the signal level (by voids 136).

Figure 2(j) illustrates a top down (plan) view of the design and layout of the suspended transmission line structure. In the design of access holes 138, special consideration is given to the arrangement of the holes to allow for reliable signal propagation. In the embodiment of Figure 2(j), an orthogonal arrangement of access holes, parallel to conductor edges, is implemented in order to minimize current disturbance. In addition, the size of the access holes 138 should be large enough to allow lateral etching of the sacrificial material, and yet small enough to cause minimal increase in signal line resistance.

After releasing the sacrificial material, one possible method for encapsulating the suspended transmission line structure is to deposit a sheet of polyimide or kapton (not shown) to completely cover the device. The layers of polyimide/kapton may then be patterned to make contact with the test pads as is necessary for further BEOL processing.

Figures 7(a) through 7(g) illustrate an alternate processing embodiment that may be implemented (beginning from the structure formed in Figure 2(g) onward), and which will be also useful to describe how the suspended transmission line structure is encapsulated. In Figure 7(b), dielectric layer 142 (preferably Si_3N_4) and ILD layer 144 (preferably SiO_2) are deposited on the signal line structure. As shown in Figure 7(c), a cavity 146 is formed above the signal line 128 using lithographic patterning and etching steps. During the etching of this cavity, the dielectric material is also removed from the cavity area around the signal line 128 and through the release holes contained in the signal line 128.

Subsequently, in Figure 7(d), the etched areas are filled with more release material 148 as previously described (e.g., with SiLK® or DLC), and is then planarized. The same sacrificial material that was initially placed below is now reused, such that the release process removes all the layers of release material. Figure 7(e) illustrates the addition of still another dielectric layer 152 atop layer 150 (collectively layers 142, 144), within which vias 154 are patterned and etched. These vias 154, which provide access to the release material 148, are then removed during the final steps of the integration scheme as shown in Figure 7(f). Finally, Figure 7(g) illustrates the final encapsulation step, which involves the deposition of another dielectric layer 158 that pinches off the small vias 154, thus hermetically sealing off the suspended transmission line structure.

Referring now to Figures 8(a) through 8(d), there is shown still another alternative method for encapsulating the suspended transmission line structure, beginning from Figure 2(i), wherein a carrier substrate is used for this encapsulation process. The carrier substrate may include, but is not limited to, Al_2O_3, glass, silicon etc. An inter-layer

dielectric material 160 (for instance SiO_2), is deposited on such a carrier substrate 162, as shown in Figure 8(b). The carrier substrate 162 is then bonded to the suspended transmission line structure, as shown in Figure 8(c), using any one of a number of well known standard processes like low-temperature bonding, eutectic bonding, etc.

The carrier substrate 162 may then be removed using any of a number of processes such as wet etch, plasma etch, planarization, grinding, etc. In any case, the carrier removal process should be terminated on the ILD layer 160, as shown in Figure 8(d). After this encapsulation process, standard BEOL processing may then be continued.

In addition to a coplanar transmission line structure having a ground plane with air dielectric, it will be appreciated that the above described process may also be adapted to form other types of transmission line structures. For example, Figure 3 illustrates a microstrip transmission line embodiment 300, including encapsulated signal transmission line 302, encapsulated ground plane 304, and support member 306. An air gap dielectric is further created by forming voids at both the ILD level and the signal line level, in a manner similar to that described above. Again, the signal transmission line 302 includes a plurality of access holes 310 for assisting in the release of sacrificial material to form the voids at the ILD level. Figure 4 illustrates an inverted microstrip transmission line embodiment 400, in which the signal transmission line 402 is formed at a lower metallization level than the ground plane 404. Accordingly, to form voids 408 for the air gap dielectric, the access holes are first created in the ground plane 404 instead of the signal transmission line 402.

Referring to Figure 5, there is shown another coplanar transmission line embodiment 500, in which there is no ground plane formed directly underneath the signal transmission line 504. Instead, the coplanar shielding lines 506 are electrically isolated from one another, but are each coupled to respective lower level lines 508 through vias 510. Figure 6 shows a coplanar waveguide structure 600, in which the ground plane only includes the two shielding lines 606 at the same level as the suspended signal line 604,

with no connections to underlying metal levels.

Still another embodiment of the suspended signal line topology is a stripline transmission line, as illustrated by the process flow drawings in Figures 9(a) through 9(c). Further BEOL processing is carried out on the structure generated at the end of the encapsulation process defined in Figures 8(a) through 8(d). In Figure 9(b), via contacts 164 are fabricated using single damascene integration to make electrical contact with the two shielding lines 130. Then, in Figure 9(c), a ground plane 166 is fabricated using single-damascene integration, although the via contacts 164 and ground plane 166 can also be fabricated using dual damascene integration processes as well.

In the transmission line embodiments including a ground plane, it will be appreciated that such a ground plane need not necessarily be located at the metallization level immediately below (or above) the signal transmission line level. In other words, the ground plane may be disposed at several levels below the signal transmission line, for example, to provide varying values of line impedance. If the structure is a coplanar transmission line that also features a ground plane, then the coplanar shielding lines can be electrically coupled to the ground plane through multiple levels of interconnect lines/vias.

Finally, Figures 10(a) through 10(d) reflect various simulation results comparing a microstrip air gap transmission line structure (such as illustrated in Figure 3) with a conventional microstrip structure with SiO_2 dielectric. As is shown in Figure 10(a) and 10(b), a suspended interconnect has lower losses over a wide range of microwave frequencies, compared to the SiO_2 dielectric structure. In particular, the graph in Figure 10(a) plots the magnitude versus frequency of the insertion loss (scattering parameter S_{21}), while Figure 10(b) plots attenuation coefficient versus frequency. As is further shown in Figure 10(c), the suspended interconnect structure also has a lower parasitic capacitance, as well as a higher impedance as shown in Figure 10(d).

As will be appreciated, the above described transmission line structure embodiments provide for lower attenuation and reduced dielectric losses (that could ordinarily be high at RF/microwave frequencies) as a result of the air gap created between the signal line and the return path. Moreover, there is a reduced capacitive cross-talk voltage due to the decrease in effective interconnect dielectric constant that, in turn, lowers the signal propagation delay. Another advantage is the increased signal broadband width provided by an extended usable range of characteristic impedances. Signals with different frequency components travel with different speeds in a lossy interconnect, thus the dispersion is also lowered when using an air dielectric. Still a further advantage stems from simpler signal modeling from electromagnetic propagation that is mostly concentrated in air. From a structural standpoint, the transmission characteristics of air gap configuration are significantly less affected by semiconductor surface conditions and bulk substrate properties.

While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

INDUSTRIAL APPLICABILITY

The invention impacts the field of semiconductor devices, and more particularly semiconductor devices that comprise formation of suspended transmission line structures.

CLAIMS

What is claimed is:

1. A back end of line transmission line structure (300) for a semiconductor device, comprising:

an interlevel dielectric layer formed over a first metallization level;

one or more voids (308) formed in said interlevel dielectric layer; and

a signal transmission line (302) formed in a second metallization level, said signal transmission line (302) being disposed over said one or more voids (308), said signal transmission line (302) further comprising a plurality of access holes (310) formed there through to provide removal access to a sacrificial material used to define said one or more voids (308);

wherein said one or more voids (308) define an air gap beneath said signal transmission line (302).

2. The transmission line structure (300) of claim 1, further comprising a support (306) structure beneath said signal transmission line (302), said support structure comprising material from said interlevel dielectric layer.

3. The transmission line structure (300) of claim 2, wherein said support structure further comprises a continuous rail.

4. The transmission line structure (300) of claim 2, wherein said support structure further comprises a plurality of individual posts.

5. The transmission line structure (300) of claim 1, further comprising a ground plane (304) formed within the first metallization level, said ground plane (304) further comprising a back end of line metallic material completely encapsulated within a

liner material.

6. The transmission line structure (300) of claim 5, further comprising a pair of coplanar shielding lines adjacent said signal transmission line (302) in said second metallization level.

7. The transmission line structure (300) of claim 6, wherein said pair of coplanar shielding lines and said signal transmission line (302) are also completely encapsulated with said liner material.

8. The transmission line structure (300) of claim 6, further comprising vias formed in said interlevel dielectric layer for electrically connecting said pair of coplanar shielding lines and said ground plane.

9. The transmission line structure (300) of claim 1, wherein said sacrificial material comprises an organic dielectric.

10. The transmission line structure (300) of claim 1, wherein said sacrificial material is removed by a dry plasma etch.

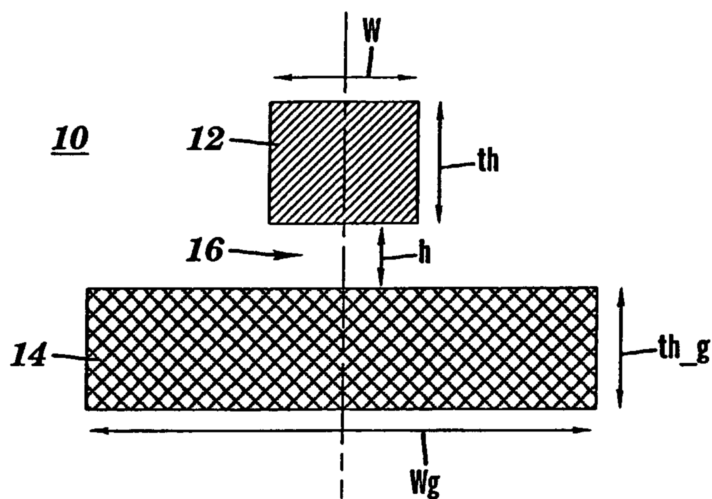


FIG. 1(a)
PRIOR ART

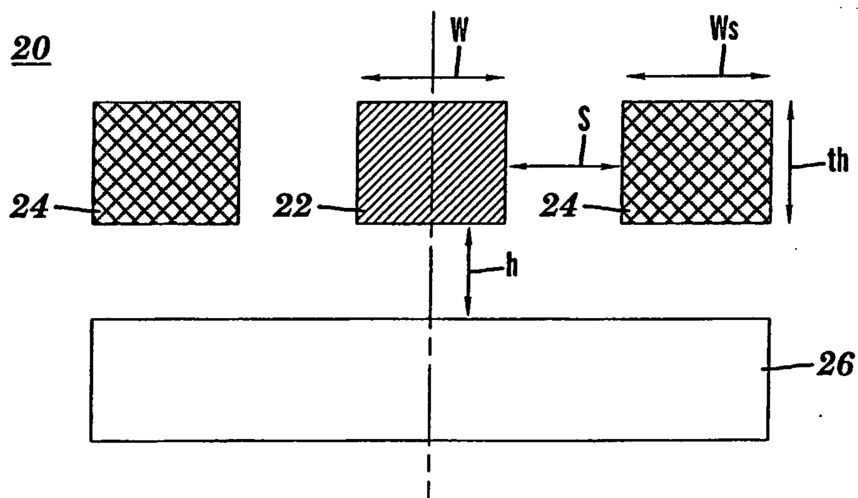


FIG. 1(b)
PRIOR ART

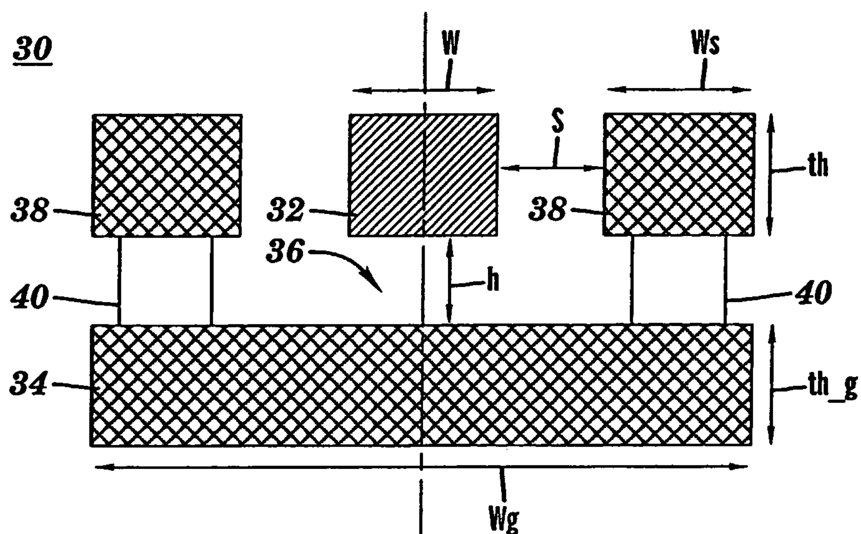


FIG. 1(c)
PRIOR ART

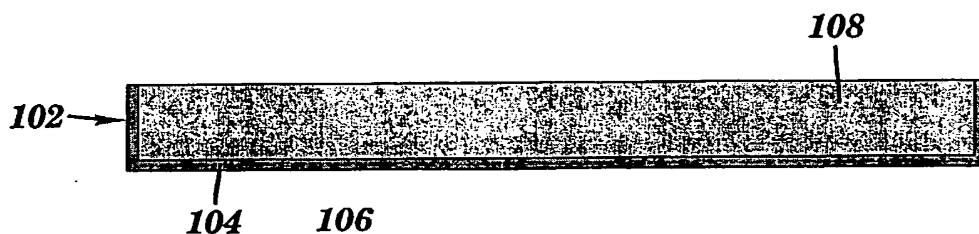


FIG. 2(a)

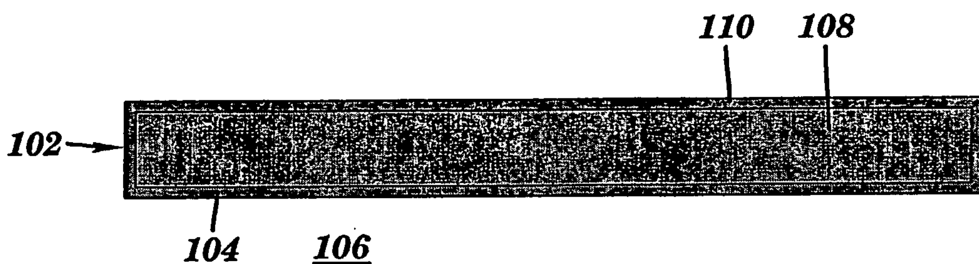


FIG. 2(b)

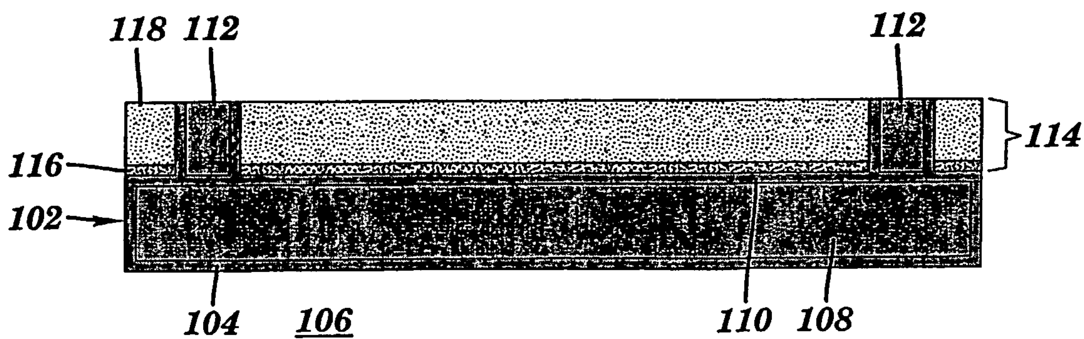


FIG. 2(c)

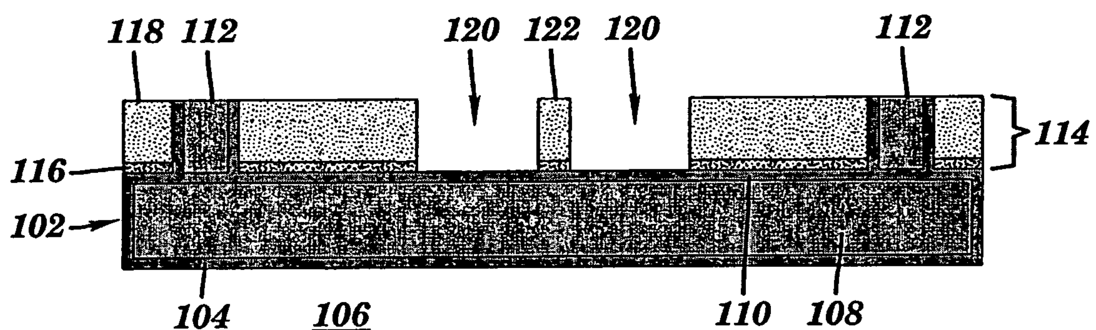


FIG. 2(d)

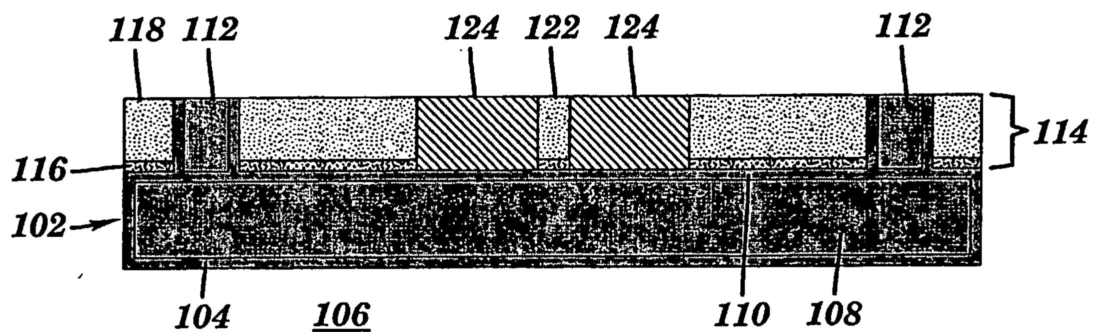


FIG. 2(e)

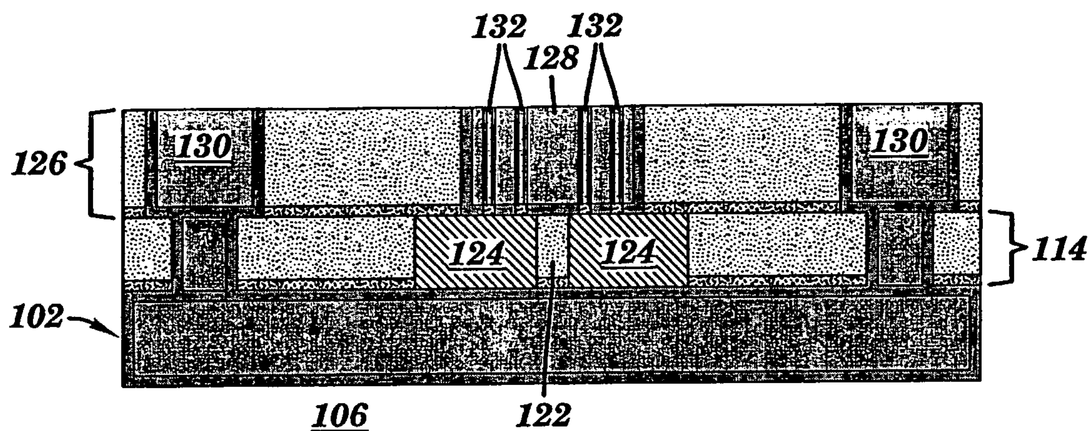


FIG. 2(f)

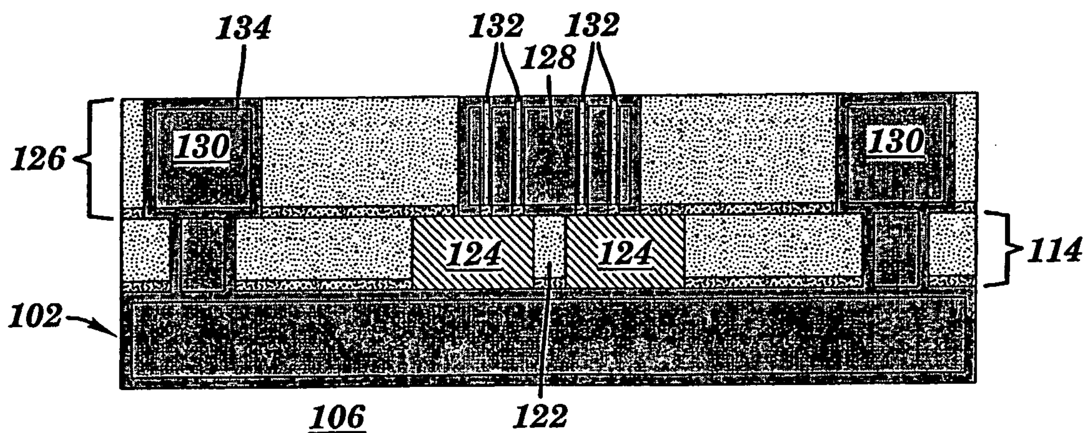


FIG. 2(g)

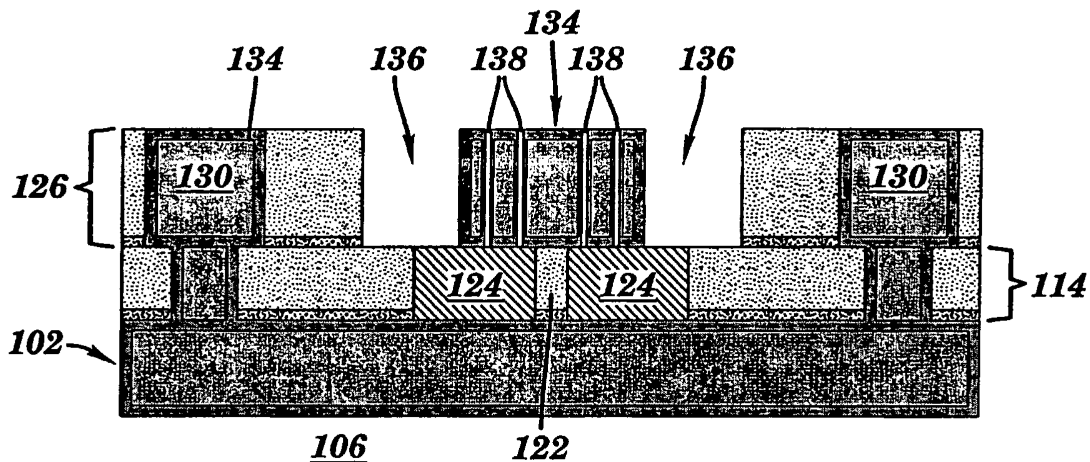


FIG. 2(h)

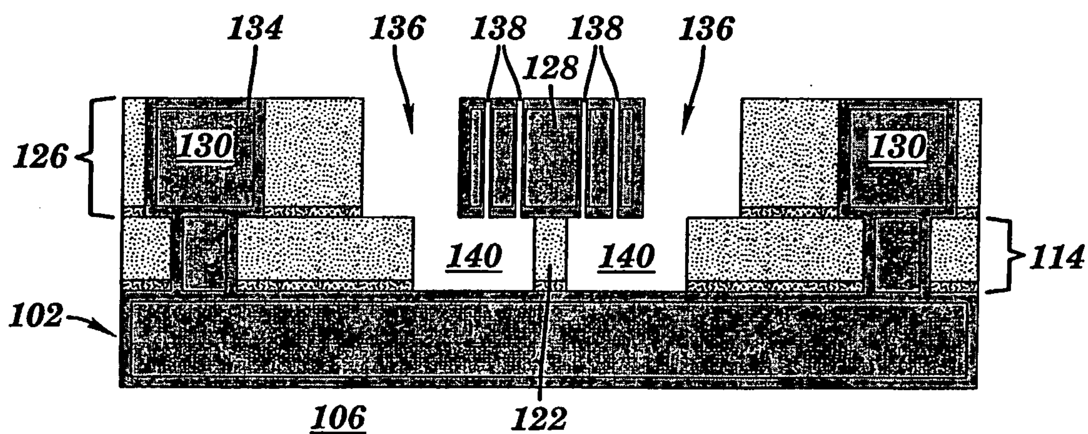


FIG. 2(i)

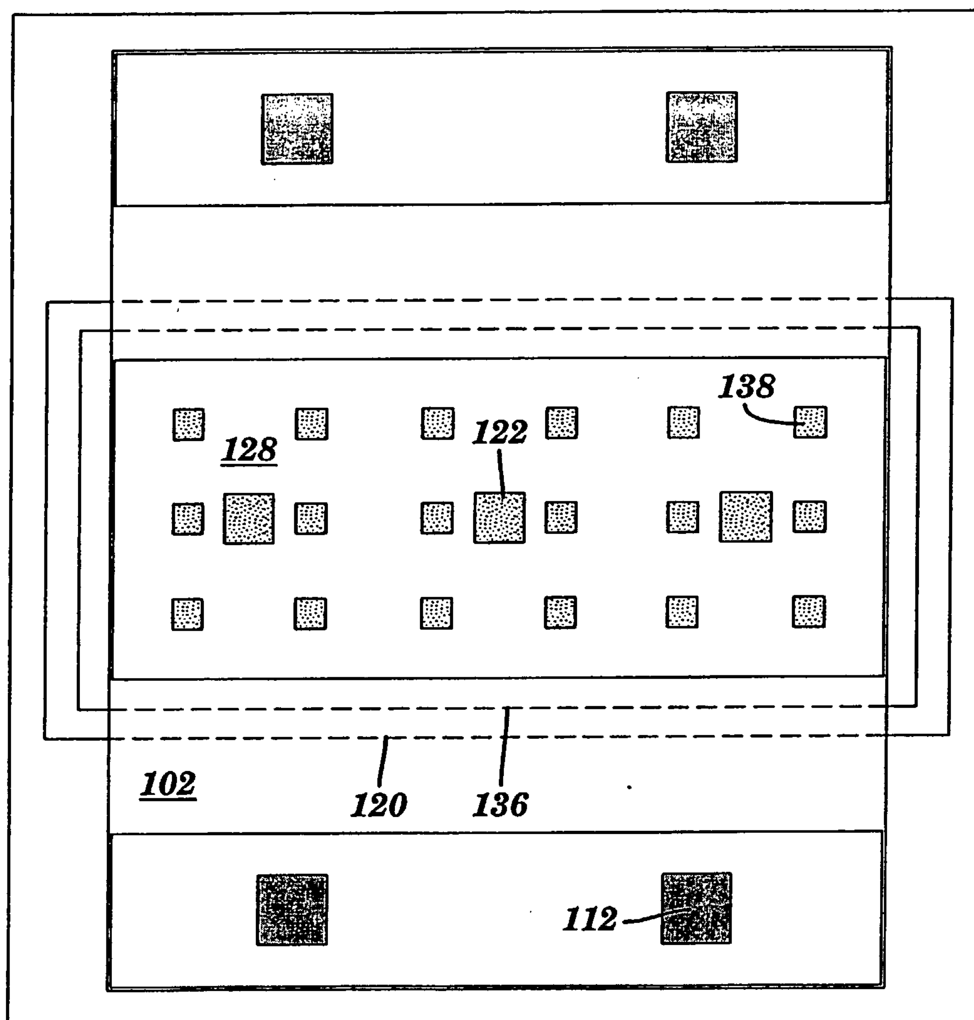


FIG. 2(j)

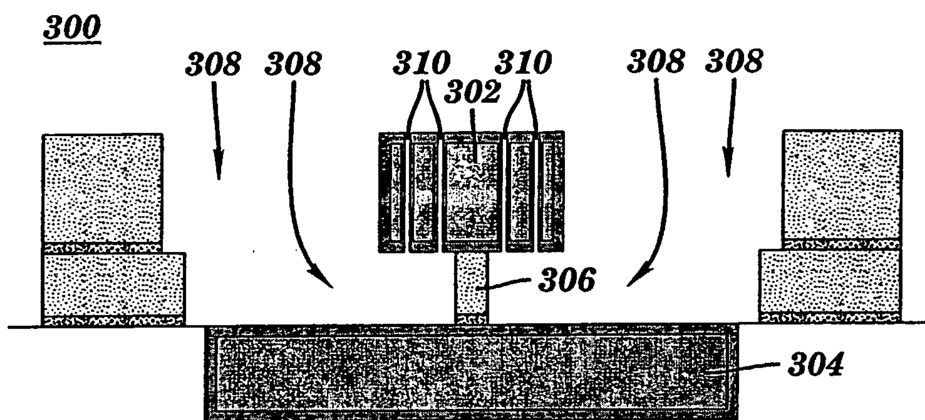


FIG. 3

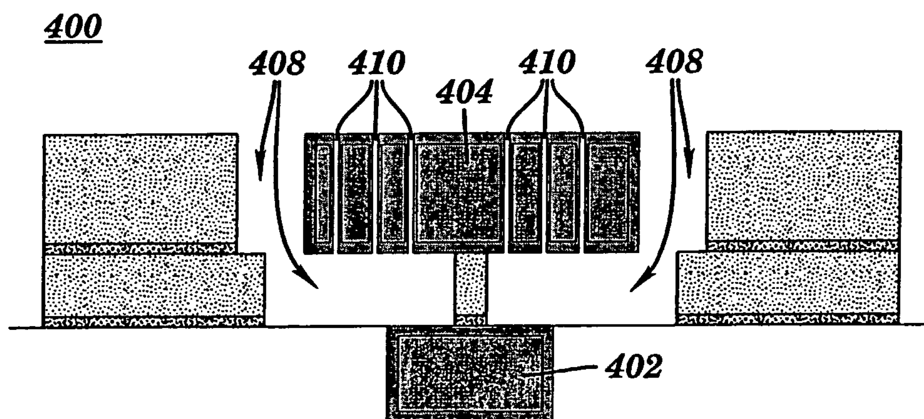


FIG. 4

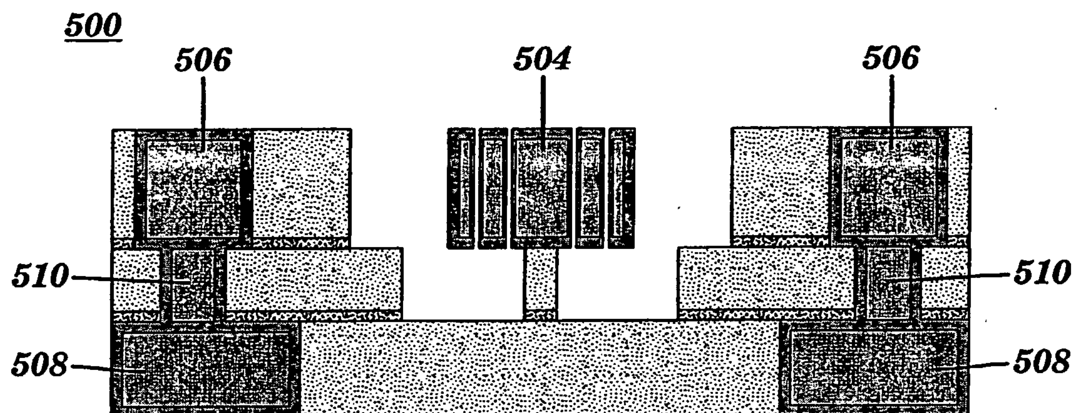


FIG. 5

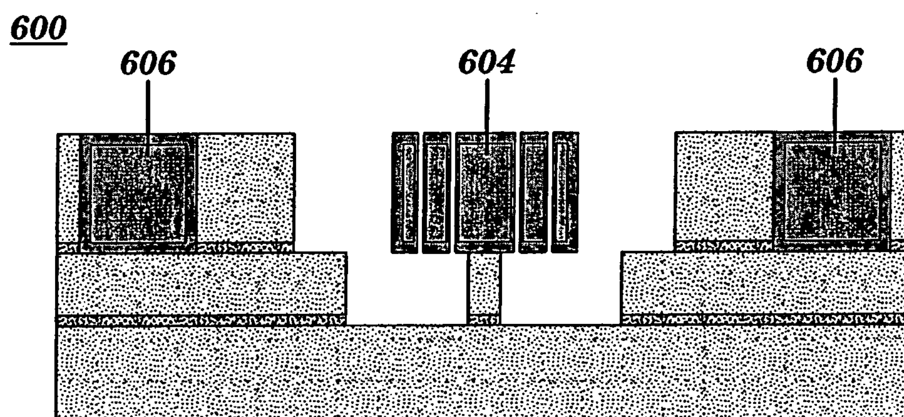


FIG. 6

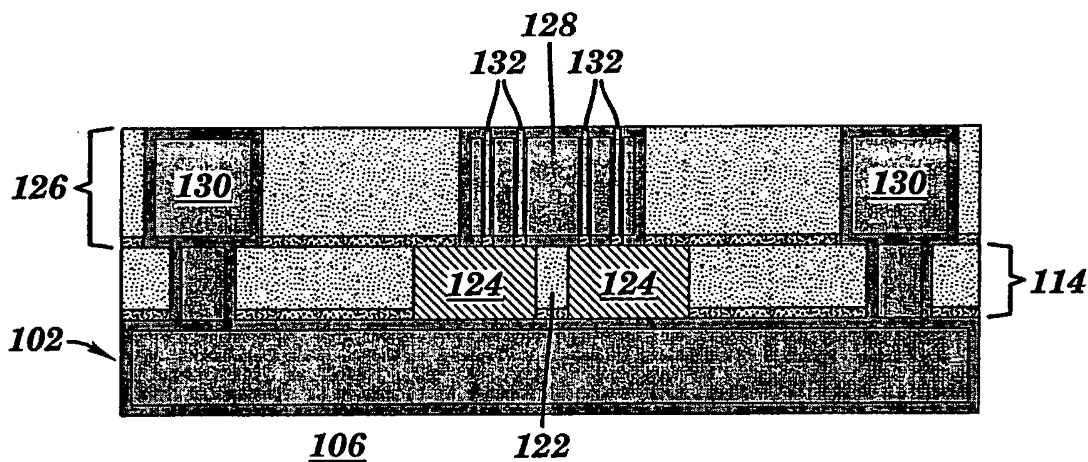


FIG. 7(a)

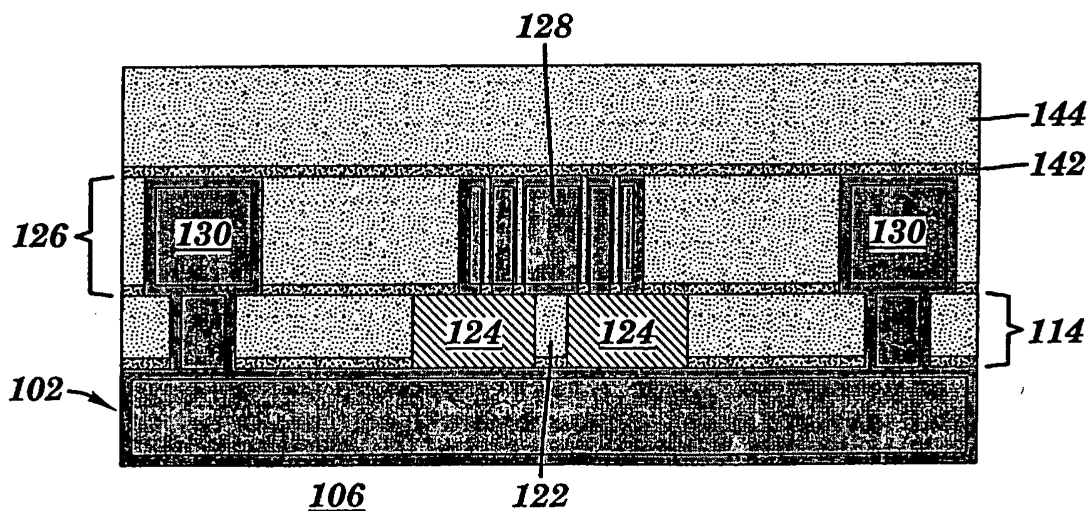


FIG. 7(b)

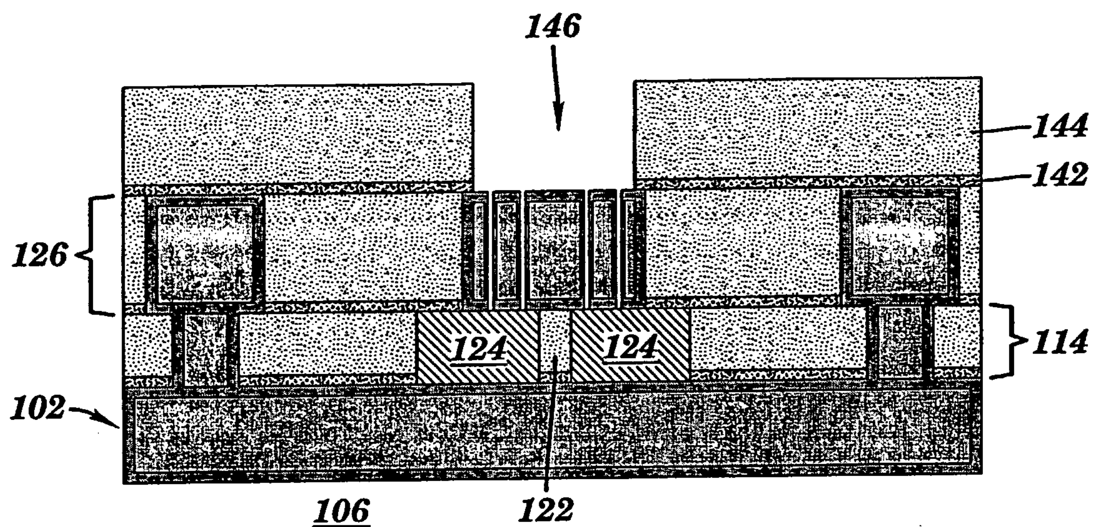


FIG. 7(c)

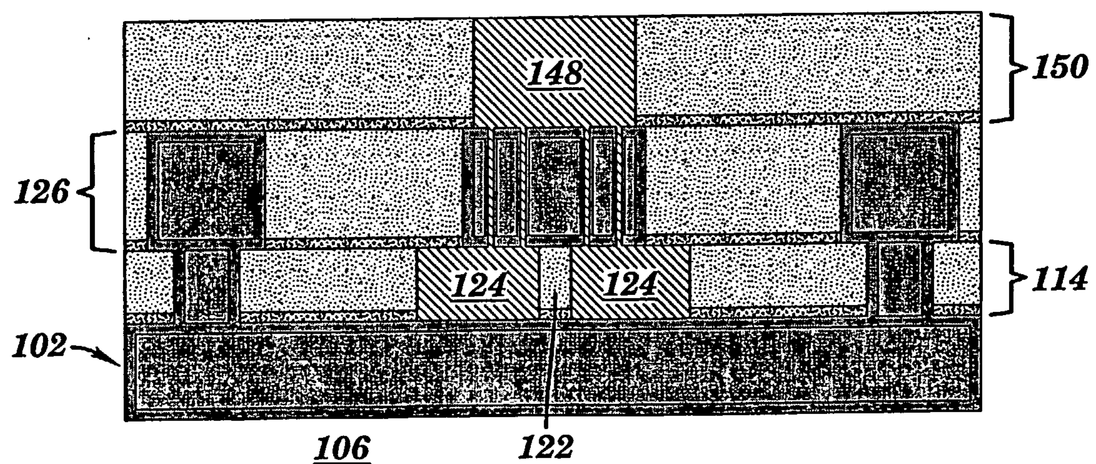


FIG. 7(d)

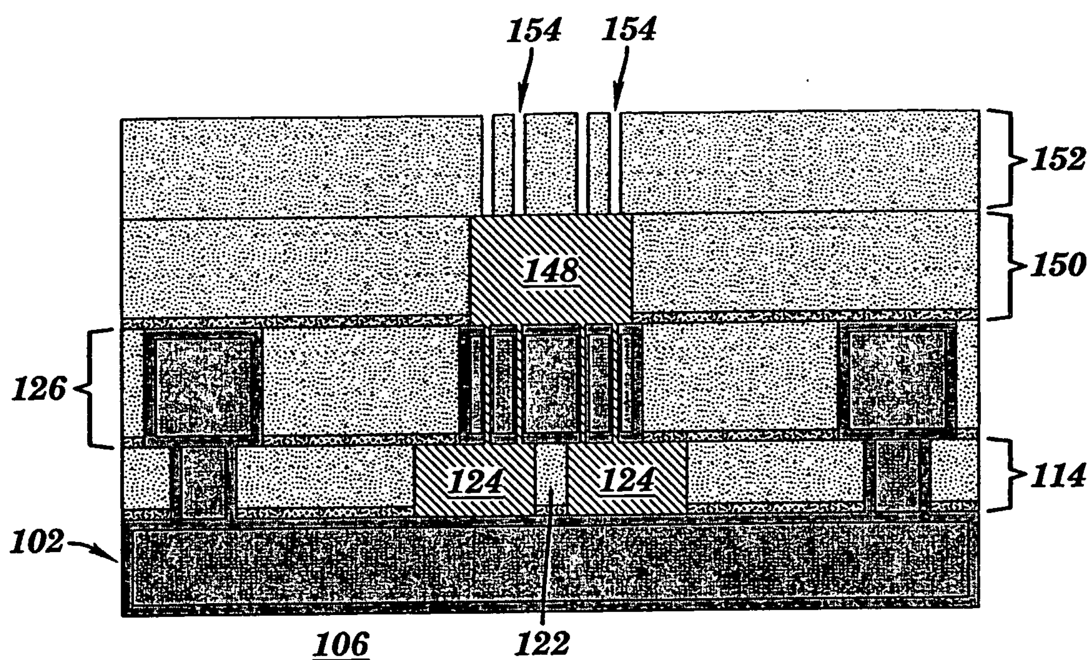


FIG. 7(e)

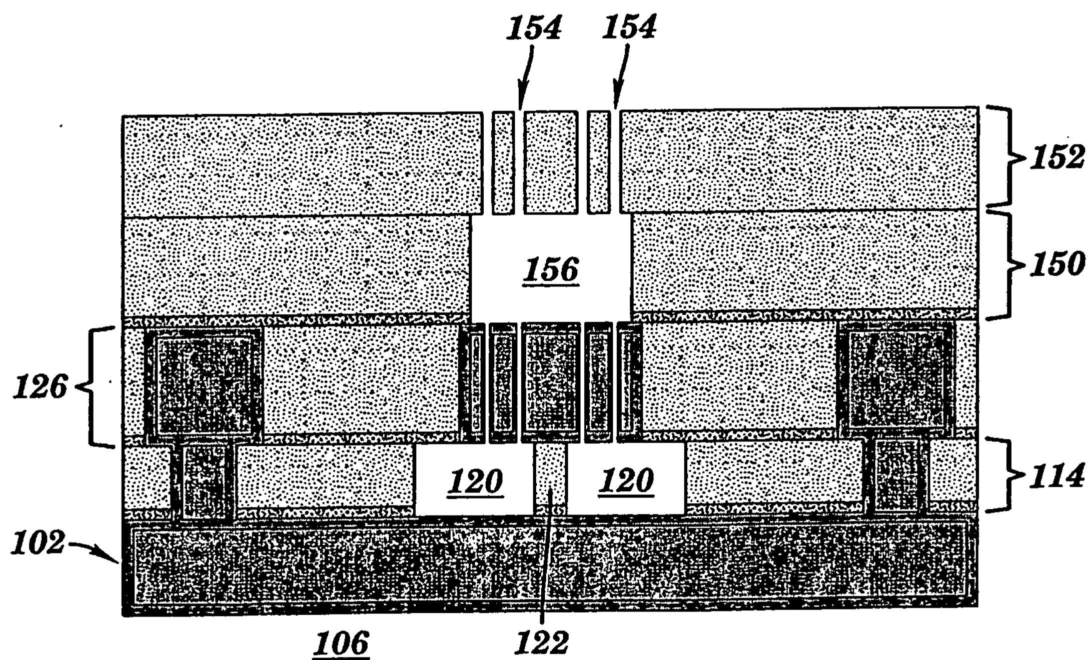


FIG. 7(f)

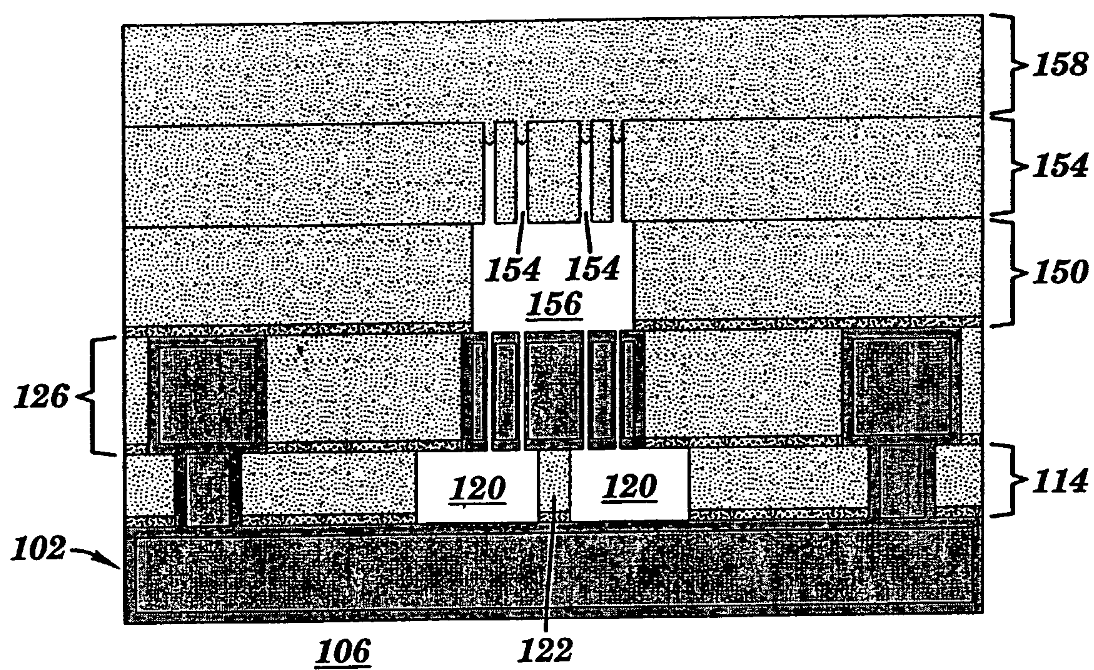


FIG. 7(g)

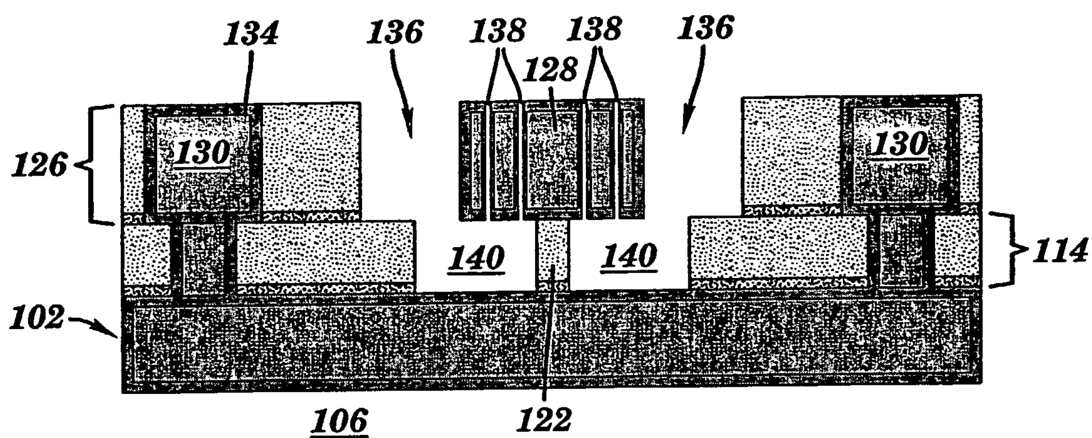


FIG. 8(a)

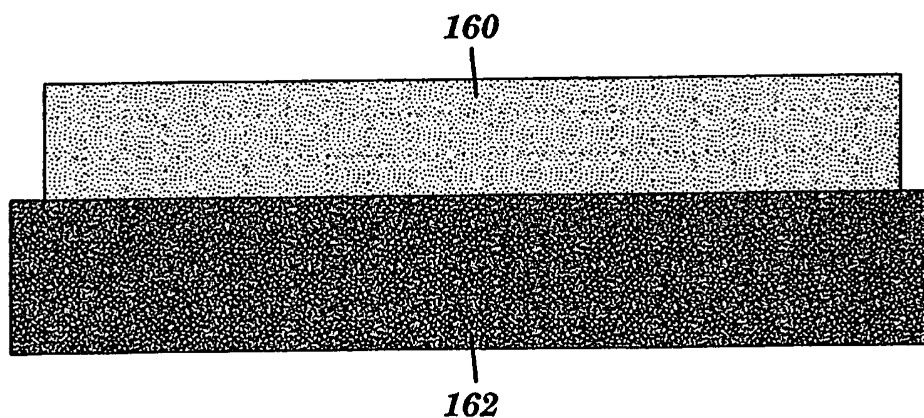


FIG. 8(b)

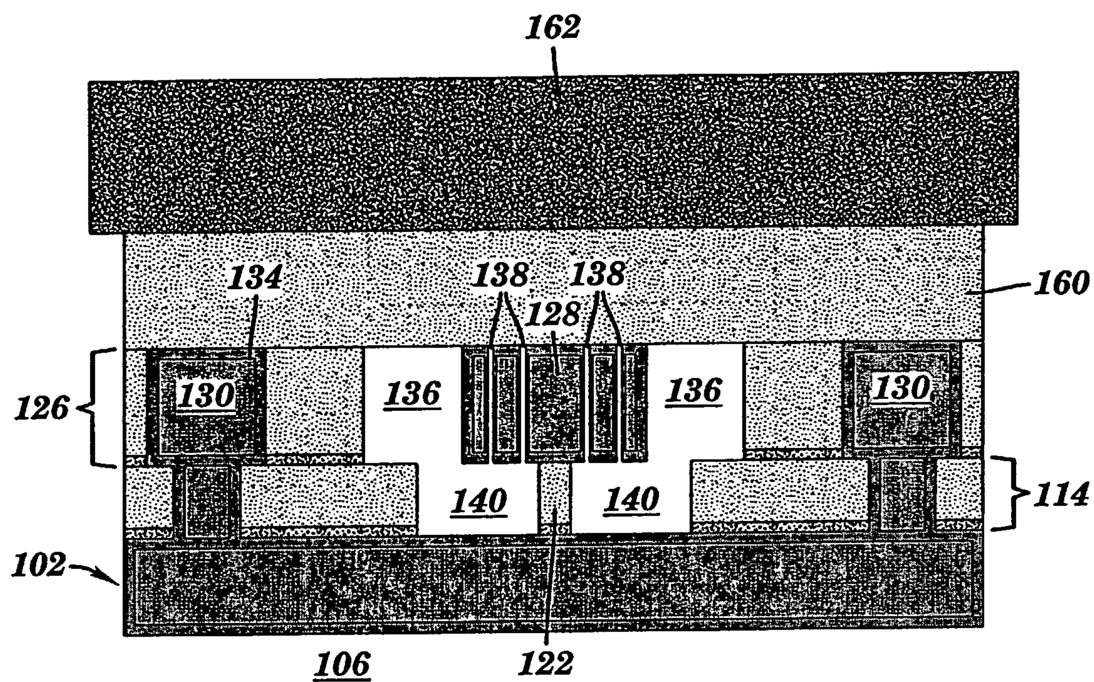


FIG. 8(c)

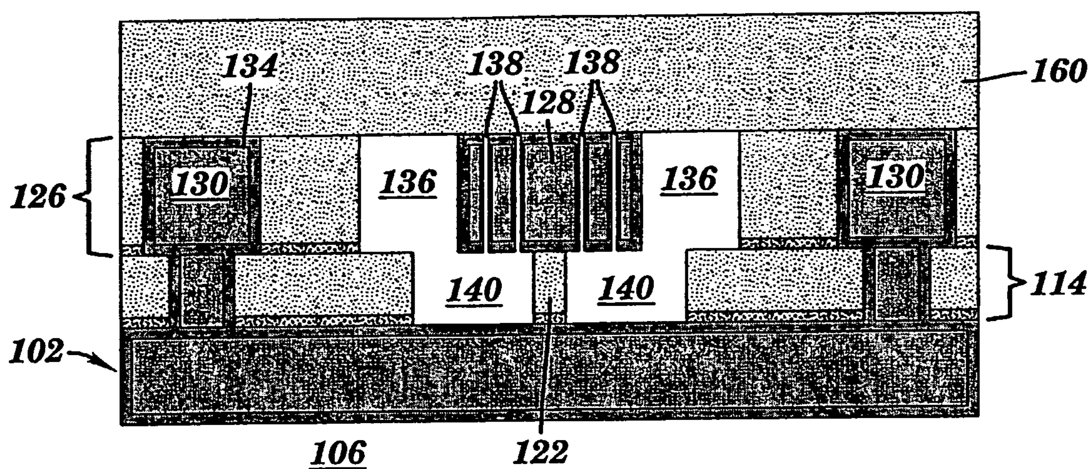


FIG. 8(d)

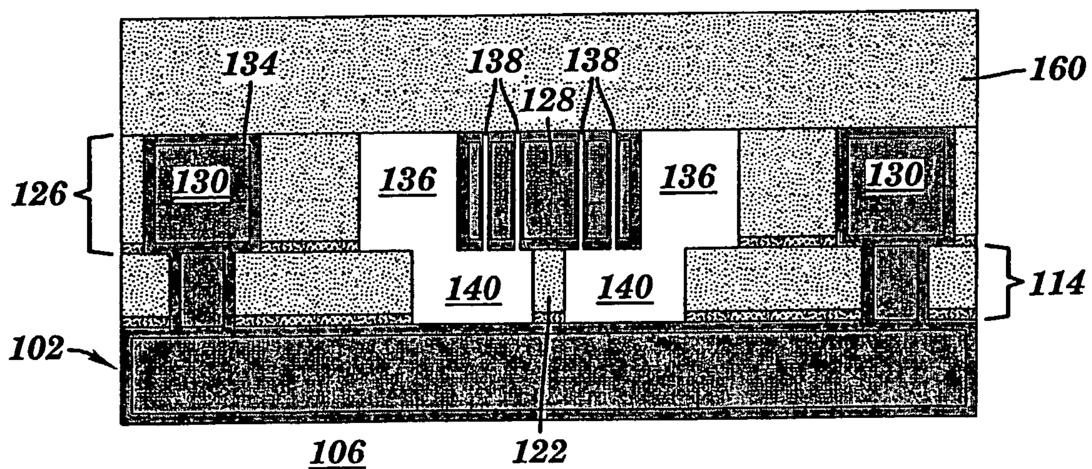


FIG. 9(a)

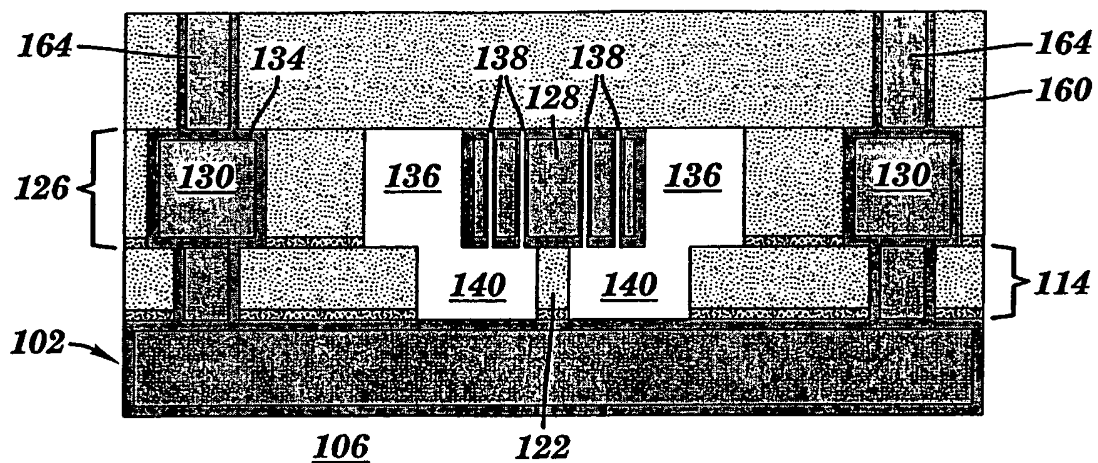


FIG. 9(b)

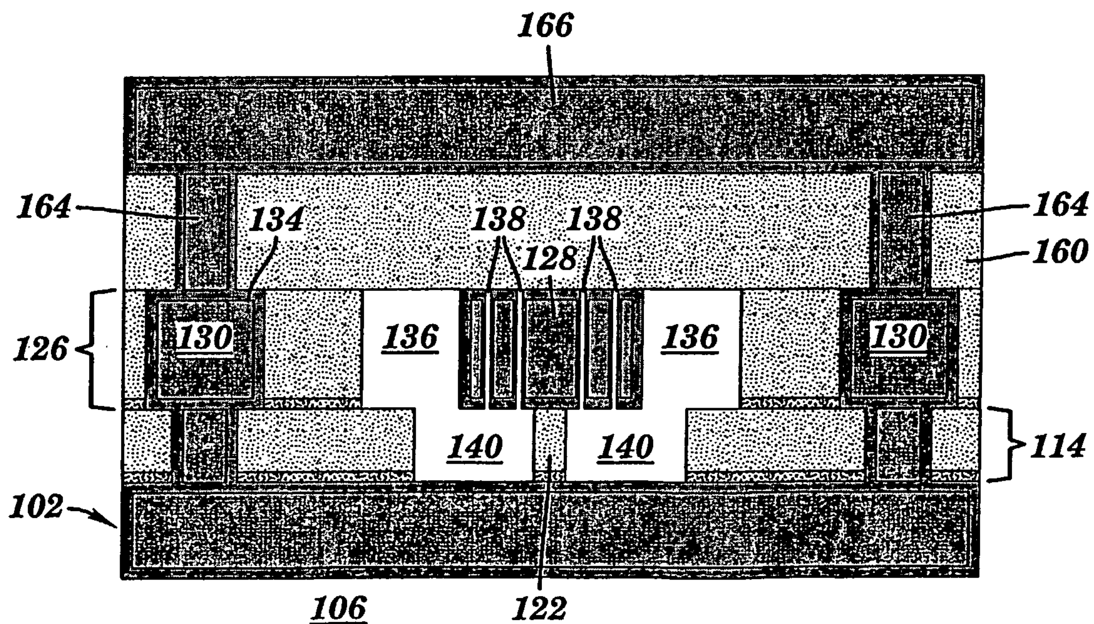


FIG. 9(c)

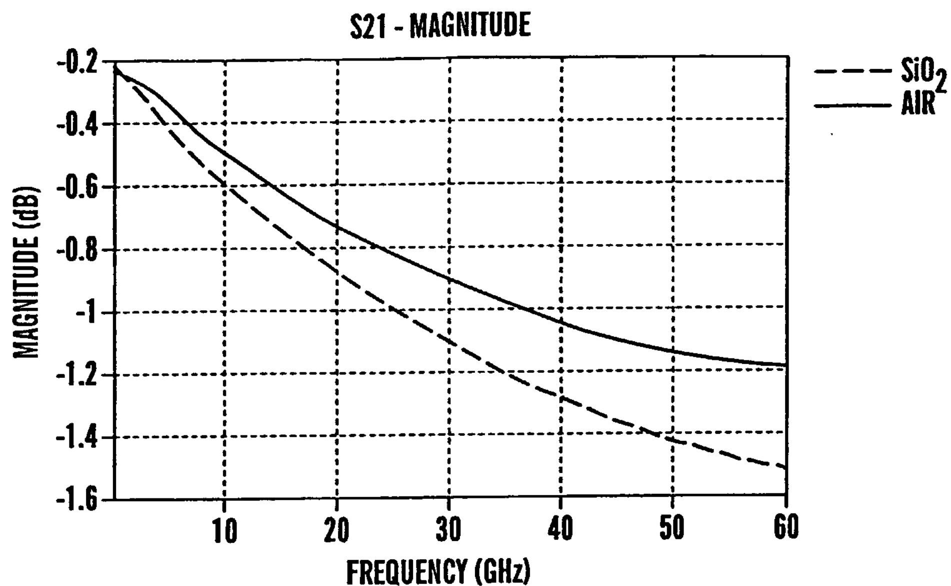


FIG. 10(a)

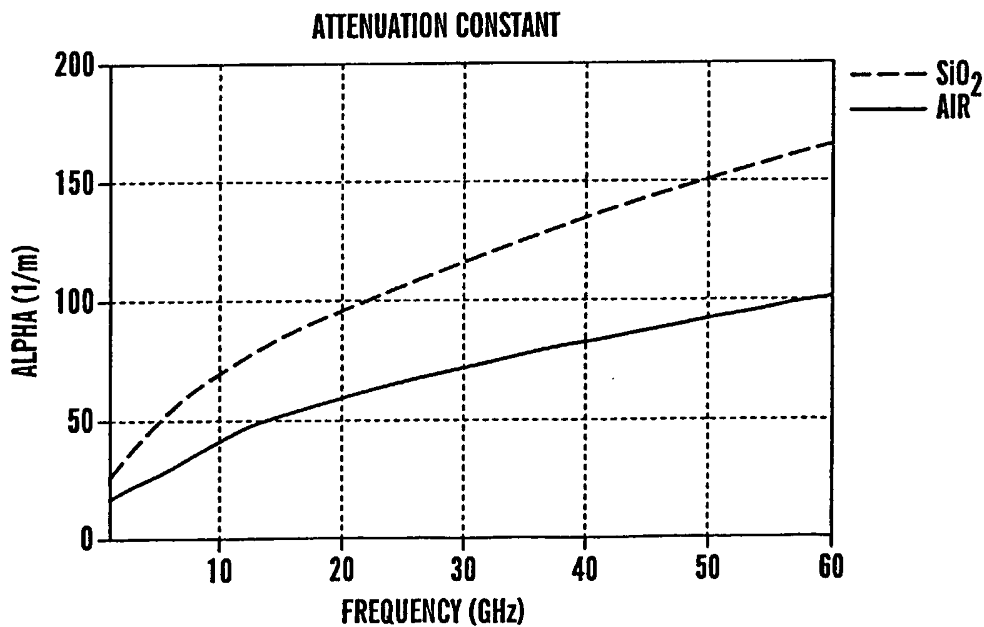


FIG. 10(b)

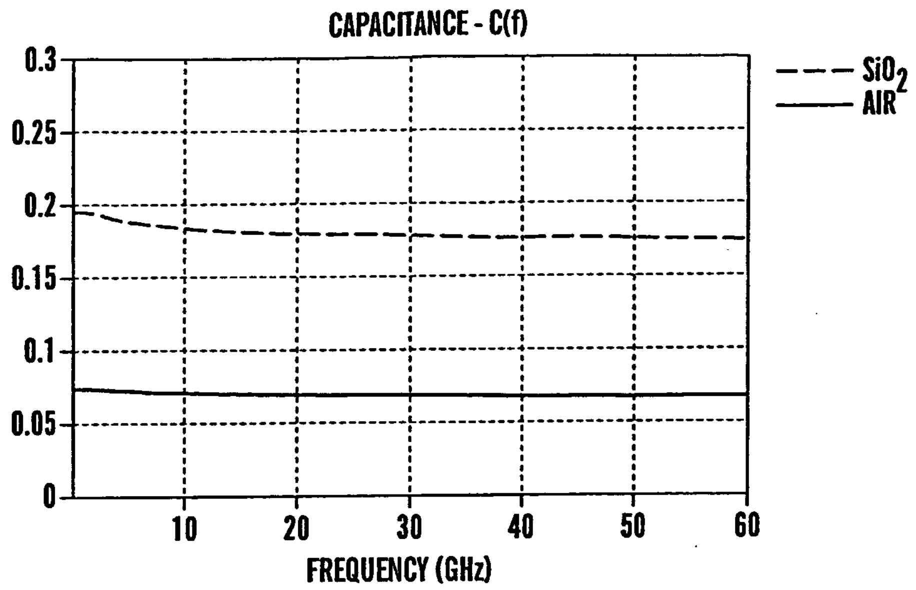


FIG. 10(c)

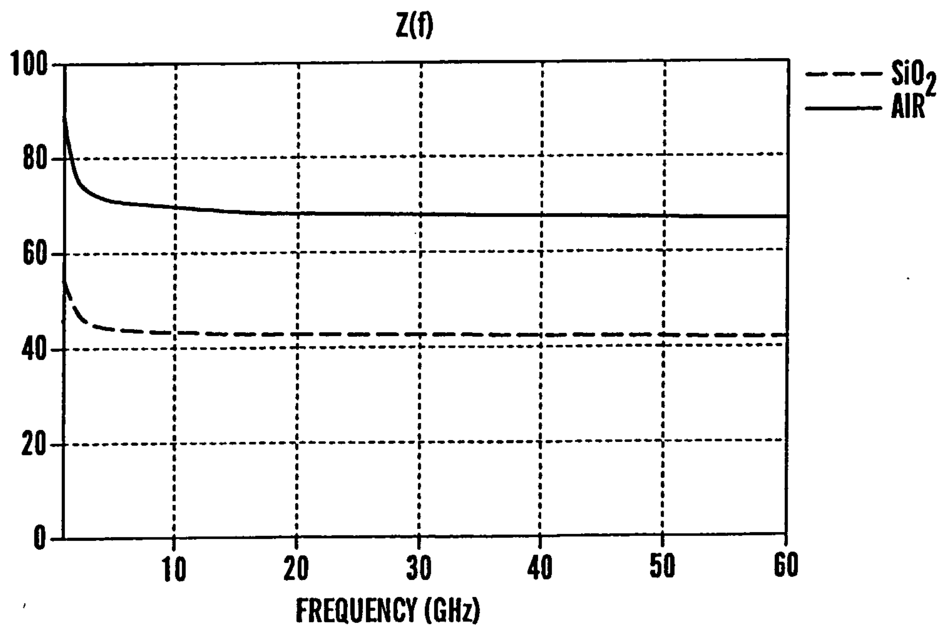
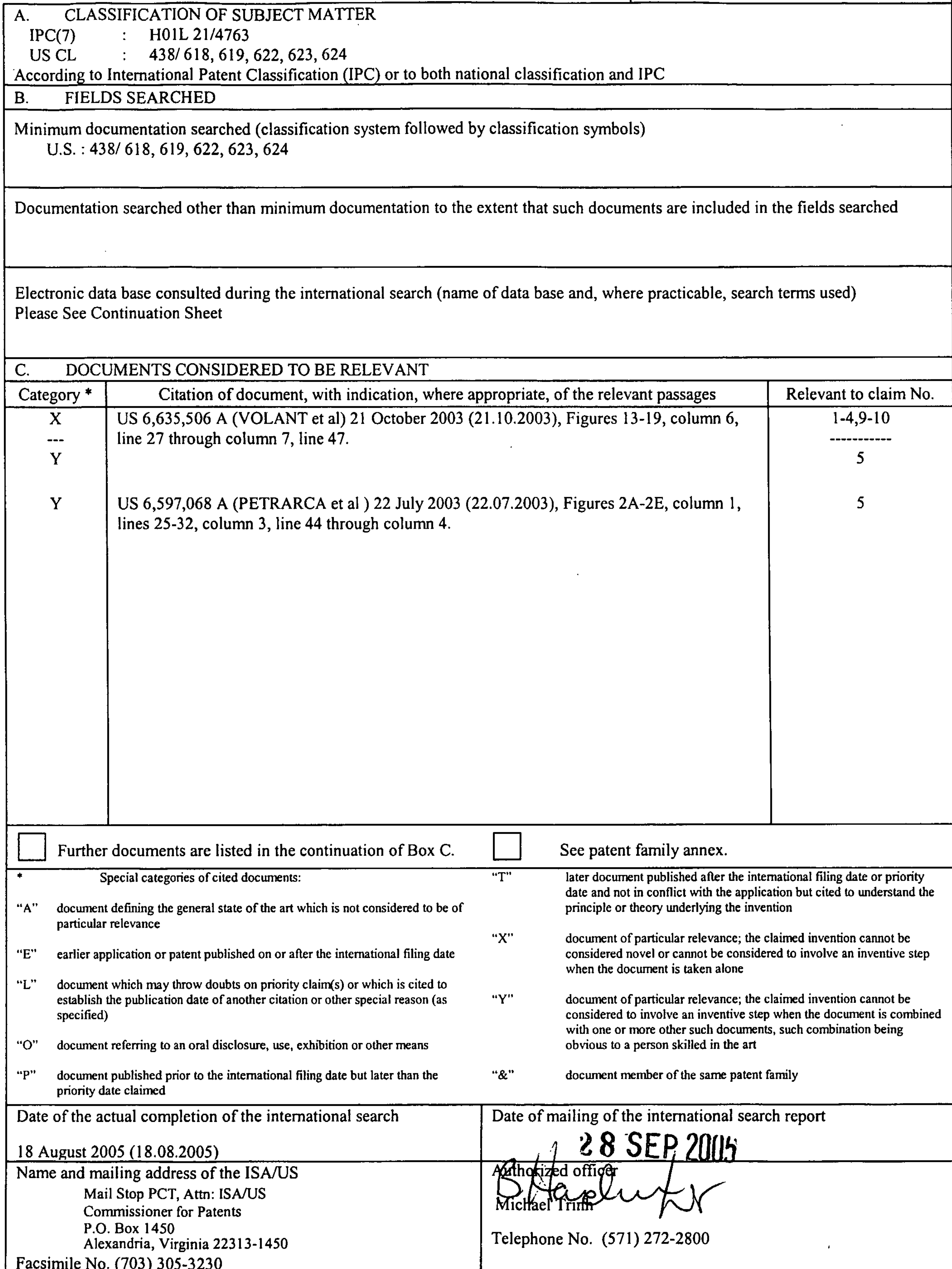


FIG. 10(d)



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/14645

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 21/4763
US CL : 438/ 618, 619, 622, 623, 624
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/ 618, 619, 622, 623, 624

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,635,506 A (VOLANT et al) 21 October 2003 (21.10.2003), Figures 13-19, column 6, line 27 through column 7, line 47.	1-4,9-10 ----------- 5
Y	US 6,597,068 A (PETRARCA et al) 22 July 2003 (22.07.2003), Figures 2A-2E, column 1, lines 25-32, column 3, line 44 through column 4.	5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 August 2005 (18.08.2005)	28 SEP 2005

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Continuation of B. FIELDS SEARCHED Item 3:
EAST Search of USPAT, US-PGPUB, JPO with terms: semiconductor, silicon, dielectric, insulator, sacrifical, transmission, microstrip, waveguide, hole, opening, etch, void, cavity, trench, gap