



(12) **United States Design Patent**
Koh et al.

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(54) **SMART CLOCK**

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(71) Applicants: **NAVER CORPORATION**,
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EM 006538070-0009 5/2019
JP HJ3101263900 6/2019

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Good Design Exhibition 2019 Installation and dismantlement guide
(Oct. 31, 2019).

(**) Term: **15 Years**

(Continued)

(21) Appl. No.: **29/758,771**

Primary Examiner — Katherine Glennon

(22) Filed: **Nov. 18, 2020**

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(30) **Foreign Application Priority Data**

Jun. 1, 2020 (KR) 30-2020-0024248

(51) **LOC (14) Cl.** **10-01**

(57) **CLAIM**

(52) **U.S. Cl.**
USPC **D10/15**

The ornamental design for a smart clock, as shown and
described.

(58) **Field of Classification Search**
USPC D10/1-5, 15, 21, 22-23, 28-29, 40-41;
D14/170-171, 175, 188
CPC G04G 17/00; G04G 17/02; G04G 17/04;
G04G 17/045; G04G 17/08; G04G
17/086; G04G 99/006; G04G 13/00;
G04G 13/02; G04G 13/021; G04G 9/00;
G04G 9/082; G04C 17/00; G04C
17/0025; G04C 17/0033; G04C 17/0041;
G04C 17/0091; G04C 19/00; G04C
19/02; G04C 19/04; G04C 21/00; G04C
21/02; G04C 21/04; G04C 21/12; G04C
21/16

DESCRIPTION

See application file for complete search history.

FIG. 1 is a top front perspective view of a smart clock,
showing our new design.
FIG. 2 is a front elevation view of the smart clock shown in
FIG. 1.
FIG. 3 is a rear elevation view of the smart clock shown in
FIG. 1.
FIG. 4 is a left elevation view of the smart clock shown in
FIG. 1.
FIG. 5 is a right elevation view of the smart clock shown in
FIG. 1.
FIG. 6 is a top plan view of the smart clock shown in FIG.
1; and,
FIG. 7 is a bottom plan view of the smart clock shown in
FIG. 1.

(56) **References Cited**

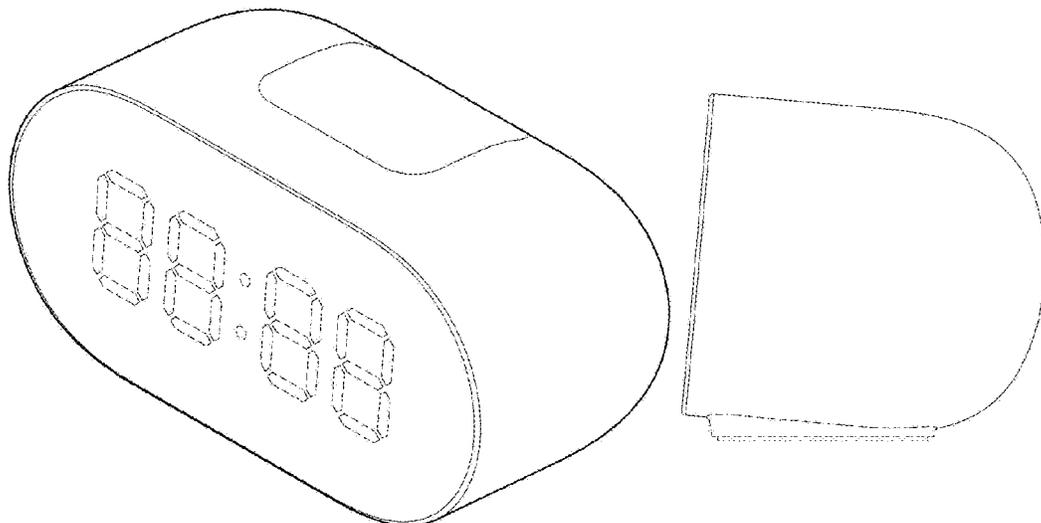
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The broken lines shown in the drawings illustrate the
portions of the article that form no part of the claimed
design.

(Continued)

1 Claim, 7 Drawing Sheets



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FIG. 1

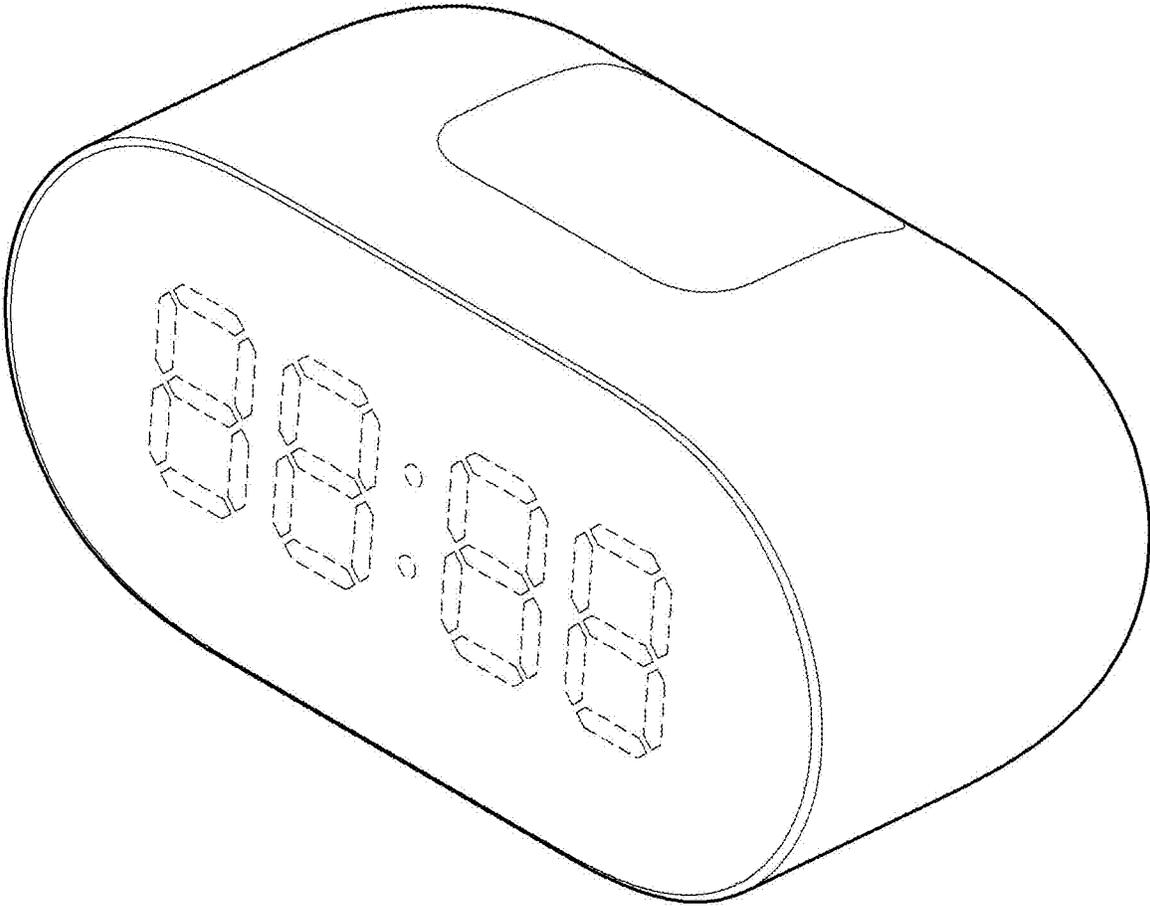


FIG. 2

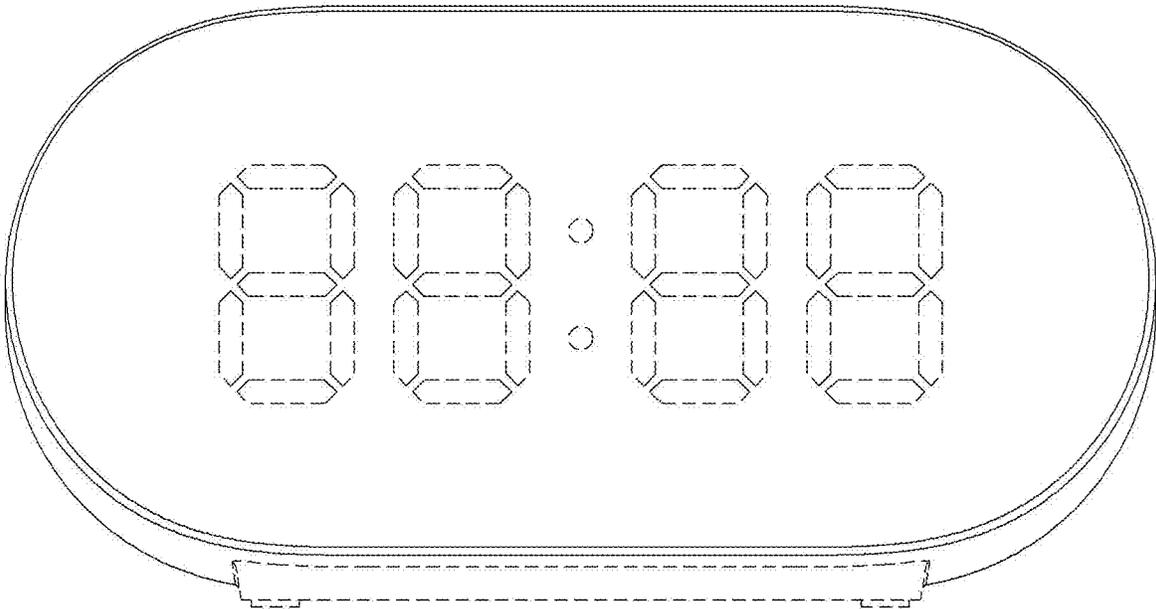


FIG. 3

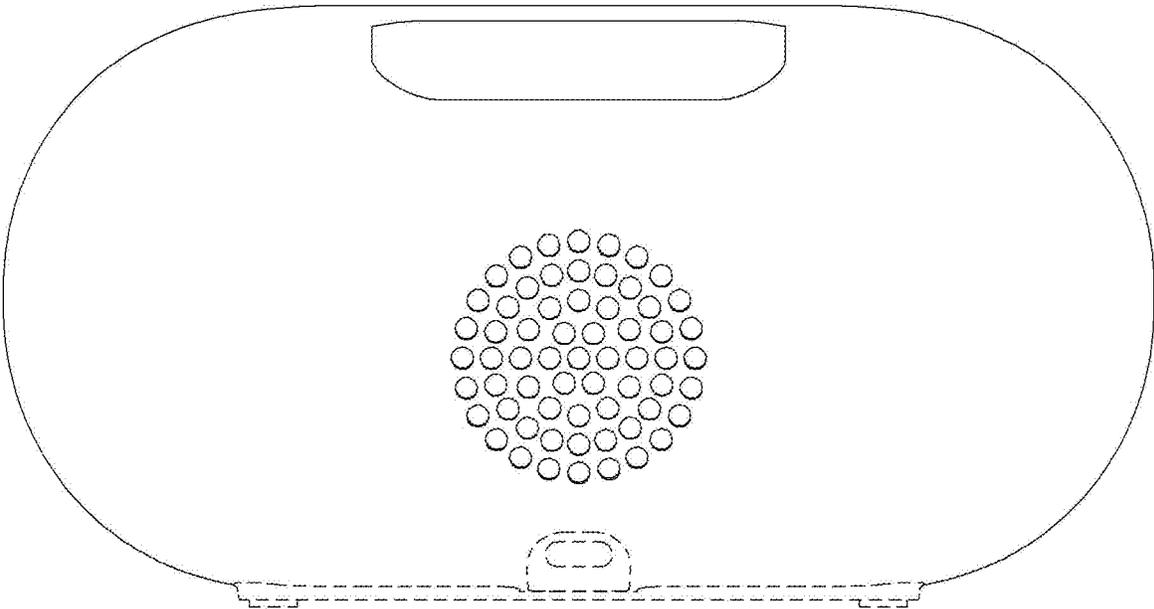


FIG. 4

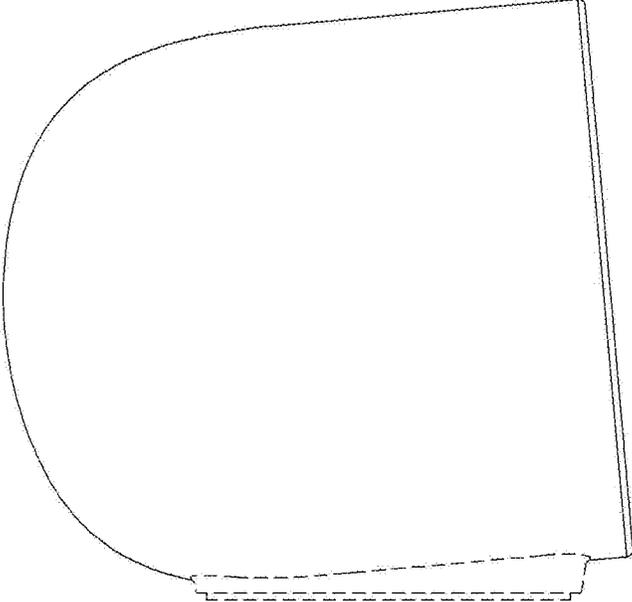


FIG. 5

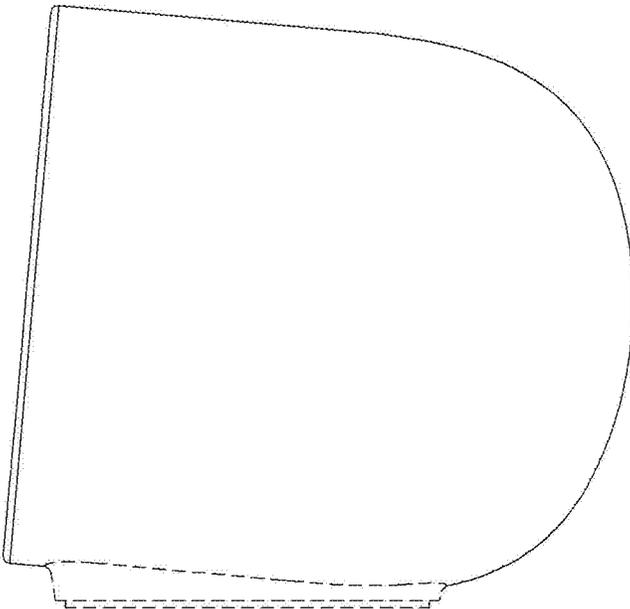


FIG. 6

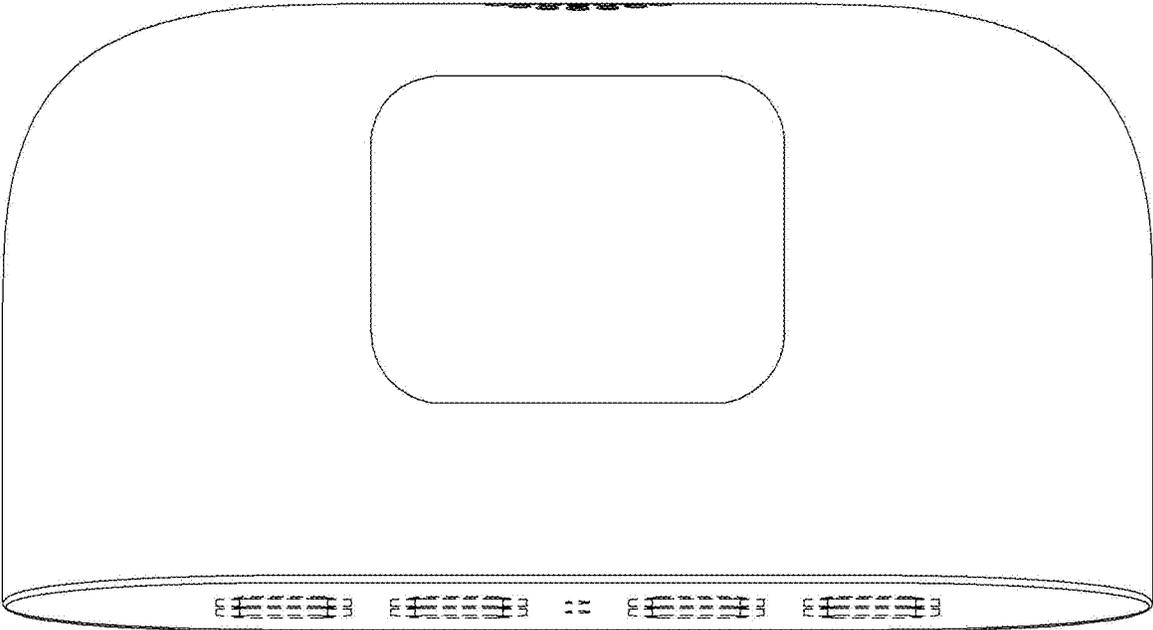


FIG. 7

