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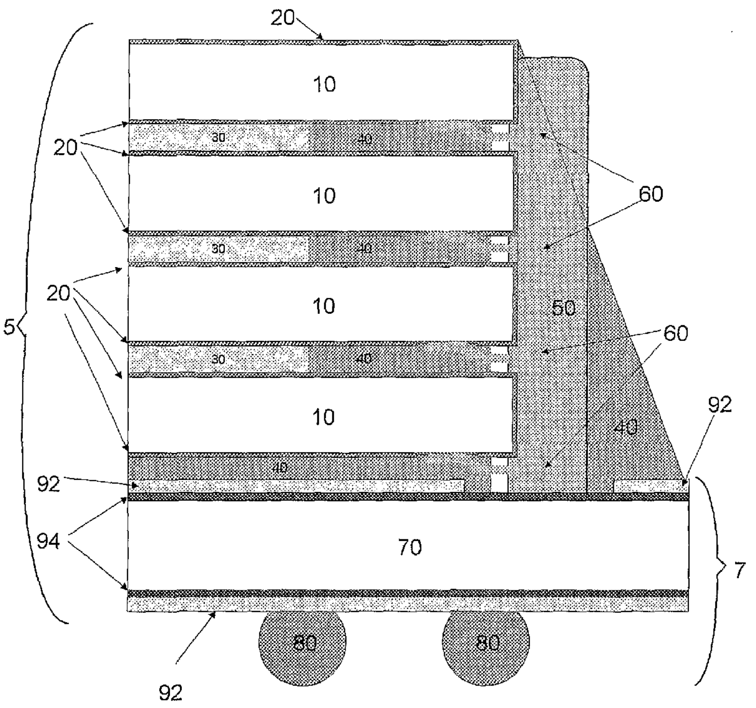
(54) **Title:** STACKED DIE BGA OR LGA COMPONENT ASSEMBLY

4-High Stack-on-BGA VIP
Cross Section



(57) Abstract: The present invention provides an apparatus for vertically interconnecting semiconductor die, integrated circuit die, or multiple die segments. Metal rerouting interconnects which extend to one or more sides of the die or segment can be optionally added to the die or multi die segment to provide edge bonding pads upon the surface of the die for external electrical connection points. After the metal rerouting interconnect has been added to the die on the wafer, the wafer is optionally thinned and each die or multiple die segment is singulated from the wafer by cutting or other appropriate singulation method. After the die or multiple die segments are singulated or cut from the wafer, insulation is applied to all surfaces of the die or multiple die segments, openings are made in the insulation above the desired electrical connection pads, and the die or multiple die segments are placed on top of one another to form a stack.. Vertically adjacent segments in the stack are electrically interconnected by attaching a short flexible bond wire or bond ribbon to the exposed electrical connection pad at the peripheral edges of the die which protrudes horizontally from the die and applying electrically conductive polymer, or epoxy, filaments or lines to one or more sides of the stack.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

STACKED DIE BGA OR LGA COMPONENT ASSEMBLY

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Title: Stacked Die BGA or LGA Component Assembly

CROSS REFERENCE TO RELATED APPLICATIONS:

The present application is related to provisional patent application No. 60/561,849, filed April 13, 2004 entitled "Stacked Die BGA or LGA Component Assembly", the details of which are hereby incorporated by reference, and the benefit of the earlier April 13, 2004 filing date is claimed in accordance with 35 USC 119 (e) (1).

Background of the Invention

The present invention relates to an apparatus for stacking and interconnecting integrated circuit die and/or multiple die segments of silicon, interconnecting the die and or multiple die segments on the edges of the stack using an electrically conductive polymer or epoxy, and mounting the stack of die on a BGA substrate.

For many years, electrical components such as transistors and integrated circuits have been made using wafers of semiconductor material, including silicon and/or germanium. Integrated circuits have been provided on the wafer using various techniques known as etching, doping, and layering. Individual integrated circuits that are provided on the wafer are referred to as die, and include contact points called bond pads for external electrical connections. Typically, the die on the wafer are separated from one another by cutting the wafer along boundaries defining the die. Once the die are cut from the wafer, they are referred to as chips or die, and are packaged for use. In recent years, the proliferation of more powerful electronic systems has led to an increased need for higher performance and higher density integrated circuit packages.

One method for creating higher density packages attempts to create an entire computer system on a single wafer using wafer scale integration (WSI) techniques. WSI technology attempts to laterally wire together all the die on a wafer using wires to interconnect the die. However, in order to create the necessary interconnections between the die, many wires are required that are extremely thin and difficult to create. Furthermore, the resulting interconnected die occupy a very large area, or footprint, on the electronic systems circuit board onto which the wafer scale integration device is attached for connection into the electronic system.

A second method for creating higher density packages attempts to reduce the area required for placing the chips on a circuit board by physically stacking the chips vertically. One chip stacking technique mounts individual die on ceramic carriers, encapsulates both the die and the carrier, stacks the carriers, and then mounts the stack on a printed circuit board. In this technique, all the die in the stack are interconnected by connecting the leads of the die to the printed circuit board via metal pins. This method results in an unusually high pin count on the circuit board which reduces the reliability of the circuitry because the high pin count increases the possibility that one of the many pins may become disconnected from the board.

Another chip stacking method uses a more complex process to stack die, as disclosed in U.S. Pat. No. 5,104,820 issued Apr. 14, 1992. This method modifies individual chips so that they may be stacked by adding a pattern of metalization, called rerouting leads, to the surface of the wafer. The rerouting leads extend from the bond pads on the chip to newly formed bond pads, and are arranged so that all the rerouting leads terminate on one side of the modified chip. Each modified chip is then cut from the wafer, and assembled into a stack. The stack is assembled in a manner such that all the leads of the modified chips are aligned along the same side of the stack. The side of the stack having the leads is then etched and polished so that a cross section of the leads on each of the modified chips is accessible. After the leads are exposed, a layer of metalization is applied to the leads along the side of the stack in order to electrically connect each of the modified chips in the stack. The stack is then mounted and connected to a substrate which in turn is connected to conventional circuitry.

This method of rerouting leads offers improvement in circuit density over prior methods but is complex and expensive. In addition, the rerouting leads extend over adjacent die, which are destroyed when the modified chip is cut out of the wafer. In this method, multiple die are sacrificed for every chip that is modified.

Another method for creating higher density circuits creates stacks from entire wafers, rather than individual chips, to form a wafer array. In some devices, the wafers in the stack are electrically interconnected using solid vertical columns of metallic conductive feed-throughs, such as copper. The use of solid feed-throughs to interconnect wafers may cause damage to the array due to differential thermal coefficients of expansion during thermal cycles. Furthermore, the process is costly and makes the wafers difficult to separate for repairs.

Other methods also exist to interconnect stacks of wafers, as disclosed in, for example, U.S. Pat. No. 4,897,708 issued Jun. 30, 1990, and U.S. Pat. No. 4,954,875 issued Sep. 4, 1990. These methods provide each wafer in the stack with coned-shaped through-holes which expose bonding pads on the wafers. The bond pads of the wafers in the stack are then electrically connected by either filling the through holes with electrically conductive liquid, or inserting an electrically conductive compliant material into the through holes, to provide a continuous vertical electrical connection between the wafers. While avoiding the disadvantages of using solid vertical columns of metal to interconnect wafers, the use of electrically conductive liquids and conductive materials requires special tooling to fill the through holes. Furthermore, for some applications, it may not be desirable to use stacks of entire wafers due to size constraints of the electrical device.

Individual semiconductor die are typically assembled in packages that allow the integrated circuit die to be attached to printed circuit boards and to allow electrical connections to be made between the integrated circuit die. There are many types of packages that are used for this purpose. The BGA package and the TSOP package are 2 types of packages in common use for assembling memory die and mounting the assembled die on a printed circuit board. There are a number of methods for stacking packaged integrated circuits, but in general, they suffer from a size disadvantage, and a performance disadvantage, due to the added electrical parasitics arising from the necessary lengths and characteristics of the inter-package interconnections. Due to the large physical size of the packages, there is a limit to the number of packages which may be stacked on top of each other, typically 2, to avoid thermo-mechanical problems. Stacks of packaged integrated circuits have been recently popular but take up too much board space, are too thick, and will not operate at the high speeds being required by advanced memory devices such as DDR2 and DDR3 DRAM.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved method and apparatus for stacking and interconnecting integrated circuit die and multiple die segments.

The present invention provides an apparatus for vertically interconnecting semiconductor die, integrated circuit die, or multiple die segments. Metal rerouting interconnects which extend to one or more sides of the die or segment can be optionally added to the die or multi die segment to provide edge bonding pads upon the surface of the die for external electrical connection points. After the metal rerouting interconnect has been added to the die on the wafer, the wafer is optionally thinned and each die or multiple die segment is singulated from the wafer by cutting or other appropriate singulation method. After the die or multiple die segments are singulated or cut from the wafer, insulation is applied to all surfaces of the die or multiple die segments, openings are made in the insulation above the desired electrical connection pads, and the die or multiple die segments are placed on top of one another to form a stack.. Vertically adjacent segments in the stack are electrically interconnected by attaching a short flexible bond wire or bond ribbon to the exposed electrical connection pad at the peripheral edges of the die which protrudes horizontally from the die and applying electrically conductive polymer, or epoxy, filaments or lines to one or more sides of the stack.

According to a further aspect of the present invention, a thermally conductive epoxy preformed sheet is provided so that the stack of segments are epoxied together. The thermally conductive epoxy preform includes a plurality of glass spheres randomly distributed within the preform.

The interconnected die stack is then mounted and electrically connected to the top surface of a substrate, consisting of conducting and insulating layers, and having electrical connection points on the top surface of the substrate aligned under the vertical filaments or lines that have been formed along the sides of the die stack, and having solder balls on the bottom of the substrate, or other connection means, for electrically connecting and mounting the bottom of the substrate to a printed circuit board.

Other objects, features and advantages of the present invention will become apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a diagram illustrating a single semiconductor die with original connection pads running down the center of the die, and rerouting lines connecting the original connection pads at the center of the die with new connection pads located at the edges of the die.

Figure 2 is a diagram illustrating a cross sectional side view of a semiconductor die showing the die coated with a conformal, insulating coating.

Figure 3 is a diagram illustrating a cross section view of the semiconductor die showing the conformal coating and openings in the conformal coating above the original connection pads which run down the center of the semiconductor die.

Figure 4 shows a semiconductor die with connection pads around the periphery of the die.

Figure 5 shows a semiconductor die with peripheral pads, either original or relocated, coated with a conformal insulative coating, and with openings in the insulative coating located above the peripherally located electrical connection pads.

Figure 6 is a cross section drawing of a completed 4-high stack on BGA.

Detailed Description of the Invention

Referring to Figure 1, semiconductor die 10, with original connection pads 60 have had an insulating layer applied to the top surface, 30 of all of the die while the die are still connected together in a wafer form. A metal layer is deposited and defined using photolithography, to reroute the electrical signals from the original connection pads 60 to new locations at the edge of the die. An additional layer of insulating material is optionally applied above the metal layer, and openings are made in the top layer of insulating material at the relocated pad locations at the edge of the semiconductor die, and optionally at the original pad locations down the center of the top surface of the die.

Referring to Figure 2, the semiconductor die, 10, has been thinned by grinding or lapping, and has been singulated from the semiconductor wafer, and said semiconductor die has been coated with a conformal insulating coating 20.

Referring to Figure 3, openings have been made in the coating, 20, above original connection pads, 60, of semiconductor die, 10.

Referring to Figure 4, this shows a semiconductor die 70 with connection pads 80 located around the periphery of the die top surface.

Referring to Figure 5, this shows openings in the conformal coating material at locations 90 on a semiconductor die whose electrical connections are located at the edges of the surface of the die.

Figure 6 depicts the vertical stack assembly component 5, consisting of semiconductor die 10, with conformal coating 20. The semiconductor die 10 having metallic conducting elements 60, one end of which are connected to electrical connection points at the periphery of the die 10, and the other end of the metallic conducting elements are embedded in the vertical conducting polymer 50. The vertical conductive polymer 50 is adjacent to the edge of the stack of the die and electrically connects the die to the top electrical conducting surface, 94, on the substrate 7.

Also shown in Figure 6 is the epoxy perform 30 used to laminate the die 10 to each other in a stack by bonding to the conformal coating 20 on each of the die.

Figure 6 shows the stack of die 10 laminated to each other with epoxy perform 30, and connected electrically by horizontal conducting elements 60 to vertical conducting element 50 and mounted on substrate 7. The substrate is shown having conducting layers 94 on its top and bottom surface, a core 70, solder mask 92 on the bottom surface, and solder balls 80 connected to the bottom of the substrate. Additionally, an underfill material 40 has been applied so that it fills the space between the bottom die in the stack and the substrate, 70, forms a filet with the edge of the stack, and fills in the gap between layers from the edge of the perform 30 to the edge of the die.

The foregoing has described a high density, low parasitic stacked die BGA or LGA component assembly. It should be apparent that numerous and various components can be utilized with the present invention, as described below.

For instance, the present invention can comprise a stack of semiconductor or integrated circuit die mounted on a substrate and laminated to each other. The die can optionally have one or more metal rerouting layers to interconnect the original die connection pads with new connection locations at the edge of the top surface of the die. The new connection locations are desirable for vertical interconnection.

The die can have a conformal, insulating coating, where the coating can be a polymer. The polymer coating can parylene, and the insulating coating can have openings above specific new connection locations at the edge of the top surface of the die as required by the specific component design.

The openings can be made, for example, by removing the polymer with laser ablation, and by removing the polymer with a plasma etcher.

The openings can be made by preventing the deposition of the polymer coating in selective areas above connection pads on the die. The die can be laminated on top of each other with an electrically insulating polymer or epoxy preform. The insulating preform can be thermally conductive.

The insulating preform optionally can include spheres to maintain a fixed spacing or separation between the semiconductor die after lamination. The spheres can be made of glass, ceramic, quartz, plastic, Teflon, polymer, or having a metal coating.

The electrically insulating polymer can be an epoxy. The die can be laminated on top of each other with a liquid polymer that is cured to form a solid bond between the layers in the stack. The insulating polymer can optionally include spheres to maintain a fixed spacing or separation between the semiconductor die after lamination, where the spheres can be made of glass, ceramic, quartz, plastic, Teflon, a polymer, and/or a metal coating.

The electrically insulating polymer can consist of epoxy, where the die can be any semiconductor die, such as memory die, where the memory die can be SDRAM, DDR-1, DDR-2, DDR-3, or any other DRAM. The memory die can be NAND Flash, NOR Flash, M-RAM, F-RAM, E^2 or any other Non-Volatile Memory. The memory die can be SRAM.

The stack can be electrically connected vertically, where the vertical electrical connection comprises a conductive polymer. The conductive polymer can be a conductive epoxy, such as silver filled (having particles of silver mixed with the polymer), gold filled (having particles of gold mixed with the polymer), the conductive epoxy being filled with metallic particles (having particles of metal mixed with the polymer).

The electrical connection can include one or more metallic conducting elements bonded to the relocated pad locations on the surface of each die and extending, both physically and electrically from the relocated pad into the vertical conductor so that one end of the conductor is embedded within the conductive polymer. The metallic conducting elements can be a bond wire, bond ribbon. The metallic conducting element can be gold, aluminum, copper, or palladium, on any combination of conducting materials such as gold, aluminum, copper, or palladium. The metallic conducting elements can exist as a metal lead frame with tie bars which is bonded to the die, and after which the tie bars of metal are removed to leave individual metal conducting elements or leads bonded to the connection pads on the die. The frame can be formed by excising holes in a thin plate of metal. The frame can be cut to remove a center ring or picture frame, leaving behind metal leads ready to attach to the bonding pads on the die, or the frame can be cut to remove an outer ring or picture frame after the leads have been bonded to the connection pads on the die.

All of the connection pads can be "gang-bonded" simultaneously to the connection pads on the die. The electrical connections can be used selectively to program, or route unique signals to unique layers of semiconductor die within the stack of semiconductor die as required by the specific component design. The electrical connections can be connected to the corresponding connection on one or more other die in the stack to connect signals of each of the semiconductor die in the stack in common, as required by the specific component design. The electrical connections can be fanned out so the similar electrical connections from different die in the stack are available at separate, unique connection points on the module (in other words "not in common").

The mounting of the stack of the semiconductor die to the substrate includes the electrical and physical connection of the vertical interconnects to the aforementioned electrical connection lands on the top surface of said substrate. The electrical connection can be done with the use of a conductive polymer "dot", or "puddle" between the vertical interconnect of the stack of die and the substrate. The mounting of the stack of the semiconductor die to the substrate can include an under-fill adhesive material between the bottom of the lowest die in the stack and the top surface of the substrate. The underfill adhesive material can be an electrical insulating material, a thermally conductive material, where the underfill material can cushion and absorb some of the physical stress that will occur as a result of temperature changes during use of the component. The underfill material can extend past the edge of the bottom die and form a fillet between the bottom die and the substrate. The underfill material can extend above the bottom die to forming a fillet between the side of the stack of die at any point above the substrate and the surface of the substrate. The underfill material can extend above the bottom die to the second, third, fourth, or nth die in the stack of die, or to the top of the stack.

The mounting of the stack to substrate can be with a polymer or epoxy perform between the bottom die in the stack and the substrate. The die in the stack can be "face-up", "face-down", or "face to face". The substrate can have multiple conducting layers for signals, ground, and power supply connections, including one or more conducting layers.

The substrate can include a means for making electrical connection between the bottom of the substrate and a printed circuit board upon which the substrate with stacked die components is attached. The substrate can have solder balls or bumps on the bottom for connection to a printed circuit board. The substrate can have LGA contacts for connection to a printed circuit board, where the contacts have a gold surface, a solder coated surface, a copper surface, an aluminum surface, a conductive surface (a metal surface).

The substrate can have flexible interconnect contacts for connection to a printed circuit board, including flat metallic connection pads (lands) for connection to a printed circuit board or for attachment of solder balls or bumps. The substrate can have electrical connection pads on the top surface for connection to a stack of semiconductor die.

The substrate can have electrical interconnection between the pads on the top surface and the solder ball pad, solder bump pads, or flat connection pads (lands) on the bottom of the substrate. The substrate can be multi-layer, with one or more extra metal layers between the top and bottom conducting layer, and insulated from the top and bottom conducting layer, and insulated from each other for ground planes, power planes, and other signal connections between circuitry on the top layer and circuitry on the bottom layer of the substrate.

A multi layer substrate includes one or more extra metal layers between the top and bottom conducting layers for heat sinking. The substrate, being multi layer, can have one or more extra metal layers above or below the top and/or bottom conducting layers for heat sinking. The substrate can comprise an organic material, such as BT, FR4, polyimide, or kapton.

The substrate can be a flexible substrate, such as a flexible tape, or a flexible film. The substrate can be made from ceramic material, silicon, a chipscale substrate, where the chipscale substrate is less than or equal to 1.2 times the die dimensions.

The assembly can optionally be without any additional coating, molding, or covering over the die, vertical connections, and/or substrate. The top die of the assembly can be covered with a material to block or attenuate light from impinging on and affecting the semiconductor die in the assembly. The assembly can be coated with a conformal polymer, such as parylene, where the conformal coating can be the final coating of the device. The conformal coating can be applied prior to further encapsulation or transfer molding, such as in the cases where the device will be molded or encapsulated.

The assembly can be over-molded with a polymer, plastic, or epoxy to completely coat and cover the stack of semiconductor die and the top of the substrate, leaving the connections at the bottom of the substrate uncovered and exposed for electrical connection. The assembly can be molded in a polymer, plastic, or epoxy to completely cover and seal the stack of semiconductor die and the top surface of the component. The molding can be a "transfer mold" process. The assembly can be covered by a heatsink, or in a hermetic package.

The stacked die BGA component is suitable for high speed circuitry due to the component having low inductance, low capacitance, low DC resistance, and/or matched AC Impedance. The component optionally can have ground and power planes included in the substrate and or the die.

WHAT IS CLAIMED IS:

1. A high density low parasitic stacked die BGA or LGA component assembly comprising:

a stack of semiconductor or integrated circuit die mounted on a substrate and laminated to each other;

the die having a conformal, insulating coating having openings above specific connection locations at the edge of the top surface of the die as required by the specific component design;

the die laminated on top of each other with an electrically insulating polymer or epoxy preform;

the stack being electrically connected vertically;

the vertical electrical connection comprised of a conductive polymer or conductive epoxy;

the electrical connections including one or more metallic conducting elements bonded to the pad locations on the surface of each die and extending, both physically and electrically from the pad into the vertical conductor so that one end of the metallic conducting element is embedded within the conductive polymer;

the mounting and connection of the stack of semiconductor die on a substrate so that the vertical conductors are electrically and physically connected to the electrical connection lands on the top surface of the substrate;

the mounting of the stack of semiconductor die to the substrate including an under-fill adhesive material between the lowest die in the stack and the top surface of the substrate;

the under-fill material extending past the edge of the bottom die and forming a fillet between the side of the die stack and the surface of the substrate;

the substrate having one or more conducting layers for connecting the die stack's vertical conductors to the top side of the substrate and to connection points such as solder balls on the bottom surface of the substrate.

2. The assembly as in Claim 1 wherein the die have one or more metal rerouting layers to interconnect the original die connection pads with new connection locations at the edge of the top surface of the die.

3. The assembly as in Claim 1 wherein the conformal, insulating coating is parylene.

4. The assembly as in Claim 1 wherein the conformal, insulating coating is a polymer or plastic.

5. The assembly as in Claim 1 wherein the openings in the conformal insulating coating have been formed by laser ablation.

6. The assembly as in Claim 1 wherein the electrically insulating polymer or epoxy preform is thermally conductive.

7. The assembly as in Claim 1 wherein the electrically insulating polymer preform includes solid spheres to maintain a fixed spacing and separation between the semiconductor die after lamination.

8. The assembly as in Claim 1 wherein the semiconductor die are memory die.

9. The assembly as in Claim 1 wherein the metallic conducting elements are formed by metal bonding wires or metal bonding ribbon.

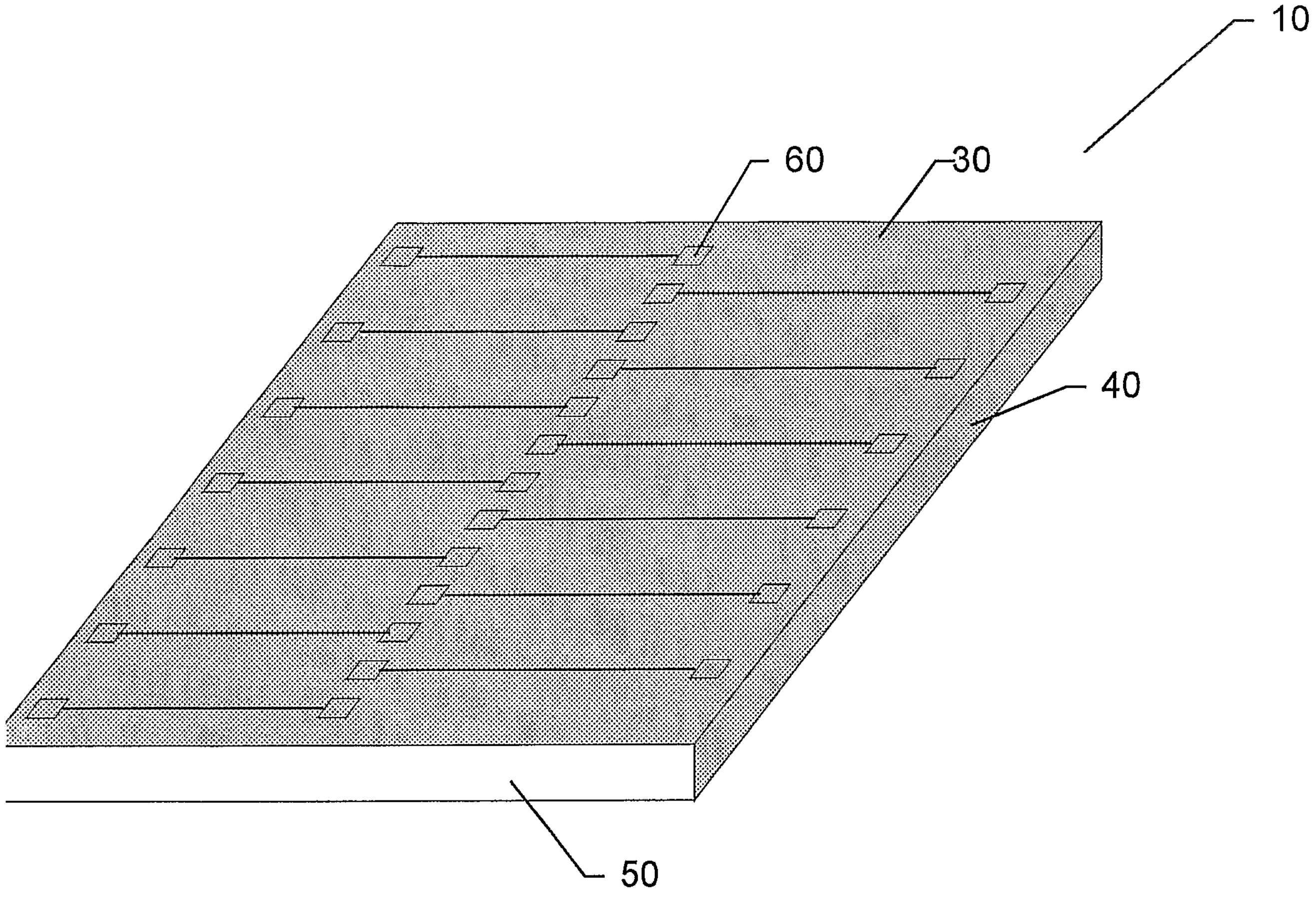
10. The assembly as in Claim 1 including means for connecting unique signals to one or more of the semiconductor layers in the die stack to program, select, route, or combine specific electrical signals to specific semiconductor die in the stack.

11. The assembly as in Claim 9, wherein the means for connecting unique signals is accomplished by selective removal and non removal of the conformal coating above the die connection pads.

12. The assembly as in Claim 9, wherein the means for connecting unique signals is accomplished by the presence or absence of the metallic conducting elements which connect the die connection pads to the vertical conductors.

13. The assembly as in Claim 1, wherein a conductive polymer or conductive epoxy is used to electrically connect the vertical conductors of the stacked die assembly to the electrical connection lands on the top surface of the substrate.

14. The assembly as in Claim 1, wherein the completed stack assembly is over-molded or encapsulated with a polymer, plastic, or epoxy, in addition to, or instead of the underfill coating, leaving the connections on the bottom of the substrate uncovered and exposed for electrical connection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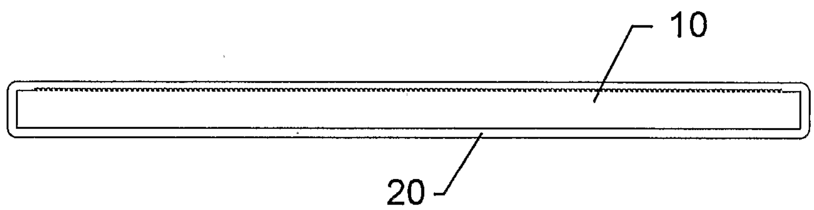
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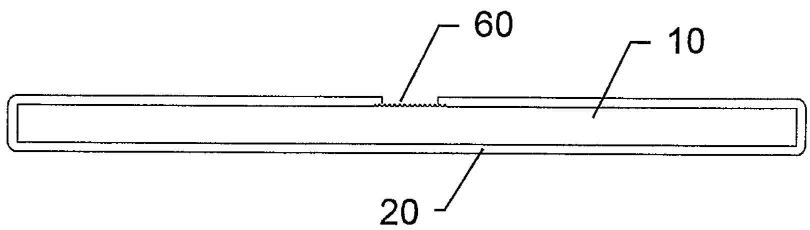
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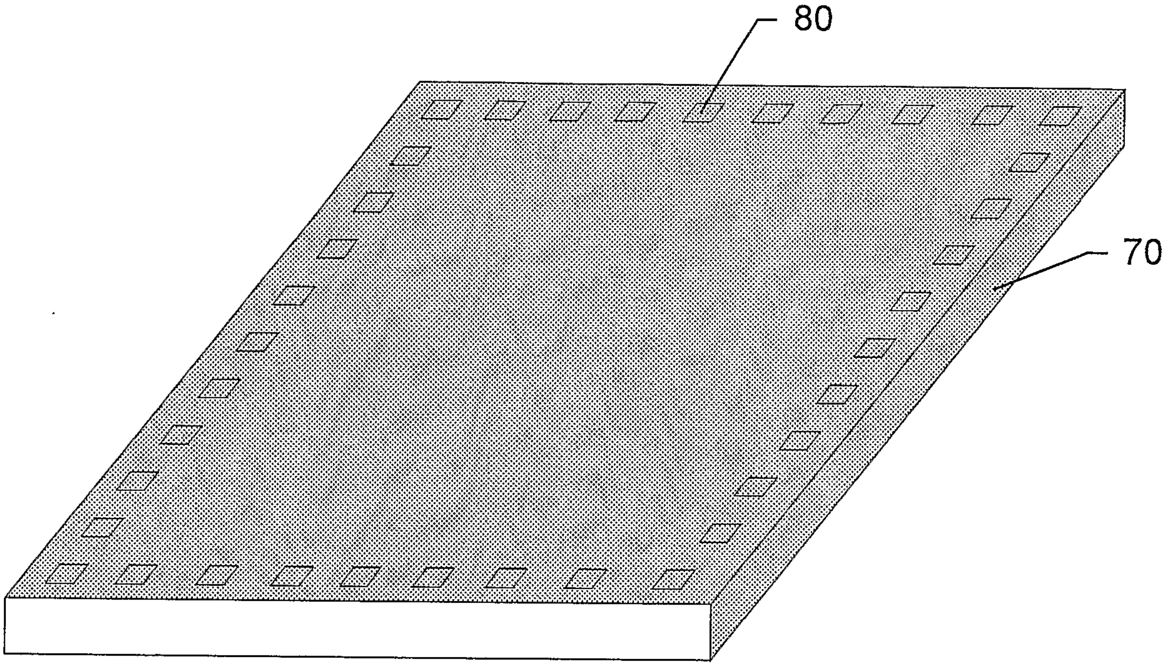
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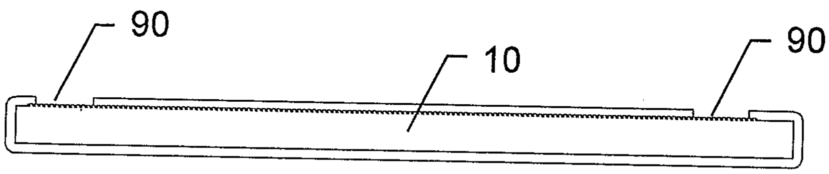
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4-High Stack-on-BGA VIP
Cross Section