



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<b>(51) International Patent Classification <sup>6</sup> :</b>  <b>H04L</b>	<b>A2</b>	<b>(11) International Publication Number:</b> <b>WO 98/37656</b>  <b>(43) International Publication Date:</b> 27 August 1998 (27.08.98)
<b>(21) International Application Number:</b> PCT/US98/02053  <b>(22) International Filing Date:</b> 4 February 1998 (04.02.98)  <b>(30) Priority Data:</b> 08/795,657      6 February 1997 (06.02.97)      US  <b>(71) Applicant:</b> RAMBUS, INC. [US/US]; 2465 Latham Street, Mountain View, CA 94040 (US).  <b>(72) Inventors:</b> DONNELLY, Kevin, S.; 1671 Noe Street, San Fran- cisco, CA 94131 (US). CHAU, Pak, Shing; 1677 Klip- springer Drive, San Jose, CA 95124 (US). HOROWITZ, Mark, A.; 2024 Colombia Street, Palo Alto, CA 94306 (US). LEE, Thomas, H.; 939 Bubb Road, Cupertino, CA 95014 (US). JOHNSON, Mark, G.; 125 Arbuelo Way, Los Altos, CA 94022 (US). LAU, Benedict, C.; 630 Celebration Court, San Jose, CA 95134 (US). YU, Leung; 2952 Gala Court, Santa Clara, CA 95051 (US). GARLEPP, Bruno, W.; 99 E. Middlefield Road #48, Mountain View, CA 94043 (US). CHAN, Yiu-Fai; 27275 Julietta Lane, Los Altos Hills, CA 94022 (US). KIM, Jun; 6 Knot Lane, Redwood City, CA 94065 (US). TRAN, Chanh, Vi; 3009 Breen Court, San Jose, CA 95121 (US). STARK, Donald, C.; 201 High Street, Palo Alto, CA 94301 (US).		<b>(74) Agents:</b> HAUGHEY, Paul, C. et al.; Townsend and Townsend and Crew LLP, 8th floor, Two Embarcadero Center, San Francisco, CA 94111-3834 (US).  <b>(81) Designated States:</b> CA, JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>Without international search report and to be republished              upon receipt of that report.</i>
<b>(54) Title:</b> DELAY LOCKED LOOP CIRCUITRY FOR CLOCK DELAY ADJUSTMENT		
<b>(57) Abstract</b>  <p>Delay locked loop circuitry for generating a predetermined phase relationship between a pair of clocks. A first delay-locked loop includes delay elements arranged in a chain, the chain receiving an input clock and generating, from each delay element, a set of phase vectors, each shifted a unit delay from the adjacent vector. The first delay-locked loop adjusts the unit delays in the delay chain using a delay adjustment signal so that the phase vectors span a predetermined phase shift of the input clock. A second delay-locked loop selects, from the first delay-locked loop, a pair of phase vectors which brackets the phase of an input clock. A phase interpolator receives the selected pair of vectors and generates an output clock and a delayed output clock, the amount of the delay being controlled by the delay adjustment signal of the first delay-locked loop circuitry. A phase detector compares the delayed output clock with the input clock and adjusts the phase interpolator, based on the phase comparison, so that the phase of the delayed output clock is in phase with the input clock. As a result, there is a predetermined phase relationship between the output clock and the input clock, the phase relationship being the amount of delay between the output clock and the delayed output clock. Different phase relationships between the input and output clock are possible depending on the number of unit delays used in the path of the delayed output clock or the output clock.</p>		

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## DELAY LOCKED LOOP CIRCUITRY FOR CLOCK DELAY ADJUSTMENT

### BACKGROUND OF THE INVENTION

The present invention relates to clock delay adjustment circuitry. In particular, the present invention relates to the generation of a set of phase vectors and the generation of output clocks that have precise phase relationships to an input clock.

Previous art includes Rambus patent, 5,485,490, Leung and Horowitz, which discloses two independent loops, the first of which creates a fixed number of phase vectors, the second of which creates an output clock that is in phase with the input clock. Also disclosed in this patent is the use of separate circuitry to create a leading phase clock to the output clock by selecting a pair of phase vectors and interpolating between them to produce an output that leads the output clock by the delay between phase vectors available from the first loop.

IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, Lee, et.al. ("Lee") discloses a pair of delay-locked loops (DLL) for transmitting and receiving data in DRAMs. IEEE Journal of Solid-State Circuits, Vol. 31, No. 4, April 1996, Tanoi et.al. shows a two-loop architecture in which an frequency locked-loop (FLL) is designed to lock onto an external input frequency and to control the DLL for lock-in to the phase of the external input clock.

It is desirable to improve on the generation of a leading output clock to the in phase output clock. There are several drawbacks to the invention disclosed in Pat. No. 5,485,490. Phase locked loop circuitry employing a VCO and single order loop filter to create phase vectors is a second order system. This second order system has stability problems associated with its operation. Furthermore, the VCO phase lock loop accumulates phase error in response to sudden change

in phase on inputs to the loop, where the input includes not only the input clock but also the power supplies to the loop. This occurs because the loop changes the frequency of the VCO in response to a sudden phase change and this frequency shift is integrated to become phase error which persists for a time on the order of the reciprocal loop bandwidth. (See Lee, above). This causes the loop to be noise sensitive when the noise is in the form of sudden phase shifts. Another drawback regarding the prior art patent is that the subloop used for generating the in-phase clock relies on the accuracy and similarity of a second phase interpolator (out-of-phase phase interpolator) to produce the leading clock. Any lack of matching between the out-of-phase phase interpolator and the in-phase phase interpolator will create a phase error in the desired phase relationship between the leading clock and the in-phase clock. Another drawback concerns the acquisition time of the VCO which can be quite long after restoration of a lost input clock, depending on how long the input clock has been absent.

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#### SUMMARY OF THE INVENTION

The present invention provides delay locked loop circuitry for generating a predetermined phase relationship between a pair of clocks. A first delay-locked loop (DLL) includes delay elements arranged in a chain, the chain receiving an input clock and generating, from the delay elements, a set of phase vectors, each shifted a unit delay from the adjacent vector. The first delay-locked loop adjusts the unit delays in the delay chain using a delay adjustment signal so that the phase vectors span a predetermined phase shift of the input clock.

In a preferred embodiment, a second DLL is used, although the second DLL could be used with another circuit which produces two different delayed clock signals. The second DLL selects, from the first DLL, a pair of phase vectors which brackets the phase of an input clock. A phase interpolator receives the selected pair of vectors and generates an output clock and a delayed output clock, the

amount of the delay being controlled by the delay adjustment signal of the first delay-locked loop circuitry.

Preferably, a phase detector in the second DLL compares the delayed output clock with the input clock and  
5 adjusts the phase interpolator, based on the phase comparison, so that the phase of the delayed output clock is in phase with the input clock. The phase interpolator is preferably adjusted with a control circuit including a digital memory for storing a count corresponding to the delay adjustment, which  
10 can be maintained in the absence of the input clock signal.

Preferably, the first DLL includes a control circuit with a digital memory for providing the desired delay adjustment to the adjustable delay elements. A filter is used between the phase detector and the control circuit to reduce  
15 loop jitter.

The present invention is advantageously used for the transmit and receive clocks in high speed DRAM and a high speed DRAM bus channel.

Other objects, features, and advantages of the  
20 present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

#### BRIEF DESCRIPTION OF THE DRAWINGS

25 The features and advantages of the present invention are illustrated by way of example and are by no means intended to limit the scope of the present invention to the particular embodiments shown, and in which:

Figure 1 shows a block diagram of a delay locked  
30 loop for generating phase vectors,  $K\langle r:0 \rangle$ ;

Figure 2 shows a more detailed block diagram than Figure 1 of a delayed locked loop for generating phase vectors,  $K\langle r:0 \rangle$ , according to one embodiment;

Figure 3 shows a more detailed architecture than  
35 Figure 2 of a delayed locked loop for generating phase vectors,  $K\langle r:0 \rangle$ , according to one embodiment;

Figure 4 shows another embodiment of a delay locked loop for generating phase vectors using buffered delay elements and a buffer clock source.

5 Figure 5 shows a block diagram of the architecture of a DLL for generating an Output Clock in precise phase relationship with an Input Clock according to one embodiment;

10 Figure 6 shows a more detailed architecture than Figure 5 of a DLL for generating an Output Clock in precise phase relationship with an Input clock according to one embodiment;

Figure 7 shows another embodiment of a DLL for generating an Output Clock in precise phase relationship with an Input Clock using an adjustable delay section in the path of both the Output clock and the feedback clock;

15 Figure 8 shows another embodiment of an adjustable delay section having one adjustable delay for use in Figure 7;

Figure 9 shows another embodiment of an adjustable delay section having at least two adjustable delays for use in Figure 7;

20 Figure 10 shows an embodiment for producing a pair of delays from the same chain for use in Figure 7;

Figure 11 shows a set of four phase vectors each separated by a 90 degree interval and spanning 360 degrees shift of the 0 degree vector;

25 Figure 12 shows a set of eight phase vectors each separated by a 45 degree interval and spanning 360 degrees shift of the 0 degree vector;

30 Figure 13 shows a set of 12 phase vectors each separated by a 30 degree interval and spanning 360 degrees shift of the 0 degree vector;

Figure 14 shows a set of four phase vectors each separated by a 90 degree interval and spanning 360 degrees shift of the 0 degree vector, with the Input Clock and feedback clock between the 90 and 180 degree phase vectors and the Output Clock between the 0 and 90 degree vectors and 90 degrees earlier in time than the input clock;

Figure 15 depicts a case in which the input clock is between the 135 and 180 degree phase vectors, with the

initially selected phase vectors being the 0 and 45 degree vectors;

Figure 16A shows an embodiment of a delay element for use in a delay locked loop;

5 Figure 16B shows another embodiment of a delay element for use in a delay locked loop;

Figure 17 shows an embodiment of a digital to analog converter for use in a delay locked loop;

10 Figure 18 shows an embodiment of a phase interpolator for use in a delay locked loop; and Figure 19A and 19B show an embodiment of a duty cycle correcting amplifier for use in a delay locked loop. Figure 19A is the amplifier in which the duty cycle is corrected and Figure 19B is the duty cycle error detecting circuit which  
15 applies a correction signal to the amplifier in Figure 19A.

Figure 20 is a block diagram of a TrimAdj circuit for use in one variation of the embodiment of Figure 7.

Figure 21 is a circuit diagram of one embodiment of a phase detector as set forth in Figure 6.

20 Figure 22 is a block diagram of a DRAM system incorporating the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

25 Embodiments of the present invention provide a method and circuitry to generate a set of phase vectors in a way that is more immune to noise on loop inputs including the power supplies, leading to a more stable set of phase vectors.

Also, an output clock that has a predetermined phase relationship with an input clock is provided. The effect of  
30 clock buffer delays between the input clock and output clock is minimized. The delay of an adjustable delay element is adjusted with a counter and a digital to analog converter, the count in the counter digitally representing the current delay adjustment of the delay locked loop. The digital count is  
35 converted to a signal suitable for adjusting an adjustable delay element used in a delay locked loop.

The setting of current delay adjustment of the loop is digitally represented so that the setting may be stored

while the loop is in a powered-down or low power state. There is quick re-acquisition of the locked state of a delay locked loop after the delay locked loop has been powered down.

In one embodiment of the present invention a delay locked loop (DLL) is employed for generating phase vectors. Referring to Figure 1, the DLL 100 receives an external clock, ClkSrc 101, and generates phase vectors,  $K\langle r:0 \rangle$  103. A convenient way to represent the set of phase vectors for a periodic signal is to draw the vectors in phase space as in Figure 11. In this figure there are four vectors each spaced apart by 90 degrees and spanning a 360 degree phase shift of the 0 degree vector. Each vector in this figure represents a time delay of one fourth of the cycle of the periodic signal. Figures 12 and 13 show alternate sets of phase vectors. Figure 12 shows a set of vectors spaced at 45 degree intervals and spanning a 360 degree phase shift of the 0 degree vector. Figure 13 shows a set of vectors spaced at 30 degree intervals and spanning a 360 degree phase shift of the 0 degree vector.

Referring to the embodiment shown in Figure 2, the DLL 100 is a first order loop comprising a set of adjustable delay section 110, a control circuit 120 and a phase detector 130. The phase detector 130 receives the external clock, ClkSrc 150 from which it derives a clock input ClkIn (not shown), a set of phase vector lines 140 and the last phase vector  $K\langle r \rangle$  on line 160. The output of phase detector 130 is coupled to the control circuit 120 which processes the output of the phase detector to generate a delay adjust signal 125 for adjusting the delay of the delay elements. The adjustable delay elements are adjusted so that the phase of  $K\langle r \rangle$  is the same as the clock input, ClkIn.

Figure 3 shows an embodiment of the DLL in more detail. In particular, adjustable delay section 205 comprise a set of four identical adjustable delay elements 210 connected in series with the output of each delay element 210 except the last element connected to the input of the next element 210. While four delay elements are shown in the particular embodiment, any number such as two, three, four, six, eight or twelve, can be used. This arrangement produces



a set of clocks, called phase vectors  $K_{r:0}$  270, each shifted in time from the next by a delay, called a unit delay, generated by the adjustable delay section 205. Each adjustable delay element 210 receives the delay adjust signal DlyAdj 260 from control circuit 230, comprising counter control circuit 240 and digital to analog converter (DAC) 250. Counter control circuit 240 receives an input, PhDiff 225, from phase detector 220 and generates count Cnt<sub>c:0</sub> 245 for input to the DAC. In one embodiment, control circuit 230 is implemented with digital circuits to permit the storage of the current delay adjustment setting of the loop, held by Cnt<sub>c:0</sub> 245, during times when the ClkSrc 200 is not present, perhaps during a period when the system is shut down to save power. The saved setting permits the loop to quickly re-acquire a locked condition when the ClkSrc is reactivated.

Continuing with Figure 3, phase detector 220 receives as inputs ClkIn 215 derived from the ClkSrc 200 via buffer 202 and the last phase vector  $K_r$  280. In another embodiment, buffer 202 performs duty cycle correction as well as amplification to assure that ClkIn 215 has a 50% duty cycle. Duty cycle correction is discussed in greater detail below.

In Figure 3, adjustable delay element 210 may be implemented according to the embodiment shown in Figure 16A, which shows a delay element 1010 and a bias circuit 1000. In Figure 16A the delay element is a differential delay element, having both true and complementary inputs and outputs. The circuit operates to delay the differential inputs IN 1005 and IN\_B 1015 to produce delayed outputs Out 1130 and Out\_B 1140. The amount of delay is adjusted by adjustable current source 1020, which controls the amount of current switched by differential pair 1100 and 1110. The greater the amount of current switched the smaller delay produced by the differential pair. Transistors 1080 and 1090 act as clamps to limit the swing of the differential pair allowing small delays to be realized by the circuit.

The adjustable delay element may also be implemented according to the embodiment shown in Figure 16B. In this

figure section 1215 functions as a fixed delay comprising a current source 1260 and a differential pair 1220 and 1230, and section 1225 operates as a phase interpolator comprising differential pair 1330 and 1340 with current source 1320 and differential pair 1290 and 1300 with current source 1310 to produce a delay that is adjustable between a stage delay to a fixed delay plus the stage delay. The stage delay represents the fixed delay time through the interpolator stage 1225. The phase interpolator delay stage 1225 is adjusted by varying the current sources Ix 1320 and Iy 1310. If Ix is at maximum and Iy is turned off the output signals Out 1380 and Out\_B 1370 are produced by transistors 1330 and 1340 in phase with the input signals but delayed by the stage delay. If Iy 1310 is maximum and Ix 1320 is off then the output signals Out 1380 and Out\_B 1370 are produced by transistors 1290 and 1300 and are delayed by amount of the fixed delay provided by the 1215 section plus the stage delay. Therefore, the phase interpolator delay stage 1225 is adjustable through a range of delay equal to the fixed delay of the 1215 section.

Figure 3 depicts a DAC which may be implemented according to the DAC shown in Figure 17, which depicts a circuit for converting a digital count Cnt<c:0> 1510 and its complement Cnt\_B<c:0> 1500 to a differential current pair, Ictl 1640 and Ictl\_B 1590 proportional to the count. Figure 17 shows three sections of circuitry, a set of binary weighted current sources 1520, a set of switches 1540 for producing the true current output Ictl 1640 and a set of switches 1530 for producing the complement output Ictl\_B 1590. If the count input Cnt<c:0> 1510 is all ones then Ictl 1640 has a maximum current, Max\_I, which is the sum of all of the current sources 1650, 1660, 1670 through 1680 and the complementary current Ictl\_B is zero. If the count input Cnt<c:0> 1510 is all zeros then Ictl\_B 1590 has the maximum current, Max I, and Ictl is zero. Intermediate counts produce intermediate amounts of current, Im, and (Max\_I - Im) on Ictl and Ictl\_B respectively. This DAC is suitable for controlling the differential input delay adjust signals of the adjustable delay element 210 shown in Figure 16B for the delay locked loop shown in Figure 3.

The system shown in Figure 3 operates as follows. Phase detector 220 compares the ClkIn signal, with the last phase vector K<r> 280 to determine the phase difference from a predetermined phase relationship between the two clocks. In one embodiment the predetermined phase difference could be zero degrees. In another embodiment the predetermined phase difference could be 180 degrees. The phase difference is represented by signal PhDiff 225. Counter control block then converts the PhDiff signal into a digital count, Cnt<c:0> 245, and DAC 250 converts the count value into an analog quantity, DlyAdj 260, for adjusting the adjustable delay elements. In some embodiments the Cnt<c:0> signal and the DlyAdj signal may be differential signals. The delay adjustment operates to change the delay of the adjustable delay elements so that the phase difference from the predetermined phase relationship between clock input, ClkIn and K<r> is made close to zero. When this condition occurs the DLL is locked, and each adjustable delay element has substantially the same delay. Thus each phase vector is displaced in time from the adjacent vector by an amount equal to the setting of the adjustable delay element. This time displacement is termed a unit delay. The result is that the phase vectors span a 360 degree phase shift of the ClkIn signal 215. These phase vectors can now be used in another DLL to lock the phase of an output clock in precise phase relationship to the arbitrary phase of an input clock.

For Figure 3, an alternate embodiment could use fewer delay elements to produce phase vectors that span the 360 degree phase shift of the ClkIn if each delay element, such as the ones depicted in Figures 16A and 16B, can produce both true and complementary outputs. For example, instead of using four delay elements each separated by 90 degrees, two delay elements separated by 90 degrees could be used if the delay element had true outputs yielding delays of 90 and 180 degrees and complementary outputs yielding 270 and 360 degrees, respectively. Alternatively, fewer delay elements could be used if the phase detector were designed to detect phase differences from a predetermined phase relationship of

180 degrees. Using such a phase detector would only require that two delay elements be used spanning a 180 degree phase shift of the ClkIn signal. The outputs of the delay elements could be inverted in a separate circuit which receives the phase vectors, so that a set of phase vectors spanning 360 degrees is obtained. For embodiments in which the phase shift of the ClkIn signal spans only 180 degrees buffer 202 may perform a duty cycle correction function to assure that the ClkIn signal 215 has a 50% duty cycle. This is especially important when the remaining span of 180 degrees is derived through inversion of the phase vectors spanning the first 180 degrees, because inversion will not generate the proper phase shift if the duty cycle is not substantially close to 50%.

Referring the embodiment in Figure 4, an additional adjustable delay element has been placed in the circuit to receive the last phase vector. This additional delay has the effect of insuring that each phase vector has the identical loading as the other phase vectors, so that phase errors caused by loading differences are substantially eliminated. Rather than connecting the delay adjust signal 265 to the DlyAdj signal 260, signal 265 may be connected to a convenient voltage, because the output of the additional delay is not used. This eliminates some of the loading on the DlyAdj signal 260.

Continuing with the embodiment of Figure 4, phase vectors 275 are buffered by buffers 212 in order to further control the loading on the vectors by isolating the loading of the phase vectors from other circuits which may receive the vectors. A buffered version of ClkIn 215 and a buffered version of the last phase vector K<r> 285 are sent to the phase detector. This guarantees that buffered version of the phase vectors K<r:0> 275 are separated in phase by a unit delay and that the set of buffered phase vectors span a 360 degree or 180 degree shift of the buffered ClkIn signal depending upon the embodiment chosen.

Also shown in Figure 4 is a version of buffer 202 which has a duty cycle correcting circuit 290 attached. The duty cycle correcting circuit 290 senses signal 214 for a

deviation from a 50% duty cycle. It then feeds a correction signal to buffer 202 to correct signal 214. In some embodiments signal 214 is a differential signal and the error signal 295 is a differential signal.

5 An embodiment of a duty cycle correcting amplifier is shown in Figures 19A and 19B. Figure 19A shows the correcting stage 2005 and the buffering stage 2055 and Figure 19B shows the duty cycle error detecting stage 2215. In Figure 19A differential pair 1960 and 1970 receive the input  
10 clock differential on In+ 1920 and In- 1930 and produce a differential output clock on Corr Clock\_B 2090 and Corr Clock 2100. If the duty cycle deviates from 50% then the circuit shown in Figure 19B will produce a differential error voltage signal pair Error+ 2300 and Error- 2200 from the differential  
15 pair 2230 and 2250 and capacitor 2260 acting as an integrator. Transistors 2220, 2280, 2290 and 2270 function as a load element especially suited for controlling the charge leakage across integrating capacitor 2260. The differential error voltage signal pair is fed back to the correcting stage 2005  
20 such that the duty cycle error in the Corr Clock and Corr Clock\_B signals is reduced by altering currents 2110 and 2120 depending on the polarity of the error. Thus, the output of the buffering stage 2055 is a clock having a duty cycle substantially close to 50%.

25 In Figure 4, as in Figure 3, Phase detector 220 compares the ClkIn signal, with the last phase vector  $K_{\langle r \rangle}$  280 to determine the phase difference from a predetermined phase relationship between the two clocks, and signal PhDiff 225 represents that difference. In Figure 3, PhDiff signal 225  
30 contains random variations due to the instantaneous phase error which, when used directly by Counter Control 240, causes an amount of overall loop jitter, thus affecting the stability of the phase vectors. In Figure 4, the amount of jitter is reduced by filtering the PhDiff signal before converting it to  
35 DlyAdj signal 260. Shown in Figure 4 is an embodiment in which control circuit 230 includes filter 235 in addition to counter control 240 and digital to analog converter (DAC) 250. Filter circuit 235 receives an input, PhDiff 225, from phase

detector 220 and CntClk 241 from buffer 238 and generates output PhDiffF 237 for input to the Counter Control 240, which receives CntClk 241 and generates count Cnt<c:0> 245 for input to DAC 250. In an embodiment in which the PhDiff signal is a digital signal, a digital filter is used, but either analog or digital filtering may be employed. CntClk 241 operates the circuitry in both Filter 235 and Counter Control 240. Buffer 238 is employed when ClkSrc is a small swing signal but Counter Control 240 and Filter 235 require a full swing signal.

Types of digital filters that can be employed to reduce loop jitter include a majority-detector filter or an unanimity-detector filter. In either filter type, CntClk 241 operates circuitry which samples and stores the state, either true or false, of PhDiff 225. A majority-detector filter saves the last N samples, where N is an odd number, of PhDiff signal 225 and determines whether a majority of the last N cycles, say 3 out of 5 (N), are the same. If so, then the majority-detector filter activates PhDiffF 237 to alter the count in counter control 240. This type of filter alters the count in counter control 240 on every sample because there is always a majority of true or false samples. An unanimity-detector filter also records the last N samples, where N can be even or odd, of the PhDiff signal but instead determines whether all N cycles are the same. If all samples are the same, the unanimity-detector filter activates the PhDiffF signal 237 to alter the count and at times during which not all the samples are the same, the PhDiffF signal will not be activated to alter the count. Both types of filters have the effect of reducing loop jitter, and either type may be used.

Turning now to Figure 5, a pair of delay locked loops is depicted for generating an output clock having predetermined phase relationship to an input clock. The first delay locked loop 320 is one which generates phase vectors K<r:0> 330 from a clock source ClkSrc 300 as described above. The phase vectors and the DlyAdj signal 340 are then used by a

second delay locked loop 350 to create a precise phase relationship between Input Clock 310 and Output Clock 360.

Figure 6 shows an embodiment of the loop of Figure 5 in more detail. First loop 400 is the phase vector loop which receives ClkSrc 410 and generates phase vectors  $K_{r:0}$  430 and DlyAdj signal 440. The second loop 500 is the loop for creating the phase relationship between the Input Clock 650 and Output Clk 640. Loop 500 comprises a selection circuitry 510, phase interpolator 560, adjustable delay section 610 which represents an integer multiple of adjustable delay elements, Clock Buffers 620 and 630, control circuit 570 and phase detector 590.

In Figure 6, selection circuitry 510 receives the phase vectors 430 and passes along a selected pair of vectors  $K_x$  520 and  $K_y$  530, which are received by phase interpolator 560. The phase interpolator generates an interpolated output clock 615 which is buffered by clock buffer 620 to become the Output Clock 640.

Adjustable delay section 610 also receives output clock 615 and feeds the delayed clock to clock buffer 630 to generate FdBkClk 600. Control circuit generates PhAdj signal 550 for controlling the interpolator 560. Control circuit 570 receives phase difference information, PhDiff 580, from phase detector 590, which detects the difference in phase between the Input Clk 650 and FdBkClk 600. As described previously, control circuit 570 may comprise counter control 240 and DAC 250 such as in Figure 3, to enable the saving of the setting of the current phase adjustment of the loop or Filter 235, Counter Control 240 and DAC 250 as in Figure 4 to additionally reduce loop jitter.

Selection circuitry 510 may be implemented as an analog or digital set of switches comprising a multiplexer, depending upon whether the phase vectors are low swing or full swing signals. Phase interpolator 560 may be implemented as shown in Figure 18. Alternately, selection circuitry 510 may be merged or combined with interpolator 560, shown in Figure 6 as block 562. In some embodiments when selection circuitry is combined with the phase interpolator, the circuit shown in

Figure 18 is duplicated several times, each duplicate connected to a different set of switches for applying a particular phase vector to the interpolator.

The operation of the circuit of Figure 18 is substantially similar to the circuit shown in Figure 16B. Differential pair 1800 and 1810 receive one of the selected phase vectors Kx 1700 and Kx\_B 1740 which is the complement of the Kx signal. Kx and Kx\_B may be generated from a delay element having differential outputs as shown in Figure 16A or 16B. Differential pair 1820 and 1830 receive the Ky 1710 phase vector and the Ky\_B 1750 complementary phase vector. The phase interpolator functions as a weighted integrator using capacitors C1 1760 and C2 1770 and coincidence detector 1860. If Ictl 1720 is set at a maximum value and Ictl\_B 1730 is zero then the output signal PIout 1870 is in phase with the Kx clock but delayed by a stage delay through the interpolator. If Ictl\_B 1730 is set a maximum value and Ictl 1720 is zero then the output signal is in phase with the Ky clock but delayed by a stage delay. By adjusting the values of adjustable currents 1720 and 1730 any delay between Kx and Ky may be achieved.

The operation of loop 500 in Figure 6 is as follows. Phase detector 590 determines what the difference in phase, if any, is between the Input Clk 650 and FdBkClk 600. This difference is then processed by control circuit 570 to select a pair of phase vectors via selection circuitry 510. The chosen pair of vectors is that pair between which the phase of Input Clk 650 lies, after accounting for fixed delays inherent in circuits in the path of the FdBkClk signal such as the phase selector, phase interpolator, adjustable delay section and clock buffer. An example of a pair of vectors meeting this requirement is shown in Figure 14, in which the Input Clk is shown between the 90 degree and 180 degree vectors and at a delay of alpha degrees from the 180 degree vector. If the starting pair of vectors is not the correct pair then the control circuit steps through the pairs of vectors one step at a time until the correct pair is discovered. Figure 15 depicts a circumstance in which the stepping of several phase



vectors must occur if loop 500 starts in the 0 degree state before the correct pair is discovered. When the first pair of vectors, 0 and 45 degrees, is selected, the phase interpolator 560 is adjusted so that the phase interpolator output 615 is in phase with the 45 degree vector. While in this condition the 0 degree vector is replaced with the 90 degree vector by the control circuit and selection circuitry. Next, the phase interpolator is adjusted to produce an output in phase with the 90 degree vector and the 45 degree vector is replaced with the 135 degree vector. The phase interpolator is then adjusted to produce an output in phase with the 135 degree vector. Finally, the control circuit replaces the 90 degree vector with the 180 degree vector. Thus, while this stepping occurs phase interpolator generates an output clock 615 which is in phase with one of the selected vectors, in particular, the one that will not be switched in selecting a new pair of vectors. The constraint that the interpolator generate the output clock in phase with the non-switched vector prevents the output clock from glitching during the stepping process. When the correct pair of vectors is determined by the loop then the phase interpolator is allowed to be adjusted by PhAdj signal 550 to precisely align the delayed output FdBkClk 600 to the phase of the Input Clock 650, which is at some phase, alpha degrees, (Figure 14) from one of the selected phase vectors. When this occurs the loop is locked. FdBkClk 600 is delayed by at least one unit delay from adjustable delay section 610, the unit delay being precisely a delay between the any two adjacent phase vectors 430 from the first loop because it is adjusted by the same DlyAdj 440 signal of the first loop. Thus, if the phase vectors from the first loop differ from each other by 90 degrees, then the unit delay is 90 degrees and the FdBkClk is delayed 90 degrees from the output of the phase interpolator 615, assuming one delay element in block 610. Figure 14 shows this condition.

It will be noted that not only is a unit delay included in the feedback path of the second loop but so are the clock buffer and other fixed delays inherent in the phase selector and phase interpolator. Clock buffers 620 and 630

are matched buffers having the same physical construction. FdBkClk is thus delayed by an amount equal to a unit delay and a clock buffer delay plus the other fixed delays from the phase selector and phase interpolator. However, because the Output Clock 640 is delayed by the same amount of fixed delays, the clock buffer delays and fixed delays cancel and the difference between the Output Clk 640 and the Input Clock 640 is only the unit delay.

It should be noted that adjustable delay section 610 could comprise an integer multiple of unit delays, in which case the delay between the Input Clk 650 and Output Clk 640 would then be the integer multiple of unit delays. For example, if the multiple of the unit delay is 3 and the value of the unit delay 10 degrees then the Output Clk would lead the Input Clk by 30 degrees. If the multiple of the unit delay is zero, then the Input Clk and Output Clk would be in phase.

Figure 7 is an alternate embodiment showing adjustable delay section 612 in the path of the Output Clk 640. This section has the same implementation as the section in the path of the FdBkClk 600 and provides a way for the Output Clk signal 640 to not only lead the Input Clk in phase but to lag it in phase. This latter condition occurs when the adjustable delay section 612 comprises a larger multiple of unit delays than adjustable delay section 610. Adjustable delay sections 612 and 610 may be implemented in a fashion similar to section 206 in Figure 4 in order to insure that phase errors due to loading differences are minimized. The delay circuits shown in Figures 16A and 16B are suitable for implementing an adjustable delay element employed in the adjustable delay section 610 or 612. Figure 7 also shows that buffers 620 and 630 may be implemented as duty cycle correcting amplifiers with the aid of duty cycle correction circuit 670. Buffers 620 and 630 may be implemented according to the circuitry shown in 19A and duty cycle correction circuit 670 may be implemented as shown in Figure 19B.

Finally, Figure 7 shows three more inputs, Fast 575, Test 585 and ExtIn 595, to the control circuit 570. In one embodiment Fast signal 575 is used to alter the control circuit so that the loop can lock more quickly by taking larger phase adjustments toward the lock condition. In an embodiment in which the control circuit 570 is implemented as a counter, the Fast signal 575 can cause the counter to count by a multiple of the smallest step between counts. The Test signal 585 is used to allow the control circuit to be under the control of external signal ExtIn 595 rather than PhDiff 580 derived from the loop. This allows loop properties to be tested more easily.

Figure 8 shows one embodiment of adjustable delay section 612. Block 612 comprises a buffer 702, similar to 202 in Figure 4, an adjustable delay element 710 similar to adjustable delay element 210 in Figure 4, and an output buffer 712 similar to the 212 buffer in Figure 4. Figure 9 shows an embodiment of adjustable delay section 610. This figure is similar to Figure 8 but has more adjustable delay elements, but is still buffered at the front of the chain and has an additional delay element at the end of the chain. The adjustable delay sections in both Figure 8 and Figure 9 are controlled from an external delay adjust signal such as 441 as shown in Figure 7, such that the setting produces a delay equal to the delay between phase vectors. If the adjustable delay sections are implemented in this fashion, loading differences are kept to a minimum and only the desired phase difference between signal 617 and 618 is generated. As may be easily seen it is not necessary that adjustable delay sections 610 and 612 be implemented as two separate and distinct sections. It is convenient in some embodiments to derive 617 and 618 from the same section 625 as shown in Figure 7 and 10. The delay adjust signal 441 in Figure 7 is buffered by buffer 442, in some embodiments, to isolate the loading effects of sections 610 and 612 from section 420.

Figure 20 discloses circuitry for biasing the predetermined phase relationship between the input clock and the output clock with a fixed offset. The fixed offset is

necessary when system requirements dictate that the predetermined phase relationship be altered by an amount that is smaller than is available from a unit a delay, for example a one degree phase shift. This fine tuning or trimming is accomplished by the TrimAdj signal 2300 which is combined with the DlyAdj signal 441 in Figure 7. The TrimAdj signal 2300 adds a small amount of adjustment current to the adjustable delay sections 610 and 612. This causes the delay elements in those sections to have a delay that is slightly smaller or larger than the unit delay provided by the delay adjustment signal from the loop which generates the phase vectors. For example, if the delay elements in 610 and 612 are increased by one degree and the unit delay is 90 degrees then each delay element has a delay of 91 degrees. Because the delay between the input clock and the output clock is the difference in delay between the path of the output clock and the path of the feedback clock, the output clock is now 91 degrees ahead of the input clock. In Figure 20, the TrimAdj signal 2300 is derived from DAC 2310 and trim word storage 2320. Trim word storage in some embodiments is a set of fuses or other permanent storage for holding a digital code TW<t:0> 2330 for setting the trim delay. DAC 2310 converts the trim word 2330 to an analog signal such as a current for controlling the delay elements in sections 610 and 612.

Figure 21 is a circuit diagram of a phase detector circuit which could be used for the phase detector of Figures 2, 3, 4, 6 and 7. A clock input 2530 is shown, and data input 2540 would correspond to the feedback clock or phase vector. Output 3000 is the phase difference signal provided to the control circuit. The phase detector is implemented as three blocks 2500, 2510, and 2520 connected in flip-flop fashion using NAND gates 2550, 2560, 2570, 2580, 2590, and 2595.

Figure 22 shows a system application for the delay locked loops of the present invention. In the case shown, master device 3100 communicates with slave device 3110 or slave device 3120. Slave devices 3110 or 3120 may communicate with master device 3100 but not with each other. The system operates from a pair of clocks generated from oscillator 3170

which generates CTM (Clock To Master) 3140 and CFM (Clock From Master) 3130. CTM travels in the direction from the slave device to the master device and is used for transmitting data to the master on data bus 3150. In the master, CTM is looped back to generate CFM which travels in the direction from master to slave device and is used for transmitting data from the master to the slave device. Each device, master or slave, has a data receiver Rcvr 3180 and a data transmitter Txmtr 3190 for receiving and sending data respectively. The Rcvr 3180 uses a signal rclk 3220 to receive the data from the data Bus and Txmtr 3190 uses tclk 3230 to transmit the data onto the data bus. Signals rclk and tclk are generated from a pair of delay locked loops 3200 and 3205 in the slave and from a single delay locked loop 3235 in the master, because the master makes no distinction between CTM and CFM.

In figure 22 DLLR 3210 is the delay locked loop for generating the phase vectors and is called the reference loop. Each device uses a single DLLR loop. DLLF 3200 is the delay locked loop for generating a predetermined phase relationship between the input clock and the output clock. The DLLF 3200 loop is used to generate a 90 degree phase relationship between CTM and tclk, because data is always transmitted in quadrature to the receive clock. The DLLF 3205 is used to generate a zero degree phase relationship between CFM and rclk. Thus, when a slave sends data to the master, the data changes occur 90 degrees out of phase with the CTM clock, the clock traveling toward the master. The master receives the clock CTM and generates the rclk signal for operating its receiver. Signal rclk in the master is in a 0 degree phase relationship with CTM so that the data is sampled when it is not changing. Similarly, when the master sends data to a slave, it clocks its transmitter changing the data on the data bus with tclk which is in a 90 degree phase relationship with the CFM. A slave 3110 receiving the data in its receiver 3180 operates its receiver using rclk which has a 0 degree phase relationship with the CFM. Thus, the receiver will sample the data when it is not changing. In this manner, data may be

transmitted using both edges of the CTM or CFM clocks and safely sampled in the receiver.

In one embodiment, the master of figure 22 is an intelligent device, such as a microprocessor, an application specific integrated circuit (ASIC), a memory controller, or a graphics engine. The slave devices may be DRAMs, SRAMs, ROMs, EPROMs, flash memories, or other memory devices.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

WHAT IS CLAIMED IS:

- 1           1.    A method for producing a set of phase vectors,  
2    the method comprising the steps of:  
3            producing a set of phase vectors from a set of delay  
4    producing elements coupled in series to form a chain, the  
5    first delay in the chain receiving a chain-input clock, the  
6    chain-input clock coupled to an input clock, wherein any two  
7    adjacent phase vectors are separated by an unit delay and all  
8    unit delays are equal; and  
9            adjusting the delays between phase vectors such that  
10   a selected phase vector is in a predetermined phase  
11   relationship with the input clock, wherein the set of phase  
12   vectors spans a predetermined degree of phase shift of the  
13   input clock.
- 1           2.    The method of claim 1, wherein the  
2    predetermined degree of phase shift of the input clock spanned  
3    by the phase vectors is 360 degrees.
- 1           3.    The method of claim 1, wherein the  
2    predetermined degree of phase shift of the input clock spanned  
3    by the phase vectors is 180 degrees.
- 1           4.    The method of claim 1, wherein the  
2    predetermined phase relationship between the input clock and  
3    the last phase vector is 180 degrees.  
4
- 5           5.    The method of claim 1, further comprising the  
6    step of storing the current adjustment of the delays in the  
7    chain, wherein the predetermined phase relationship between  
8    the input clock and the selected phase vector and the  
9    predetermined degree of phase shift of the input clock are  
10   preserved during a period of time when the clock source is not  
11   present.
- 1           6.    The method of claim 1, wherein the step of  
2    adjusting the delays between the vectors includes the step of:

3           detecting the deviation from the predetermined phase  
4 relationship between the input clock and the selected phase  
5 vector.

1           7. The method of claim 6, further comprising the  
2 step of filtering the detected deviation from the  
3 predetermined phase relationship to reduce loop jitter.

1           8. The method of claim 1, wherein the chain-input  
2 clock and the outputs of each delay in the chain are buffered  
3 to produce the input clock and the set of phase vectors,  
4 respectively.

1           9. The method of claim 1, wherein a delay element  
2 is coupled to the end of the chain so that all phase vectors  
3 produced by the chain have the same loading characteristics.

1           10. The method of claim 1, wherein the chain-input  
2 clock is coupled through a buffer to a clock source.

1           11. The method of claim 10, wherein the buffer is a  
2 duty cycle correcting amplifier.

1           12. A method for generating a predetermined phase  
2 relationship between an input clock and an output clock, the  
3 method comprising the steps of:

4           selecting a pair of phase vectors from a set of  
5 phase vectors, each vector separated in time from an adjacent  
6 vector by an unit delay;  
7           producing the output clock from an interpolator that  
8 receives the selected pair of phase vectors;  
9           delaying the output clock from the interpolator by a delay  
10 equal to a multiple of the unit delay to produce a feedback  
11 clock;

12           adjusting the selection of a pair of phase vectors  
13 received by the interpolator so that the phase of the input  
14 clock lies between the selected pair of phase vectors;



15 detecting the difference in phase between the input clock and  
16 the feedback clock;

17 interpolating between selected pair of vectors so  
18 that the feedback clock is in phase with the input clock based  
19 on the detected phase difference between the input clock and  
20 the feedback clock; and

21 wherein the output clock from the interpolator has  
22 the predetermined phase relationship with the input clock,  
23 when the feedback clock is in phase with the input clock, the  
24 predetermined phase relationship being a multiple of the unit  
25 delay.

1 13. The method of claim 12, wherein the step of  
2 detecting the difference in phase includes the step of  
3 filtering the detected phase difference between the input  
4 clock and the feedback clock.

1 14. The method of claim 12, further comprising the  
2 step of storing the current selection of phase vectors and the  
3 current adjustment of the interpolator, wherein the current  
4 selection of phase vectors and the current adjustment of the  
5 interpolator are preserved during a period of time when the  
6 input clock not is not present or the set of phase vectors is  
7 not present.

1 15. The method of claim 12, wherein the multiple of  
2 the unit delay includes zero.

1 16. The method of claim 12, further comprising the  
2 step of delaying the output clock from the interpolator by a  
3 delay equal to a multiple of the unit delay to produce the  
4 output clock, wherein the output clock has a predetermined  
5 phase relationship with the input clock, the predetermined  
6 phase relationship being a multiple of the unit delay.

1 17. The method of claim 16, wherein the output  
2 clock may lead or lag the input clock by a multiple of the  
3 unit delay.

1           18. The method of claim 12, wherein the output  
2 clock from the interpolator is buffered with a first clock  
3 buffer to produce the output clock; and

4           wherein the feedback clock is buffered with a second  
5 clock buffer to produce the feedback clock, the first and  
6 second clock buffers having substantially the same delay and  
7 the output clock having a predetermined phase relationship  
8 with the input clock, the predetermined phase relationship  
9 being a multiple of the unit delay.

1           19. Circuitry for producing a set of phase vectors,  
2 the circuitry comprising:

3           at least two adjustable delay elements each having a  
4 delay adjust signal, the delay elements coupled in series to  
5 form a chain for producing a set of phase vectors, wherein at  
6 least one phase vector is produced at the output of each delay  
7 element and wherein the first delay element in the chain  
8 receives a chain-input clock, the chain-input clock coupled to  
9 an input clock; and

10          a delay adjusting circuit receiving the input clock  
11 and a selected phase vector, the delay adjusting circuit for  
12 adjusting the delays between the phase vectors with the delay  
13 adjust signal such that the input clock is in the  
14 predetermined phase relationship with the selected phase  
15 vector and the set of phase vectors spans a predetermined  
16 degree of phase shift of the input clock.

1           20. The circuitry of claim 19, wherein the  
2 predetermined degree of phase shift of the input clock spanned  
3 by the phase vectors is 360 degrees.

1           21. The circuitry of claim 19, wherein the  
2 predetermined degree of phase shift of the input clock spanned  
3 by the phase vectors is 180 degrees.

1           22. The circuitry of claim 19, wherein the  
2 predetermined phase relationship between the input clock and  
3 the last phase vector is 180 degrees.

1           23. The circuitry of claim 19, further comprising:  
2           a set of buffers each coupled to the output of a  
3 delay element in the chain, the set of buffers for producing a  
4 set of phase vectors at the output of the set of buffers; and  
5           a clock buffer having an input connected to the  
6 chain-input clock, the clock buffer for producing the clock  
7 input, wherein the set of buffers and the clock buffer have  
8 substantially the same delay.

1           24. The circuitry of claim 19, wherein a delay  
2 element is added to the chain, the delay element receiving the  
3 last phase vector in the chain so that all phase vectors  
4 produced by the chain have the same loading characteristics.

1           25. The circuitry of claim 19, wherein the delay  
2 adjusting circuit comprises:  
3           a phase detector receiving the input clock and the  
4 last phase vector, the phase detector for determining whether  
5 the input clock is in a predetermined phase relationship with  
6 the last phase vector and for producing a phase detector  
7 output signal based on the difference from the predetermined  
8 phase relationship between the input clock and last phase  
9 vector; and  
10          a control circuit receiving the phase detector  
11 output signal and for generating the delay adjust signal based  
12 on the phase detector output signal.

1           26. The circuitry of claim 25, wherein the control  
2 circuit includes a digital storage circuit having state  
3 information for representing the current delay adjustment of  
4 the loop.

1           27. The circuitry of claim 26, wherein the state  
2 information of the digital storage circuit is preserved when  
3 the clock source is not present.

1           28. The circuitry of claim 25, wherein the control  
2 circuit comprises:

3 a counter circuit receiving the phase detector  
4 output signal and generating a digital count based on the  
5 phase detector output signal; and

6 a digital to analog converter receiving the digital  
7 count and generating the delay adjust signal, wherein the  
8 delay adjust signal is an analog signal proportional to the  
9 digital count.

1 29. The circuitry of claim 25, wherein the control  
2 circuit comprises:

3 a filter receiving the phase detector output signal  
4 and generating a filtered phase detector output signal for  
5 reducing loop jitter;

6 a counter circuit the counter circuit receiving the  
7 filtered phase detector output signal and generating a digital  
8 count based on the phase detector output signal; and

9 a digital to analog converter receiving the digital  
10 count and generating the delay adjust signal, wherein the  
11 delay adjust signal is an analog signal proportional to the  
12 digital count.

1 30. The circuitry of claim 29, wherein the filter  
2 is a digital filter.

1 31. The circuitry of claim 25, further comprising:  
2 a duty cycle correcting amplifier having an input  
3 coupled to a clock source, the duty cycle correcting amplifier  
4 generating the chain-input clock; and

5 a duty cycle correcting circuit receiving the  
6 chain-input clock and adjusting the duty cycle correcting  
7 amplifier such that the chain-input clock has a duty cycle  
8 substantially close to 50%.

1 32. Circuitry for generating a predetermined phase  
2 relationship between a pair of clocks, the circuit comprising:

3 selection circuitry having as inputs a set of phase  
4 vectors and a selection control signal, each vector separated  
5 in time from an adjacent vector by an unit delay, the

6 selection circuitry for selecting a pair of phase vectors from  
7 the set;

8 a phase interpolator circuit receiving the selected  
9 pair of phase vectors and a phase adjust signal and generating  
10 a phase interpolator output clock, the phase interpolator for  
11 adjusting the phase of phase interpolator clock, wherein the  
12 output clock is coupled to the phase interpolator output  
13 clock;

14 at least one feedback delay element coupled to the  
15 phase interpolator output clock to produce a first delayed  
16 clock, the feedback delay element delaying the first delayed  
17 clock from the phase interpolator output clock by an amount  
18 equal to a multiple of the unit delay, wherein a feedback  
19 clock is coupled to the first delayed clock; and

20 a phase adjusting circuit receiving the input clock  
21 and the feedback clock, wherein the phase adjusting circuit  
22 produces the selection control signal for adjusting the  
23 selection of a pair of phase vectors produced by the selection  
24 circuitry so that the phase of the input clock lies between  
25 the selected pair of phase vectors and wherein the phase  
26 adjusting circuit produces the phase adjust signal for  
27 adjusting the phase interpolator so that the feedback clock is  
28 in phase with the input clock, wherein the output clock has  
29 the predetermined phase relationship with the input clock,  
30 when the feedback clock is in phase with the input clock, the  
31 predetermined phase relationship being a multiple of the unit  
32 delay.

1 33. The circuitry of claim 32, wherein the multiple  
2 of the unit delay includes zero.

1 34. The circuitry of claim 32, further comprising:  
2 at least one output delay element coupled to the  
3 phase interpolator output clock to produce the output clock;  
4 and

5 wherein the output delay element delays the output  
6 clock delayed by an amount equal to a multiple of the unit  
7 delay and wherein the output clock has a predetermined phase

8 relationship with the input clock, the predetermined phase  
9 relationship being a multiple of the unit delay.

1 35. The circuitry of claim 34, wherein the output  
2 clock may lead or lag the input clock by a multiple of the  
3 unit delay.

1 36. The circuitry of claim 32, wherein the output  
2 clock from the interpolator is buffered with a first clock  
3 buffer to produce the output clock and wherein the feedback  
4 clock is buffered with a second clock buffer to produce the  
5 feedback clock, the first and second clock buffers having  
6 substantially the same delay and the output clock having a  
7 predetermined phase relationship with the input clock, the  
8 predetermined phase relationship being a multiple of the unit  
9 delay.

1 37. The circuitry of claim 32, wherein the phase  
2 adjusting circuit comprises:  
3 a phase detector receiving the input clock and the  
4 feedback clock, the phase detector for determining whether the  
5 feedback clock is in phase with the input clock and for  
6 producing a phase detector output based on the difference in  
7 phase between the feedback clock and the input clock; and  
8 a control circuit receiving the phase detector  
9 output signal, the control circuit producing the selection  
10 control signal for adjusting the selection of a pair of phase  
11 vectors generated by the selection circuitry and producing the  
12 phase adjust signal for adjusting the phase interpolator.

1 38. The circuitry of claim 37, wherein the control  
2 circuit includes a digital storage circuit having state  
3 information for representing the current selection of phase  
4 vectors and the adjustment of the phase interpolator.

1 39. The circuitry of claim 38, wherein the state  
2 information of the digital storage circuit is preserved when

3 the input clock not is not present or the set of phase vectors  
4 is not present.

1 40. The circuitry of claim 37, wherein the control  
2 circuit includes:

3 a counter circuit receiving the phase detector  
4 output signal and generating a digital count based on the  
5 phase detector output signal; and

6 a digital to analog converter receiving the digital  
7 count and generating the phase adjust signal, wherein the  
8 phase adjust signal is an analog signal proportional to the  
9 digital count.

1 41. The circuitry of claim 37, wherein the control  
2 circuit includes:

3 a filter receiving the phase detector output signal  
4 and generating a filtered phase detector output signal for  
5 reducing loop jitter;

6 a counter circuit receiving the filtered phase  
7 detector output signal and generating a digital count based on  
8 the phase detector output signal; and

9 a digital-to-analog converter receiving the digital count  
10 and generating the phase adjust signal, wherein the phase  
11 adjust signal is an analog signal proportional to the digital  
12 count.

1 42. The circuitry of claim 41, wherein the filter  
2 is a digital filter.

1 43. The circuitry of claim 32, further comprising:  
2 a first duty cycle correcting amplifier receiving  
3 the first delayed clock, the first duty cycle correcting  
4 amplifier generating the feedback clock;

5 a second duty cycle correcting amplifier receiving  
6 the phase interpolator output clock, the second duty cycle  
7 correcting amplifier generating the output clock; and

8 a duty cycle correcting circuit receiving the  
9 feedback clock and adjusting the first and second duty cycle

10 correcting amplifiers such that the feedback clock and output  
11 clock have substantially the same duty cycle, wherein the duty  
12 cycle is substantially close to 50%.

1 44. A method for generating a predetermined phase  
2 relationship between a pair of clocks, the method comprising  
3 the steps of:

4 operating a first delay locked loop circuitry to  
5 generate a set of phase vectors from an input clock, wherein  
6 any two adjacent phase vectors are separated by an unit delay  
7 and all unit delays are equal and wherein the set of phase  
8 vectors spans a predetermined degree of phase shift of the  
9 input clock, when the first loop is locked; and

10 operating a second delay locked loop circuitry to  
11 generate the predetermined phase relationship between the pair  
12 of clocks, wherein a delayed version of the output clock is in  
13 phase to the input clock, when the second loop is locked, the  
14 delayed version of the output clock being a multiple of the  
15 unit delay between the phase vectors generated from the first  
16 loop and the unit delay being derived from the first delayed  
17 locked loop.

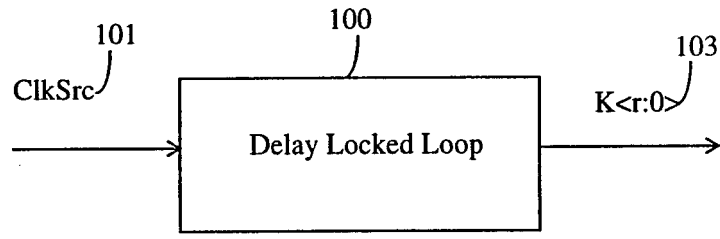
1 45. A memory system comprising:  
2 a controller;  
3 a least one memory circuit;  
4 a data bus coupling said controller to said at least  
5 one memory circuit;

6 a data transmitter and data receiver circuit in at  
7 least one of said controller and said one memory circuit, at  
8 least one of said data transmitter and data receiver being  
9 coupled to clock circuitry for producing a set of phase  
10 vectors, said clock circuitry including

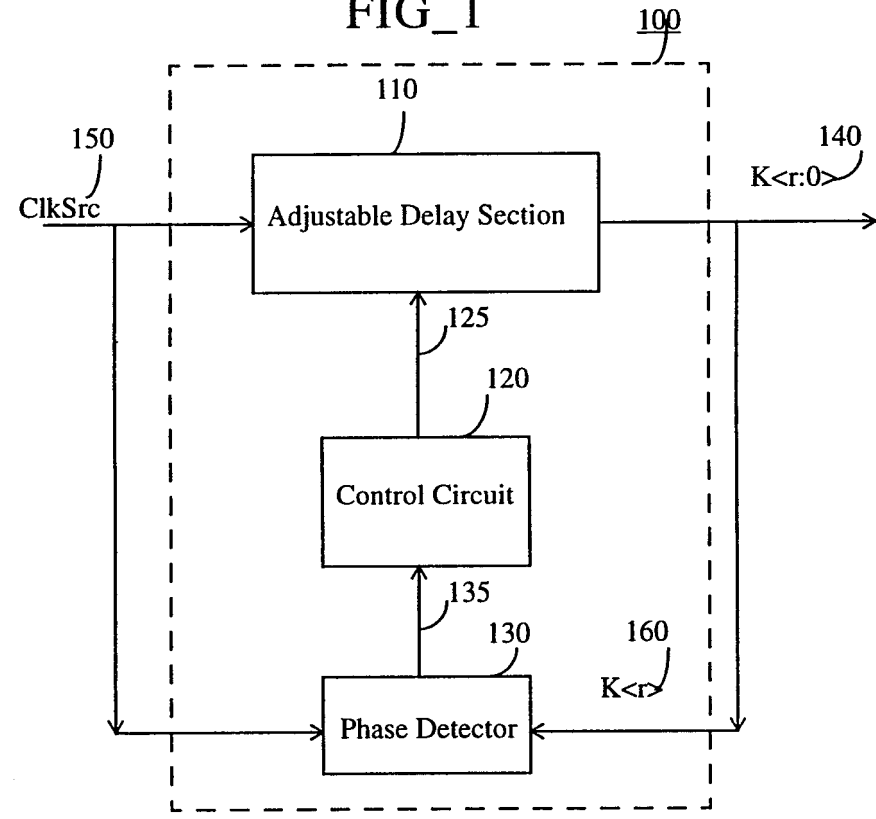
11 at least two adjustable delay elements each  
12 having a delay adjust signal, the delay elements coupled  
13 in series to form a chain for producing a set of phase  
14 vectors, wherein at least one phase vector is produced at  
15 the output of each delay element and wherein the first



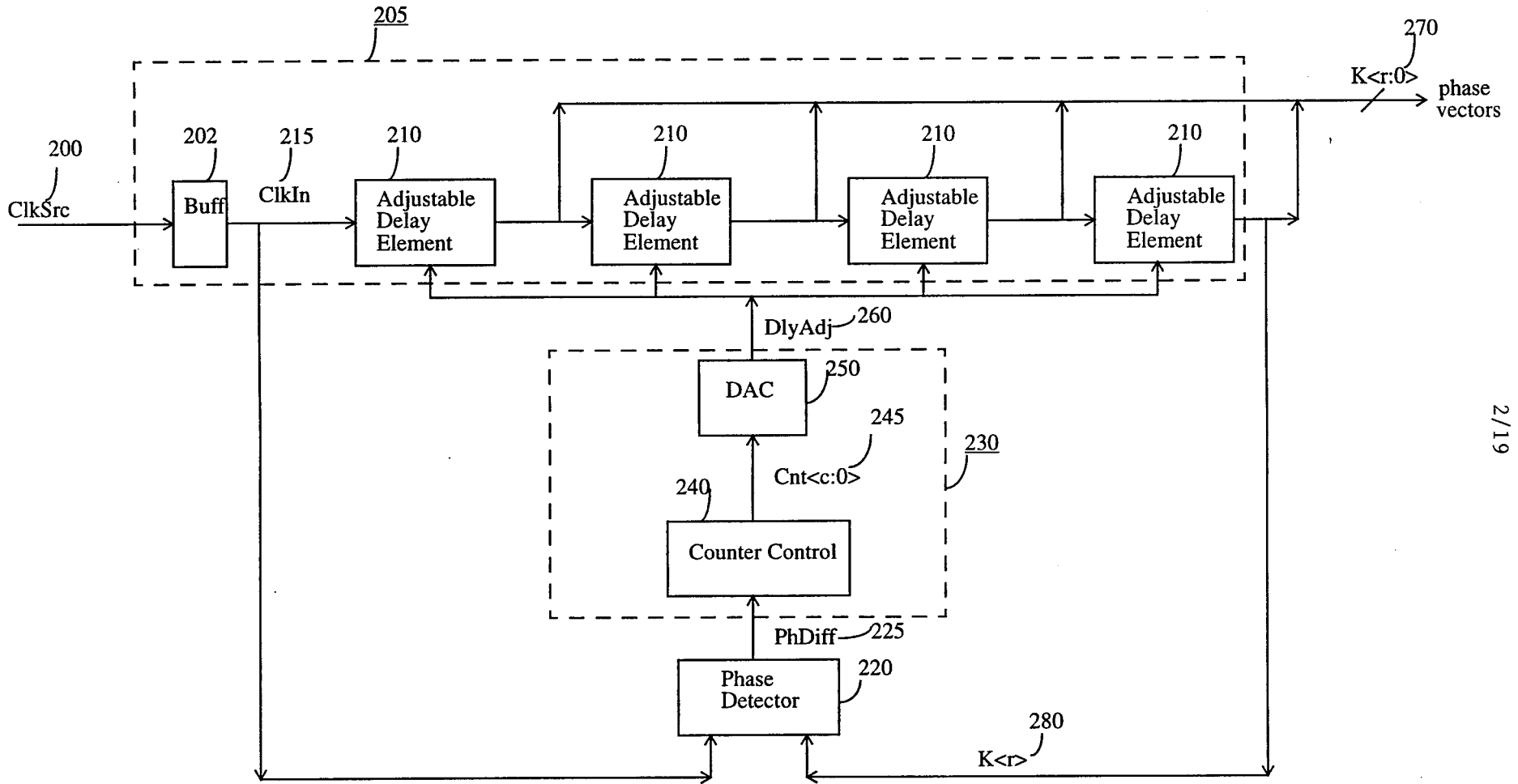
16 delay element in the chain receives a chain-input clock,  
17 the chain-input clock coupled to an input clock; and  
18 a delay adjusting circuit receiving the input  
19 clock and a selected phase vector, the delay adjusting  
20 circuit for adjusting the delays between the phase  
21 vectors with the delay adjust signal such that the input  
22 clock is in the predetermined phase relationship with the  
23 selected phase vector and the set of phase vectors spans  
24 a predetermined degree of phase shift of the input clock.



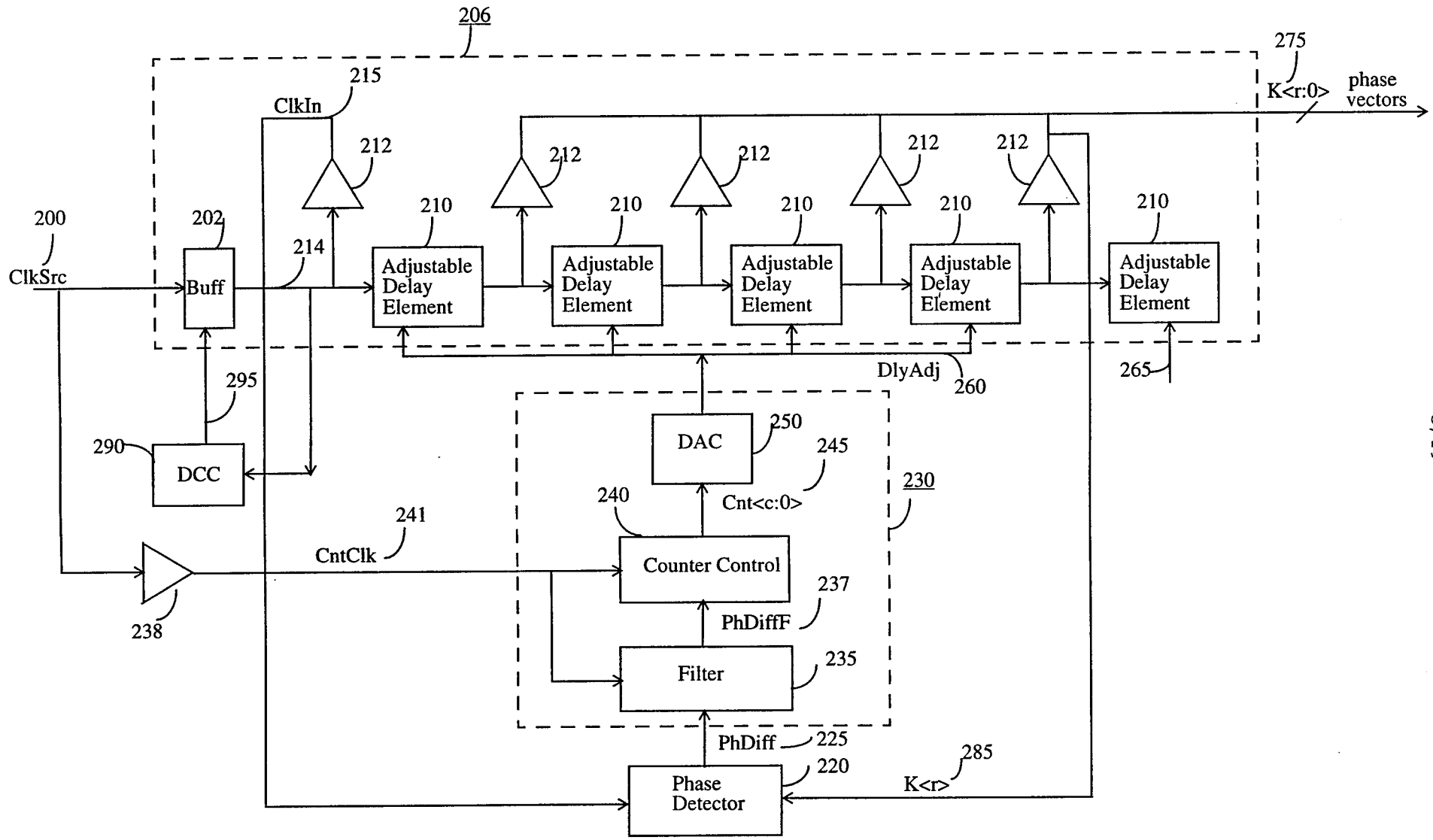
FIG\_1



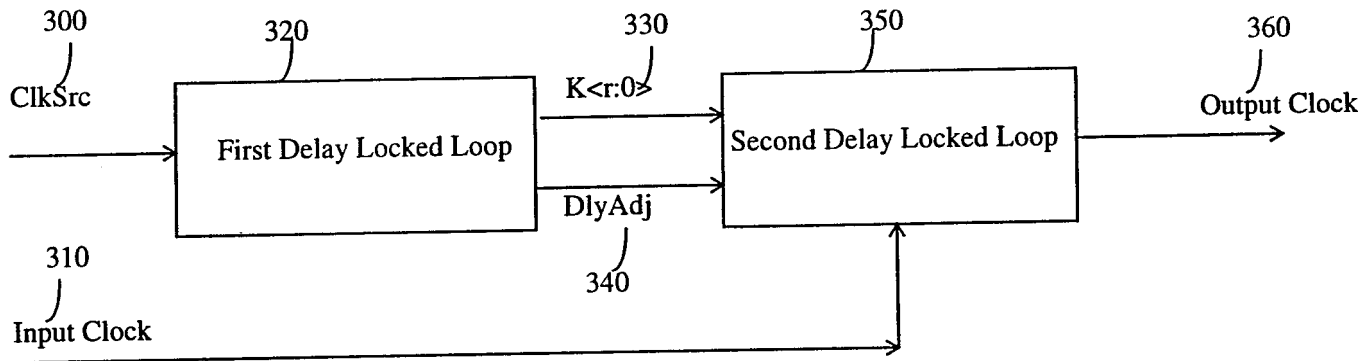
FIG\_2



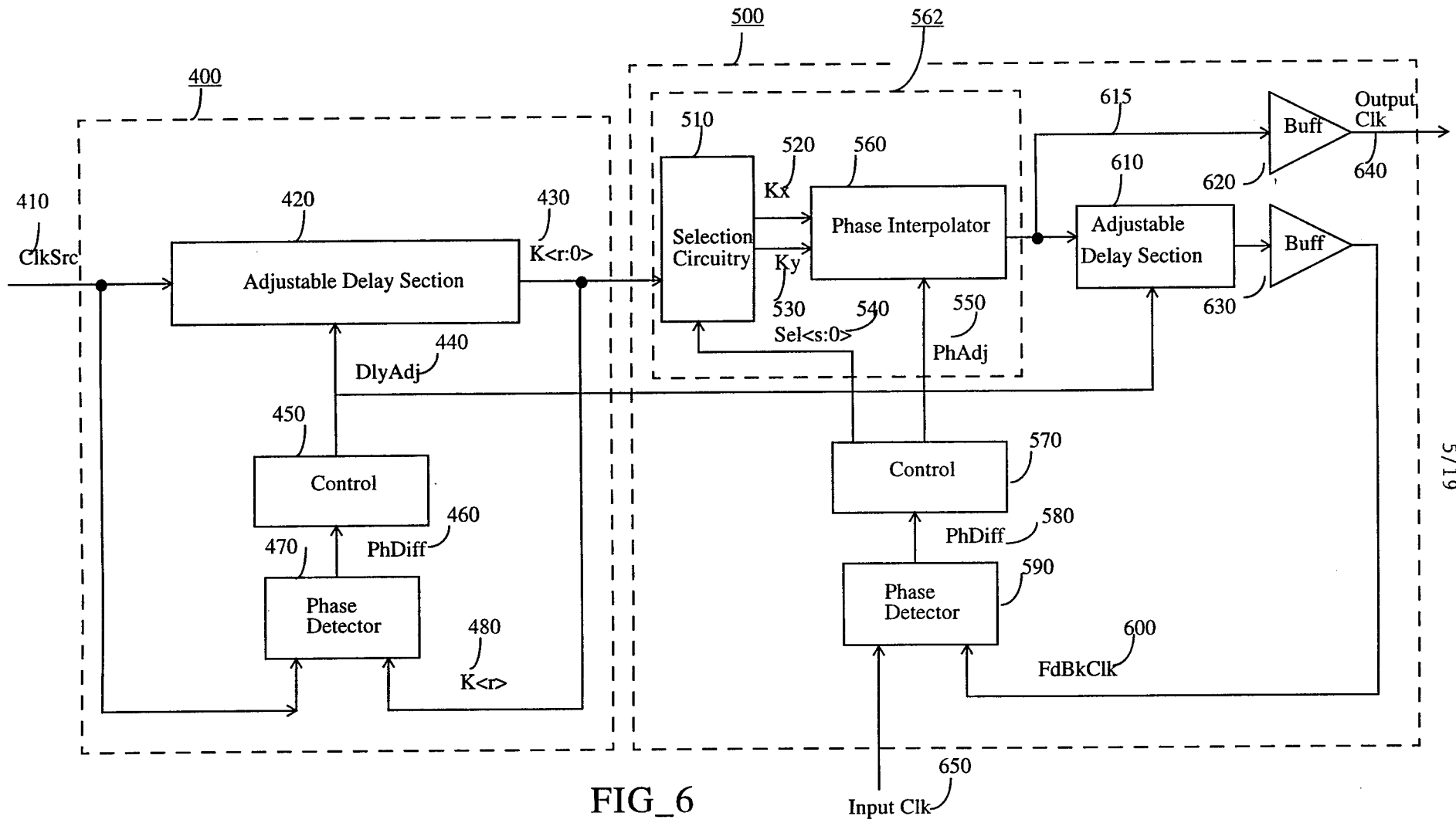
FIG\_3



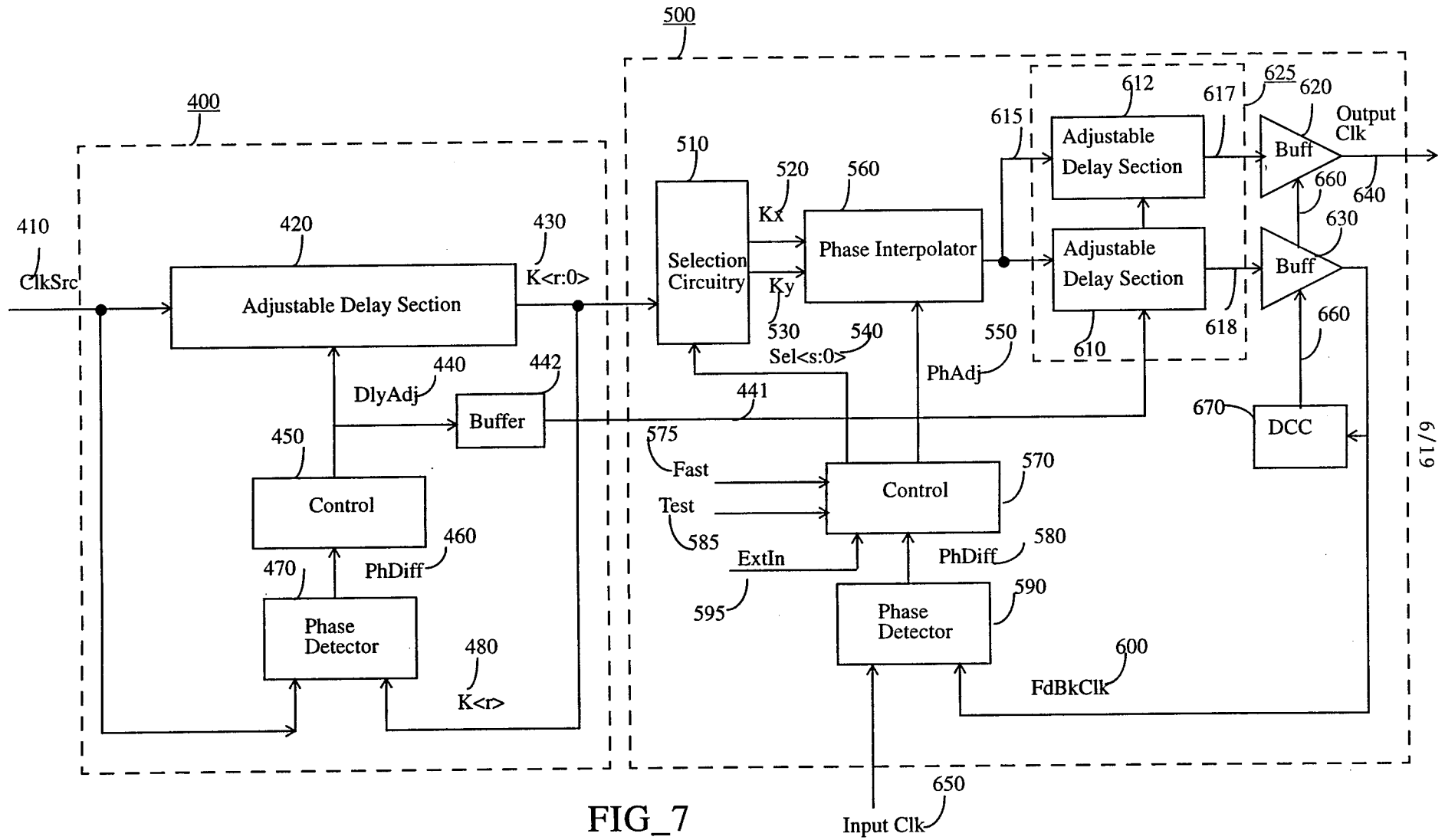
FIG\_4



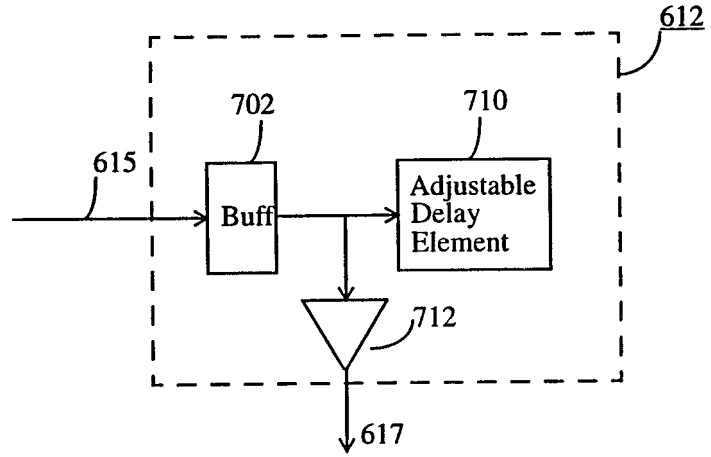
FIG\_5



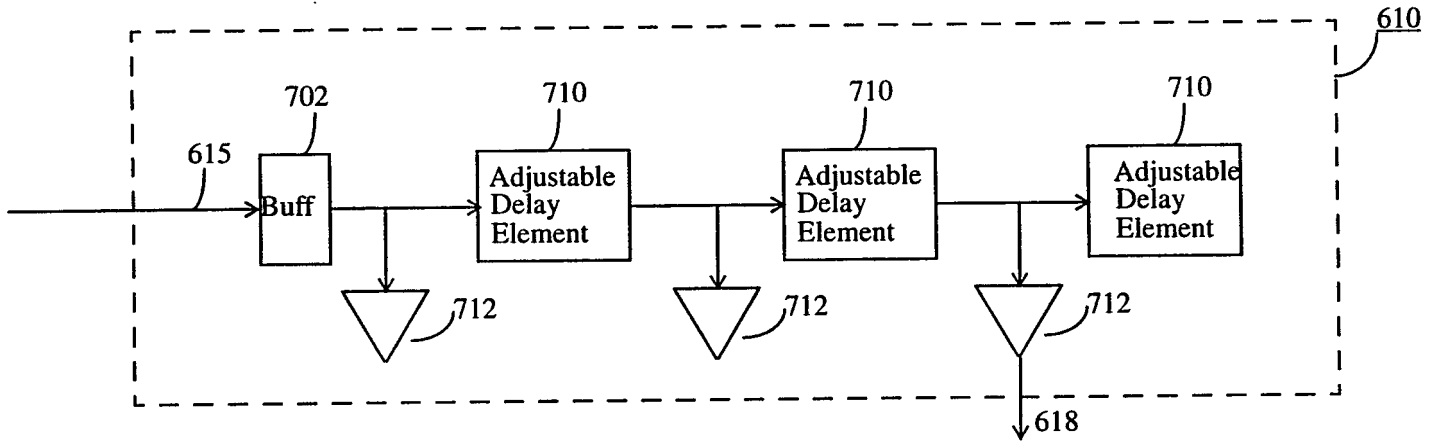
FIG\_6



FIG\_7

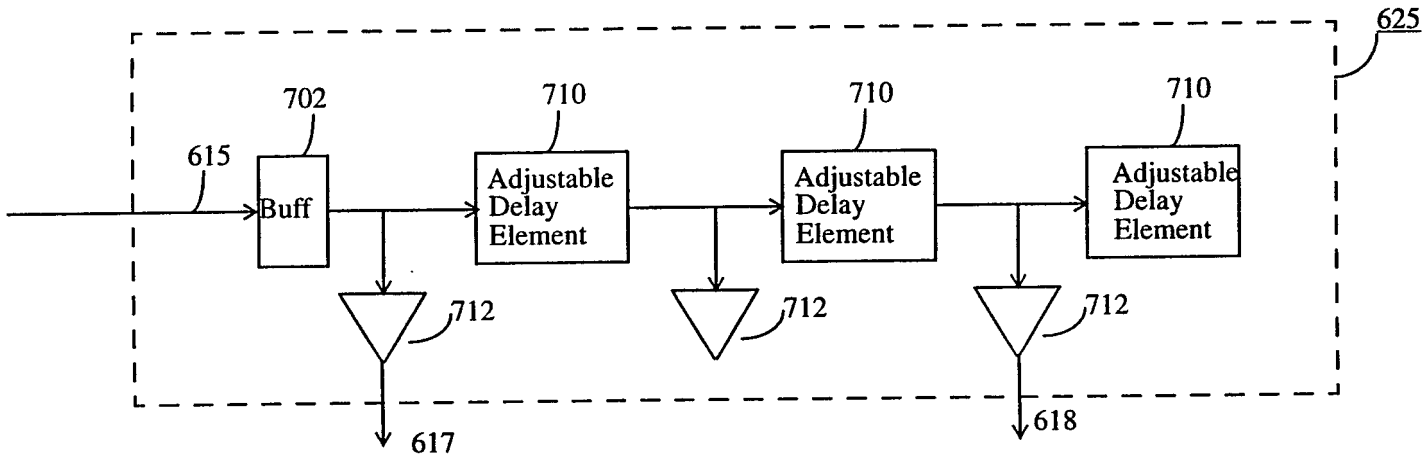


FIG\_8

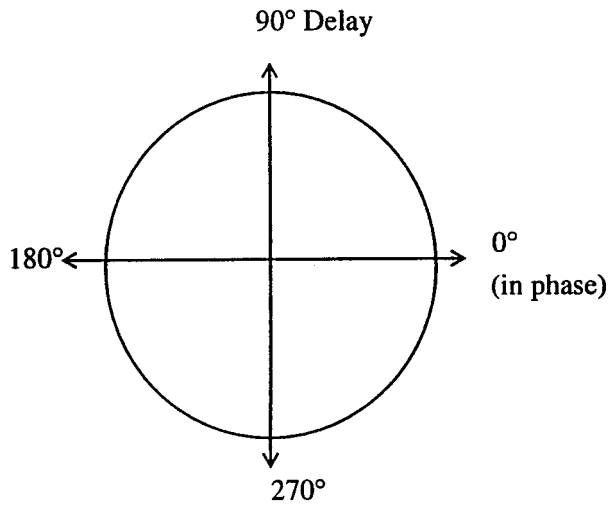


FIG\_9

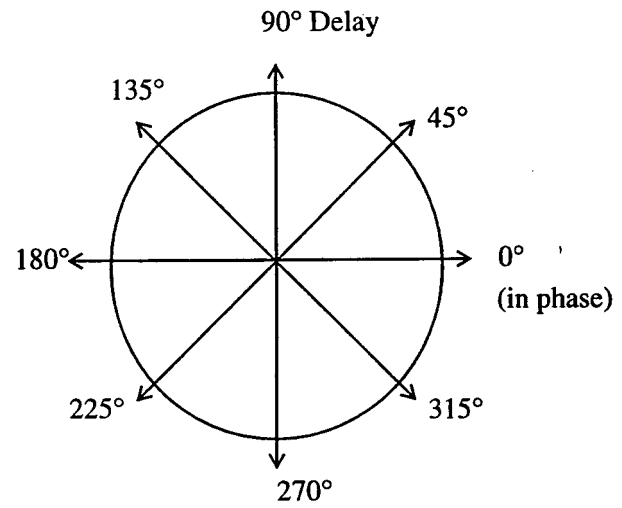




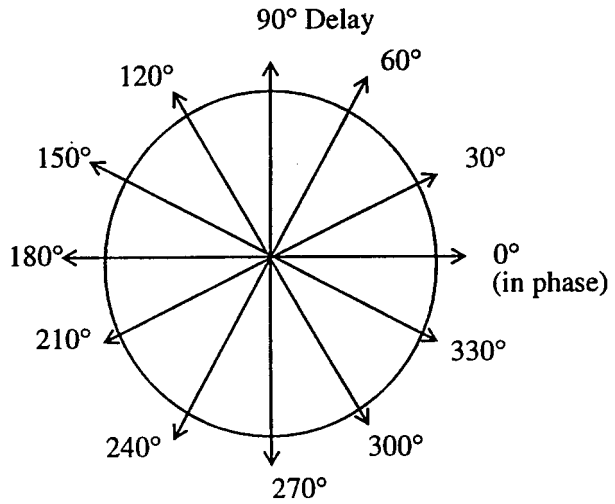
FIG\_10



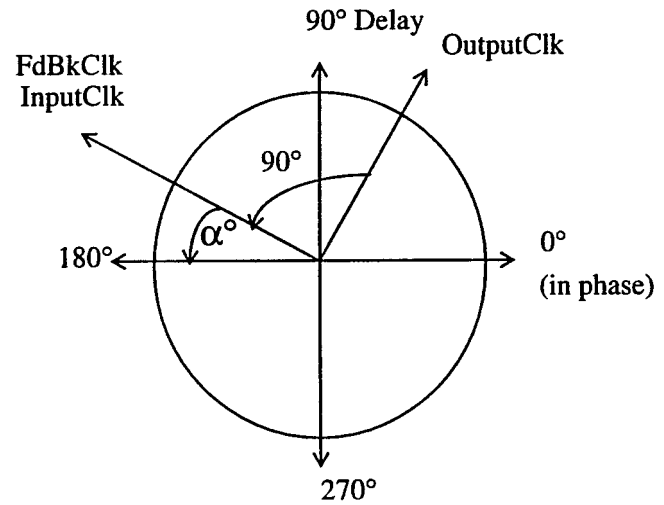
FIG\_11



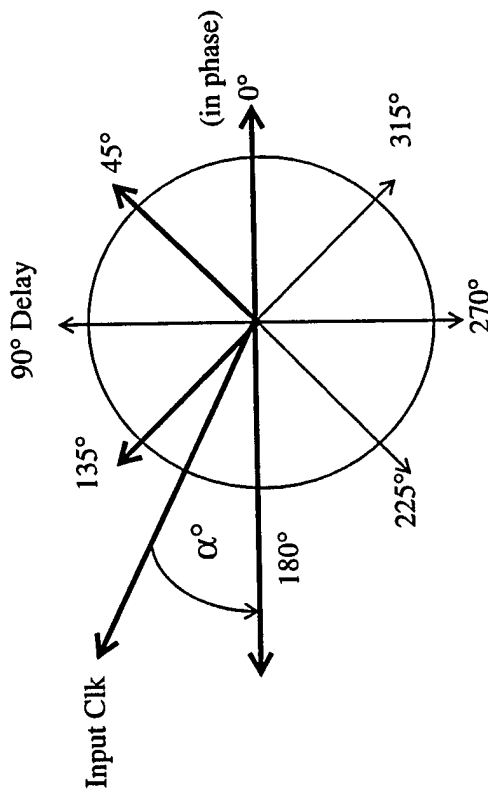
FIG\_12



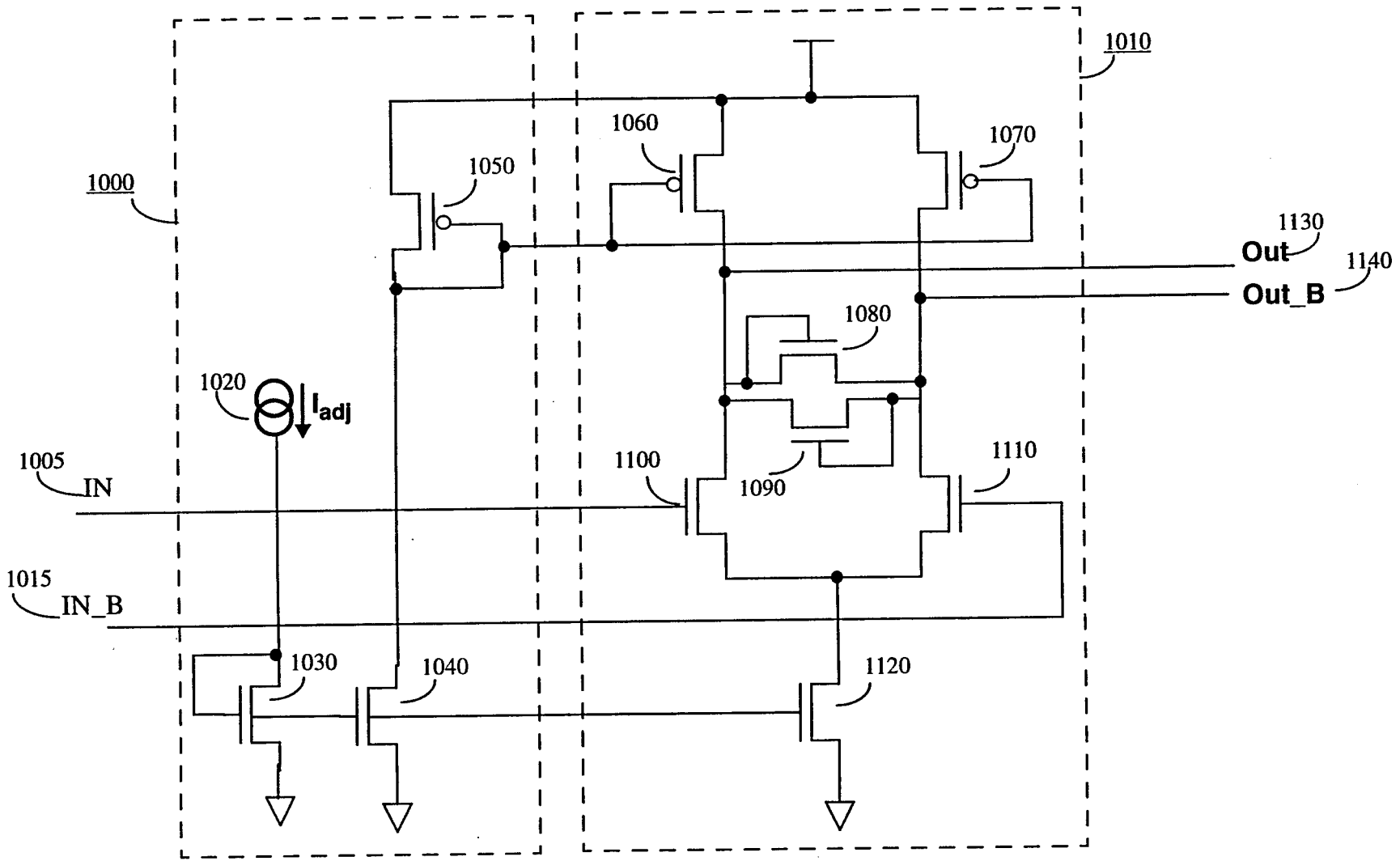
FIG\_13



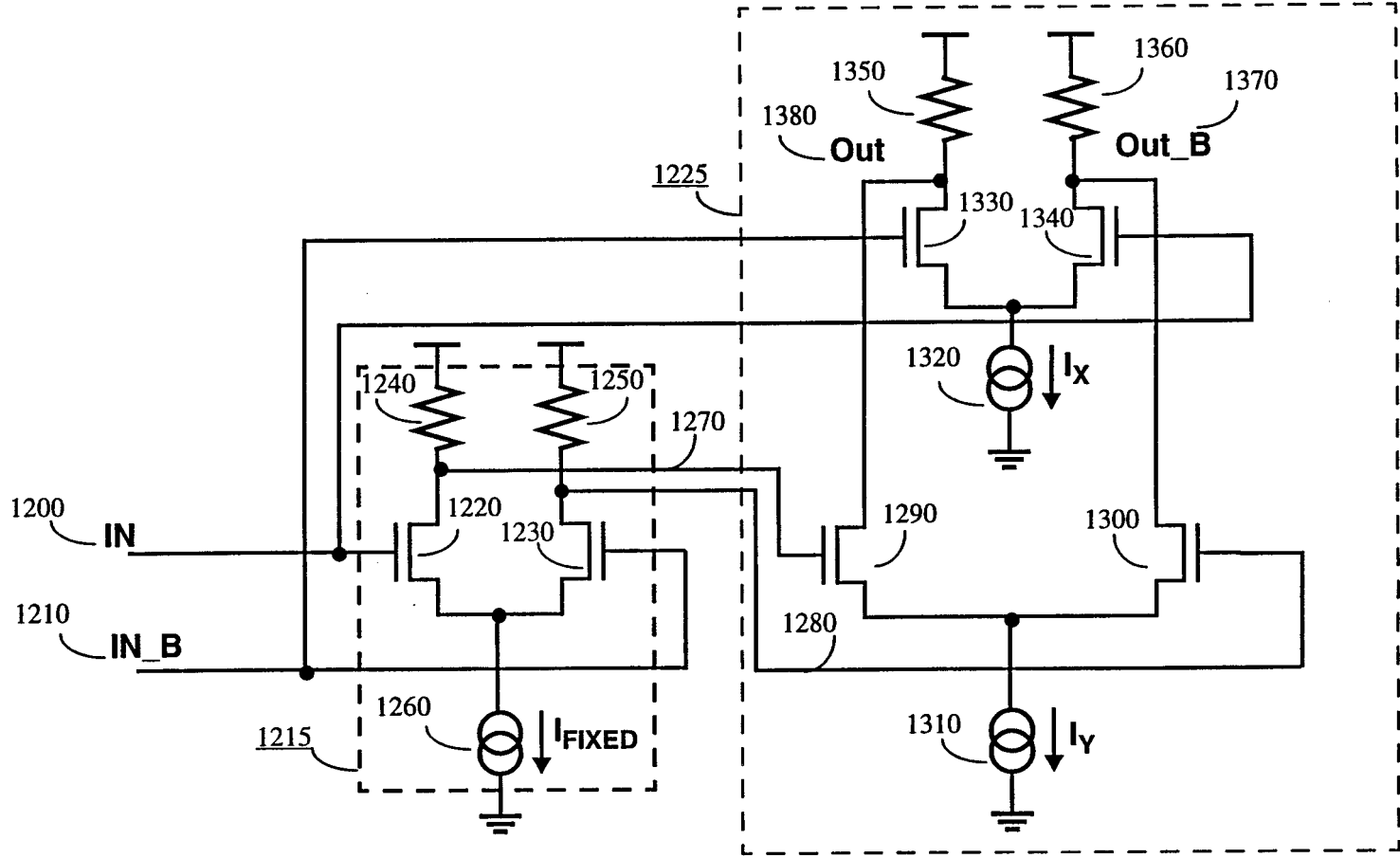
FIG\_14



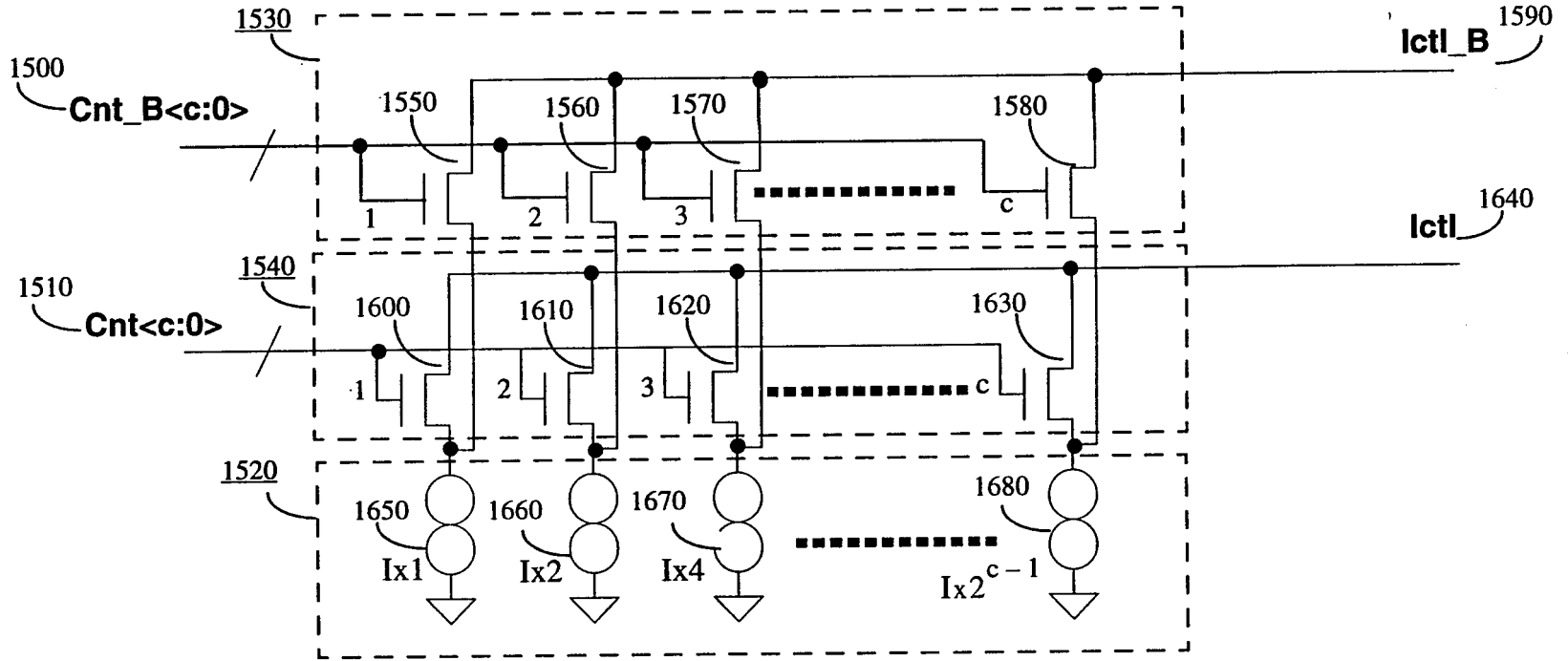
FIG\_15



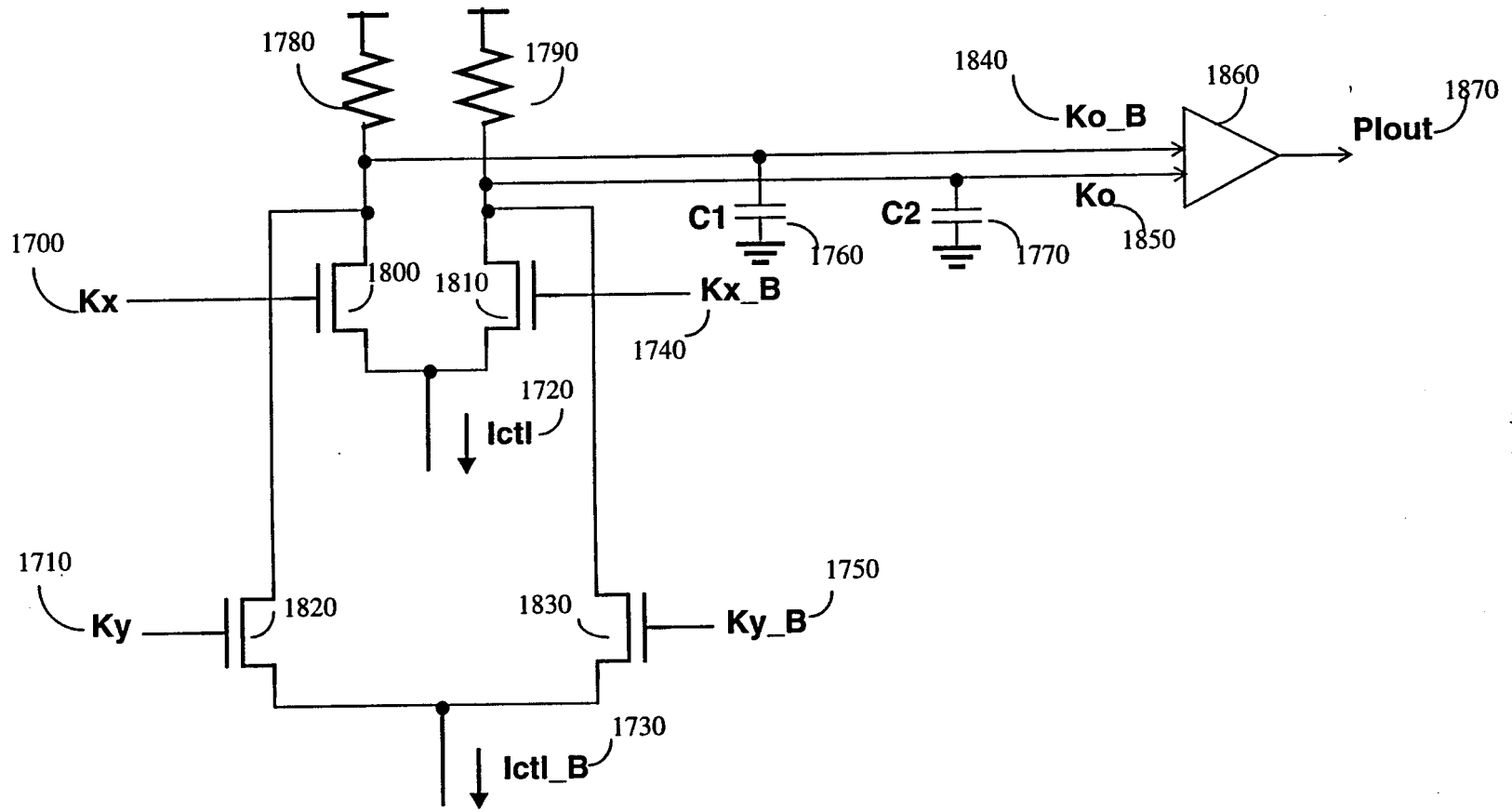
FIG\_16A



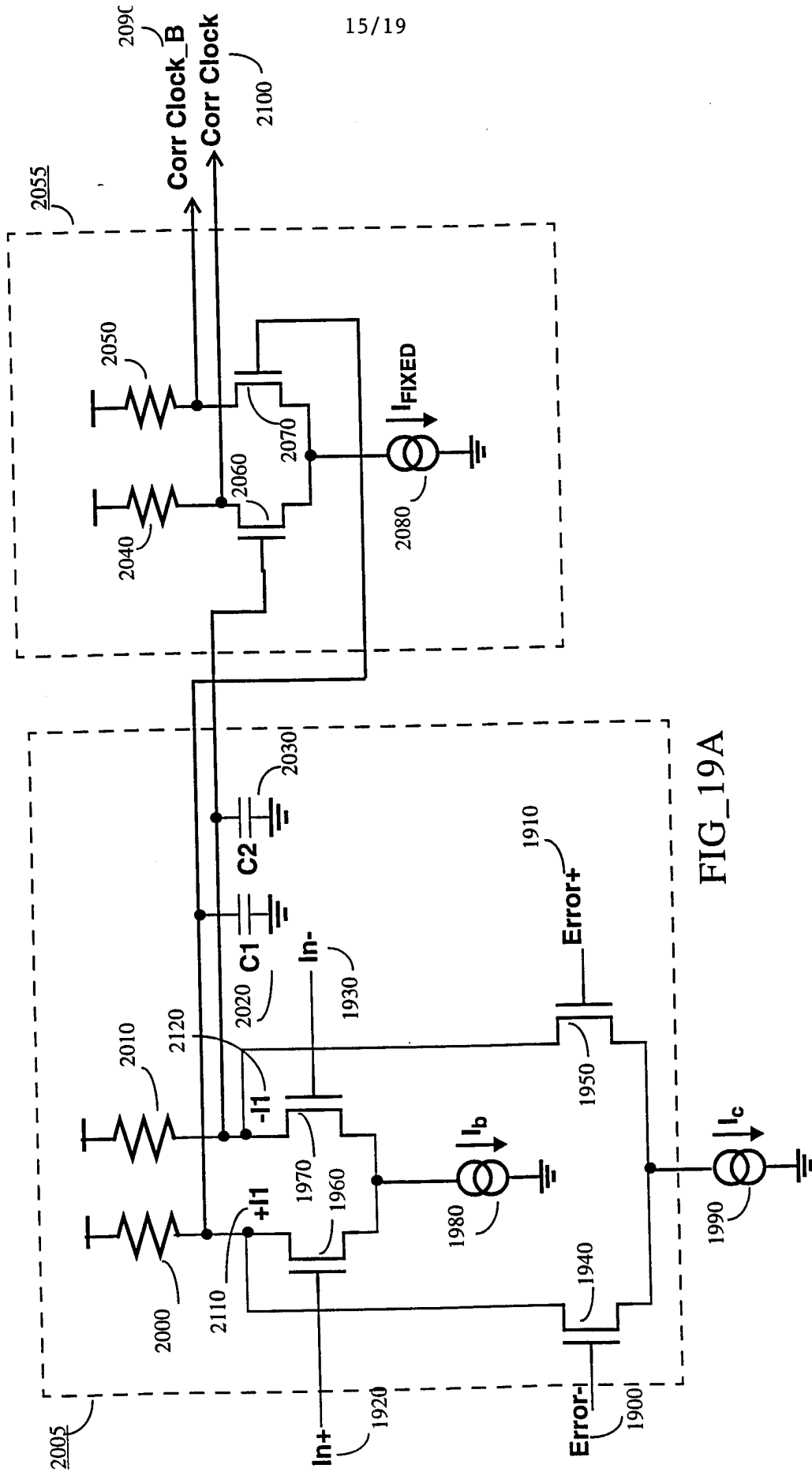
FIG\_16B



FIG\_17

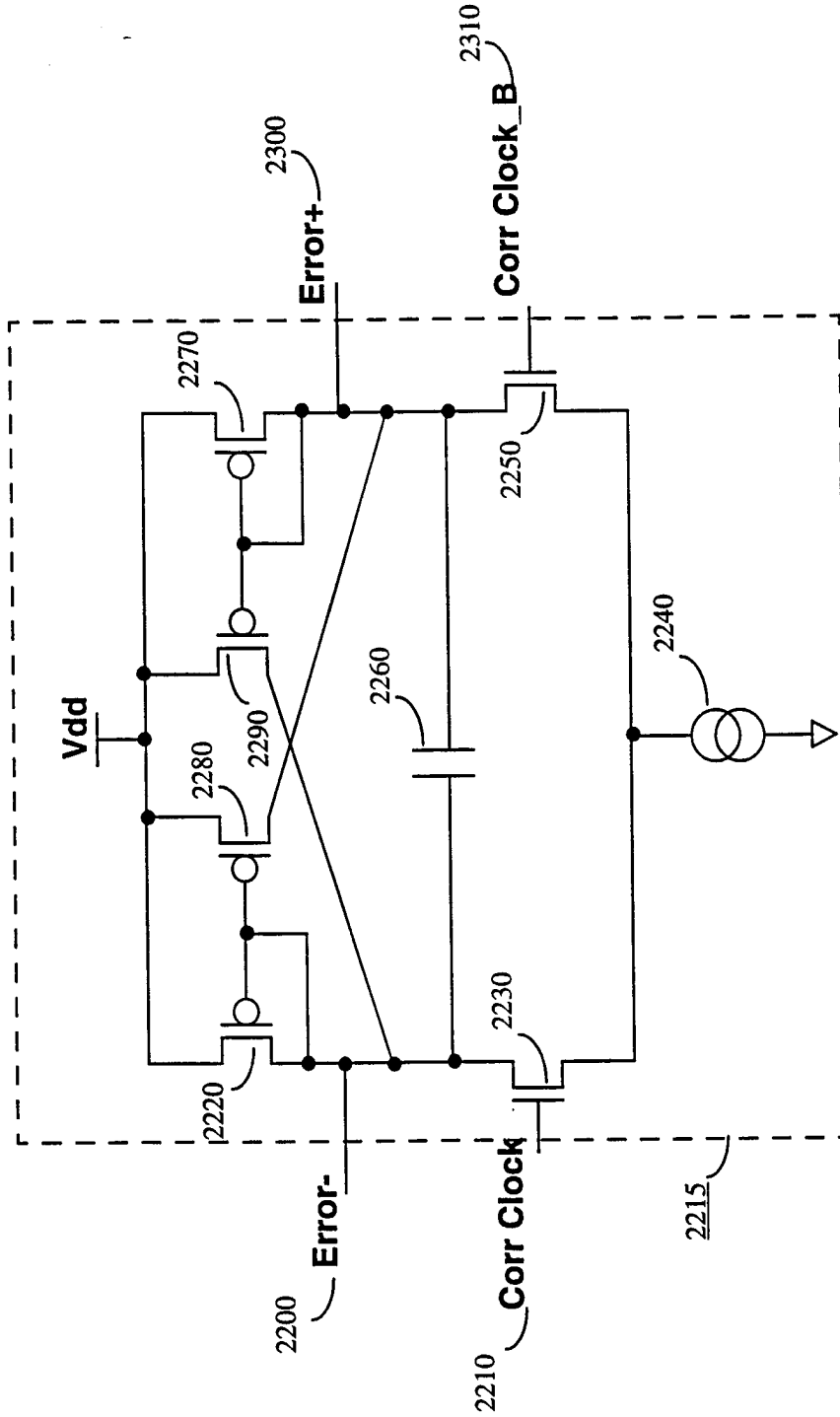


FIG\_18

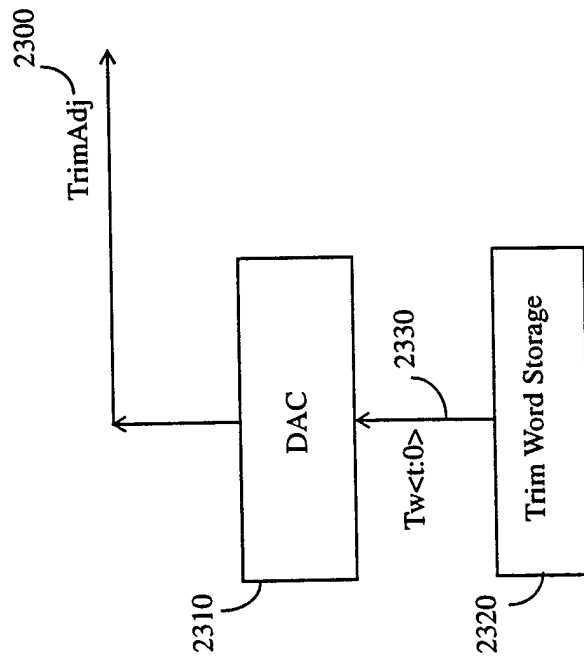


FIG\_19A

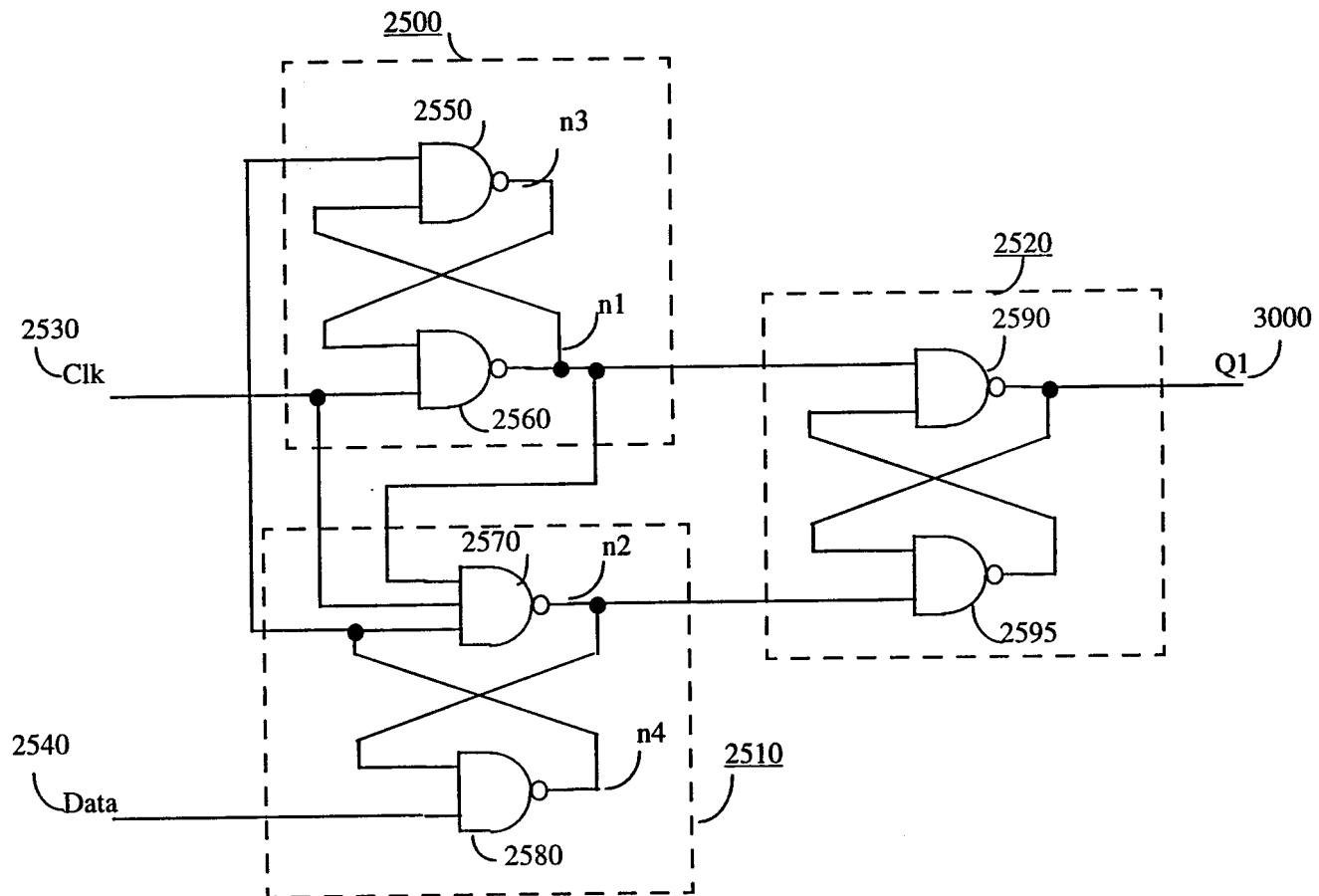




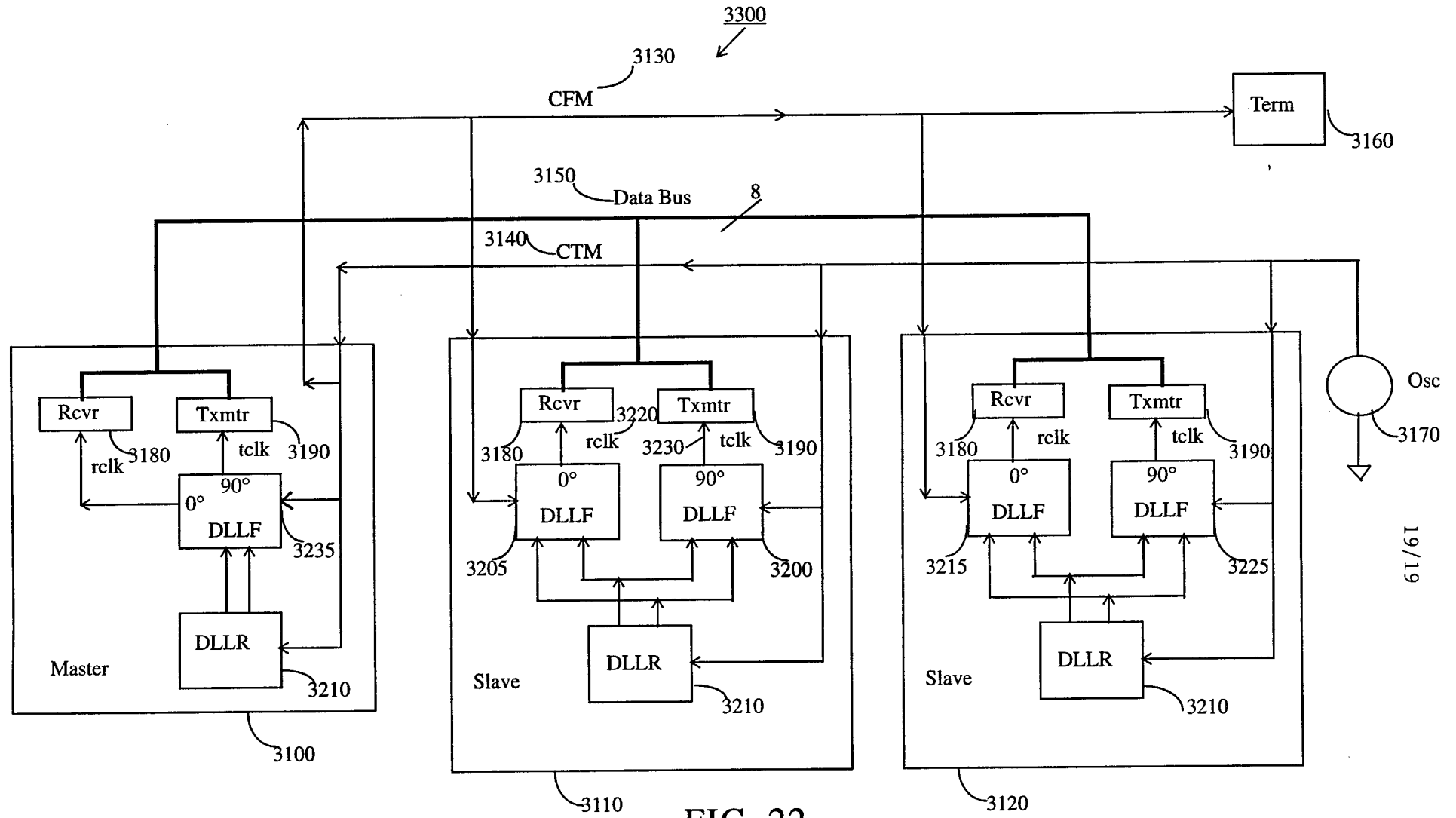
FIG\_19B



FIG\_20



FIG\_21



FIG\_22