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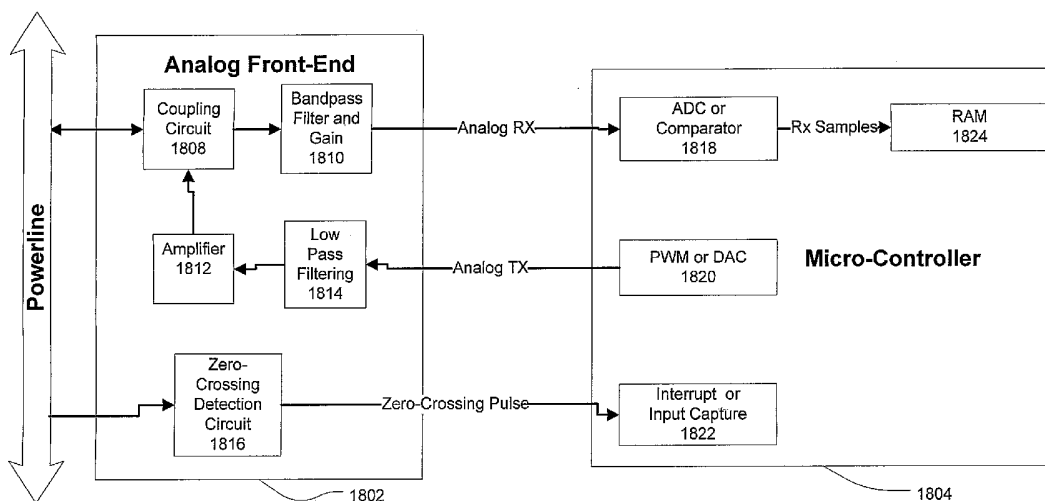
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(54) Title: SYSTEM AND METHOD FOR POWER LINE COMMUNICATIONS



(57) Abstract: A communication system for a power line is described. A transmission system of the communication system divides the time axis into a number of time slots synchronized such that one time slot can start about a zero crossing of the power line signal. These time slots are referred to as channels and are numbered from 1 to n. A modulation method is described to is narrow band continuous phase FSK, where a number m of modulating frequencies are used, arranged such that an integral number of full cycles fit into each channel time slot for all m frequencies. The system transmits during only a subset of the available time slots (channels) concentrated near the zero crossing of the power line waveform where the noise is typically minimal.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SYSTEM AND METHOD FOR POWER LINE COMMUNICATIONS

FIELD OF THE INVENTION

[0001] This invention relates to a system and method of communications for power line media, particularly transmission in the presence of high amplitude, non-stationary noise sources connected to the line.

BACKGROUND

[0002] Current high speed communication on power line media (e.g. standard in house wiring) uses a variety of modulation techniques to overcome the highly noisy environment. Two types of systems have been commonly used. Firstly, wideband systems that use spread spectrum to combat the interference may be used, see for example U.S. patent nos.: 5574748; 5090024; 5263046; 6243413; 6616254; 5579335; and 5748671, the contents of which are hereby incorporated by reference.

[0003] Secondly, narrow band systems that use one or more frequencies modulated in frequency or phase may also be used. See for example U.S. patent nos.: 5504454 and 4475217, the contents of which are hereby incorporated by reference.

[0004] It is noted that a type of modulation techniques may also use various kind of synchronization. Exemplary techniques are described in U.S. Patent nos.: 6734784; 6577231; 6784790; 6907472; and 5553081, the contents of which are hereby incorporated by reference.

[0005] The type of system used is also a function of the frequency spectrum allowed in the country of use. Most countries do not allocate enough spectrum for the wideband spread spectrum systems, so narrowband systems have been favoured, see for example:

- USA: FCC, PART 15 47 CFR CH.1 A , RADIO FREQUENCY DEVICES
(PART 15);
- EUROPE: EN50065-1 - SIGNALING ON LOW-VOLTAGE ELECTRICAL
INSTALLATIONS IN THE FREQUENCY RANGE 3 kHz TO 148.5
kHz; and

- CANADA: ICES-006 , Issue 1, August 25, 2001, AC Wire Carrier Current Devices (Unintentional Radiators),

the contents of which are hereby incorporated by reference.

[0006] One feature of these systems is that they use continuous transmission for each message, where a message typically consists of 100's of bits. However it has been observed from a large sample of data from the field that the noise on typical power lines where a number of disturbing devices are connected is not constant in either time or frequency, but exhibits quiet periods in both dimensions. Current systems do not efficiently handle these situations.

[0007] There is a need to provide a system and method of signal transmission that addresses at least some of these issues.

SUMMARY OF THE INVENTION

[0008] In a first aspect, a method for encoding data to be transmitted over a power line carrying an AC-power signal over a time period is provided. The method comprises: situating the time period about a zero crossing of the power signal; and encoding the data into the power signal in at least one signal over the time period using a signal diversity scheme. The diversity scheme can include time and frequency diversification techniques for the transmitted data signals.

[0009] In the method, the step of encoding the data may comprise: dividing the time period into a number of time slots; modulating the data signal using different signals for each of the time slots and adding the resulting signal to the power signal. This process of selectively adding a modulated data signal to the power signal may be referred to as encoding the data into the power signal in the remainder of the specification.

[0010] In the method, the step of modulating the data may utilize FSK signals to encode the data into the power signal; and m modulating frequencies may be used to modulate the data, and m may be selected such that an integral number of full cycles fit into each time slot for all m frequencies.

[0011] In the method, the data may be encoded over two or more time slots. Alternatively or additionally, the data may be encoded using two or more signals each

having a different frequency. Still further the initial phases of the signals may differ. Still further, the data may be encoded over two timeslots and differences in energies detected during each of those two time slots may be used to determine the value of the data.

[0012] The method may further comprise decoding the data from the power signal by detecting differences in energies in each of those two time slots.

[0013] In the method, the data may be encoded over at least two of the time slots.

[0014] The method may further comprise decoding the data from the time slots by summing and merging signals extracted from the slots.

[0015] In a second aspect, a circuit for transmitting outbound data and receiving inbound data in an AC-power signal is provided. The system comprises: a connection to the AC-power signal; a circuit to detect a zero crossing of the power signal; an encoding module to encode and inject the outbound data into the power signal in at least two signals over a time period around the zero crossing; and a decoding module to extract and decode the inbound data from the power signal around the time period around the zero crossing. In the system, FSK signals are used to encode and decode the inbound and outbound data.

[0016] In the circuit, the outbound data may be encoded over two or more time slots in the time period around the zero crossing. Additionally or alternatively, in the circuit, the outbound data may be encoded in two signals having different frequencies, the two signals encoded into the AC-power signal around the zero crossing. Further still, the initial phases of the signals may differ.

[0017] In the circuit, the inbound data may be decoded by evaluating differences in energies detected during two time slots around the zero crossing.

[0018] In the circuit, the outbound data may be encoded in parallel over at least two of the time slots.

[0019] In the circuit, the outbound data may be encoded in parallel over at least two of the time slots.

[0020] In the circuit, the inbound data may be encoded over multiple time slots of the time slots and may be decoded by summing and merging signals extracted from each of the multiple time slots. The signals may include real and complex voltage values.

[0021] In a third aspect, a method for transmitting data over a power line in a time period is provided. The method comprises: dividing the time period into a number of time slots synchronized such that one time slot starts about a zero crossing of a power line signal for transmitting the data, each time slot being relating to a channel and being numbered from 1 to n; modulating a narrow band continuous phase FSK in which a number m of modulating frequencies are used, and arranged such that an integral number of full cycles fit into each time slot for each channel for all m frequencies; and transmitting data during only a subset of the available time slots concentrated near the zero crossing of the power line signal.

[0022] In other aspects, various combinations of sets and subsets of the above aspects are provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Aspects of the invention will become more apparent from the following description of specific embodiments thereof and the accompanying drawings which illustrate, by way of example only, the principles of the invention. In the drawings, where like elements feature like reference numerals (and wherein individual elements bear unique alphabetical suffixes):

[0024] Figure 1a is a graph of exemplary FSK burst slots in one half power line cycle produced by an embodiment;

[0025] Figure 1b is another view of the FSK burst slots of Figure 1a;

[0026] Figure 2 is a block diagram of correlation receiver for a two frequency FSK of the embodiment related to Figure 1a;

[0027] Figure 3 is block diagram of an analog front end (AFE) of an embodiment related to Figure 1a;

[0028] Figure 4 is a schematic diagram of a transmitter circuit of the AFE of Figure 3;

- [0029] Figure 5 is a schematic diagram of a low pass filter of the AFE of Figure 3;
- [0030] Figure 6 is a schematic diagram of a high pass filter of the AFE of Figure 3;
- [0031] Figure 7 is a schematic diagram of a protection circuit of the AFE of Figure 3;
- [0032] Figure 8 is a schematic diagram of a band pass filter and amplifier of the AFE of Figure 3;
- [0033] Figure 9 is a schematic diagram of a high pass filter of the AFE of Figure 3;
- [0034] Figure 10 is a schematic diagram of a protection diode circuit of the AFE of Figure 3;
- [0035] Figure 11 is a schematic diagram of a band pass filter and amplifier of the AFE of Figure 3;
- [0036] Figure 12 is a schematic diagram of another low pass filter of the AFE of Figure 3;
- [0037] Figure 13 is a schematic diagram of another band pass filter and amplifier of the AFE of Figure 3;
- [0038] Figure 14 is a schematic diagram of a limiter of the AFE of Figure 3;
- [0039] Figures 15a and 15b are schematic diagrams of an automatic gain control amplifier of the AFE of Figure 3;
- [0040] Figure 16 is chart showing an optimized reception and transmission of multiple frequencies using a sine wave for the embodiment of Figure 3;
- [0041] Figure 17 is a graph showing a spectral density graph of signals processed by the embodiment of Fig. 3;
- [0042] Figure 18 is a block diagram of another analog front end (AFE) of another embodiment connected to a microcontroller;
- [0043] Figure 19 is a flow chart of a zero-crossing algorithm used by the AFE of Figure 18;
- [0044] Figure 20 is a voltage-time graph of a set of signals processed by the AFE of Figure 18;

[0045] Figure 21 is a flow chart of a receive window signal algorithm implemented by the AFE of Figure 18;

[0046] Figure 22 is a block diagram of a merged channels algorithm implemented by the AFE of Figure 18;

[0047] Figure 23 is a signal magnitude calculation formula used by the AFE of Figure 18;

[0048] Figure 24 is a collection of tables of frequency values and associated bit codings used by the AFE of Figure 18;

[0049] Figure 25 is a voltage-time graph of a set of signals generated by a differential bit encoding algorithm used by the AFE of Figure 18; and

[0050] Figure 26 is a block diagram of an exemplary processing of signals in a six (6) window arrangement for the zero-crossing algorithm of Figure 19 used by the AFE of Figure 18.

DETAILED DESCRIPTION OF EMBODIMENTS

[0051] The description which follows, and the embodiments described therein, are provided by way of illustration of an example, or examples, of particular embodiments of the principles of the present invention. These examples are provided for the purposes of explanation, and not limitation, of those principles and of the invention. In the description, which follows, like parts are marked throughout the specification and the drawings with the same respective reference numerals.

[0052] Briefly, a signal transmission system and method related to an embodiment of the present invention uses both time and frequency diversity in the transmitted signal to improve the robustness of the system. The robustness is improved notably in the presence of large amounts of non-stationary power line noise. As such, the embodiment achieves significantly improved performance in very adverse conditions.

[0053] In an aspect of the embodiment, the transmission system divides the time axis into a number of time slots synchronized such that one time slot starts at the zero crossing of an alternative current (AC) power line signal (50 or 60 Hz depending on the region).

These time slots are called channels and numbered from 1 to n. For the embodiment, the notion of a channel and a timeslot may be used interchangeably. However, if necessary, the terms can be used to mean different concepts. In particular, a channel can be thought to be a logical boundary while a time slot can be a specific implementation of the channel. The modulation method preferably used is narrow band continuous phase FSK, where a number m of modulating frequencies are used, arranged such that an integral number of full cycles fit into each channel time slot for all m frequencies. The system transmits during only a subset of the available time slots (channels) concentrated near the zero crossing of the power line waveform where the noise is typically minimal. In addition the initial phase of the individual frequencies may be varied (from zero going positive to zero going negative). This allows differential reception where only the difference in energy between two bursts is used instead of the actual value, leading to further robustness in the presence of noise.

[0054] The different channels may be used to transfer data to different clients at the same time. In addition they may also be combined to provide diversity as outlined below.

[0055] The system can use diversity of signal transmissions by transmitting the same bit over one or more channels (time slots) and one or more frequencies as well as one of the two phases. It uses a positive acknowledgment protocol with a reverse channel to tell the transmitter which redundancy method to use at any given time. The transmitter and receiver are both synchronized to the power line signal zero crossing and the default transmission method is the lowest bit rate using the maximum diversity. The system preferably uses a cyclic redundancy check (CRC) polynomial to detect the correct reception of messages. If the CRC is not received correctly, no acknowledgment is sent and the transmitter will revert to its default high redundancy state after some programmable delay.

[0056] In the descriptions that follow, an embodiment of the system is described using a particular example of 4 channels and 2 frequencies on a 60 Hz power line. However it should be clear to anyone versed in the art that this can be readily changed to

a n channels and m frequencies as well as the use on other power line frequencies (e.g. 50 Hz), in other embodiments.

Burst mode FSK

[0057] For the embodiment, one transmission method that can be used is traditional FSK with two frequencies. Referring to Figures 1a and 1b, a power wave 102 is shown. The period of the power line waveform is divided into a number of segments and transmission of data occurs during some but not all these segments. Thus consider segments of 600 μ sec - in a 60 Hz power line the period is 16.67 msec and the half period is 8.33 msec, giving 14 time slots of 595 μ sec in one half period. Of these the system transmits in four (4) timeslots of 595 μ sec, leaving the rest of the period empty. The four timeslots are arranged asymmetrically with one before the zero crossing and three after, as illustrated in Figures 1a and 1b. The timeslots are numbered as channels 1 to 4. The exemplary signals shown in Figure 1 correspond to the simplest case where no redundancy is used. The channels 104 and 108 are modulated with frequency 1 and coded as 0, while the channels 106 and 110 are modulated at frequency 2 and coded as 1. The data representing bit pattern is 0101 and is transmitted during this one burst.

[0058] The system of the embodiment uses continuous phase FSK with the transmitted signals:

$$s_m(t) = \sqrt{\frac{2\varepsilon}{T}} \cos(2\pi f_c t + 2\pi m \Delta f t) \quad m = 1,2$$

and Δf chosen such that:

$$\Delta f = \frac{k}{T}$$

which provides seamless switching at the end of the burst T. Choosing T = 600 μ sec and:

$$f_1 = f_c = \frac{70}{T} = 116.7 \text{ kHz}$$

$$\Delta f = \frac{10}{T} = 16.7 \text{ kHz}$$

$$f_2 = f_1 + \Delta f = 133.3 \text{ kHz}$$

completes the definition of the bursts. The receiver uses a bank of correlators as shown in Figure 3. The correlators are synchronized to the zero crossing of the power line waveform and the output is sampled at the nearest peak at the end of the period T, minimizing the effect of any jitter in the zero crossing detection.

[0059] Referring to Fig. 2, cross-correlation of these signals sampled at T is provided by:

$$\begin{aligned} \rho_{mk} &= \frac{1}{2\varepsilon} \int_0^T s_m(t) s_k(t) dt \\ &= \frac{1}{2\varepsilon} \int_0^T \sqrt{\frac{2\varepsilon}{T}} \cos(2\pi f_c t + 2\pi m \Delta f t) \cdot \sqrt{\frac{2\varepsilon}{T}} \cos(2\pi f_c t + 2\pi k \Delta f t) dt \end{aligned}$$

[0060] Referring to Figure 2, an exemplary matched-filter receiver for FSK waveforms is shown. In the upper branch the input signal 202 ($r(t)$) is multiplied by the first FSK frequency reference $s_1(t)$ in the multiplier 204 and the result is integrated in the integrator 208 over a full period T. The resulting signal is sampled by 212, scaled by adder 216 and fed to the decision circuit 220.

[0061] In the lower branch the input signal 202 ($r(t)$) is multiplied by the second FSK frequency reference $s_2(t)$ in the multiplier 206 and the result is integrated in the integrator 210 over a full period T. The resulting signal is sampled by 214, scaled by adder 218 and fed to the decision circuit 220.

[0062] The decision circuit 220 chooses the larger of the two signals fed to it, making the decision that if the result of adder 216 is greater than the result of adder 218 then signal $s_1(t)$ was sent, otherwise making the decision that signal $s_2(t)$ was sent.

[0063] This equation has two parts, one part at DC and the other part at twice the carrier frequency f_c . The result of the integration of the two parts is:

$$\begin{aligned}
 \rho_{mk} &= \frac{1}{T} \int_0^T \cos(2\pi(m-k)\Delta f t) dt \\
 &+ \frac{1}{T} \int_0^T \cos(4\pi f_c t + 2\pi(m+k)\Delta f t) dt \\
 &= \frac{\sin(2\pi(m-k)\Delta f T)}{2\pi(m-k)\Delta f T} + \frac{\sin(4\pi f_c T + 2\pi(m+k)\Delta f T)}{4\pi f_c T + 2\pi(m+k)\Delta f T} \\
 &= 1 \quad \text{if } m = k \\
 &= 0 \quad \text{otherwise}
 \end{aligned}$$

where $f_c \cdot T = 70$ and $\Delta f \cdot T = 10$. Note that this correlation is normalized to 1 by dividing the value by the signal power. This correlation also indicates the effect of jitter in the zero crossing mentioned above. In this case the correlation is over a shorter period, resulting in less energy at the output. If the correlator is synchronized by taking the largest output sample near the end of the original burst, the effect can be approximated as the ratio the reduced burst length due to jitter T_{red} to the original burst length T as shown below:

$$\begin{aligned}
 \rho_{mk} &= \frac{1}{2\mathcal{E}} \int_0^{T_{red}} s_m(t) s_k(t) dt \\
 &= \frac{1}{2\mathcal{E}} \int_0^{T_{red}} \sqrt{\frac{2\mathcal{E}}{T}} \cos(2\pi f_c t + 2\pi m \Delta f t) \cdot \sqrt{\frac{2\mathcal{E}}{T}} \cos(2\pi f_c t + 2\pi k \Delta f t) dt \\
 &= \frac{T_{red}}{T} \left\{ \frac{\sin(2\pi(m-k)\Delta f T_{red})}{2\pi(m-k)\Delta f T_{red}} + \frac{\sin(4\pi f_c T + 2\pi(m+k)\Delta f T_{red})}{4\pi f_c T + 2\pi(m+k)\Delta f T_{red}} \right\} \\
 &= \frac{T_{red}}{T} \quad \text{if } m = k \\
 &= 0 \quad \text{otherwise}
 \end{aligned}$$

where it is assumed that $T_{red} \cdot f_c$ and $T_{red} \cdot \Delta f$ are still integers. This indicates that a correlation is made over an integral number of cycles of f_1 and f_2).

[0064] For the case where both phases of a cosine waves are used for modulation, the correlation results in

$$\begin{aligned}\rho_{mk} &= \frac{1}{2\mathcal{E}} \int_0^T s_m(t)s_k(t) dt \\ &= \frac{1}{2\mathcal{E}} \int_0^T \sqrt{\frac{2\mathcal{E}}{T}} \cos(2\pi f_c t + 2\pi m\Delta f t + \pi) \cdot \sqrt{\frac{2\mathcal{E}}{T}} \cos(2\pi f_c t + 2\pi k\Delta f t) dt\end{aligned}$$

which gives

$$\begin{aligned}\rho_{mk} &= \frac{1}{T} \int_0^T \cos(2\pi(m-k)\Delta f t + \pi) dt \\ &\quad + \frac{1}{T} \int_0^T \cos(4\pi f_c t + 2\pi(m+k)\Delta f t + \pi) dt \\ &= \frac{\sin(2\pi(m-k)\Delta f T + \pi)}{2\pi(m-k)\Delta f T + \pi} + \frac{\sin(4\pi f_c T + 2\pi(m+k)\Delta f T + \pi)}{4\pi f_c T + 2\pi(m+k)\Delta f T + \pi} \\ &= 0 \quad \text{since} \quad (m-k)\Delta f T = \text{integer} \\ &\quad \quad \quad f_c T = \text{integer}\end{aligned}$$

Transmission methods using time and frequency diversity

[0065] The four time slots may be viewed as four independent channels. Thus signal diversity techniques can be used to improve robustness in the presence of noise. In particular, both time and frequency diversities can be used by transmitting multiple copies on different channels and using one or two frequencies as well as one of two possible phases, as further explained below. Thereafter, various combining techniques can be used to improve the robustness of the detection.

[0066] In addition to exploiting the time, frequency and phase diversity, the embodiment also uses a differential receive technique to improve robustness. In this method, rather than relying on the energy at a given frequency, phase and time, a combination of two energy bursts in a specific order are preferably used to signal a bit (e.g. a “1”)– the opposite combination being used to signal the opposite bit (e.g. a “0”). In this way, dependence on the amount of energy on the channel at a given phase, time and frequency is replaced by the detection of specific transitions between two energy bursts, further enhancing robustness on very noisy channels. Several examples of this are

given below, although this redundancy can be implemented through other techniques by those skilled in the art.

[0067] For the embodiment, the following transmission parameters A – E may be used:

- A. 480 bps / 2 frequencies / 1 bit per channel / 4 bits per burst.
- B. 240 bps / 2 frequencies / 2 bits per burst / Channel 0 and 1 merged / Channel 2 and 3 merged
- C. 120 bps / 2 frequencies / 1 bit per burst / Channel 0 and 1 merged / Channel 2 and 3 merged / A '0' is considered to be a transition from F1 to F2; and a '1' is considered to be a transition from F2 to F1
- D. 120 bps / 2 frequencies / 1 bit per burst / All channel merged
- E. 60 bps / 2 frequencies / 1/2-bit per burst / All channel merged / A '0' is a considered to be a transition from F1 to F2; and a '1' is a transition from F2 to F1

Other methods made by used using more channels and more frequencies.

[0068] Implementation of these parameters are illustrated in Tables 1 to 5 and described below:

Burst 1			
b0	b1	b3	b4

Table 1 Method A

Burst 1			
b0	b0	b1	b1

Table 2 Method B

Burst 1			
F1	F1	F2	F2
0			
F2	F2	F1	F1
1			

Table 3 Method C

Burst 1			
b0	b0	b0	b0

Table 4 Method D

Burst 1				Burst 2			
F1	F1	F1	F1	F2	F2	F2	F2
0							
F2	F2	F2	F2	F1	F1	F1	F1
1							

Table 5 Method E

Detection algorithms using time, frequency and phase diversity

[0069] For the embodiment, the detector uses time and frequency diversity methods to improve the robustness of the transmission. The four channels and the two frequencies are used to make a combined decision depending on the transmitted sequence. The receiver monitors the channel and makes a decision on which transmission method is likely to yield the best result. A reverse channel protocol is used to communicate this decision to the transmitter.

[0070] Outlined below with reference to Tables 1-5 are some of the detection methods that can be used, although other methods may also be used as known to those skilled in the art. A basic feature is to use time diversity first by either repeating the same information in a number of time slots or by reducing the number of time slots used by ignoring the ones that are too noisy. The detected signal is then combined with frequency diversity by using only one of the two frequencies to make the decision, ignoring the other one judged to be too noisy. In a general case, k of n time slots are used and l of m frequencies are used.

[0071] Method A:

1. Use maximum likelihood decision from correlator

[0072] Method B

1. Use maximum likelihood decision from correlator on merged channels

2. Use maximum likelihood decision from correlator only on merged channels 1,2

[0073] Method C

1. Use maximum likelihood decision from correlator on merged channels 1,2 and 3,4 then apply differential decoding
2. Use maximum likelihood decision from correlator only on merged channels 1,2 then apply differential decoding
3. Same as 1 or 2 but monitor only change in F1
4. Same as 1 or 2 but monitor only change in F2

[0074] Method D

1. Use maximum likelihood decision from correlator on merged channels 1,2,3,4
2. Use maximum likelihood decision from correlator only on merged channels 1,2
3. Use maximum likelihood decision from correlator only on channel 1
4. Use maximum likelihood decision from correlator only on channel 2

[0075] Method E

1. Use maximum likelihood decision from correlator on merged channels 1,2,3,4 in burst 1 and burst 2 and apply differential decoding
2. Use maximum likelihood decision from correlator only on merged channels 1,2 in burst 1 and burst 2 and apply differential decoding
3. Use maximum likelihood decision from correlator only on channel 1 in burst 1 and burst 2 and apply differential decoding
4. Use maximum likelihood decision from correlator only on channel 2 in burst 1 and burst 2 and apply differential decoding
5. Same as 1 to 4 but monitor only change in F1
6. Same as 1 to 4 but monitor only change in F2

Synchronization, startup and tracking

[0076] For the embodiment, the embodiment preferably uses a link layer protocol for startup and tracking. Synchronization is achieved by detecting the zero crossing of the power line signal and then looking for the maximum of the larger correlator output to determine the end of the burst near T microseconds after the zero crossing (note that the correlator will contain part of the second burst if the zero crossing is detected late or noise only if it is detected early due to jitter. However, the effect of this is small as shown above). The zero detection circuit can use any signal monitoring or detection circuit known to those skilled in the art. Other embodiments may use other synchronization points for determining where to insert and expect data in the power signal. The zero detection circuit can be designed to trigger a synchronization signal when the value of the power signal is about zero, that is, approaching or near zero volts.

[0077] The link layer protocol transmits messages bounded by a start of message sync pattern at the beginning and a CRC byte at the end of the message. The receiver uses this CRC to determine if correct operation has been achieved and sends a positive acknowledgement to the transmitter to that effect.

[0078] It is noted that other link layer protocols may also be used in conjunction with the transmission system in other embodiments, as will be evident to those skilled in the art.

[0079] Startup is achieved by transmitting at the lowest bit rate, ($\frac{1}{2}$ bit per burst in this case). Once successful transmission at this bit rate is achieved (correct CRC received), the receiver monitors all channels and all frequencies to determine if a higher bit rate could be sustained. It then communicates to the transmitter via a control message to use one of the other transmission patterns and switches its detection algorithm accordingly. It should be noted that another implementation can start with the highest bit rate and reduce it in case of bad CRC. Improved robustness can be provided by positively acknowledging each message. This allows the transmitter to revert to the lowest bit rate in case the channel deteriorates to the point where the receiver is not receiving correct data and does not send an acknowledgement. For the embodiment, this

provides synchronisation with a frequency or frequencies so that the receiver can receive information from the transmitter.

Analog Front End

[0080] Referring to Fig. 3, the analog front end (AFE) is an analog circuit composed of a transmission circuit and a reception circuit. This circuit provides the connection from the digital signal processing portions of the system to the analog portion of the power line. The receiver circuit is always on, whereas the transmitter circuit must be enabled with a logical high (1) on the TX_Enb pin. Both circuits have a protection diode circuit to limit spikes and signals present on the powerline and pass through the coupling. For the embodiment, the AFE is a discrete circuit separate from the microcontroller, such as microcontroller 1804 described below in Figure 18. However, one of skill in this art would appreciate that other circuit arrangements may be used in other embodiments.

[0081] A simplified block diagram of the AFE is shown at 300. For the embodiment, the following provides a summary of different filters that may be used in the AFE:

Description	Value	Note
Filter 1 Characteristics		
Filter type	Butterworth Low-Pass	
Order	4	
Cut off Frequency	180 KHz	@ -3 dB
Filter 2 Characteristics	Butterworth High-Pass	
Filter type		
Order	2	
Cut off Frequency	190 KHz	@ -3 dB
Filter 3 Characteristics		
Filter type	(Type) Band-Pass	
Order for the high pass	10	
Order for the low pass	4	
Cut off Frequency (Low)	106 KHz	@ -6 dB
Cut off Frequency (High)	160 KHz	@ -6 dB
Frequency Center	125 KHz	
Gain	20 dB	
AGC Characteristics		
Gain	>30 dB	
Response delay	30 μ S	
Power Amplifier		

Characteristics		
Input impedance	600 Ω	
Output impedance	<1 Ω	
Gain	11 \pm 1 dB	
Bandwidth	80-150 kHz	
Power	2.25 W _{peak}	(3 V _{peak} in 4 Ω)
Protection	Short circuit and over voltage	Protected by coupler impedance
Distortion	-60 dB (3 rd harmonic)	Output impedance: 50 Ω

Table 6 - AFE Specifications

[0082] Details regarding different aspects of the AFE are now briefly described below. More details regarding AFE's is provided in U.S. Patent No. 6,727,804, the contents of which are hereby incorporated by reference. Referring now to Figure 3, there is provide an exemplary AFE 300. AFE 300 includes amplifiers 306 and 312, low pass filters 304 and 310, band pass filters 314 and 318, and high pass filter 316. Connection 320 couples AFE 300 to a coupling circuit, connection 302 and 308 provides to a power line for transmitter and receiver circuits, as described below.

Transmitter Circuit

[0083] Referring to Figure 4, the exemplary amplifier section 400 of the AFE is made up of two stages:

- The transmission filter (TX filter); and
- A voltage/current stage amplifies the input signal with low-distortion to meet FCC, ICES and CENELEC requirements. Preferably, the output stage has low output impedance. The amplifier is controlled by the Tx_Enb signal. When Tx_Enb is low, the current stage is high impedance to allow power line signal to be received by the RX section. When Tx_Enb is high, the current stage amplifies the signal from the voltage amplifier and transmits it to the coupler.

[0084] The amplification is 11 \pm 1 dB. As such, the range is 1.7 volts peak-to-peak. The output impedance is less than 1 Ω when transmitting and more than 250 Ω in idle state. The transmitter preferably uses an integrated circuit provide the amplification. The

amplifier preferably supports low impedance on the power line without distorting the signal transmission.

[0085] For the embodiment, the two amplifiers 306 and 312 work with a bridge configuration to transmit a 6 V_{pp} signal on the line from a single 5V supply. The output of the transmission amplifier 306 is not protected against shorts between ground and output. The output signal is transmitted at 6 V_{pp} for a load greater than 6 Ω. For a load smaller than 6 Ω, the output signal decreases, but the distortion stays at a low level to avoid transmitting harmonics on the power line.

[0086] The band-pass filter of the amplifier preferably has a pass range from 80 kHz to 150 kHz. As the circuit provides a pulse width modulation signal, it is preferably to filter it using a passive low pass filter to reshape the signal to amplify. The transmitting filter is used to filter the signal taken from the circuit and to feed it to the voltage/current amplifier 306. This is accomplished by eliminating the high frequencies of the TX signal at the input of the amplifier. This may be done by a low pass filter 500 as shown in Figure 5. An exemplary circuit 600 for a high pass filter is shown in Figure 6.

Receiver Circuit

[0087] For the embodiment, the receiving circuit is preferably always enabled. It receives the signal from the power line and filters it for the circuit. The receiver provides the following functions:

- Extract the inbound signal of the noise present at the output of the coupling circuit by a efficiency filtering
- Compress the signal without clipping it to preserve the shape when the maximum amplitude is reached
- Amplify the signal when it is necessary; depending of the attenuation present on the powerline
- Warn the circuit when the signal is being compressed and when the line is noisy

[0088] To perform these functions, the receiver is divided in several sections which are independent of each other. Depending of performances required for different applications, different sections can be added and taken out of the circuit. For the embodiment, the following sections are available:

- A high pass filter
- A protection diode circuit
- A band-pass filter and amplifier
- A high pass filter
- A protection diode circuit
- A band-pass filter and amplifier
- A low pass filter
- A band-pass filter and amplifier
- A limiter that react as a protection for the circuit
- An automatic gain control amplifier which control gain of two of the three amplifiers

[0089] The sections preferably clean the signal, but do not saturate and preferably preserve the shape of the signal. The minimum signal to be detected by the AFE is 30 μ V if the noise floor is lower than -97 dB (Vpp). This gives a sensitivity of -97 dB.

[0090] Each of the sections of the receiver circuit now described in turn. Referring first to Figures 6 and 9, high-pass filters 600 and 900 respectively are shown. It will be appreciated that each filter operates in a manner known to those skilled in the art. It will also be appreciated that the pass point for either filter may be set according to operation characteristics required by the system.

[0091] Referring to Figures 7, 10 and 14, protection circuits 700, 1000 and 1400 are shown. Either protection circuit may clamp voltages to a predetermined level to prevent overloading of the circuits downstream to them. Other protection circuits may be provided. In particular, limiter 1400 that react as a protection for a processing circuit.

[0092] Referring to Figures 8, 11 and 13, a band-pass filter and amplifier circuits 800, 1100 and 1300 respectively are shown. It will be appreciated that each band-pass filter

operates in a manner known to those skilled in the art. It will also be appreciated that the pass points for each filter may be set according to operation characteristics required by the system. Each amplifier operates to amplify the output signal of the band-pass filter. The level of amplification can be designed to meet operation characteristics required by the system.

[0093] Referring to Figure 12, a low pass filter 1200 is shown. It will also be appreciated that the pass point for the filter may be set according to operation characteristics required by the system.

[0094] Referring to Figures 15a and 15b, an automatic gain control (AGC) amplifier 1500a and 1500b that controls gain of two of the three amplifiers are shown. The AGC is designed to have fast response within 80 μ S. This is enough fast to control amplification of the different section of the receiver and gives feedback to the circuit.

[0095] Referring now to Figure 16, an optimized reception and transmission of multiple frequencies using a single sine wave is now described and shown in graph 1600. As shown, there is a 356 point 2.5 kHz sine wave stored in RAM memory (for a sampling rate of 888888.8 samples per seconds). This single sine wave is used by the DSP to perform discrete time Fourier transfer (DTFT) on any frequency that is a multiple of 2.5 kHz.

[0096] The following function performs the DTFT at 110 kHz using this table. It is noted that only N register needs to be modified in order to select any frequency:

```

moveu.w #356,LC           // 2c
moveu.w #(32768 + 356-1), M01 // R0 and R1 are configured as MOD(356) Addressing
move.w #44,N              // 44 x 2.5 kHz = 110 kHz parameter

moveu.w #DFTTable + 89,R0 // Imaginary Part (Cos) offset of 90 degrees
moveu.w #DFTTable,R1      // Real Part (Sin) no offset
moveu.w #TestBuffer,R3    // ADC Data Ptr

clr a x:(r1)+N,y1         // real part + add(N) to r1
nop
clr b x:(r0)+N,y0 x:(r3)+,x0 // imaginary part + add(N) to r0

DOSLC _ENDOFLOOP
    mac y1,x0,a x:(r1)+N,y1 // real part + add(N) to r1
    mac y0,x0,b x:(r0)+N,y0 x:(r3)+,x0 // imaginary part + add(N) to r0
_ENDOFLOOP:

```

[0097] Referring to Fig. 17, graph 1700 shows relationships between the various input signals and channels. In particular, it provides a three dimensional portrayal of the information shown in Fig. 1. Therein, an exemplary system utilizes twelve channels in twelve sequential time slots [0], [1], [2] ...[11]. In other embodiments, more or less slots can be used. Data is encoded in the channels around the zero crossing of the AC signal. These are shown in burst signals shown grouped as blocks of signals 1702, 1704 and 1706. Each burst signal includes data encoded in each of the 12 channels. The peak signal in each channel in each zero crossing is the encoded data element. Other energies in the signal in the channel include noise and harmonics associated with the injected signals. The regions 1708 show less energies therein because they represent the power signal around non zero crossing regions and as such, no data encoded in the power signal at those regions.

Transmitter and Receiver Circuit

[0098] Referring now to Figures 18-26 aspects of another embodiment are shown. In particular, a complementary transmit and receive module is described implementing aspects of the earlier described synchronization, transmission and reception techniques.

[0099] Figure 18 shows system 1800, where AFE 1802 receives analog signals from and inserts data in the signals on powerline 1806. Powerline 1806 is the medium over which data may be exchanged through its power signals. Microcontroller 1804 provides the modules for encoding and decoding data from the power signals using systems and methods described herein. Software operating on microcontroller 1804 is stored in a non-volatile memory location (not shown) and controls operation of the microcontroller in how it processes information and data received and sent to the AFE 1802. Referring to Figure 20, at initialization, transmitters and receivers synchronize themselves by the means of the powerline 2002 having zero-crossings 2006, 2008. The zero-crossing 2006, 2008 point of the powerline 2002 is used to estimate where a "burst" to be transmitted by the transmitter or as to be captured by the receiver is located.

[00100] Referring again to Figure 18, on reception a data signal is received from powerline 1806 by the AFE 1802 by way of coupling circuit 1808. Bandpass filter and gain 1810 is used to filter the signal and to increase its strength. After this stage, the

signal is routed through to the micro-controller ADC or comparator 1818 on microcontroller 1804. The samples received are then stored to RAM 1824 as needed. Microcontroller 1804 can then decode data from the signal. In decoding the data, microcontroller can determine what channel (if any) the data came from and can then use the data to reconstruct an original data string, if additional data is required from additional channels or bursts.

[00101] On transmission, the microcontroller 1804 determines what data is to be encoded, what channel (if any) that the data is to be sent on and then encodes the data into a PWM signal via its pulse width modulator or DAC 1820. This analog signal is then sent to AFE 1802 and filtered in order to meet any applicable regulations by filter 1814. Once filtered, the signal is amplified by amplifier 1812 and is transmitted to powerline 1806 via coupling circuit 1808 for transmission. Timing of the insertion of the signal can be controlled, in part, by the zero-detection circuit.

[00102] Referring to Figures 19 and 20, the zero crossing circuit implements algorithm 1900 is shown. Referring first to Figure 19, there is an example of a zero-crossing synchronization shown on flowchart 1900, in which 2 timers are used and where a “burst” begins before the zero-crossing point. In relation to Figure 20, the timer described in Figure 19 is for calculating a delay between a previous zero-crossing (such as 2008 in Figure 20) and the current zero-crossing pulse (such as 2006 in Figure 20). A second timer is then loaded with this calculated value minus the “burst” offset. This second timer may then expire at the start of the “burst” (such as identified as 2004 in Figure 20) and depending on the device state, it can issue a transmission or a reception. This process can be repeated indefinitely.

[00103] Referring to Figure 21, the RX WindowProcessing step of chart 1900 is shown in greater detail. As RX WindowProcessing begins, the receiver and transmitter are already synchronized, and synchronization is no longer an issue. The goal of the RX WindowProcessing is to show how various channels and frequencies can be processed during the “burst”. This processing is performed by the microcontroller 1804 of Figure 18. The signal received is the output of the ADC or comparator 1818. At the beginning of a burst, the RX samples are buffered for the entire duration of the burst at step 2102.

As such, n samples are buffered into RAM memory 1824. The burst is separated into many channels, where the samples are equally distributed. Once the buffering is complete, discrete Fourier transforms (DFTs) are calculated for each channel and each frequency at steps 2108-2116. For example, if there are 4 channels in each burst and if 8 frequencies are analyzed by the receiver then 32 DFTs are performed.

[00104] Once each channel's frequency DFTs results are stored into memory, the merged channel processing step 2118 is performed, as described in greater detail below. Thereafter, the calculate frequency magnitude step 2120 is performed, and after all magnitudes are processed at step 2120, the bit processing step is performed at step 2122. For the embodiment, once each channel's frequency DFTs results are stored into memory, the merged channel processing step 2118 is performed, as described in greater detail below. Thereafter, the calculate frequency magnitude step 2120 is performed. This step is used in order to determine the relative power of each frequency based on the complex numbers outputted from previous steps. After all magnitudes are processed at step 2120, the bit processing step is performed at step 2122. This step is used to determine if the device is receiving 0s or 1s by comparing the various frequency magnitudes.

[00105] Referring to Figure 22, a block diagram of elements used to provide merged channel processing from step 2118 described above is shown at 2200. At this stage, all the signal filtering and processing has been completed, and the merged channels processing is no longer concerned with signal samples but rather with complex numbers that are the output of the DFT or FFT as described above. In the embodiment, channel merging is performed in order to support lower-baud rate and increase robustness against noise. For example, Figure 22 shows the sum of many channels can be analysed to create a slower process that tends to be more robust against noise.

[00106] Since the output of the DFT is a complex number, merged channel processing may add two channels by performing a complex addition of the complex number DFT output of the two channels. As there may be many frequencies per channel, a separate sum is performed for each frequency. The complex sum is therefore the addition of the

imaginary part of both channels to be merged and the addition of both real parts of the channels to be merged:

$$\text{Channel 1 of 4 REAL} = (\text{Channel 1 of 8 REAL} + \text{Channel 2 of 8 REAL})$$

$$\text{Channel 1 of 4 IMG} = (\text{Channel 1 of 8 IMG} + \text{Channel 2 of 8 IMG})$$

[00107] For example, referring to Figure 22, 7 merged channels are created by merging the 8 base channels, as shown in flow chart 2200. Seven sum operations per supported frequency are required to create these extended channels. It will be appreciated that it is also possible to create other channels, for example one can create a merged channel by the sum of (Channel 2 of 4) and (Channel 3 of 4).

[00108] Referring to Figure 23, a formula for calculating the magnitude of the frequency per step 2120 above is shown at 2300. As described above, the output of the FFTs and DFTs process from Figure 21, and the output of the channel merge processing in Figure 22, are expressed as a complex number for each channel by each frequency. For example, for a 2-frequency modulation, if there are 2 channels per burst and 1 merged channel that is the sum of the 2 channels, the output of the processing from merged channel processing will be the following 6 complex numbers

Complex Number 1 (Channel 1 Frequency 1)

Complex Number 2 (Channel 1 Frequency 2)

Complex Number 3 (Channel 2 Frequency 1)

Complex Number 4 (Channel 2 Frequency 2)

Complex Number 5 (Sum of Complex Number 1 and Complex Number 3)

Complex Number 6 (Sum of Complex Number 2 and Complex Number 4)

[00109] A complex number can be expressed as a 2-dimension vector with a real and an imaginary part. The angle of this vector is the phase of the entry signal for the given frequency. The length of this vector is the power (or magnitude) of the frequency. The equation shown in Figure 23 is thus used to calculate the power of the frequency based on the complex number associated with that frequency. The magnitude of each frequency is also calculated in order find the frequency with the higher power.

[00110] Referring to Fig. 24, a set of tables indicating how frequencies are mapped to bit codings are shown, per step 2122 described above. The input of the process bit processing step is a magnitude for every channel and frequency. With this magnitude of each frequency one can determine which frequency was most likely transmitted by the transmitter device (i.e., the frequency with the highest magnitude) in relation to FSK demodulation, as described above.

[00111] The tables of figure 24 set out an exemplary bit coding for each frequency, depending on the number of frequencies supported by the devices. Another example of a table showing another set of frequencies is shown below:

Frequency #	Frequency in kHz (example)	Bit Coding
0	100	0000b
1	105	0001b
2	110	0010b
3	115	0011b
4	120	0100b
5	125	0101b
6	130	0110b
7	135	0111b
8	140	1000b
9	145	1001b
10	150	1010b
11	155	1011b
12	160	1100b
13	165	1101b
14	170	1110b
15	175	1111b

Frequency #	Frequency in kHz (example)	Bit Coding
0	100	000b
1	110	001b
2	120	010b
3	130	011b
4	140	100b
5	150	101b
6	160	110b
7	170	111b

[00112] Additionally, another example of bit coding for a differential bit receiver is shown below:

Burst 0		Burst 1		Bit Coding
Frequency #	Frequency in kHz (example)	Frequency #	Frequency in kHz (example)	
0	100	1	110	0b
1	110	0	100	1b

[00113] Referring to Figures 25 and 26, an example of differential bit coding processing for a signal is provided. Figures 25 and 26 show an example of a differential bit coding transmission. Figure 25 shows 6 bursts required to transmit '011' on the medium, as shown at 2500. Figure 26 shows a graph 2600. For each bit, 2 bursts are required. A '0' requires a 100 kHz burst followed by a 110 kHz burst while a '1' requires a 110 kHz burst followed by a 100 kHz burst. The bursts 1 to 6 are mapped to time into the figure 26. The bursts are synchronized with the powerline (see for example, Figure 18 section 1806) and zero-crossings (see for example, Figure 18, section 1816 and 1822).

[00114] It will be appreciated that the same principles may be used in transmission in order to generate a pulse width modulated wave.

[00115] The embodiments above have described systems and methods for encoding data into AC signal in timeslots about a zero crossing of the AC signal. It will be appreciated that in other embodiments, other predetermined point(s) of the AC signal may be used. For example, a peak/trough detect circuit can be used and the data may be inserted at or near a peak/trough value of the signal. Alternatively the data can be inserted at a predetermined offset from the peak/trough value.

[00116] Further still, in other embodiments, data may be inserted in non-AC signals. Such DC-based signals may be provided, for example, on twisted pair transmission lines.

[00117] Although the invention has been described with reference to certain specific embodiments, various modifications thereof will be apparent to those skilled in the art without departure from the scope of the invention.

WE CLAIM:

1. A method for encoding data to be transmitted over a power line carrying a power signal over a time period, the method comprising:

associating the time period with a predetermined point for the power signal; and
encoding the data into the power signal in at least one signal over the time period using a signal diversity technique.

2. The method for encoding data to be transmitted over a power line as claimed in claim 1, wherein

the predetermined point is a zero crossing point for the power signal;

the power signal is an AC signal;

the step of encoding the data comprises dividing the time period into a number of time slots; and

modulating the data into the power signal using the at least one signal for each of the time slots.

3. The method for encoding data to be transmitted over a power line as claimed in claim 2, wherein

the step of modulating the data utilizes FSK signals to encode the data into power signal; and

m modulating frequencies are used to modulate the data, and m is selected such that an integral number of full cycles fit into each time slot for all m frequencies.

4. The method for encoding data to be transmitted over a power line as claimed in claim 3, wherein the data is encoded in signals in two or more time slots.

5. The method for encoding data to be transmitted over a power line as claimed in claim 3, wherein the data is encoded using two or more signals each having a different frequency.
6. The method for encoding data to be transmitted over a power line as claimed in claim 5, wherein initial phases of the signals differ.
7. The method for encoding data to be transmitted over a power line as claimed in claim 6, wherein
 - the data is encoded in signals in two time slots; and
 - the method further comprises decoding the data from the power signal by detecting differences in energies in each of the two time slots.
8. The method for encoding data to be transmitted over a power line as claimed in claim 3, wherein the data is encoded over at least two of the time slots.
9. The method for encoding data to be transmitted over a power line as claimed in claim 8, further comprising decoding the data from the at least two of the time slots by summing and merging signals extracted from such slots.
10. A circuit for transmitting outbound data and receiving inbound data in an AC-power signal, the system comprising:
 - a connection to the AC-power signal;
 - a circuit to detect a zero crossing of the power signal;
 - an encoding module to encode and inject the outbound data into the power signal in at least one signal over a time period around the zero crossing; and

a decoding module to extract and decode the inbound data from the power signal around the time period around the zero crossing,

wherein FSK signals are used to encode and decode the inbound and outbound data.

11. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 10, wherein the outbound data is encoded over two or more time slots in the time period around the zero crossing.

12. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 11, wherein the outbound data is encoded in two signals having different frequencies, the two signals encoded into the AC-power signal around the zero crossing.

13. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 12, wherein initial phases of the signals differ.

14. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 13, wherein the inbound data is decoded by evaluating differences in energies in the signals detected during two time slots around the zero crossing.

15. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 14, wherein the outbound data is encoded in parallel over at least two of the time slots.

16. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 14, wherein the step of evaluating differences monitors for transitions between signals detected during the two time slots.

17. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 11, wherein the inbound data is encoded over multiple time slots of the time slots is decoded by summing and merging signals extracted from each of the multiple time slots.

18. The circuit for transmitting outbound data and receiving inbound data in an AC-power signal as claimed in claim 17, wherein the inbound data comprises signals having real and complex voltage components.

19. A method for transmitting data over a power line in a time period, the method comprising:

dividing the time period into a number of time slots synchronized such that one time slot starts about a zero crossing of a power line signal for transmitting the data, each time slot being relating to a channel and being numbered from 1 to n;

modulating a narrow band continuous phase FSK in which a number m of modulating frequencies are used, and arranged such that an integral number of full cycles fit into each said time slot for each said channel for all m frequencies; and

transmitting data during only a subset of the available time slots concentrated near the zero crossing of the power line signal.

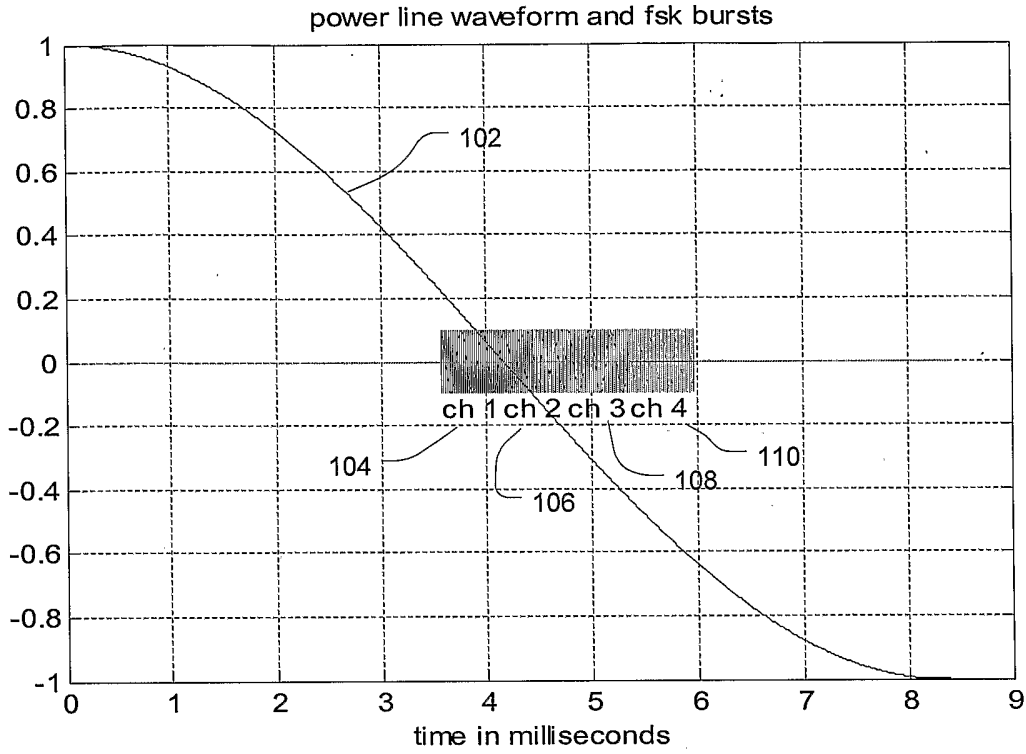


Figure 1a - FSK burst slots in one half power line cycle

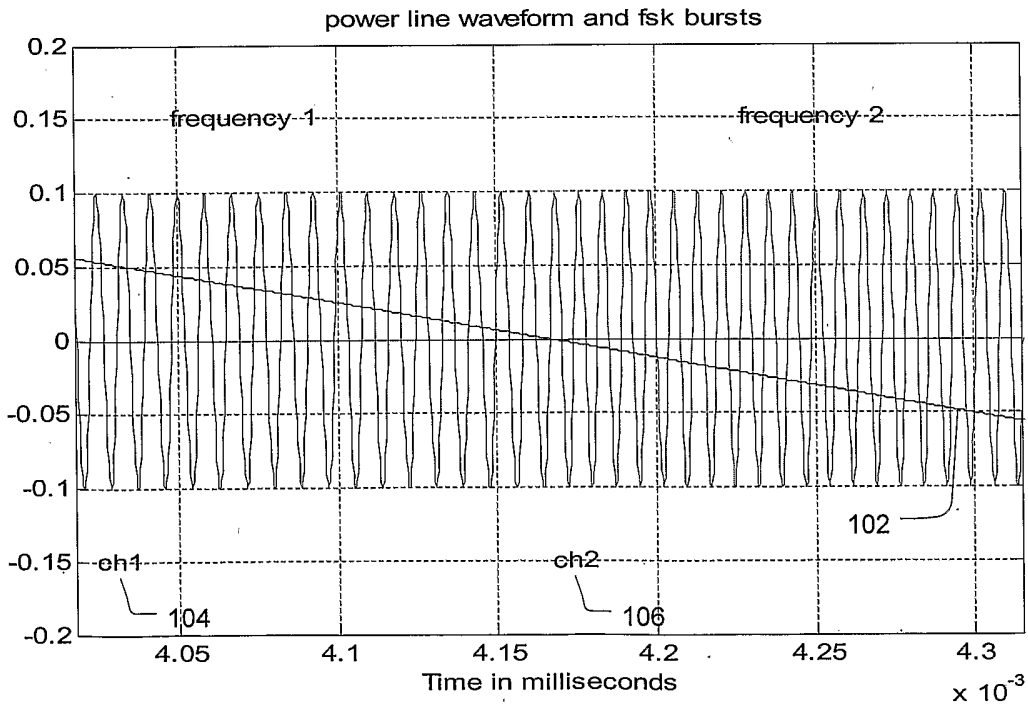


Figure 1b - FSK burst slots around the zero crossing

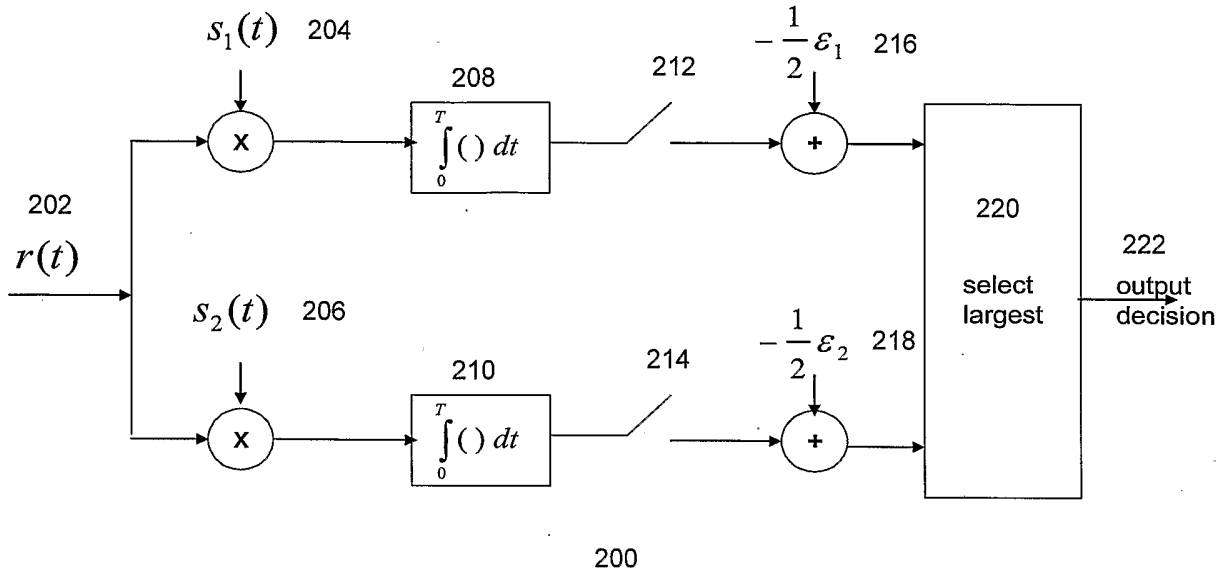


Figure 2 - Correlation receiver for two frequency FSK

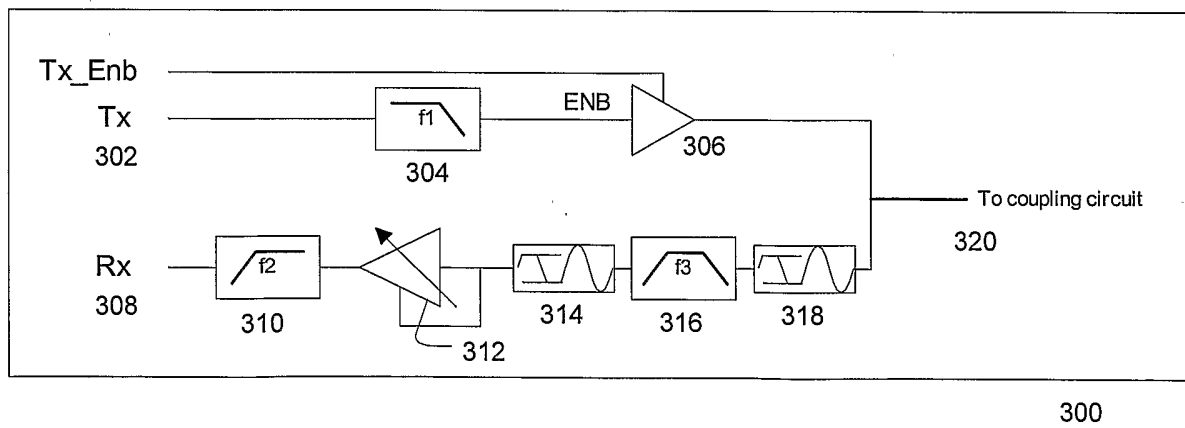


Figure 3 - AFE Block Diagram

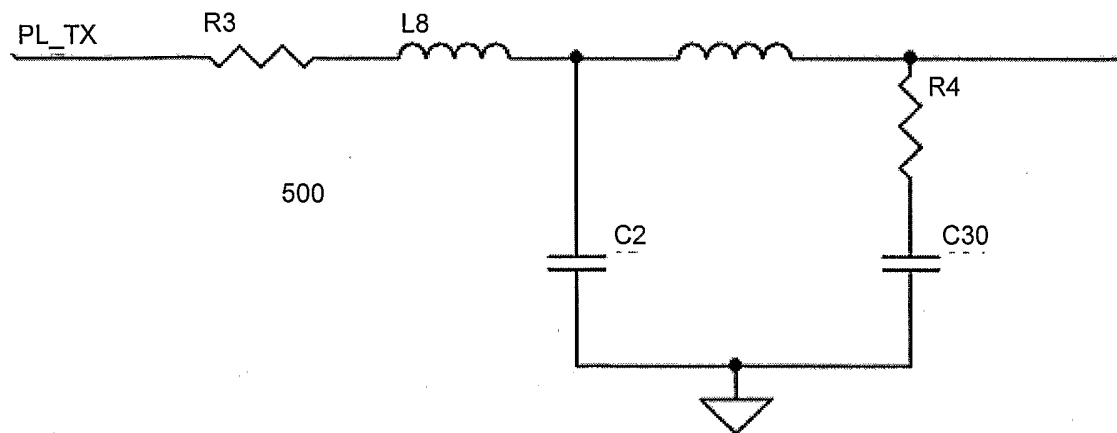


Figure 5 - Low Pass Filter

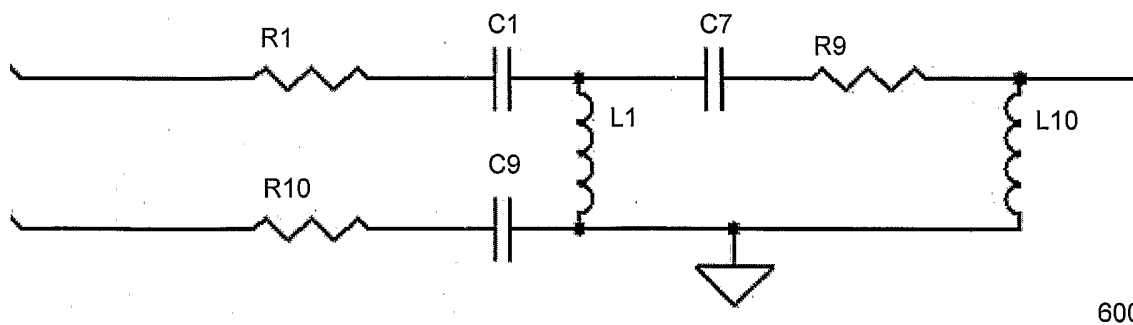


Figure 6 - High Pass Filter

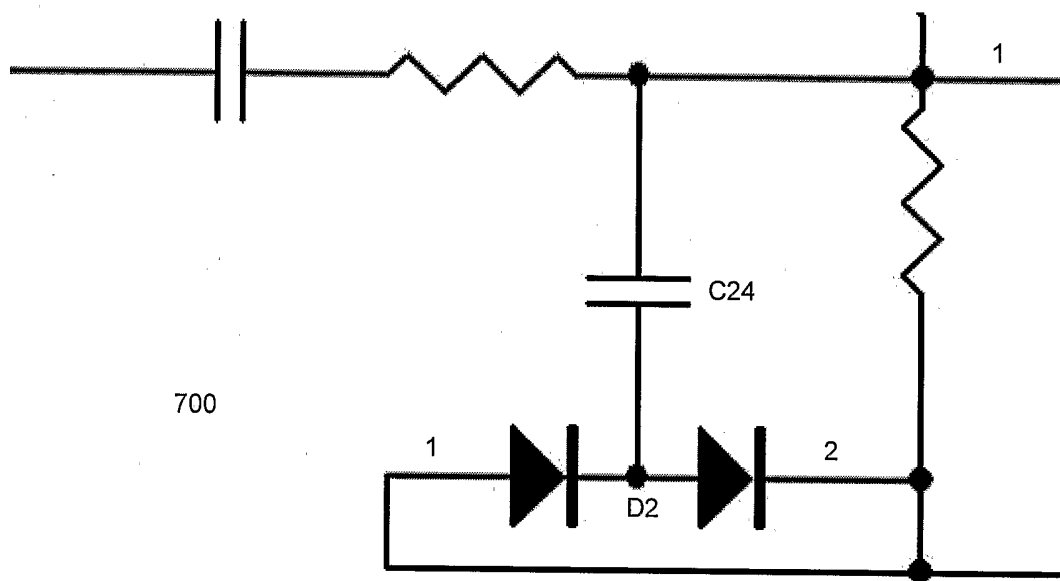


Figure 7 - Protection Circuit

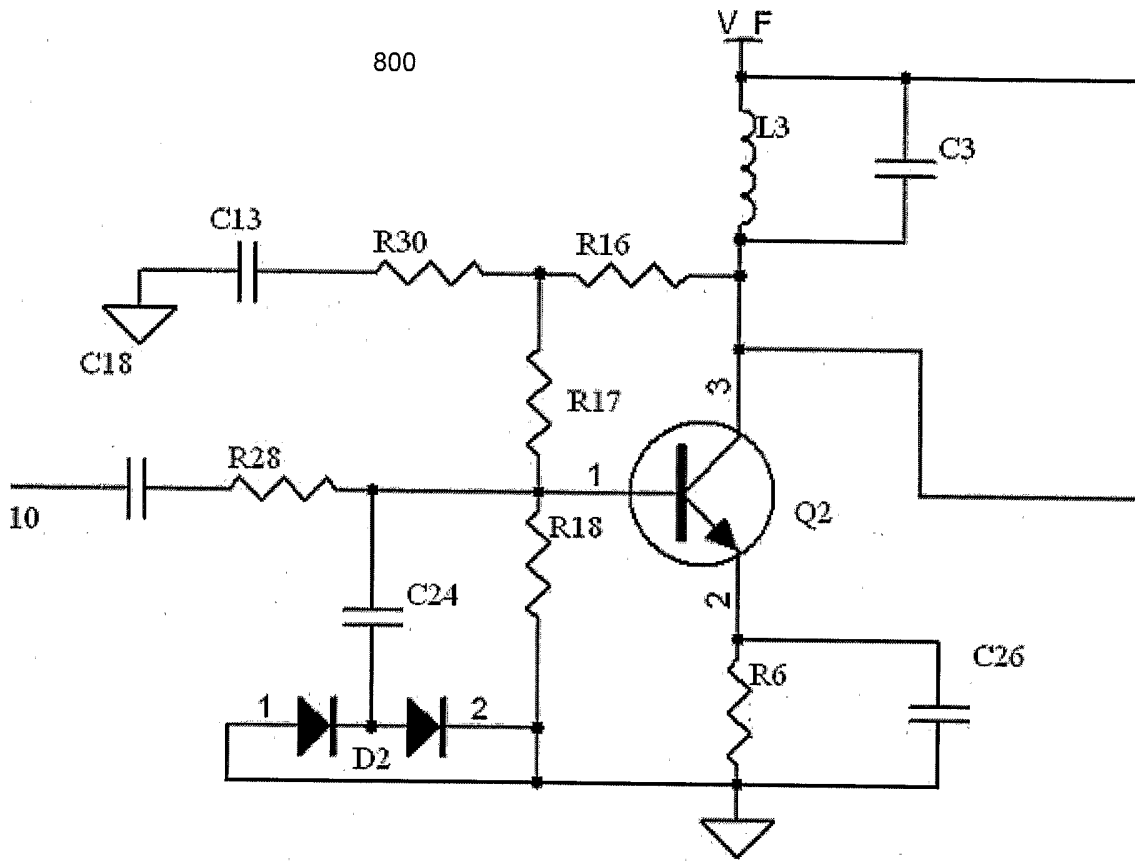


Figure 8 - Band Pass Filter and Amplifier

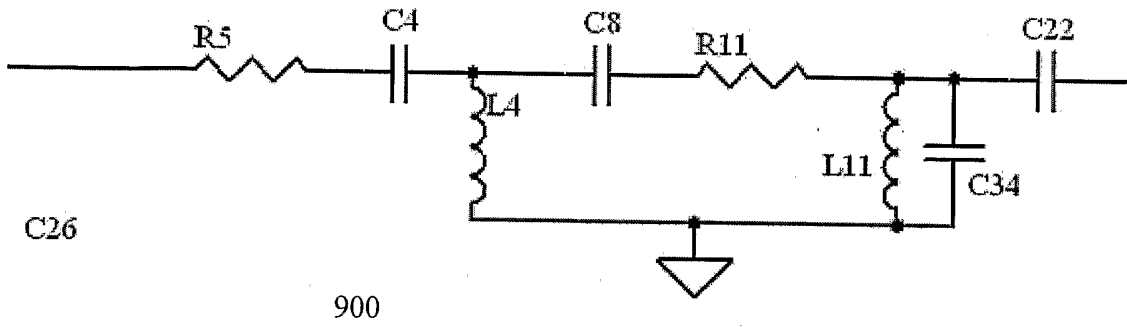


Figure 9 - High Pass Filter

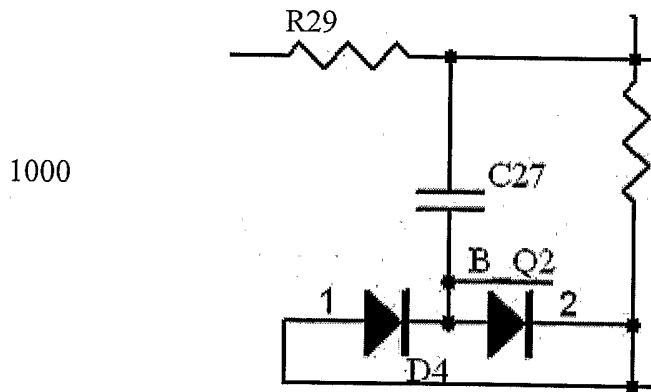


Figure 10 - Protection Diode Circuit

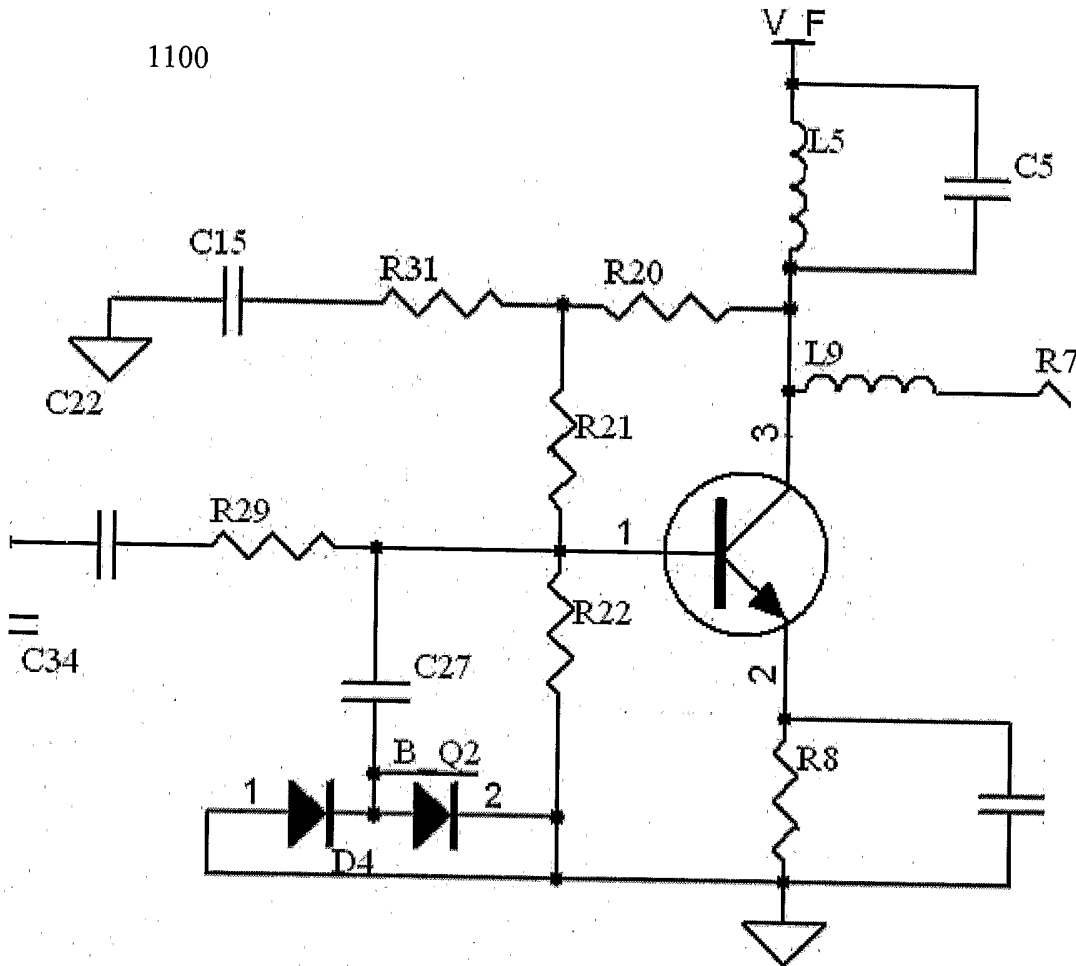


Figure 11 – Band Pass Filter and Amplifier

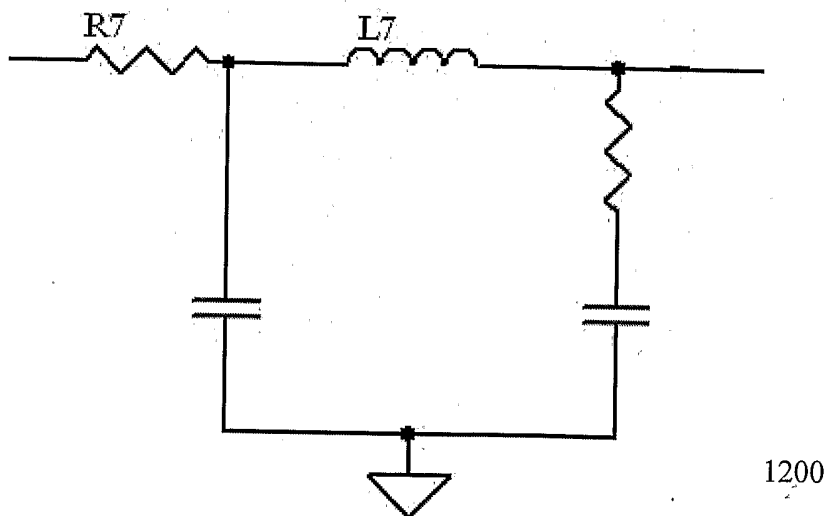


Figure 12 – Low Pass Filter

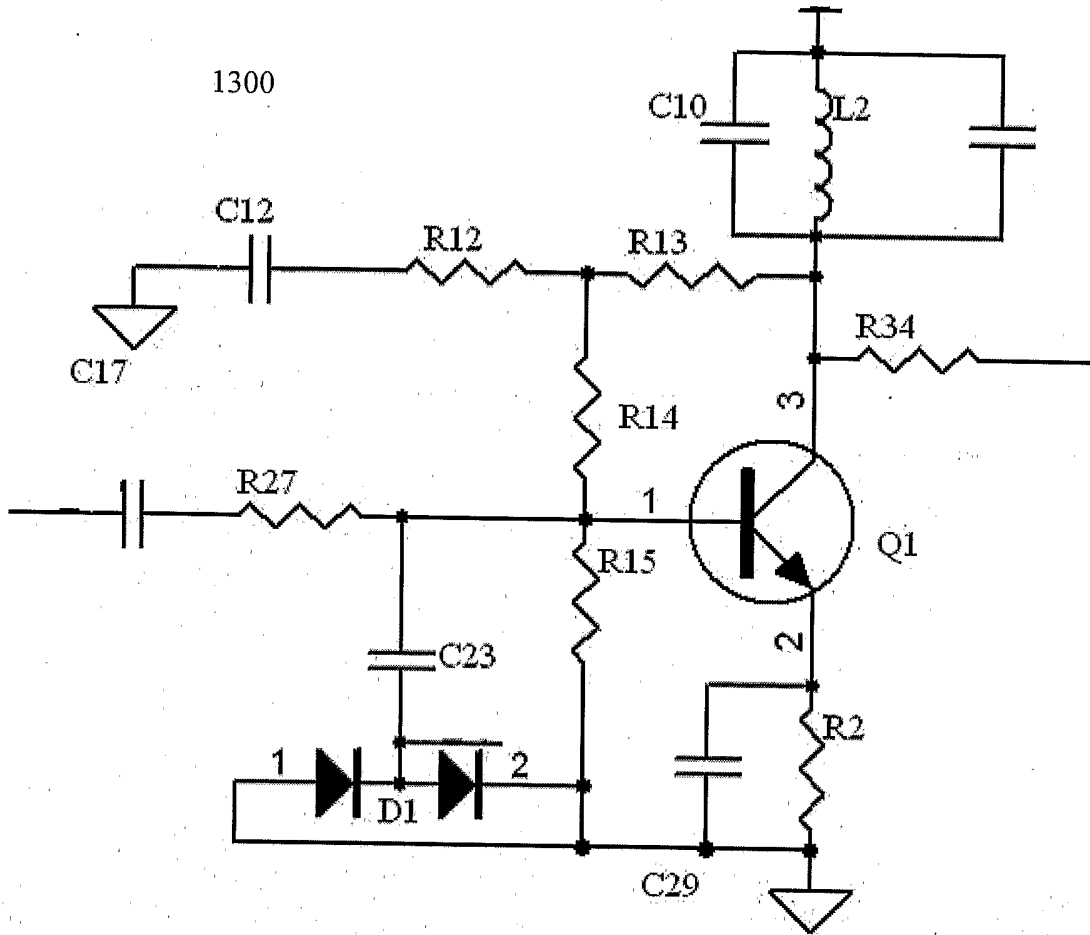


Figure 13 - Band Pass Filter and Amplifier

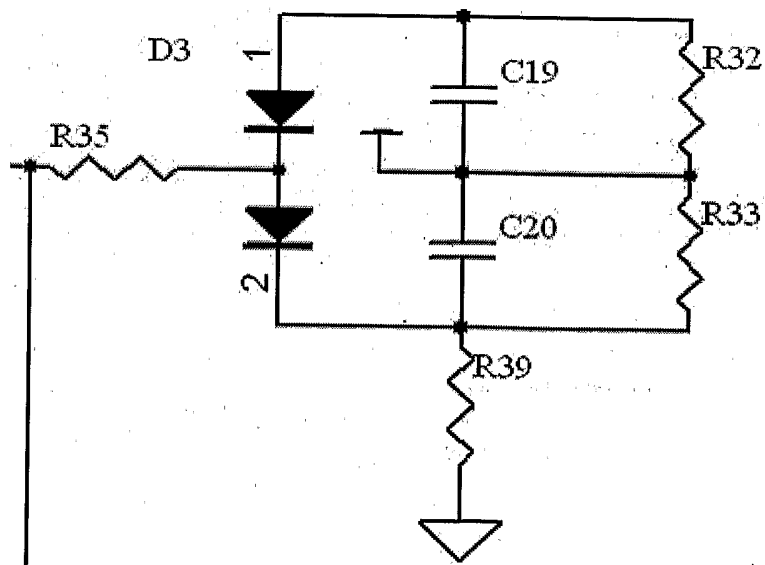
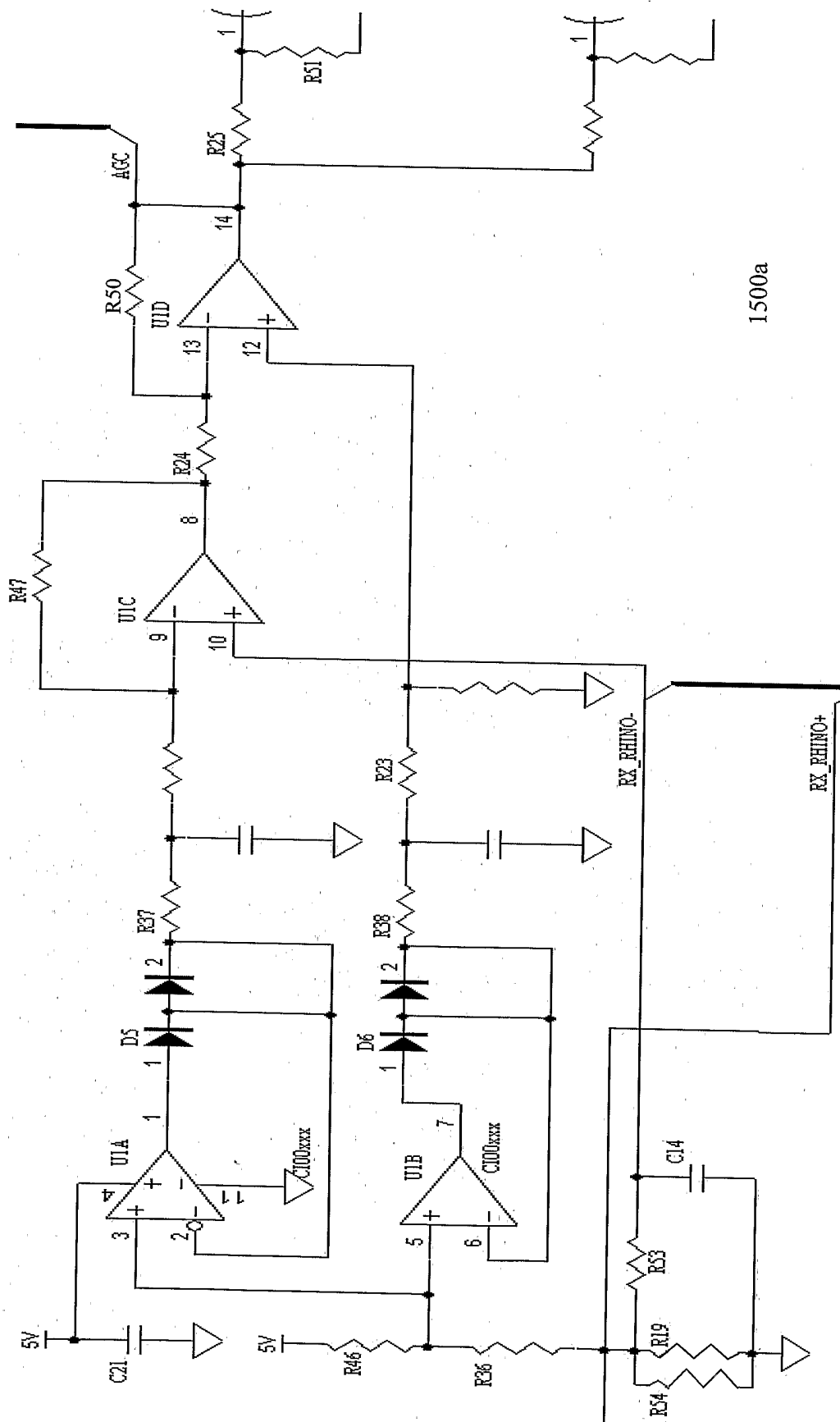


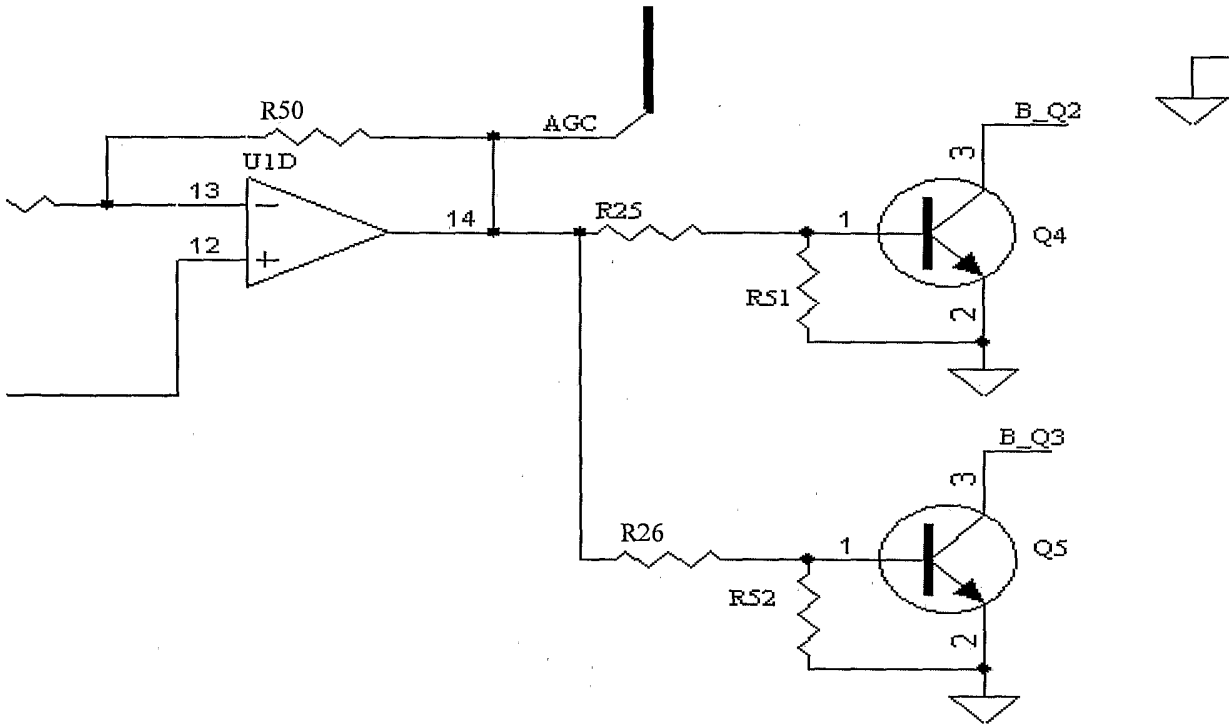
Figure 14 - Limiter

1400



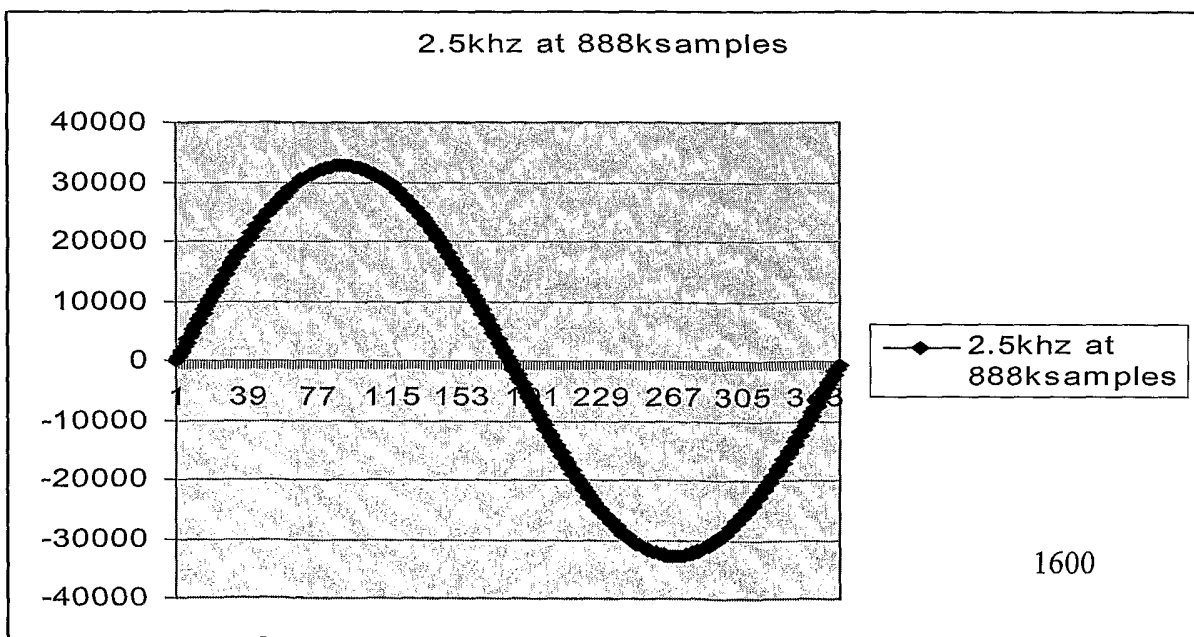
1500a

Figure 15a – Automatic Gain Control Amplifier



1500b

Figure 15b – Gain Control Amplifier



1600

Figure 16

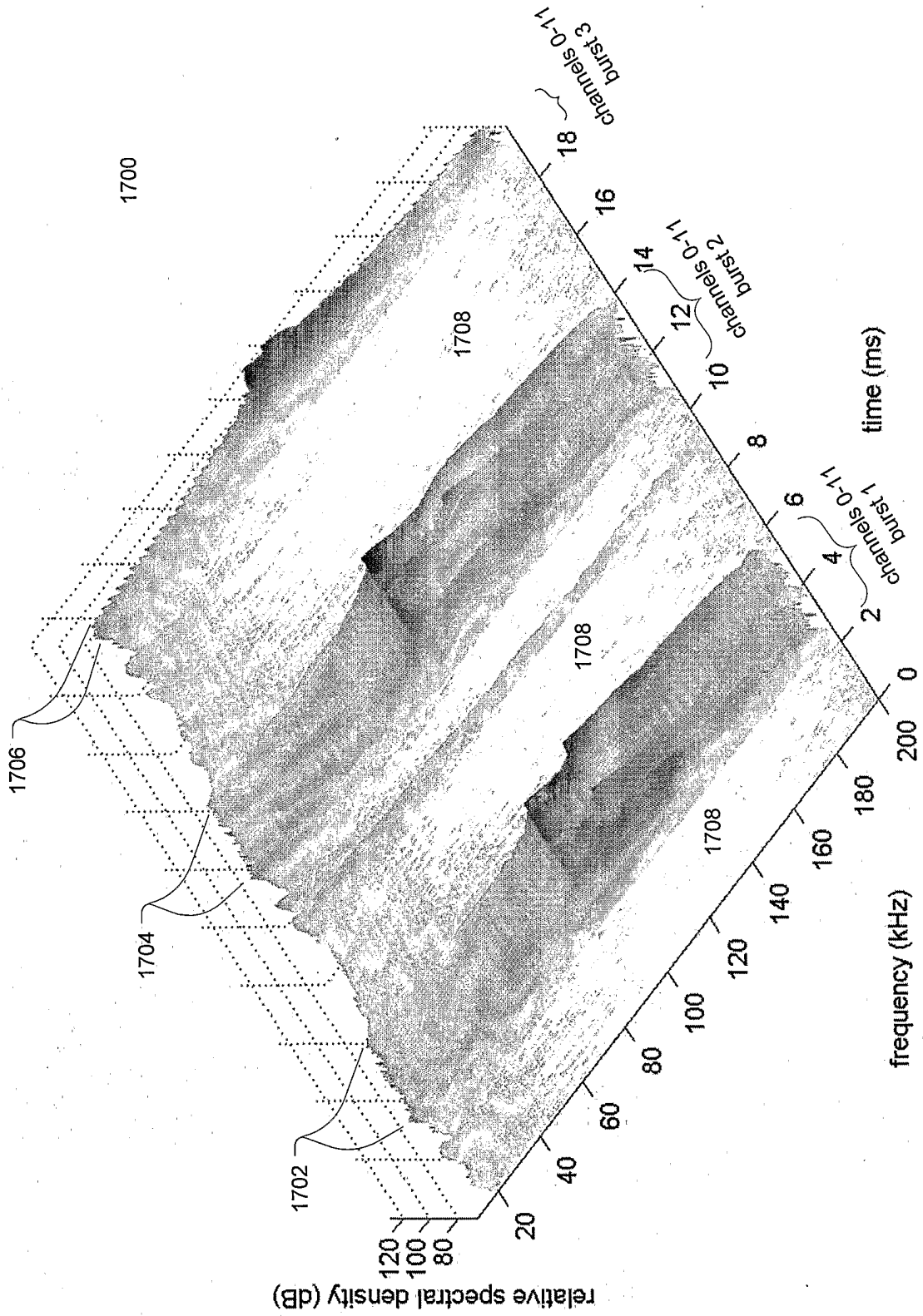
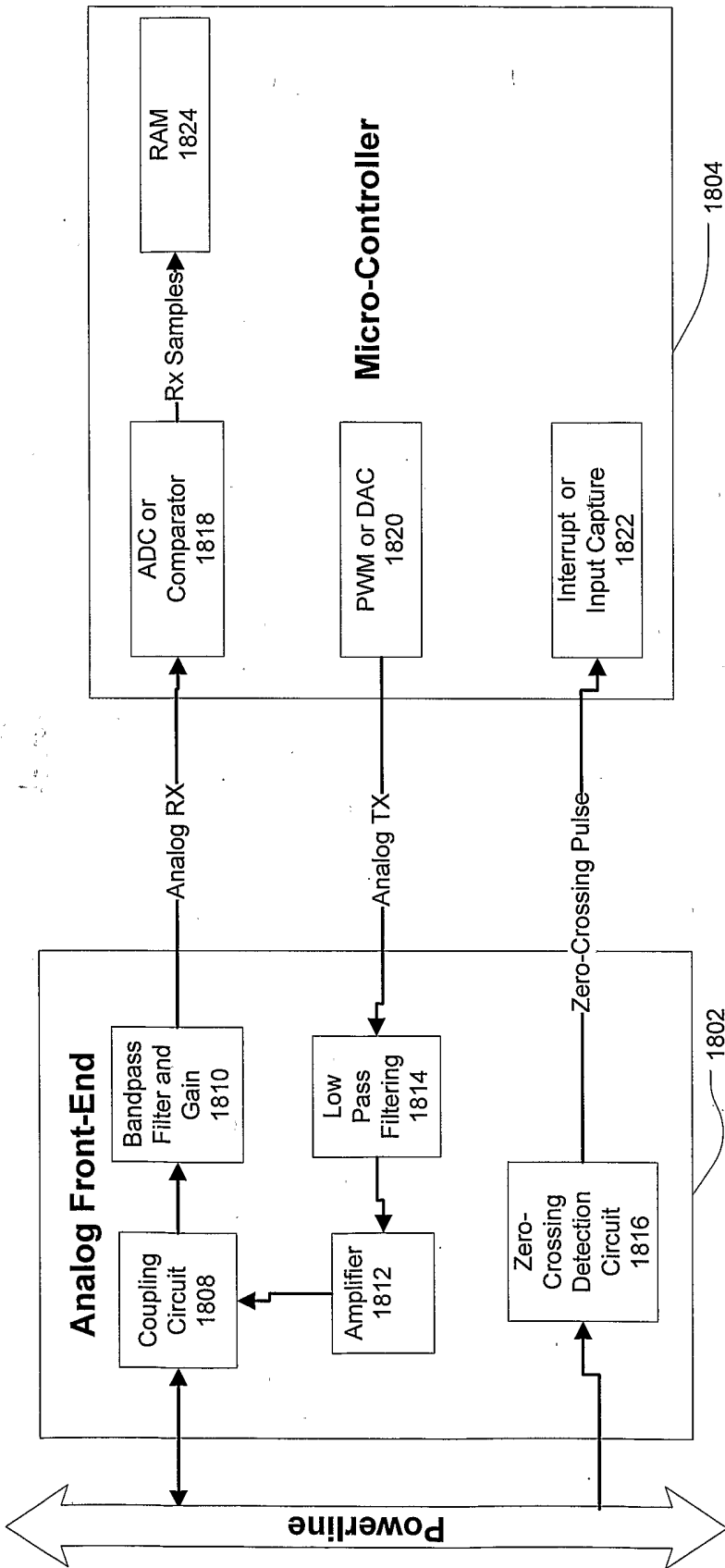


Figure 17



The powerline is the medium where the data is exchanged.

Reception

The data signal is received by the analog front-end by means of the coupling circuit. A bandpass filter and a gain are used to filter the signal and to increase its strength. After this stage, the signal is routed through the micro-controller ADC or comparator. The samples received are then stored to RAM if needed.

Transmission

The micro-controller initiates the transmission via its pulse width modulator or DAC. This analog signal is then filtered in order to respect regulations. Once filtered the signal is amplified and transmitted to the powerline via the coupling circuit.

Figure 18

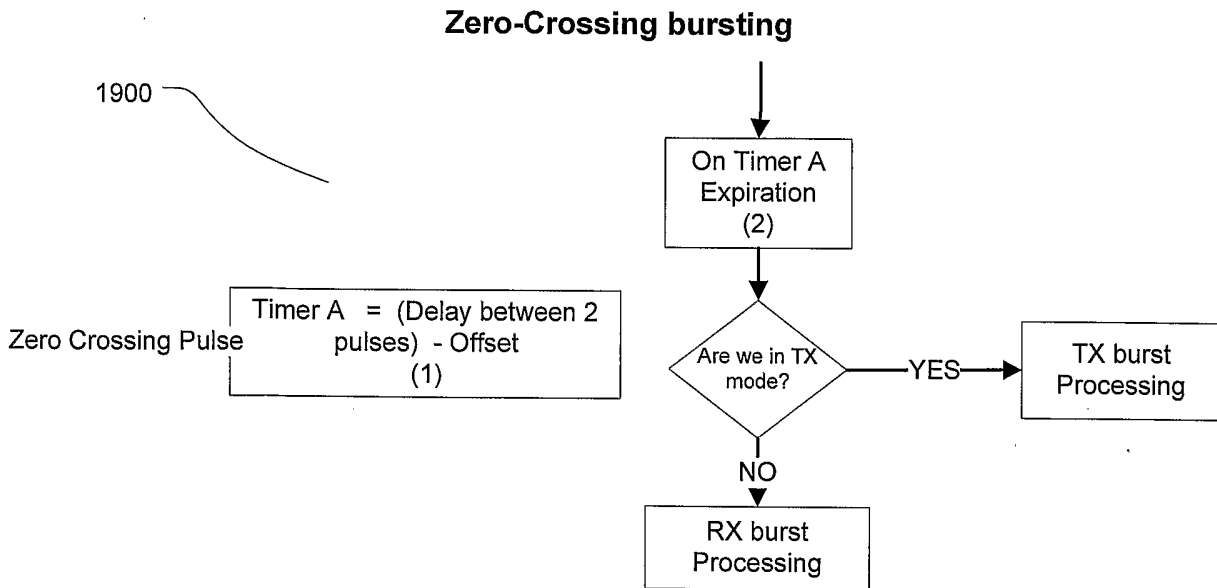
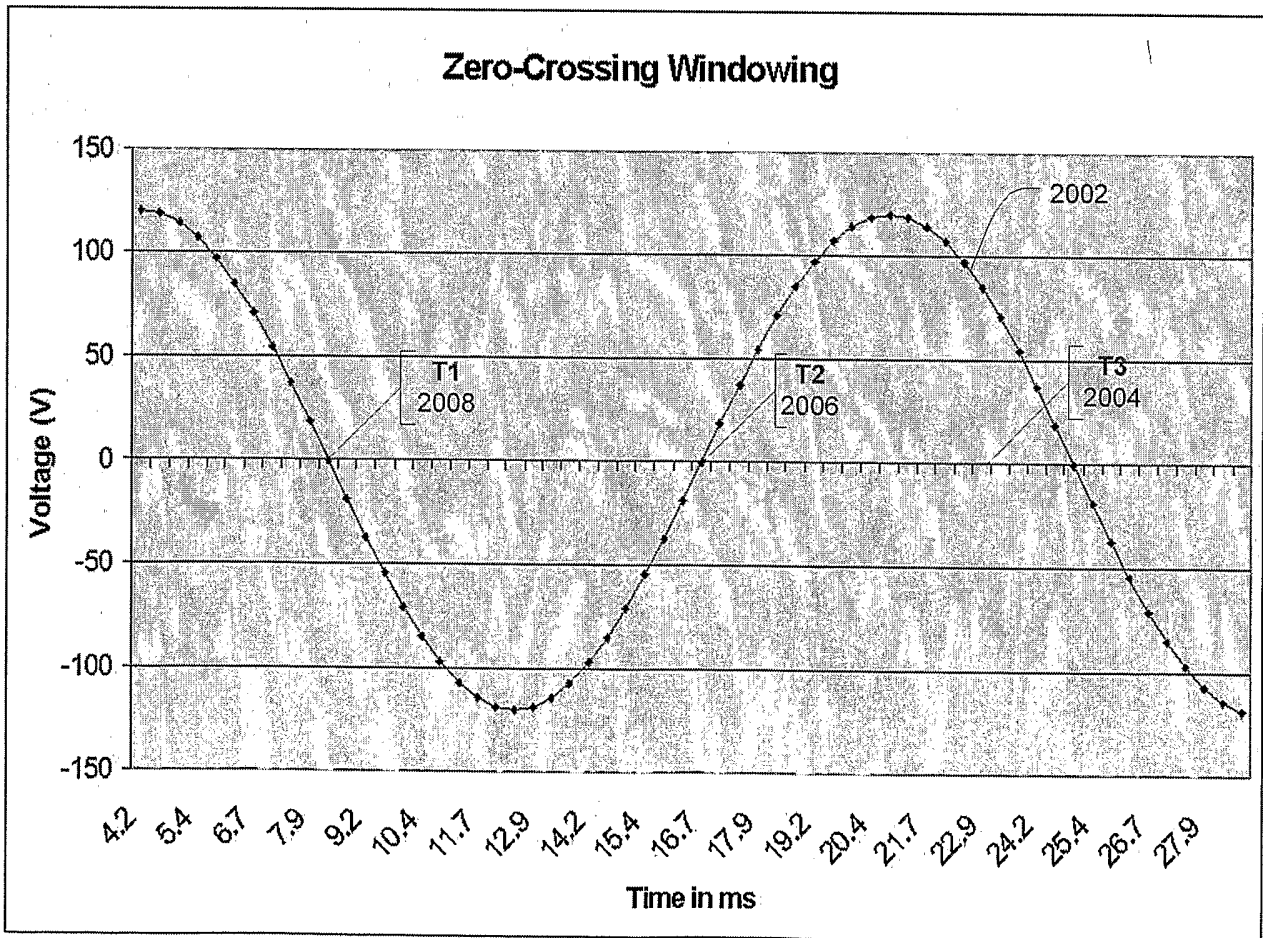
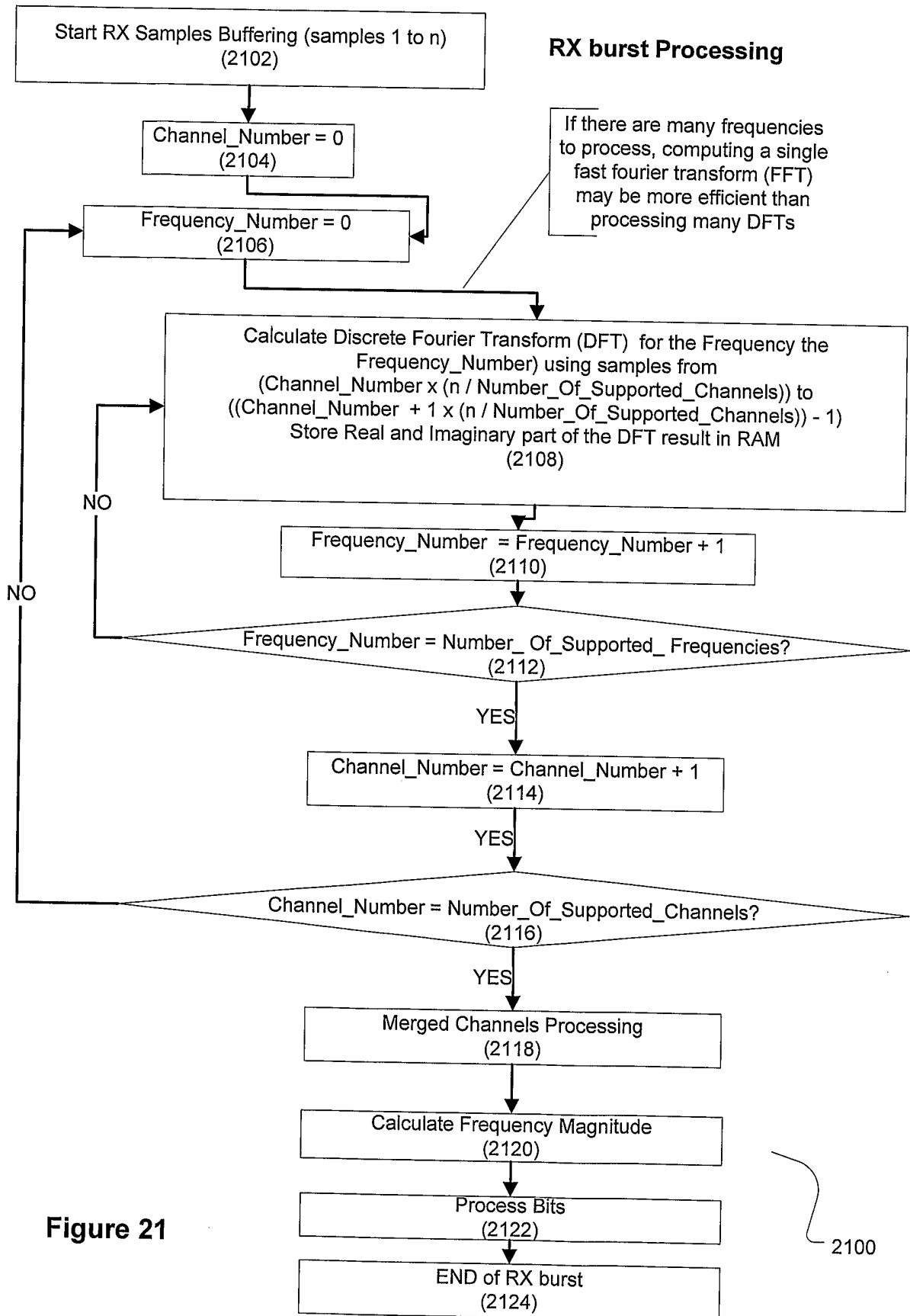


Figure 19



In this example, the zero-crossing pulses occur at T1 and T2. The Timer A (1) will be loaded with a duration equals to (T2 - T1) - Offset. The Timer A (2) will expire at T3 at which time the burst is processed whether in TX or RX mode.

Figure 20



At the beginning of the burst, the RX samples are buffered for the entire duration of the burst. Therefore n samples are buffered into the RAM memory.

The burst is separated into many channels, where the samples are equally distributed.

Once the buffering is completed, discrete fourier transforms (DFTs) are calculated for each channel and each frequency. Therefore, if there are 4 channels in each burst and if 8 frequencies are supported by the receiver then 32 DFTs are performed.

Once each channel's frequency DFTs results are stored into memory, the Merged channel processing function is called.

Once merging is done, the calculate frequency magnitude process is called.

When all magnitudes are processed, the bit processing function is called.

Figure 21 continued

Merged Channels Processing

Channel merging is done in order to support lower baud rate modulation/demodulation techniques and to increase robustness in many noisy environments.

Since the output of the discrete fourier transform is a complex number, it is easy to add two channels by performing a complex addition of both channels complex number DFT output. Note that since many frequencies are supported by channels, a separate sum must be performed for each frequency .

The complex sum is the addition of the imaginary part of both channels to be merged and the addition of both real parts of the channels to be merged.

Channel 1 of 4 REAL = (Channel 1 of 8 REAL + Channel 2 of 8 REAL)
 Channel 1 of 4 IMG = (Channel 1 of 8 IMG + Channel 2 of 8 IMG)

In the example below, 7 merged channels are created by merging the 8 base channels. 7 sum operations per supported frequency are required to create these extended channels.

It is also possible to create other channels, for example we could have created a merged channel by the sum of (Channel 2 of 4) and (Channel 3 of 4).

Example of Channel Merging for a Receiver Supporting 8 Channels.

Note that this merging must be performed for every supported frequency by the receiver

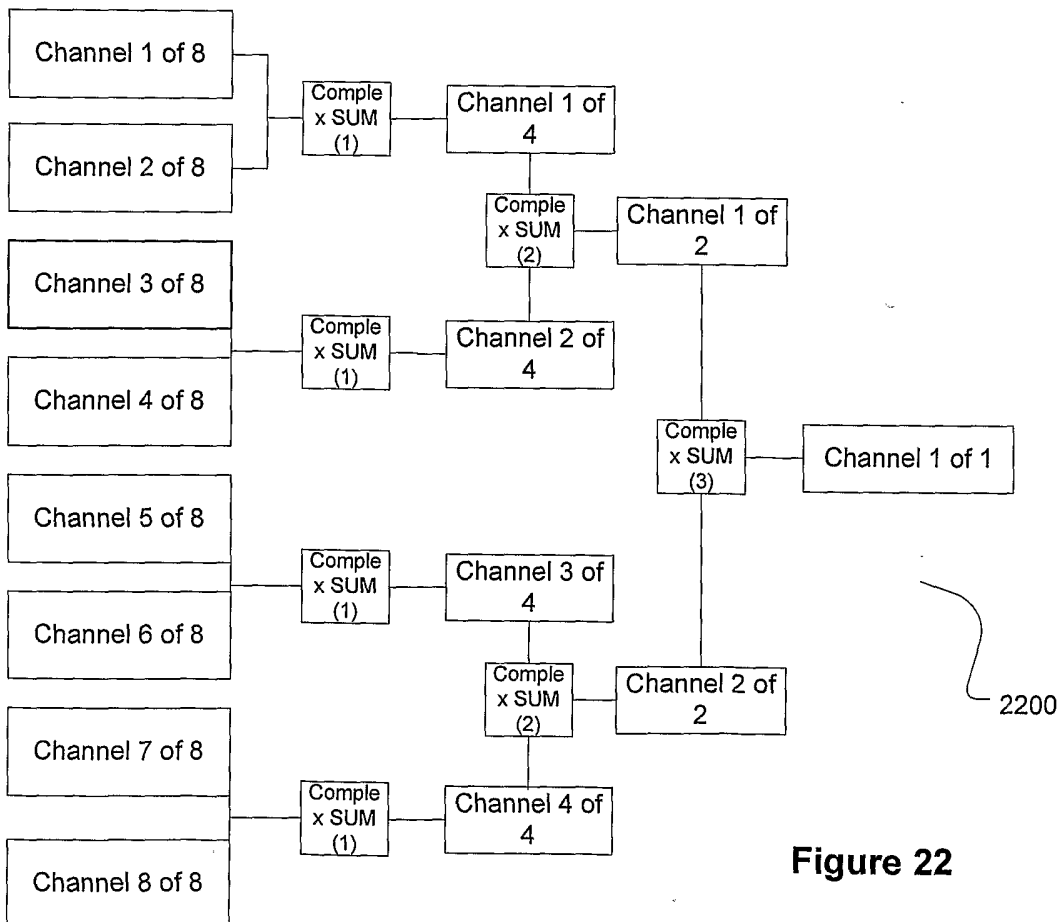


Figure 22

Calculate Frequency Magnitude

This process is executed for every channel (base and merged) by every supported frequency

The frequency magnitude for a channel is simply

$$Magnitude = \sqrt{Imaginary^2 + Real^2}$$

Figure 23

Process Bits

Bits are processed by comparing the various channel magnitudes for each frequency. The highest magnitude normally determines which frequency was received and therefore which bit.

Example 1: High speed technique using 16 frequencies and 24 channels (11520bps on a 60hz powerline)

For each channel, 4 bits are calculated. The bit values are simply the binary values of the frequency number having the biggest magnitude (therefore from 0000 to 1111)

Frequency #	Frequency in kHz (example)	Bit Coding
0	100	0000b
1	105	0001b
2	110	0010b
3	115	0011b
4	120	0100b
5	125	0101b
6	130	0110b
7	135	0111b
8	140	1000b
9	145	1001b
10	150	1010b
11	155	1011b
12	160	1100b
13	165	1101b
14	170	1110b
15	175	1111b

Example 2: Medium speed technique using 8 frequencies and 6 merged channels over the 24 base channels (2160bps on a 60hz powerline)

For each channel, 3 bits are calculated. The bit values are simply the binary value of the frequency number having the biggest magnitude (therefore from 000 to 111)

Frequency #	Frequency in kHz (example)	Bit Coding
0	100	000b
1	110	001b
2	120	010b
3	130	011b
4	140	100b
5	150	101b
6	160	110b
7	170	111b

Example 3: Very low speed differential technique using the 1 merged channel over the 24 base channels and 2 frequencies.

The bits are calculated as the variation of the magnitude over 2 bursts.

-> If the magnitude for frequency 0 decreases, the bit is 0, otherwise the bit is 1.

-> Same thing can be done for frequency 1, if the magnitude for frequency 0 decrease, the bit is 1, otherwise 0.

This means that 1/2 bit is calculated at every burst, 60bps....

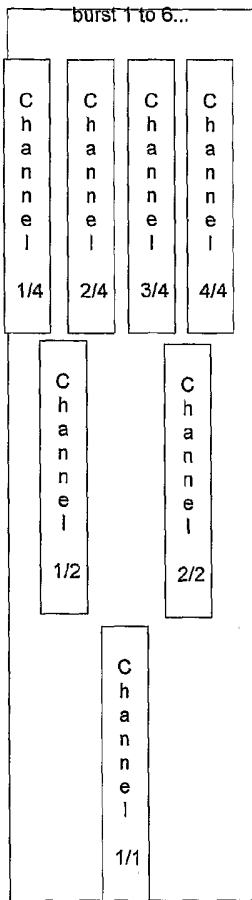
More details are found in the differential bit reception section.

Example of bit coding for a differential bit receiver. See [0091]

Burst 0		Burst 1		Bit Coding
Frequency #	Frequency in kHz (example)	Frequency #	Frequency in kHz (example)	
0	100	1	110	0b
1	110	0	100	1b

Frequency Window		Bit Coding
Window 1	Window 2	
0	1	0
1	0	1

Figure 24



In this example there are 6 bursts transmitted near the zero-crossing of the powerline voltage. Each burst is divided into 4 base channels that generate 3 merged channels.

Let's say that the communication method is method E (60bps differential using an all channel merged and 2 frequencies).

In this case, to send a 0, the device must transmit frequency 0 in the first burst and frequency 1 in the second burst.

To transmit the 3 following bits 0,1,1 the bursts would look like:

burst 1		burst 2		burst 3		burst 4		burst 5		burst 6	
Bit 0		Bit 1		Bit 1		Bit 0		Bit 1		Bit 1	
F0	F1	F1	F0	F1	F0	F1	F0	F1	F0	F1	F0
(100kH)	(110kH)	(110kH)	(100kH)	(110kH)	(100kH)	(110kH)	(100kH)	(110kH)	(100kH)	(110kH)	(100kH)
z)	z)	z)	z)	z)	z)	z)	z)	z)	z)	z)	z)

2500

To decode these bits, the demodulator simply compares the variations of the magnitudes for the given frequencies over the bursts.

If the F0 magnitude decreases, a 0 is detected otherwise a 1 is detected. The same thing can be done for F1 in parallel.

The selected frequencies and bit coding are given as examples and refer to the table given in figure 24 for differential bit coding.

Figure 25

2600

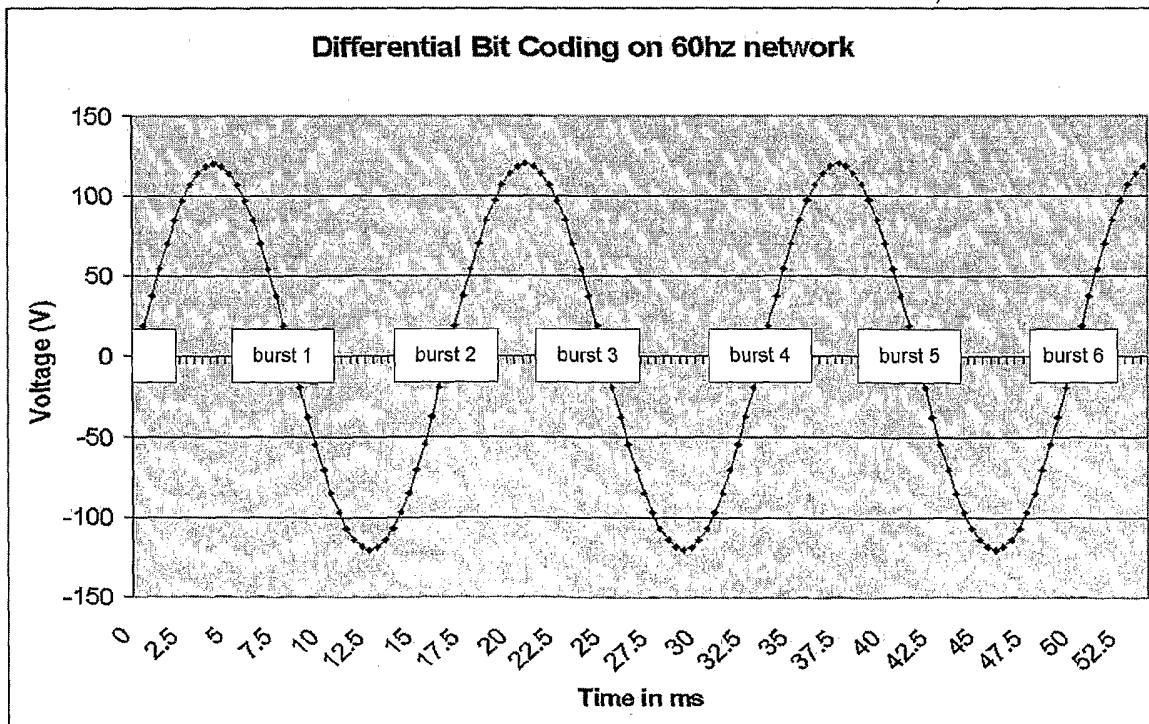


Figure 26

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2006/000400

A. CLASSIFICATION OF SUBJECT MATTER
 IPC: **H04B 3/54** (2006.01) , **H04L 27/10** (2006.01) , **H04L 27/00** (2006.01)
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC(7): H04B 3/54 (2006.01) , H04L 27/10 (2006.01) , H04L 27/00 (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
 Delphion, Canadian Patent Database, USPTO, IEEE, European Patent Database, [Keywords: power line communications, signal diversity, tdma, FSK, time slot, zero crossing, zero crossing detector, power signal]

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,300,126 (Gajjar), 10 November 1981 (10-11-1981) (column 1, lines 60-64, FIG.'S 3a-3d)	1, 10
Y	US 2004/0037311 A1 (Willes et al.), 26 February 2004 (26-02-2004) (paragraph[0006], [0007], [0011])	1
Y	EP 1,259,007 (Jin-Tae) 20 November 2002 (20-11-2002) (abstract)	10
Y	US 6,144,292 (Brown), 7 November 2000 (7-11-2000) (column 3, lines 5-7)	10

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents :	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 7 June 2006 (7-06-2006)	Date of mailing of the international search report 21 June 2006 (21-06-2006)
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Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001(819)953-2476	Authorized officer Camran Syed (819) 934-4550
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International application No.
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Information on patent family members

International application No.
PCT/CA2006/000400

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