PATENT SPECIFICATION (11) 1 587 129

1 587 129

(21) Application No. 21585/77 (22) Filed 23 May 1977

(31) Convention Application No. 2 623 219 (32) Filed 24 May 1976 in

(33) Fed. Rep. of Germany (DE)

(44) Complete Specification published 1 April 1981

(51) INT. CL.[3] G11C 7/06

(52) Index at acceptance H3T 2T3F MC

(54) IMPROVEMENTS IN OR RELATING TO DYNAMIC MOS-STORE READ-OUT CIRCUITS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, German Federal Republic,

do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to dynamic MOS-store read-out circuits of the type in which two parallel arms each contains a switching transistor in series with a load transistor, feed-back being provided from the connection point of the switching transistor and the load transistor in each arm to a control electrode of the switching transistor in the other arm, and said connection points each being connected to a respective subportion of a bit line, and also controllably connected to one another via a balance transistor. The source electrodes of the switching transistors are connected to a node which is charged prior to the beginning of the cycle, a read-out and evaluation sequence and is discharged in order to evaluate a read-out signal.

For the evaluation of the read-out signals of dynamic MOS-stores, it is known to divide each bit line into two sub-portions, and to arrange a read-out amplifier circuit designed as a flip-flop stage between the two sub-portions, as described for example in IEEE Journal of Solid-State Circuits, Vol. SC7, No. 5, October 1972, pages 336 to 340. A read-out amplifier circuit of this type is constructed in the manner of a keyed flip-flop stage, and its fundamental properties consist in its symmetry, its low dependence upon parameter fluctuations, and on automatic regeneration of any stored signals. Read-out amplifier circuits of this type are used, in particular, in MOS-stores in which the individual storage cells consist of one-transistor storage cells.

Recent developments in MOS-store technology have resulted in an increasing storage density per storage module, which has in turn led to smaller read-out signals, and to the need to tolerate component-parameters exhibiting greater fluctuations. For the evaluation of read-out signals from these MOS-stores a more suitable amplifier circuit is described in IEEE Journal of Solid-State Circuits, Vol. SC8, No. 5, October 1973, pages 310 to 318, or in IEEE Journal of Solid-State Circuits, Vol. 9, No. 2, April 1974, pages 49 to 54. In this latter type of read-out amplifier circuit, the load transistors of the flip-flop stage serve only to pre-charge the sub-portions of the bit lines at the connection points between a load transistor and a switching transistor, and during evaluation of a read-out signal, the load transistors remain blocked. After any signal voltage has been set up on a sub-portion of a bit line, following the read-out of an item of information from a storage cell, the voltage is then slowly reduced at the connection point between the source electrodes of the switching transistors, so that it is ensured that only one of the switching transistors, namely that one switching transistor whose drain electrode is connected to any read-out signal, is rendered conductive. With this mode of operation, the amplification of the flip-flop stage is very high, and fluctuations in the geometry of the transistors and the capacitances of the bit line have virtually no significance. However, a disadvantage of this read-out amplifier circuit consists in the relatively long evaluation time. Therefore attempts have been made to reduce the voltage at the connection point of the source electrodes of the switching transistors in accordance with an optimum curve that is calculated to be such that one of the switching transistors is exactly at the blocking boundary, or alternatively operates in a weakly conductive state, in which the current is constant. This measure serves to shorten the resultant evaluation time, but nevertheless, the evaluation time is still relatively long.

One object of the present invention is to provide a read-out circuit having the

above-mentioned features which operates in such manner that the evaluation time required for a read-out signal is substantially shortened, without impairment of the evaluation reliability.

The invention consists in a dynamic MOS-store read-out circuit in which two parallel arms each contain a switching transistor in series with a load transistor, feed-back being provided from the connection point of the switching transistor and of the load transistor in each arm to a control electrode of the switching transistor of the other arm, and said connection points each being connected to a respective sub-portion of a bit line, and also controllably connected to one another via a balance transistor, and in which the source electrodes of the switching transistors are connected to a node which is charged prior to the beginning of a read-out and evaluation sequence, and is discharged for the evaluation of a read-out signal in such manner that if eihter switching transistor whose drain electrode is subjected to the voltage change which is to give rise to a read-out circuit output signal it is rendered conductive, means being provided which act following the charging of the node to cause the load transistors to be rendered non-conductive and to temporarily maintain the balance transistor in the conductive state, and the balance transistor then being rendered non-conductive for the evaluation of the read-out signal, during which evaluation the discharge curve of the node is such that the other switching transistor temporarily passes into a freely conductive state to shorten the time required for the evaluation.

Whereas in the prior art circuits only one of the switching transistors is brought into the freely conductive state during the evaluation process and possibly the other into a weakly conductive state, in a circuit constructed in accordance with the invention the discharge curve of the node is such that a switching transistor whose drain electrode is connected to a portion of the bit line to which no information has been read out is also temporarily brought into a freely conductive state during the evaluation time of the read-out signal. The discharge curve then proceeds in such manner that the flip-flop stage of the read-out amplifier circuit triggers back into the state which corresponds to the information to be evaluated.

When the balancing transistor between the connection points is rendered non-conductive, the parasitic capacitances of this transistor tend to reduce the voltage at the connection points of the two arms. In this way, at the end of the process, the two switching transistors of the flip-flop stage are blocked, irrespectively of which threshold voltages the switching transistors possess, and irrespectively of the magnitude of the capacitances of the sub-portions of the bit line.

The invention will now be described with reference to the drawings, in which: —

Figure 1 schematically illustrates a first exemplary embodiment, including a function generator for the production of the discharge curve;

Figure 2 schematically illustrates a first embodiment of a function generator for use in the embodiment shown in Fig. 1;

Figure 3 graphically illustrates a curve relating to an inverter circuit which is used in the function generator shown in Fig. 2;

Figure 4 is a set of explanatory waveform diagrams relating to the read-out circuit illustrated in Fig. 1;

Figure 5 schematically illustrates part of another exemplary function generator;

Figure 6 schematically illustrates a sub-circuit for operation in the circuit arrangement shown in Fig. 5; and

Figure 7 schematically illustrates another sub-circuit for operation with the circuit arrangement shown in Fig. 6.

The read-out circuit illustrated in Fig. 1 consists of a flip-flop stage FF and a function generator FG.

The flip-flop stage FF, in each case, consists of two arms, each containing a load transistor TL in series with a switching transistor TS, one arm comprising a load transistor TL1 and a switching transistor TS1, whereas the second arm contains a load transistor TL2 and a switching transistor TS2. The connection point between each switching transistor and its load transistor is connected to a respective sub-portion of a bit line B. Accordingly, a sub-portion BL of the bit line is connected to connection point p1 that lies between the load transistor TL1 and the switching transistor TS1, whereas a sub-portion BR of the bit line is connected to connection point p2 that lies between the load transistor TL2 and the switching transistor TS2. In addition, the connection points p1 and p2 are connected together via a transistor TO, which is referred to as a balance transistor.

The connection forming a junction K between the source electrodes of the switching transistors TS1 and TS2 is referred to as a node, and the load transistors TL1 and TL2 are operated with the aid of a timing signal S2, whilst a fixed voltage VDD remains connected to the load transistors TL1 and TL2, and the node K is connected to another supply terminal via the function generator FG.

The function generator can be constructed from a discharge circuit E and an

inverter I in an arrangement as shown in Fig. 2. The discharge circuit E consists of transistors T1, T2, T3 and a capacitor C1. The transistor T3 is operated by a timing signal S1, and is arranged between the node K and a parallel arrangement of the transistor T1 and the capacitor C1. The transistor T1 has its control electrode connected to the output of the inverter I. The transistor T2 is operated by a timing signal S2, and connects the node K to a fixed voltage supply terminal VSS. The capacitor C1 and the transistor T1 are likewise connected to this terminal VSS.

The inverter I is composed of a transistor T5 connected in series between two transistors T4 and T6 that are connected as diodes. The node K is connected to the control electrode of the transistor T5, to apply a voltage V3, which is formed at the node K. The output of the inverter I is connected to the control electrode of the transistor T1 of the discharge circuit E. The fixed voltage terminal VDD is connected to the diode T6, and the fixed voltage terminal VSS is connected to the diode T4.

The mode of operation of the read-out amplifier circuit illustrated in Fig. 1 will now be explained with reference to Figs. 3 and 4. It has been assumed that the transistors are in the form of *n*-channel transistors, so that the voltages shown in Fig. 4 are positive voltages.

Before a read-out signal connected to the bi tline portions BL and BR can ve evaluated, it is necessary to pre-charge the read-out amplifier circuit. For this purpose, the balance transistor TO is rendered conductive by a signal S3. In the same way, the load transistors TL1 and TL2 can be brought into the conductive state by the connection of a timing signal S2. As shown in Fig. 3, which plots the output voltage V4 against control input voltage V3, in this case the node K still carries a low potential. Under these circumstances, the bit line portions BL and BR become charged to the voltage VDD-VT, where VT is the threshold voltage of the load transistors TL1 and TL2. Naturally it is also possible to charge the bit line portions BL and BR via auxiliary tarnsistors (not illustrated), possibly by transistors connected to a control signal SO (Fig. 4). In this case it would be possible to charge the bit line portions BR and BL to a voltage VDD-2VT, for example. For this reason the portion of the signal waveform S2 which occurs during the pre-charging period between $t1$ and $t2$ has been shown as a broken line curve in Fig. 4. As the switching transistors TS1 and TS2 are likewise in the conductive state, the node K also becomes charged, to the voltage V3, which approximately equals VDD-VT-(VT + ΔVT max), where ΔVT max is the maximum occurring difference in transient switching potential between all the switching transistors which are connected to the node K.

At the end of the pre-charging phase, which lasts from the time $t1$ to the time $t2$, the node K has charged, and the signal SO or the control timing signal S2 applied for pre-charging is disconnected, so that the load transistors TL1 and TL2 pass into the blocking state.

The pre-charging is followed by a time period for read-out preparation, which is composed of successive time zones from $t2$ to $t3$, and from $t3$ to $t4$.

During the time zone $t2$ to $t3$ the timing signal S3 is still connected to the balance transistor TO, so that the latter is still rendered conductive to connect the bit line portions BL and BR to one another. The switching transistors TS1 and TS2 are still in the conductive state.

During the subsequent time zone from $t3$ to $t4$ the timing signal S3 is disconnected and the balance transistor TO is blocked. In this way the direct connection path between the bit line portions BR and BL is broken. The reluction in the timing signal S3 results in the voltage of the bit line portions BR and BL being reduced on account of the parasitic capacitances of the balance transistor T10. Consequently the switching transistors TS1, TS2 are safely blocked after the time $t4$.

In the zone from $t4$ to $t5$, an item of information is read-out from a storage cell, and accordingly any voltage difference read-out signal USig is set up on the two halves of the bit line, as is indicated by two arrows in Fig. 4 in the time zone from $t4$ to $t5$, when the voltages VBL and VBR in the bit line portions BL and BR respectively have a significant difference, as the voltage difference VSig is set up on the bit line portions BR and BL. The switching transistors TS1 and TS2 of the flip-flop stage FF both remain blocked.

At the time $t5$ the evaluation process commences. Firstly, a signal S1 causes the transistor T3 of the discharge circuit E to be rendered conductive. Via the inverter I, with the characteristic curve shown in Fig. 3, the voltage V3 at the node K determines the voltage V4 at the control electrode of the transistor T1, where the transistor T5 is initially still in the conductive state. It can be seen from Fig. 3 that the voltage V4 which is emitted under these circumstances from the inverter I is approximately twice VT, where VT is the threshold voltage of the diode T4 and of the transistor T5. As a result of the voltage V3, the transistor T5 is held in its conductive state.

If the signal S1 is now connected to the transistor T3, the latter becomes conduc-

tive and a current can flow from the node K via the transistor T3 and the capacitor C1. Firstly this results in the voltage at the node K dropping very rapidly (see Fig. 4, voltage V3). The rapid reduction in the voltage V3 at the node K now causes that switching transistor of the flip-flop stage FF whose drain electrode is suvjected to a voltage change resultant from the read-out of the information to be rendered freely conductive. If it is assumed that information from a storage cell which is connected to the bit line portion BL is read-out, the switching transistor TS1 is rendered freely conductive, and therefore a current can flow through this switching transistor, the currents through the switching transistors TS1 and TS2 being illustrated in Fig. 4 as currents IS1 and IS2 respectively.

During a time from $t6$ to $t7$ the voltage V3 at the node K is reduced only very slowly, and remains virtually constant, because the transistor T1 in the discharge circuit remains in the same state, as can be seen from the curve in Fig. 3.

The node K now begins to discharge at an increasing rate, and this process is intensified by the inverter I. During the time zone from $t7$ to $t8$, the voltage waveform V4 now changes very rapidly, in accordance with the steep gradient of the curve shown in Fig. 3, and the transistor T1 therefore assumes its conductive state rapidly. This results in a reduction in the voltage V3, with an increase in gradient of the curve (Fig. 3). The previously blocked switching transistor (e.g. TS2) becomes conductive. (See the curves of the voltages VBL, VBR and of the currents IS1 and IS2 in Fig. 4. The curve of the reduction in the voltage V3 is now such that in spite of differences in the geometry of the switching transistors TS1, TS2 and in the capacitances of the bit line portions BR and BL, thus even under unfavourable conditions, the flip-flop stage again reaches its trigger point, and therefore the switching transistor TS2 becomes blocked again, at a time $t8$. The current flowing through the switching transistor TS2 thus reduces again, and the voltage differences on the bit line portions increase rapidly.

At a time $t9$ the timing signal S2 is connected to the load transistors TL1 and TL2, and to the transistor T2 of the discharge circuit, to render these transistors conductive, so that the respective bit line portions BR and BL are set to the "zero" or "one" levels. The transistor T2 continues to accelerate the discharge of the node K until a time $t10$, when the node is discharged, and the transistor T5 of the inverter I is blocked. On that bit line portion, e.g. BR, on which a read-out signal existed, a level has set up which is used to regenerate the read-out storage cell.

At the time $t10$ the timing signal S1 is disconnected and thus the discharge circuit is cut off from the flip-flop stage FF. At a time $t11$, the read-out and regenerating processes are ended.

Figures 5, 6 and 7 illustrate another embodiment of the function generator, which has no inverter I corresponding to that used in Fig. 2. The circuits shown in Fig. 5 and Fig. 7 are composed in such manner that both are connected to the node K and together form the function generator. The circuit arrangement illustrated in Fig. 7 is responsible for ensuring that in the time zone from $t5$ to $t6$ (Fig. 4) the voltage at the node K is reduced very rapidly, whereas during the remainder of the discharge process of the node K the rate is determined by the circuit arrangement shown in Fig. 5. The circuit arrangement shown in Fig. 7 is referred to as a jump-function generator.

The jump-function generator shown in Fig. 7 consists of a parallel arrangement of a capacitor C10 and a transistor T8. A transistor T9 is arranged in series with this parallel connection. The transistor T9 is operated by the timing signal S1. The capacitor C3 shown in Fig. 7 represents the parasitic capacitance of the node K.

During the time zone from $t2$ to $t3$ the connection point P5 of the jump-function generator shown in Fig. 7 is charged to the voltage V3 of the node K, the transistor T8 being rendered conductive. At the beginning of the evaluation process, the timing signal S1 renders the transistor T9 conductive, and the transistor T8 is blocked. However, when the transistor T9 is rendered conductive, there is a charge compensation between the capacitance C3 of the node K and the capacitance C10. In this case, a jump occurs at the node K, as illustrated in Fig. 4 in the time zone from $t5$ to $t6$.

The node K is still connected to the circuit corresponding to Fig. 5, which acts as a controlled voltage source. The latter consists of transistors T10, T11 and T12, whose controlled paths are connected in parallel. The timing signal S1 is fed directly to the first transistor T10, and is fed via a first delay circuit VS12 to the transistor T11, and thence via a further delay circuit VS23 to the transistor T12. Thus, when a timing signal S1 is connected, firstly the transistor T10 is rendered conductive, and the node K is initially discharged via this transistor T10. On the expiration of the delay time of the delay circuit VS12, the transistor T11 is additionally brought into the conductive state, as a result of which the discharge process is accelerated. On the expiration of the delay time of the delay circuit VS23, the transistor T12 is also rendered conductive, so that now all three

transistors T10, T11, T12 are in the conductive state. By an appropriate selection of a ratio W/L for the transistors T10, T11 and T12 it is possible to determine the shape of the discharge curve. Here W is the width of the channel, and L is the length of the channel of the particular transistor. It is expedient, for example, to select the ratio of W to L to have a value of 5 for the transistor T10, a value of 20 for the transistor T11, and a value of 200 for the transistor T12. In addition, the shape of the discharge curve is influenced by the delay times of the delay circuits VS12 and VS23.

Fig. 6 shows the construction of a delay circuit. This consists of five transistors T20, T21, T22, T23 and T23. A timing signal CE is connected to the transistor T22, and a timing signal CE is connected to the transistor T23. The control electrode of the transistor T20 is connected to an input terminal to which is supplied an input signal VE, and on the expiration of the delay time this input signal appears at an output terminal as an output signal VA. The delay time itself is basically determined by the ratio W to L of the transistor T20. When no signal is present at the input of the delay circuit, the transistor T23 is rendered conductive and a node $p4$ is charged. Accordingly the transistor T24 goes conductive, and the output voltage VA is held approximately at earth potential (VSS in this case).

If a signal is connected to the input of the transistor T20, and the timing signal CE is switched over, the node $p4$ is discharged and after a certain length of time the transistor T24 is blocked. Then the voltage VA increases.

Thus, with the function generator illustrated in Figures 5 to 7, it is also possible to form a discharge curve corresponding to that shown in Fig. 4. The charging process during the time zone from $t1$ to $t2$ of the node K, and also the curve of the voltage at the node K between the charging of the node and the discharging, corresponds in full to the conditions described with reference to Fig. 1. If the discharge of the node K is to be initiated, a timing signal S1 is once more connected to the function generator, and thus the jump-function generator shown in Fig. 7 and the controlled voltage source shown in Fig. 5 are connected With the aid of the jump-function generator, during the time zone from $t5$ to $t6$ the voltage at the node falls very rapidly; and subsequently the time-staggered connection of the transistors T10, T11, and T12 ensures that the controlled voltage source gives a discharge curve of the node K having a form which guarantees that during the time zone from $t7$ to $t9$ both the switching transistors of the flip-flop stage FF are in the conductive state, whereas at the end of this time zone the flip-flop stage triggers into the state which is determined by the read-out signal on the bit line portions.

In the exemplary embodiments the invention has been described with the assumption that n-channel transistors are used. Naturally a construction with a p-channel transistors is also possible.

The advantages of the read-out amplifier circuit corresponding to the invention consist, in particular, in that the evaluation time is fundamentally shortened. This improvement is achieved in that, during the evaluation of the read-out signals, both of the switching transistors of a flip-flop stage are rendered conductive in a quite specific time zone. Extremely simple circuit arrangements are proposed for the realisation of the corresponding discharge curve across the node K. The timing signals may be obtained from a common pulse generator source of known design (not shown) or may be derived from timing control units provided for general operation of a store arrangement.

WHAT WE CLAIM IS: —

1. A dynamic MOS-store read out circuit in which two parallel arms each contain a switching transistor in series with a load transistor, feed-back being provided from the connection point of the switching transistor and of the load transistor in each arm to a control electrode of the switching transistor of the other arm, and said connection points each being connected to a respective sub-portion of a bit line, and also controllably connected to one another via a balance transistor, and in which the source electrodes of the switching transistors are connected to a node which is charged prior to the beginning of a read-out and evaluation sequence, and is discharged for the evaluation of a read-out signal in such manner that if either switching transistor whose drain electrode is subjected to the voltage change which is to give rise to a read-out circuit output signal it is rendered conductive, means being provided which act following the charging of the node to cause the load transistors to be rendered non-conductive and to temporarily maintain the balance transistor in the conductive state, and the balance transistor then being rendered non-conductive for the evaluation of the read-out signal, during which evaluation the discharge curve of the node is such that the other switching transistor temporarily passes into a freely conductive state to shorten the time required for the evaluation.

2. A read-out circuit as claimed in Claim 1, in which the node is connected to a func-

tion generator which produces the discharge curve of the node.

3. A read-out circuit as claimed in Claim 2, in which the charging of the node is effected via the switching transistors.

4. A read-out circuit as claimed in any preceding Claim, in which means are provided which act following the evaluation of the read-out signal to render the load transistors conductive so that voltages corresponding to a binary "one" signal or binary "zero" signal are set up on the bit line portions.

5. A read-out circuit as claimed in Claim 2, or in Claim 3 or Claim 4 when dependent upon Claim 2, in which said function generator is constructed from a discharge circuit and an inverter connected to the node, the discharge circuit consisting of a third transistor which is rendered conductive during the evaluation time and which is connected to the node, together with a parallel arrangement of a fourth transistor and a capacitor which are connected between the third transistor and a fixed voltage supply terminal, and wherein the control electrode of the fourth transistor is connected to the output of the inverter, a fifth transistor being arranged between the node and the fixed voltage terminal and rendered conductive when the load transistors are rendered conductive.

6. A read-out circuit as claimed in Claim 5, in which said inverter is composed of a sixth transistor whose control electrode is connected to said node, a second electrode is connected to said supply terminal via a transistor connected as diode, and whose third electrode is connected via a further diode-connected transistor to a second fixed voltage terminal, said third electrode forming an output terminal of the inverter.

7. A read-out circuit as claimed in Claim 2, or in Claim 3 or Claim 4 when dependent upon Claim 2, in which said function generator possesses a jump-function generator which serves to rapidly discharge the node at the beginning of the discharge process, and serves as a controlled voltage source for the remainder of the discharge process.

8. A read-out circuit as claimed in Claim 7, in which said jump-function generator consists of a parallel arrangement of an eighth transistor and a capacitor, and of a ninth transistor which is located between the parallel arrangement and said fixed voltage terminal, the parallel arrangement being connected to the node, and means being provided to act during the time between the charging and discharging of the node to render the eighth transistor conductive, whilst the ninth transistor is rendered conductive during the evaluation time.

9. A read-out circuit as claimed in Claim 7 or Claim 8, in which there is provided a controlled voltage source composed of a tenth transistor whose controlled path is located between said fixed voltage terminal and the node with its control electrode connected to a timing signal source, a first delay circuit whose input is supplied with the timing signal, an eleventh transistor whose controlled path is located between said fixed voltage terminal and the node, and whose control electrode is connected to the output of the first delay circuit, a second delay circuit which is connected to the output of the first delay circuit, and a twelfth transistor whose controlled path lies between said fixed voltage terminal and said node, and whose control electrode is connected to the output of the second delay circuit, the ratio W to L of the tenth transistor being smaller than that of the eleventh transistor, and that of the eleventh transistor being smaller than that of the twelfth transistor, where W is the width of the channel of each particular transistor and L is the length of the channel of that transistor.

10. A dynamic MOS-store read out circuit substantially as described with reference to Figures 1 and 2, or Figures 1, 5, 6 and 7.

For the Applicants,
G. F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing, BN11 2BT.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1981.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1587129 COMPLETE SPECIFICATION
3 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

Fig.1

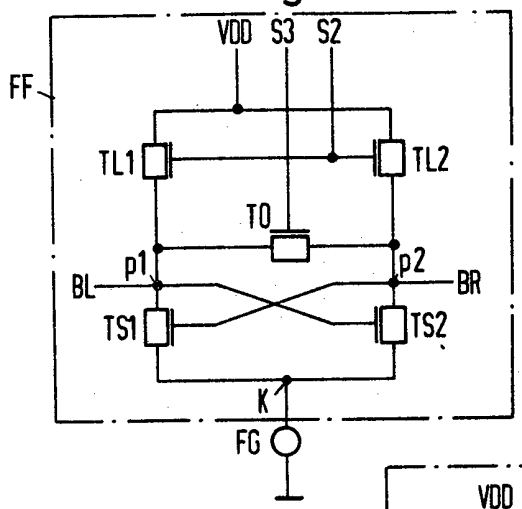


Fig. 2

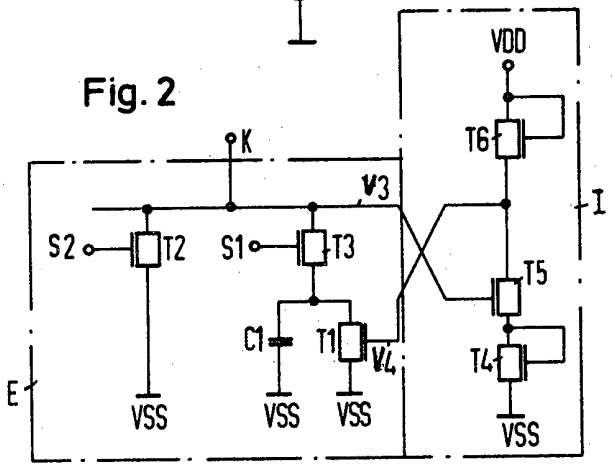


Fig. 3

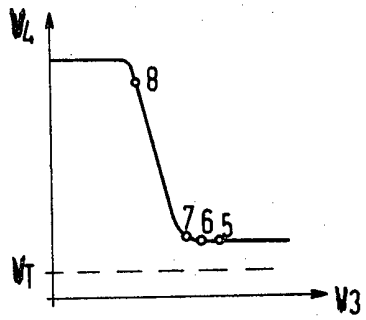


Fig. 5

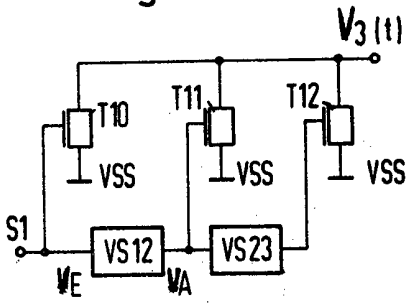


Fig. 6

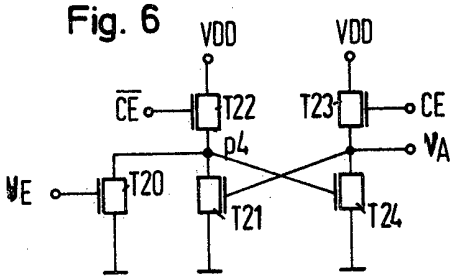


Fig. 7

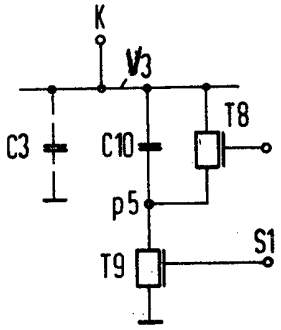
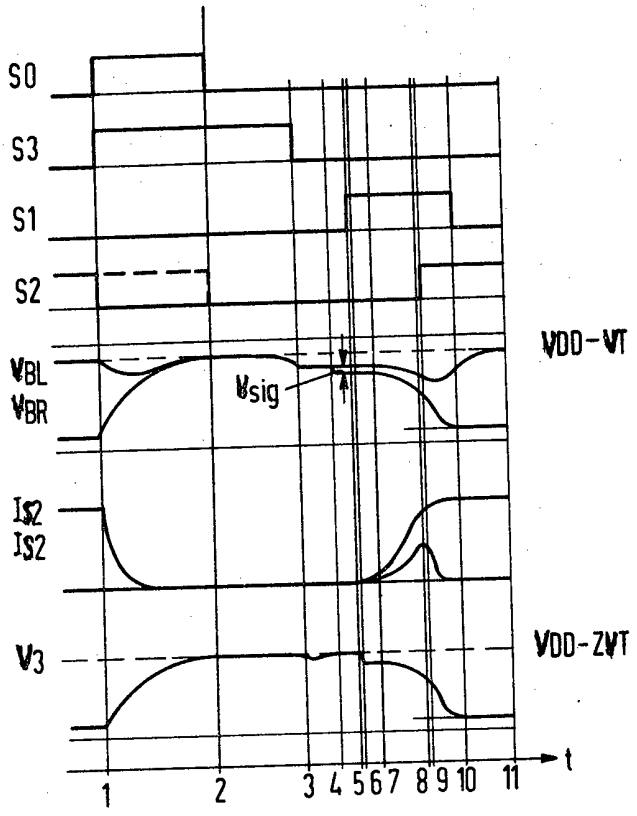


Fig. 4


S0
S3
S1
S2
VBL
VBR
Vsig
VDD-VT
IS2
IS2
V3
VDD-ZVT
t
1
2
3
4
5
6
7
8
9
10
11