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down signal being connected to a control line of a gate buffer of a respective farther upper leg switching device, or further lower leg switching device, - for each upper leg switching device and each lower leg switching device, a positive gate command connection path from a positive gate command output of a pre-driver, to provide a reset signal for a gate pull down signal of the respective further upper leg switching device, and the respective further lower leg switching device.

[DESCRIPTION]

[TITLE OF INVENTION]

OVERLAPPING REDUCTION FOR CURRENT SOURCE CONVERTERS USING  
GATE CURRENT MIRRORS

[Technical Field]

[0001]

This disclosure pertains to the field of current source converters, comprising at least two switching half-bridges each having an upper switching device and a lower switching device, and where an ON state overlapping between upper switching devices or between lower switching devices of two half-bridges having opposite switching transition periods is needed to avoid a current interruption, which would cause an overvoltage in the converter. Priority is claimed on European Patent Application No. EP23306949.1, filed November 10, 2023, the contents of which are incorporated herein by reference.

[Background Art]

[0002]

Current source converters are used for different applications, such as HVDC, motor drive or power factor correction. The main limitation of such converters mainly is the use of bulky input inductances and power modules, designed for conventional switching cells. However, the growing emergence of wide bandgap devices, e.g. Silicon Carbide and/or Gallium Nitride, with lower conductive and switching losses opened up new possibilities for current fed converter design, by reducing size and improving efficiency.

[Summary of Invention]

[PROBLEM TO BE SOLVED BY THE INVENTION]

[0003]

Current source power converters, abbreviated as “CSC”, comprise at least two half-bridges where the switches of the upper legs of two half-bridges and the switches of the lower legs of two half-bridges are controlled in a complementary way, with conducting to blocking, and blocking to conducting transitions. Between these transitions, overlapping where either of both upper switches or both lower switches are ON is used. The main reason of the overlapping is due to the nature of the current source which is an inductive

source that should not be interrupted. Current interruption may be caused by multiple factors, including wrong control signal of one of the two switches, a faulty device failed in open circuit, or a failed gate driver. In such cases, no current path for the DC current may lead to tremendous damage, since current interruption in the current source or the current fed converter induces a fast increase in a voltage across the semiconductor device, higher than the breakdown voltage of such semiconductor, which may cause destruction of the power converter. In such a case, the power switch devices which incur the overvoltage may enter in an “avalanche mode”, where the energy stored in the inductance is dissipated. Since these devices are not capable of withstanding prolonged conditions of high voltage and high current, such conditions may destroy such devices. Such a situation already creates the necessity of an overlap between the upper switching devices or between the lower switching devices, having opposite switching transition periods of half-bridges of current source converters, such as an inverter type shown in FIG. 1. Nonetheless, a reduction of overlapping time is beneficial for the overall converter operation. First, an overlapping time that is too high would lead to a high “Total Harmonic Distortion” (THD) of the output current. Some software solutions may be implemented within the control loop, to mitigate such side effects. In addition, reduction of the overlapping time could reduce losses in case of a CSC having a feature of current bi-directionality, as with the device assembly presented in the circle A of FIG. 1. The control of the two devices placed in series depends on the overlapping time, the longer the overlapping time, the longer is the conduction of one of the body diodes. Therefore, the conduction losses increase due to high forward voltage.

[MEANS TO SOLVE THE PROBLEM]

[0004]

The present disclosure improves the aforementioned situation, by providing a switching system where overlapping between conducting to non-conducting, and non-conducting to conducting power semiconductor switches in a current fed converter is reduced, without the need to reduce the overlapping calculated by a controller of the converter.

More precisely, the present disclosure proposes a control circuit for a current source converter, having a current generator comprising an inductance, and having two or more half bridges, each half bridge having an upper leg provided with an upper switching device, and a lower leg provided with a lower switching device. Said upper legs switching devices and said lower legs switching devices being controlled by a controller, to provide

an overlap between an upper leg turning off switching device, and an upper leg turning on switching device, and to provide an overlap between a lower leg turning on switching device, and a lower leg turning off switching device, through gate pull up and gate pull down pulse signals to gate driver buffers of said switching devices, characterized in that said gate driver circuit comprises:

- for each upper leg switching device and each lower leg switching device, a gate current mirroring circuit on a source branch of the gate driver buffer of said switching device to provide a gate pull down signal upon turning OFF of said switching device, said gate pull down signal being connected to a control line of a gate buffer of a respective further upper leg switching device or further lower leg switching device,

- for each upper leg switching device and each lower leg switching device, a positive gate command connection path from a positive gate command output of a pre-driver, to provide a reset signal for a gate pull down signal of the respective further upper leg switching device, and the respective further lower leg switching device.

Said gate pull-down signal may be output from a MOS transistor whose gate receives a pulse generated from said gate current mirroring circuit, said MOS transistor having or not having a filtering capacitor, between the gate and a source of said MOS transistor.

Said gate pull-down signal may be an output of an SR gate having a current image of the gate current as an input, and is generated from said gate current mirroring circuit.

The control circuit may comprise an inverter gate to provide said reset signal from said positive gate command connection path.

Said reset signal may polarize a gate of said MOS transistor to discharge the gate of said MOS transistor or to discharge the gate of said MOS transistor and said filtering capacitor.

When said gate pull-down signal is an output of an SR gate having as input a current image of the gate current and generated from said gate current mirroring circuit, said reset signal may be connected to a reset input of said SR gate.

The pre-driver may provide a first galvanic insulation, between a controller circuit and the gate buffer.

The control circuit may comprise a second galvanic insulation between the gate current mirroring circuit and the gate pull down signal circuit.

Said second galvanic insulation may be provided with a transformer in a collector branch of a current mirror transistor.

Said second galvanic insulation may also be provided with a photo-coupler in the collector branch of a current mirror transistor or another insulating component.

The present disclosure also pertains to a converter or an inverter comprising a current source, a controller, at least two half-bridges provided with upper legs switching devices and lower legs switching devices, each of said switching devices being controlled by said controller through gate drivers, wherein said gate drivers comprise control circuits according to any one of the preceding claims.

The present disclosure further pertains to a method for switching power switch devices of legs of half-bridges of a current source converter with reduced overlapping time, where ON, OFF states of said power switch devices of said legs are driven by a controller, through gate drivers provided with gate buffers, characterized in that during a switching transition between a first upper leg power switch device, and a second upper leg power switch device, or a switching transition between a first lower leg power switch device and a second lower leg power switch device, said switching transitions being initiated by a controller through said gate drivers of the power switch devices, the method comprising: using a mirrored gate current, or a voltage proportional to such mirrored gate current, from one of said power switch devices having an OFF state to ON state transition, in order to commutate the other of said switch devices from a ON state to an OFF state, prior to a gate pulse generated from said controller, to a gate driver of said second switch device provided for commutating said other of said switch devices, from said ON state to said OFF state.

[0005]

The method may comprise providing a gate pull down pulse signal generated from said mirrored gate current, or a voltage proportional to such mirrored gate current, said gate pull down pulse signal being used for commutating the other of said switch devices from said ON state to said OFF state.

[0006]

Said mirrored gate current may be a mirrored source current of gate buffers driving said power switch devices.

[0007]

The method may comprise latching said mirrored gate current or voltage proportional to said mirrored gate current to provide said gate pull down pulse signal and resetting said gate pull down pulse signal at an end of said transition.

[EFFECTS OF THE INVENTION]

[0008]

An object of the present disclosure is to provide a switching system where overlapping between conducting to non-conducting, and non-conducting to conducting power semiconductor switches in a current fed converter is reduced, without the need to reduce the overlapping calculated by a controller of the converter.

[Brief Description of Drawings]

[0009]

Other features, details and advantages will be shown in the following detailed description and on the figures, on which:

FIG. 1 is a schematic view of a single phase current source inverter.

FIG. 2 is a schematic view of an example of control circuit according to an embodiment of the present disclosure.

FIG. 3 shows an example of control circuit of two legs of a converter of the present disclosure.

FIG. 4 shows a schematic view of a traditional three phase current source inverter.

[Description of Embodiments]

[0010]

FIG. 1 is a schematic view of a DC/AC current source converter also called an “inverter”. Such converter comprises a DC source 1, an inductance 2, and two half bridges. A first half-bridge comprises a first upper leg power switch device 11 with IGBT Q1 and a diode 21, and a first lower leg power switch device 12 with IGBT Q2 and diode 22. A second half-bridge includes a second upper leg power switch device 13 with IGBT Q3 and a diode 23, and second lower leg power switch device 14 with IGBT Q4 and diode 24. The IGBT+ diode design shown may be replaced with serial opposite polarity IGBTs having reverse freewheeling diodes, or serial reverse polarity MOSFET having inherent body diode, or with additional freewheeling diodes such as in circle A.

[0011]

The half-bridges of the current source converter are connected to an alternating voltage and current load 4.

[0012]

The switches are controlled through gate drivers. A first gate driver 31 for the first half-bridge first upper leg switch device 11, a second gate driver 32 for the first half-bridge first lower switch device 12, a third gate driver 33 for the second upper leg switch device 13 of the second half bridge, and a fourth gate driver 34 for the second lower leg switch device 14 of the second half-bridge. In such a converter, opposite switching between upper legs power switch devices and opposite switching between lower legs power switch devices is needed to create an alternating current in the alternative load 4. Due to the inductive current source caused by the inductance 2, it is mandatory that an overlapping occurs when a power switch device turns OFF while another turns ON in the upper leg side or in the lower leg side.

[0013]

Starting from the basic schematics of FIG. 1, the present disclosure pertains to a driver circuit that aims to reduce the overlap, in order to reduce losses in the converter, and heat dissipation in the power switches.

[0014]

To achieve this, the driver circuit is designed as in FIG. 2 or in FIG. 3 to add an early turn OFF function of a first switch, upon turning ON of a second switch on the same leg level (upper leg level or lower leg level) in the driver circuit.

[0015]

In FIG. 2 the driver circuit 31 comprises a pre-driver 7 which provides a first galvanic insulation between the controller power supply  $V_{DD}$ ,  $V_{SS}$  and the power switch X gate buffer circuit 6 having a  $V_{DDx}$  and  $V_{SSx}$  power supply.

[0016]

In the presented circuit, a gate current mirroring circuit 51 having transistors T3 and T4 is positioned in the source branch of the push pull buffer 6, having transistors T1 and T2.

[0017]

The image of the source current of the buffer 6 is taken at the junction of the resistor  $R_{MON}$  and the collector of transistor T5.

[0018]

This source current corresponds to the gate current of the power switch device X during the OFF to ON transition thereof.

[0019]

In FIG. 2, a second galvanic insulation 52 made with an photo-coupler 52a transfers the signal extracted from the current mirror to an SR gate which outputs a signal  $Gp_y$  used as discussed hereunder to turn off a power switch device Y, as seen in FIG. 3, prior to reception of the controller switch closing signal I-.

[0020]

On the other side, the same driver circuit is realized for the power switch Y, and the power device Y provides in turn a  $Gp_x$  signal which will turn the power switch device X to OFF, prior to reception of the controller signal during an OFF to ON transition of the power switch device Y.

[0021]

The aforementioned may be seen in FIG. 3 where the complete driver circuit for two upper or lower legs of a converter is shown.

[0022]

In FIG. 3 the SR gates are replaced by MOS transistors Q1x, Q2x in the driver circuit of the gate Y of power switch Y, and Q1y, Q2y in the driver circuit of the gate X of power switch X.

[0023]

These MOS transistors receive an image of the gate driver current through transformers  $TR_x$  and  $TR_y$  which provide the second galvanic insulation in replacement of the photo-couplers 52a.

[0024]

Here the image from the gate driver current of switch Y goes through a Schottky diode D1x, and on to the gate of Q2x to provide the signal  $GP_x$  that pulls down the gate buffer of switch X. The image from the gate driver current of switch X goes through a Schottky

diode D1y and on to the gate of Q2y to provide the signal GPy that pulls down the gate buffer of switch Y.

[0025]

On the other side, the O+ signal to turn on switch Y provides the signal RSTy through an inverter 71, such signal being provided so as to pull down the gate of MOS transistor Q2y through MOS transistor Q1y. The O+ signal to turn on switch X provides the signal RSTx through a further inverter 71, such signal being provided so as to pull down the gate of MOS transistor Q2x through MOS transistor Q1x.

[0026]

This second realization mode only based on transistors and passive components is simpler to embed in a power module, than logic components as in FIG. 2, and provides the same function.

[0027]

The disclosed circuits provide a simple method to reduce the ON overlap between switches without creating open circuit conditions, since the method is based on detection of the OFF to ON transition of a first switch to anticipate the ON to OFF transition of the second switch, which is controlled in a complementary way from the first switch.

[0028]

The present invention is not limited to the circuits described herewith, and as an example, the control circuit described may be adapted to a three-phase output current source converter as per FIG. 4, with the use of adapted logic circuits and insulation to combine the gate command signals and gate pull down detection signals of three half-bridges. The present disclosure may also be applied to DC/AC converters, along with AC/DC converters, with the source and load being reversed.

[0029]

In addition, the present invention may be combined with a circuit designed to protect the current source converter, such circuit using a sink current mirroring circuit, similar to the source current mirror depicted.

[Reference Signs List]

[0030]

2...Inductance 6...Buffer 7...Pre-driver 11, 13...Upper Switching Device 12,  
14...Lower Switching Device 40...Controller 51...Gate Current Mirroring Circuit  
52...Second Galvanic Insulation 52a...Photo-Coupler 53...SR Gate 71...Inverter  
Gate Cl...Control Line C2x, C2y...Filtering Capacitor G+...Positive Gate  
Command Connection Path Gpx, Gpy...Gate Pull Down Signal Q2x, Q2y...MOS  
Transistor RSTx, RSTy...Reset Signal Q1x, Q1y...MOS Transistor TRx,  
TRy...Transformer T5x, T5y...Current Mirror Transistor

## [CLAIMS]

## [Claim 1]

A control circuit for a current source converter, having

a current generator comprising an inductance, and having

two or more half bridges, each half bridge having an upper leg provided with an upper switching device, and a lower leg provided with a lower switching device, said upper legs switching devices and said lower legs switching devices being controlled by a controller, to provide an overlap between an upper leg turning off switching device, and an upper leg turning on switching device, and to provide an overlap between a lower leg turning on switching device, and a lower leg turning off switching device, through gate pull up and gate pull down pulse signals to gate driver buffers of said switching devices, characterized in that said gate driver circuit comprises:

- for each upper leg switching device and each lower leg switching device, a gate current mirroring circuit on a source branch of the gate driver buffer of said switching device, to provide a gate pull down signal upon turning OFF of said switching device, said gate pull down signal being connected to a control line of a gate buffer of a respective further upper leg switching device, or further lower leg switching device,
- for each upper leg switching device and each lower leg switching device , a positive gate command connection path from a positive gate command output of a pre-driver, to provide a reset signal for a gate pull down signal of the respective further upper leg switching device, and the respective further lower leg switching device.

## [Claim 2]

The control circuit according to claim 1, wherein

said gate pull-down signal is output from a MOS transistor, whose gate receives a pulse generated from said gate current mirroring circuit, said MOS transistor having or not having a filtering capacitor, between the gate and a source of said MOS transistor.

## [Claim 3]

The control circuit according to claim 1, wherein

said gate pull-down signal is an output of an SR gate, having a current image of the gate current as an input, and is generated from said gate current mirroring circuit.

[Claim 4]

The control circuit according to claim 1, further comprising:

an inverter gate to provide said reset signal, from said positive gate command connection path.

[Claim 5]

The control circuit according to claims 2 and 4, wherein

said reset signal polarizes the gate of said MOS transistor to discharge from the gate of said MOS transistor, or to discharge from the gate of said MOS transistor and said filtering capacitor.

[Claim 6]

The control circuit according to claims 3 and 4, wherein

said reset signal is connected to a reset input of said SR gate.

[Claim 7]

The control circuit according to any one claims 1 to 6, wherein

the pre-driver provides a first galvanic insulation, between a controller circuit and the gate buffer.

[Claim 8]

The control circuit according to any one of claims 1 to 7 further comprising:

a second galvanic insulation between the gate current mirroring circuit and the gate pull down signal circuit.

[Claim 9]

The control circuit according to claim 8, wherein

said second galvanic insulation is provided with a transformer in a collector branch of a current mirror transistor.

[Claim 10]

The control circuit according to claim 8, wherein

said second galvanic insulation is provided with a photo-coupler in the collector branch of a current mirror transistor.

[Claim 11]

A converter, such as an inverter comprising:

a current source,

a controller,

at least two half-bridges provided with upper legs switching devices, and lower legs switching devices, each of said switching devices being controlled by said controller through gate drivers, wherein

said gate drivers comprise control circuits according to any one of claims 1 to 10.

[Claim 12]

A Method for switching power switch devices of legs of half-bridges of a current source converter with reduced overlapping time, where ON, OFF states of said power switch devices of said legs are driven by a controller, through gate drivers provided with gate buffers, characterized in that

during a switching transition between a first upper leg power switch device, and a second upper leg power switch device, or a switching transition between a first lower leg power switch device and a second lower leg power switch device, said switching transitions being initiated by said controller through said gate drivers of the power switch devices, the method comprising:

using a mirrored gate current, or a voltage proportional to such mirrored gate current, from one of said power switch devices having an OFF state to ON state transition, in order to commutate the other of said switch devices from a ON state to an OFF state, prior to a gate pulse generated from said controller, to a gate driver of said second switch device provided for commutating said other of said switch devices, from said ON state to said OFF state.

[Claim 13]

The method according to claim 12 further comprising:

providing a gate pull down pulse signal generated from said mirrored gate current,

or

a voltage proportional to such mirrored gate current, said gate pull down pulse signal being used for commutating the other of said switch devices from said ON state to said OFF state.

[Claim 14]

The method according to claim 12 or 13, wherein

said mirrored gate current is a mirrored source current of gate buffers driving said power switch devices.

[Claim 15]

The method according to claim 13, further comprising:

latching said mirrored gate current or voltage proportional to said mirrored gate current, to provide said gate pull down pulse signal and resetting said gate pull down pulse signal at an end of said transition.

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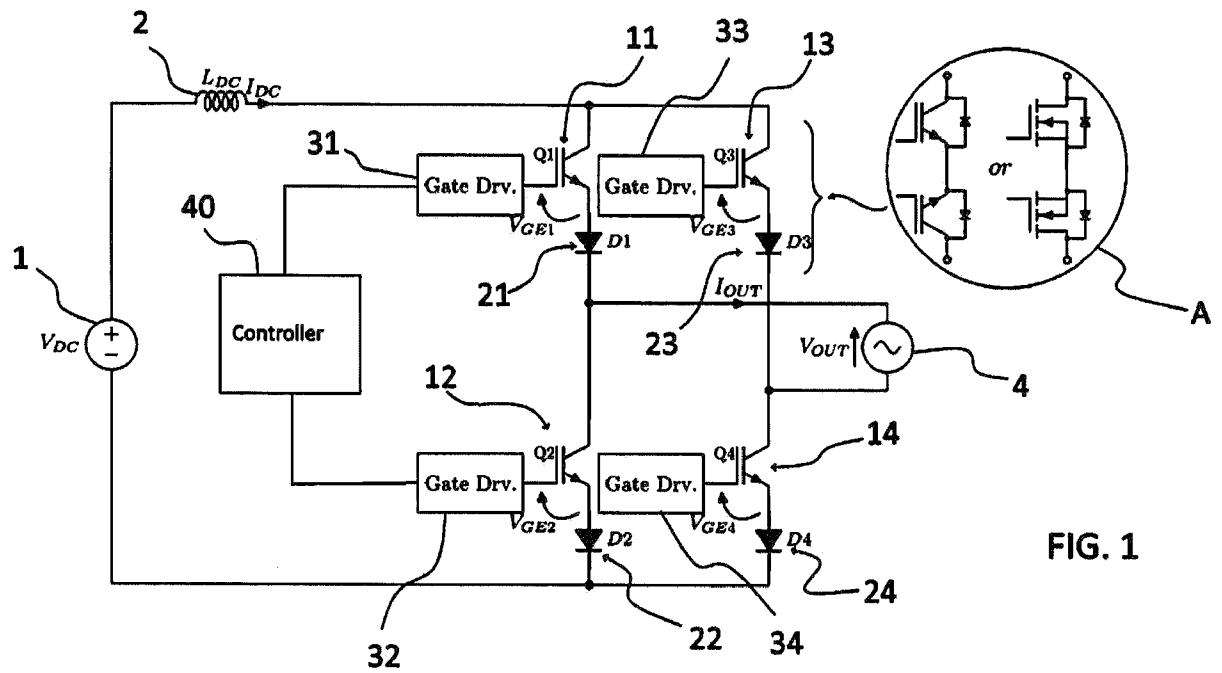


FIG. 1

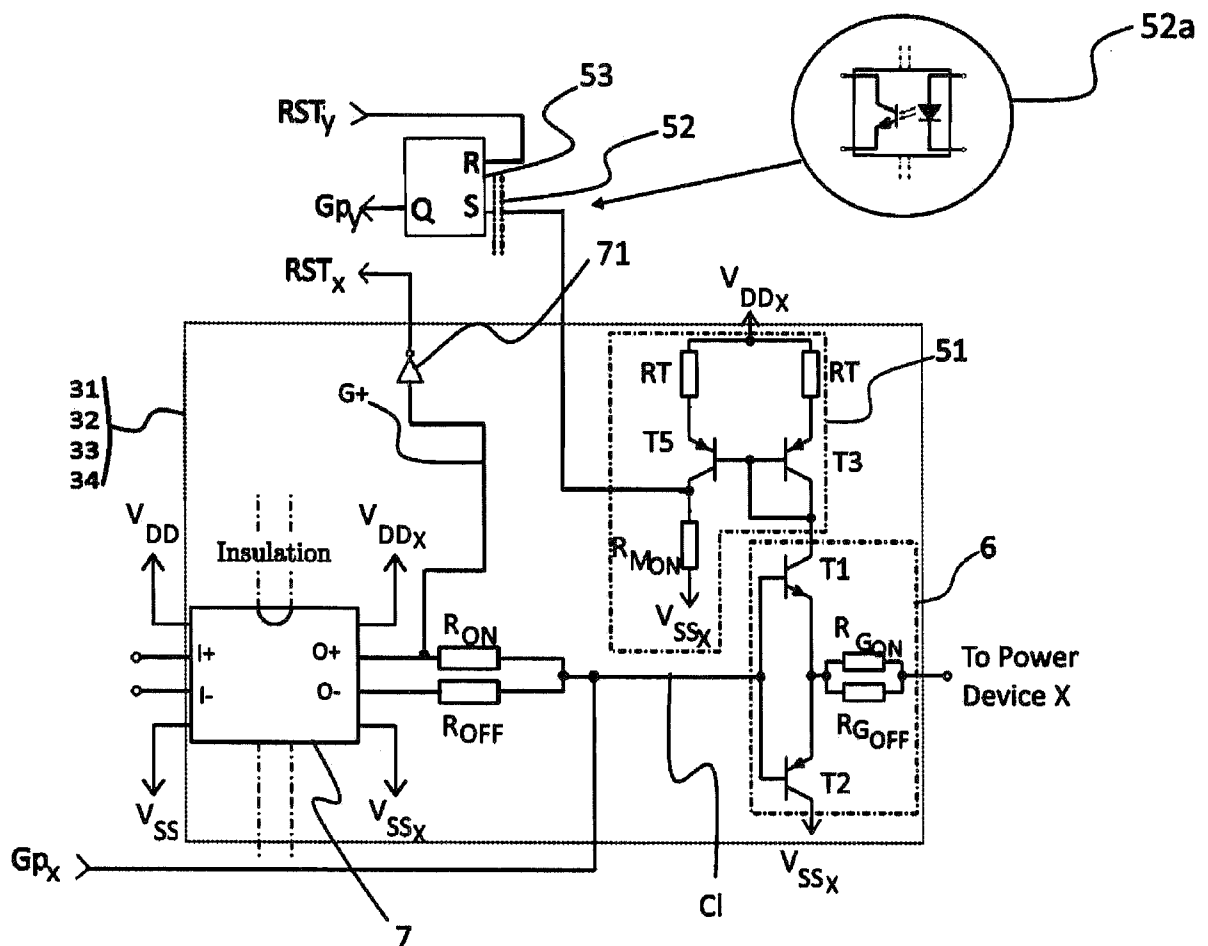
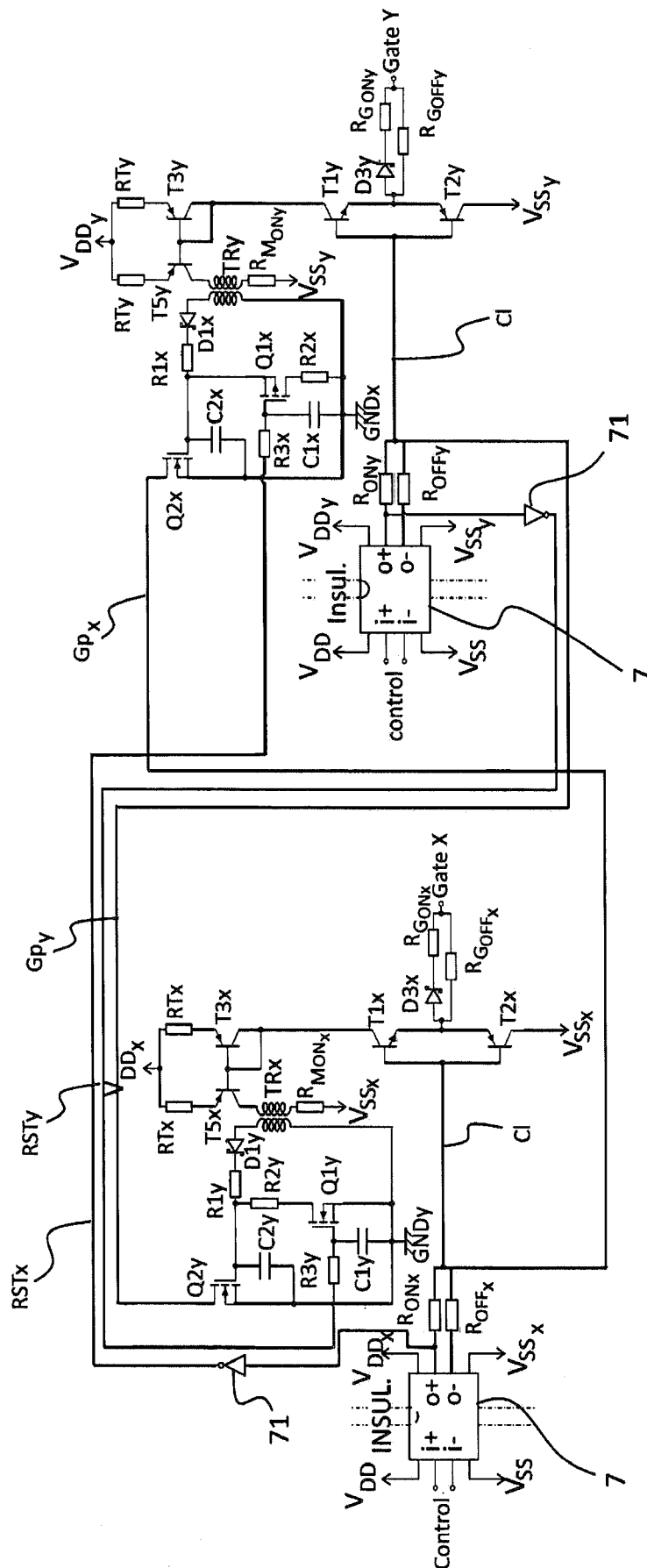


FIG. 2



**FIG. 3**

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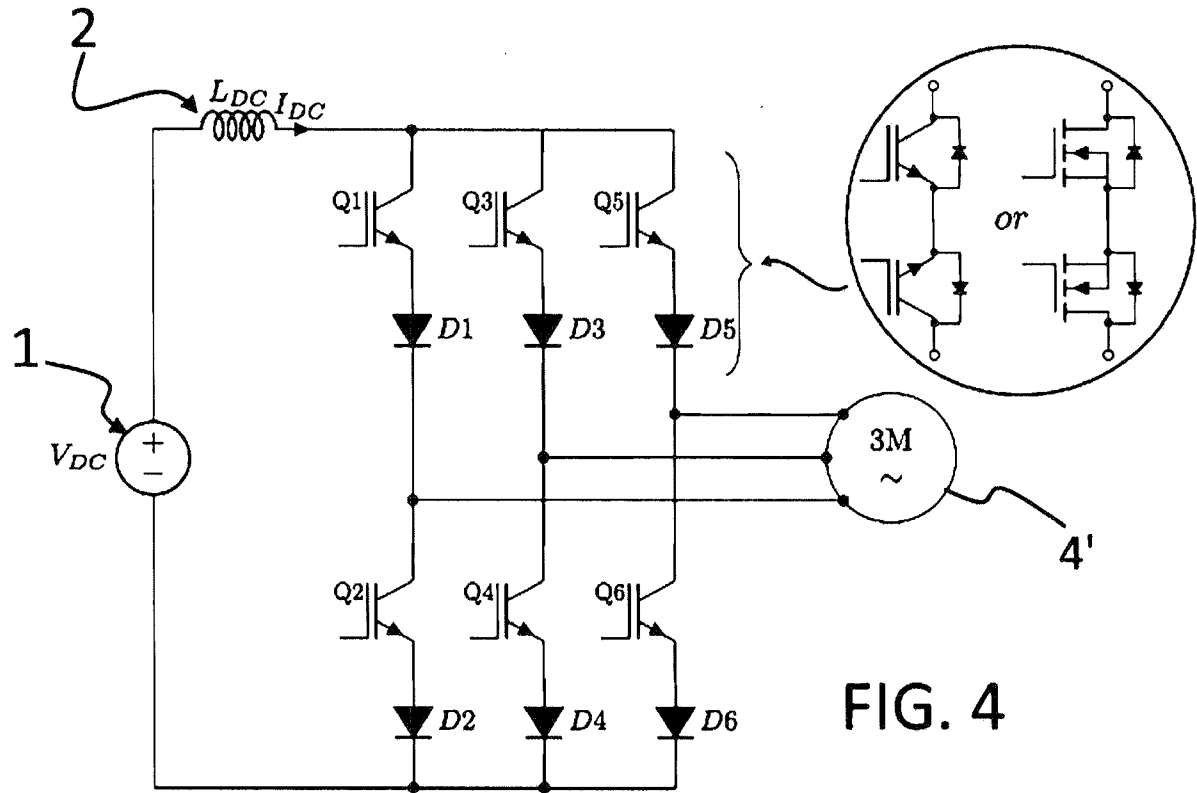


FIG. 4

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/JP2024/080103

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| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>INV. H02M1/08 H03K17/18 H03K17/691 H03K17/78<br>ADD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| According to International Patent Classification (IPC) or to both national classification and IPC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| <b>B. FIELDS SEARCHED</b><br>Minimum documentation searched (classification system followed by classification symbols)<br>H02M H03K<br><br>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched<br><br>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)<br><br>EPO-Internal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| Category*                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                                  | Relevant to claim No.                                                |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | CN 114 221 567 A (DONGGUAN DUAL FLAT POWER TECH LIMITED COMPANY)<br>22 March 2022 (2022-03-22)<br>the whole document<br>-----                                                                                                                                                                                                                                                                                       | 1 - 15                                                               |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | BEN GUO ET AL: "Compensation of input current distortion in three-phase buck rectifiers",<br>APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION (APEC), 2013 TWENTY-EIGHTH ANNUAL IEEE, IEEE,<br>17 March 2013 (2013-03-17), pages 930-938, XP032410447,<br>DOI: 10.1109/APEC.2013.6520325<br>ISBN: 978-1-4673-4354-1<br>paragraphs [B.ModifiedPulse] -<br>[basedCompensationMethod]; figures 1, 3,<br>11<br>----- | 1 - 15                                                               |
| <input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| <p>* Special categories of cited documents :</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&amp;" document member of the same patent family</p> |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                      |
| Date of the actual completion of the international search<br><br>16 September 2024                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                     | Date of mailing of the international search report<br><br>04/10/2024 |
| Name and mailing address of the ISA/<br>European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                     | Authorized officer<br><br>Fermentel, Thomas                          |

## INTERNATIONAL SEARCH REPORT

### Information on patent family members

International application No

PCT/JP2024/080103

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
|-------------------------------------------|---------------------|----------------------------|---------------------|
| CN 114221567                              | A                   | 22-03-2022                 | NONE                |
| -----                                     |                     |                            |                     |