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Saito et al.

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[45] **May 14, 1974**

[54] **KEYBOARD OPERATED PATTERN GENERATING DEVICE**

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[73] Assignee: **Matsushita Electric Industrial Co. Ltd.,** Osaka, Japan

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[21] Appl. No.: **316,537**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 46,041, June 15, 1970, abandoned.

[30] **Foreign Application Priority Data**

June 21, 1969 Japan 44-49169

[52] **U.S. Cl.** ..... **340/172.5,** 340/324 A, 340/324 AD

[51] **Int. Cl.** **G06f 3/14,** G06f 3/06, G06f 3/02

[58] **Field of Search** ..... 340/172.5, 324 A, 324 AD, 340/365 R; 35/5; 40/52 R, 52 A

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Primary Examiner—Paul J. Henon
Assistant Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Stevens, Davis, Miller & Mosher

[57] **ABSTRACT**

A pattern generating device for displaying figures such as letters, pictures and the like on a display means such as a cathode ray tube (CRT) and the like by arranging picture elements in a mosaic. The device is adapted to decompose a figure to be displayed into picture elements of red, green and blue colors by an equal number of switches respectively corresponding to the picture elements so that the resulting component figures may be stored in respectively corresponding memory means, and to scan the stored figures with a scanning circuit to reproduce them on a color CRT for monitoring so that the figures may be recorded in a recording means after errors have been corrected. By employing this device, figures consisting of a large number of picture elements can be obtained in a short time, and a moving picture of a mosaic pattern can be easily made.

9 Claims, 26 Drawing Figures

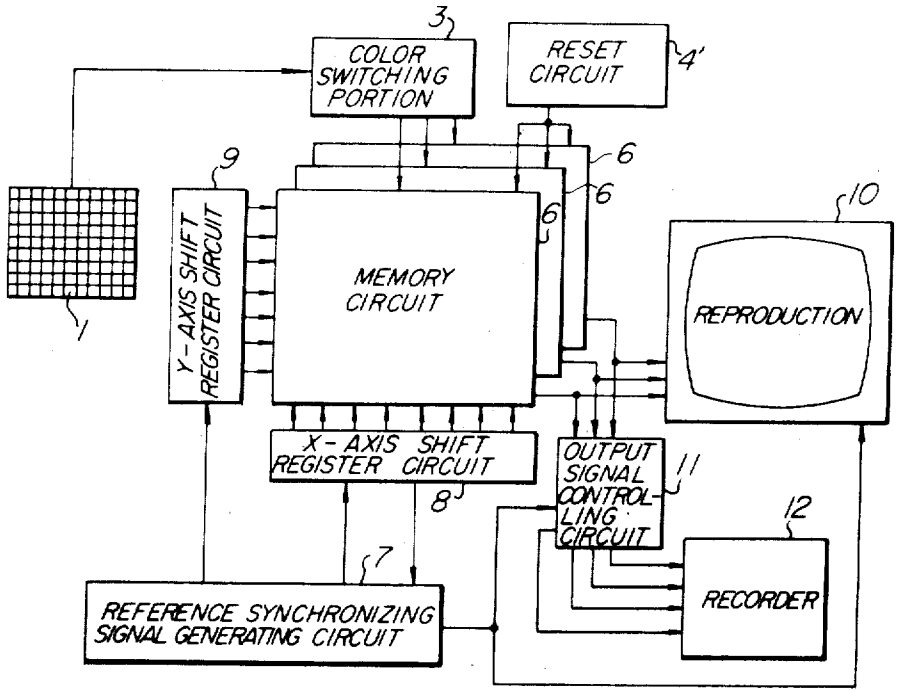


FIG. 1

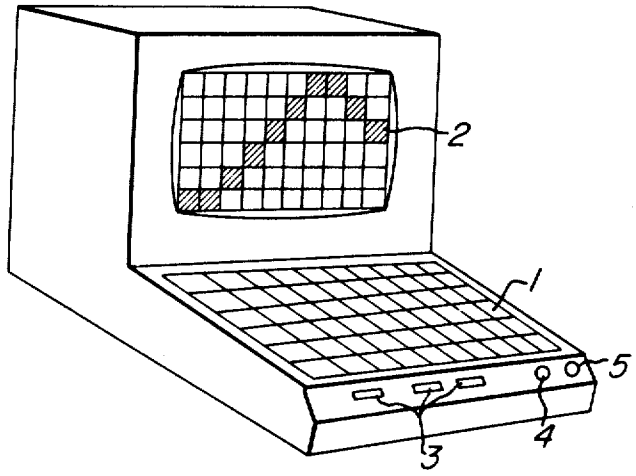

2
1
5
3
4

FIG. 2

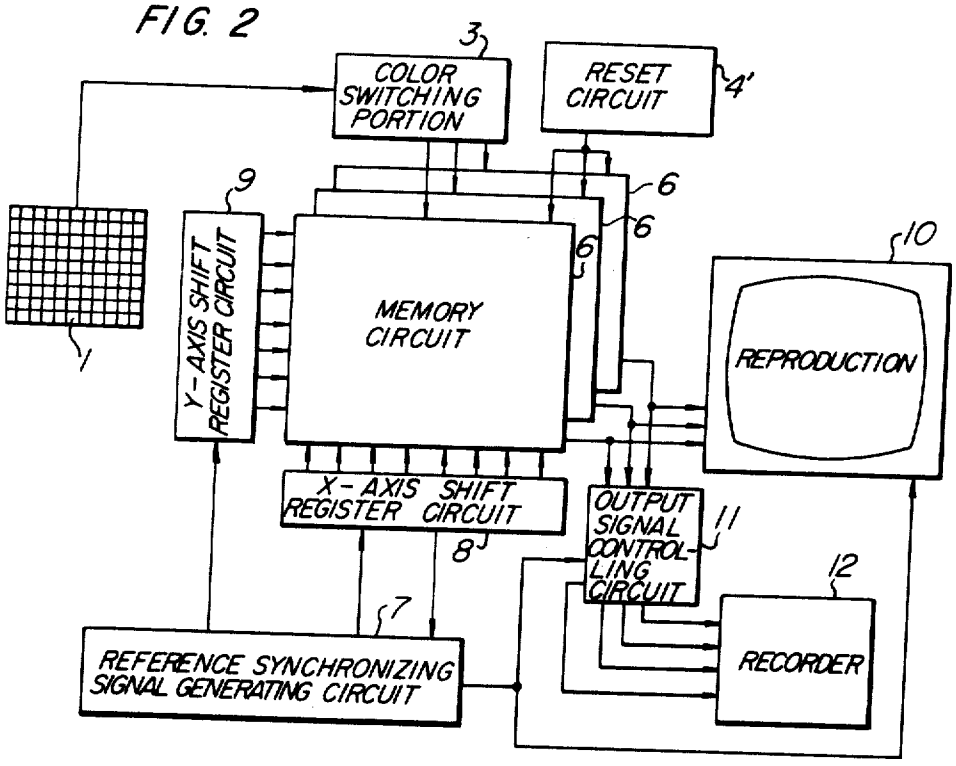

3
COLOR SWITCHING PORTION
RESET CIRCUIT
4'
9
Y-AXIS SHIFT REGISTER CIRCUIT
MEMORY CIRCUIT
6
6
6
10
REPRODUCTION
1
X-AXIS SHIFT REGISTER CIRCUIT
8
OUTPUT SIGNAL CONTROLLING CIRCUIT
11
12
7
REFERENCE SYNCHRONIZING SIGNAL GENERATING CIRCUIT
RECORDER

FIG. 3

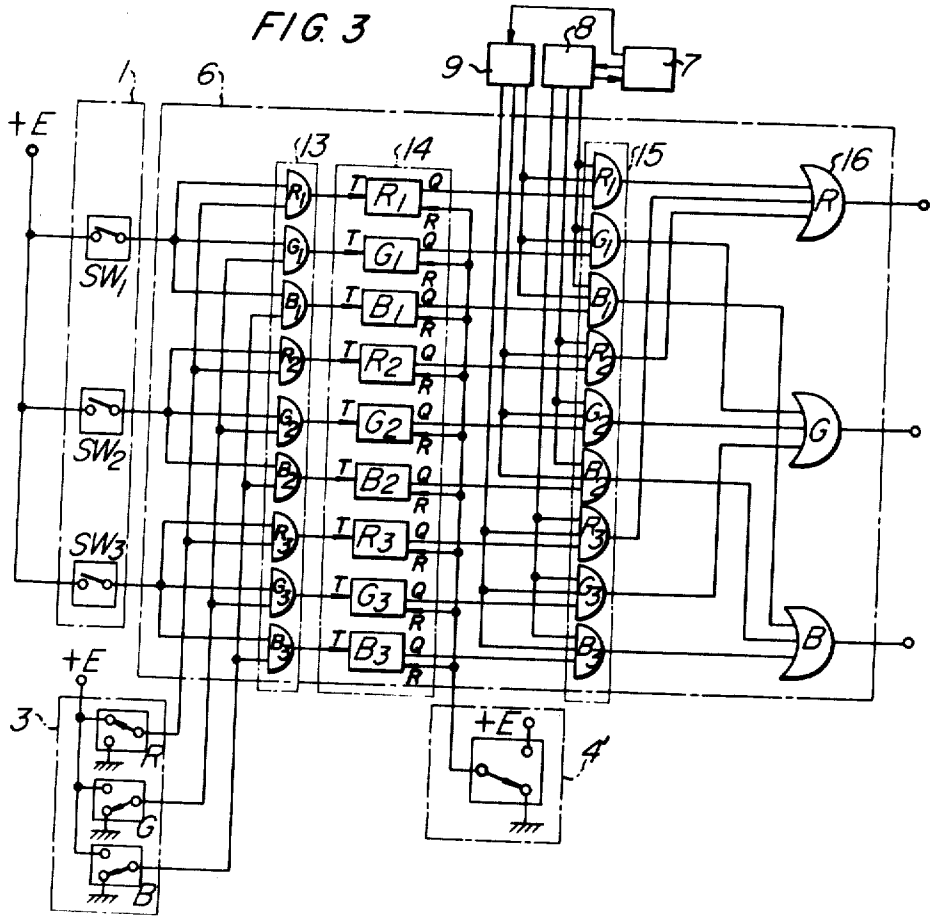


FIG. 4a

FIG. 4b

FIG. 4c

FIG. 4d

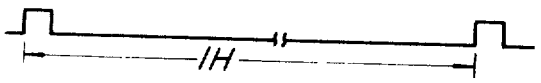


FIG. 4e

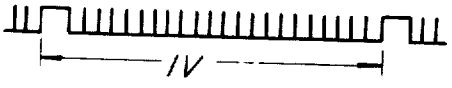


FIG. 5a

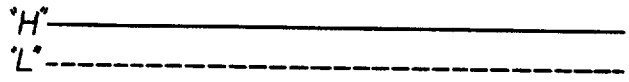


FIG. 5b



FIG. 5c



FIG. 5d



FIG. 6

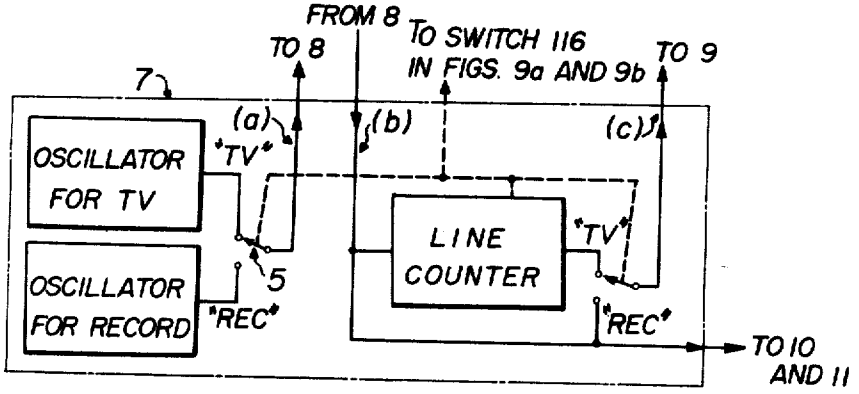


FIG. 7a



FIG. 7b

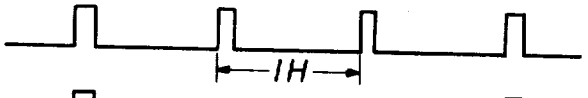


FIG. 7c

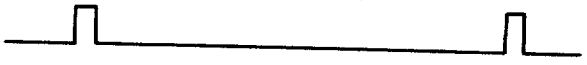


FIG. 8a



FIG. 8b

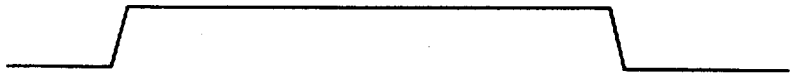


FIG. 8c



FIG. 8d



FIG. 8e

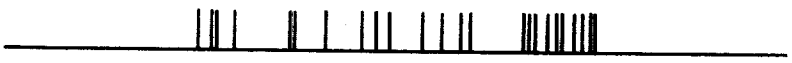


FIG. 8f



FIG. 8g

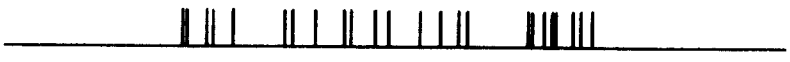


FIG. 8h



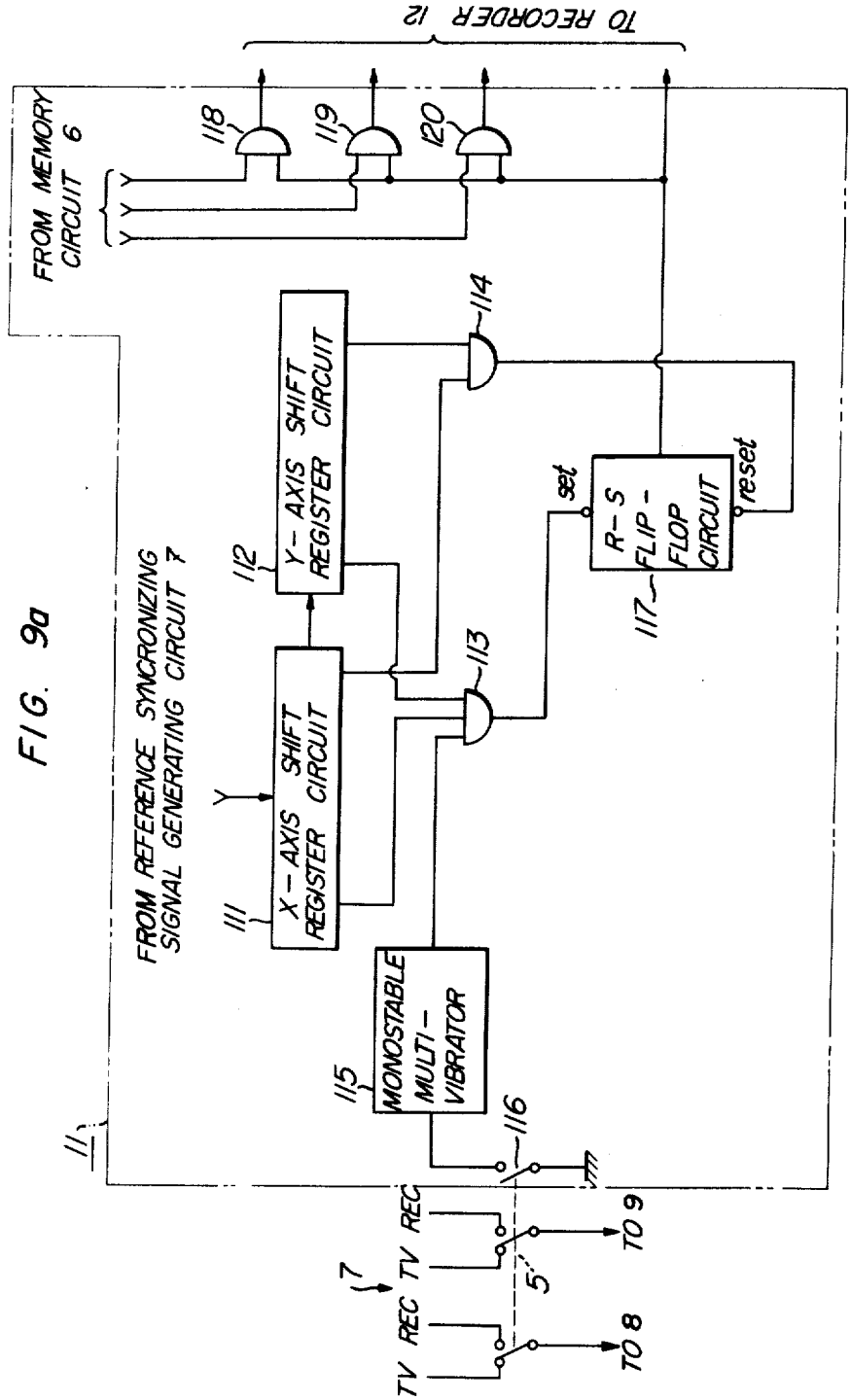
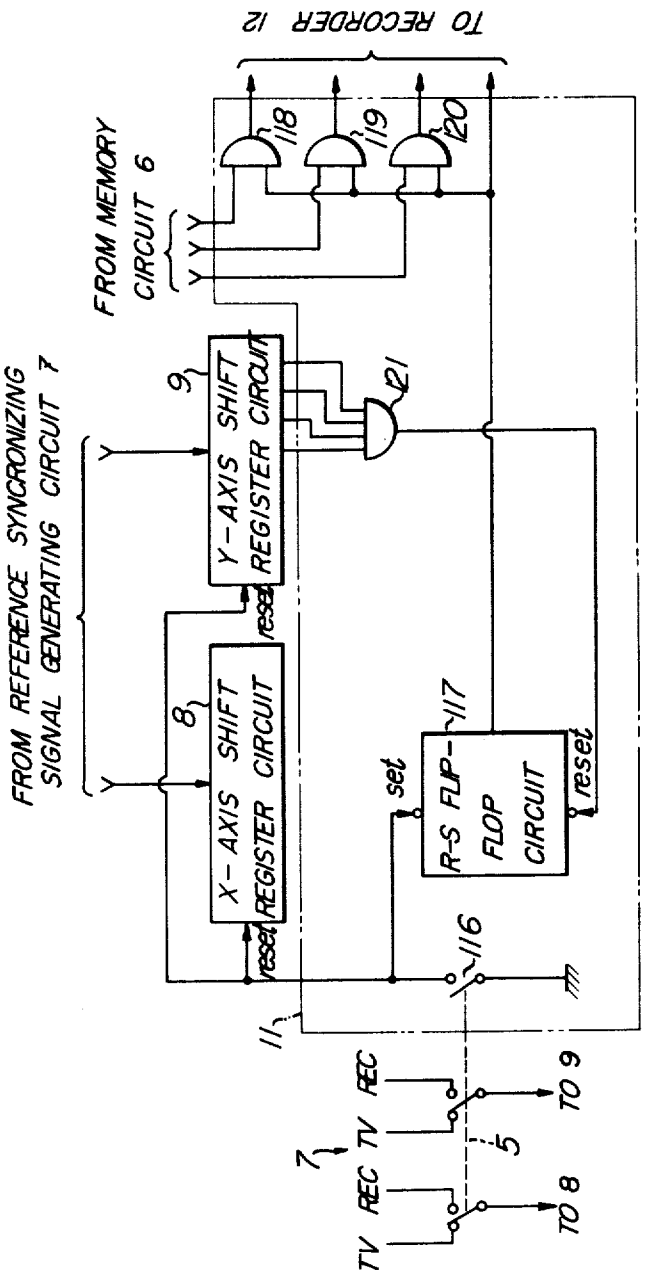

TO RECORDER 12
FROM MEMORY CIRCUIT 6
118
119
120
Y
Y
Y
114
Y- AXIS SHIFT REGISTER CIRCUIT
112
set
R- S FLIP - FLOP CIRCUIT
reset
117
FROM REFERENCE SYNCRONIZING SIGNAL GENERATING CIRCUIT 7
113
Y
X- AXIS SHIFT REGISTER CIRCUIT
111
MONOSTABLE MULTI - VIBRATOR
115
116
11
7
TV REC
TV REC
5
TO 9
TO 8

FIG. 9a

FIG. 9b


TO RECORDER 12
FROM MEMORY CIRCUIT 6
FROM REFERENCE SYNCRONIZING SIGNAL GENERATING CIRCUIT 7
Y-AXIS SHIFT REGISTER CIRCUIT
X-AXIS SHIFT REGISTER CIRCUIT
R-S FLIP-FLOP CIRCUIT
set
reset
REC
TV
TO 9
TO 8
118
119
120
121
116
117
11
9
8
7
5

KEYBOARD OPERATED PATTERN GENERATING DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of application Ser. No. 46,041, filed June 15, 1970, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a mosaic pattern generating device for generating colored mosaic patterns.

The system of this invention is adapted for making a recorded tape for a large display system, such as the system which is described in U. S. Pat. application Ser. No. 842,501, now U. S. Pat. No. 3,611,024, issued Oct. 5, 1971.

SUMMARY OF THE INVENTION

According to this invention, a pattern is formed electrically by pushing switching buttons rather than by picking out with an image pickup tube a painted picture, for example, and the electrically formed pattern is turned into and extracted as electrical signals. Further, when another pattern similar to an original one is required to be formed, the new pattern can be made by modifying only a part of the original pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a perspective view of a device according to this invention.

FIG. 2 shows the block diagram of the device shown in FIG. 1.

FIG. 3 shows the circuit diagram of an example of the device utilizing this invention.

FIGS. 4*a* to 4*e* show the waveforms of the output signals employed in this invention.

FIGS. 5*a* to 5*d* show the waveforms of the output signals of the shift registers and the memory circuit.

FIG. 6 shows the structure of a reference synchronizing signal generating circuit.

FIGS. 7*a* to 7*c* show the waveforms of the output signals of the reference synchronizing signal generating circuit.

FIGS. 8*a* to 8*h* show the waveforms of the output signals of the output signal controlling circuit.

FIG. 9*a* schematically shows the construction of the output signal controlling circuit in FIG. 2.

FIG. 9*b* shows a modification of the construction of the output signal controlling circuit shown in FIG. 9*a*.

In the drawings, like reference numerals refer to like parts.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, referring to FIG. 1, 1 is a keyboard comprising a large number of switching buttons which are arranged to correspond to the picture elements of a pattern to be formed and are adapted to cause the pattern to be formed by depressing them. The buttons are normally opened and are closed only when they are depressed. Numeral 2 is a monitoring panel for displaying the pattern thus formed, which comprises the face of a color CRT. When a pattern is desired to be formed, the switching buttons on the keyboard 1 may be depressed by an operator watching the monitoring panel 2. A color switching portion 3 consists of red, green and blue switches which can produce eight colors as a result of the combined operation of the three switches. A clearing button 4 clears the pattern formed on the monitoring panel 2. By depressing an image transcription button 5 output signals are transmitted to a recording device 12, as shown in FIG. 2.

FIG. 2 illustrates the whole block diagram of the device shown in FIG. 1, in which the parts identical to those in FIG. 1 are indicated with identical numerals.

The keyboard and the color switching portion 3 have been described above. A memory circuit 6 comprises memory elements, such as flip-flops or core-memories, each thereof corresponding to each of the switches on the keyboard 1, and the memory circuit 6 stores the signals from the respective switches. Further, the memory circuit 6 comprises three circuits of identical construction each of which stores signals each thereof representing one of red, green and blue colors.

A reference synchronizing signal generating circuit 7 is composed of two oscillators, a line counter and the image transcription button 5. The two oscillators are for TV display and for recording, respectively. The line counter of the circuit 7 reads out signals on the same horizontal line repeatedly in order to display figures on the CRT panel in a mosaic pattern. This line counter of the circuit 7 is not used during recording (because it is wasteful to record repeatedly the signals on the same horizontal line). The arrangement of the line counter is shown in FIG. 6. The button 5 is normally placed on the "TV" position, but switched to the "REC" position when it is depressed, and is automatically restored to the "TV" position when the termination of display of one complete figure is sensed by the line counter. By such a switching operation, the frequency of the reference clock signal is changed and the operating condition is concurrently changed from the case where the signals pass through the line counter to the case where the same do not pass through the line counter, or vice versa. X-axis and Y-axis shift register circuits 8 and 9 actuate the memory circuit 6 with reference synchronizing signals generated by the reference synchronizing signal generating circuit 7, where the X-axis refers to a horizontal scanning direction in the memory circuit 6 having a two-dimensional arrangement, while the Y-axis refers to a vertical scanning direction. Shift registers 8 and 9 act as line selectors. Their output lines sequentially become high in level one at a time without fail upon application of an input clock pulse. A pulse is generated at every one cycle of the register 8 and is supplied to the line counter of the circuit 7. The point where the signals from registers 8 and 9 occur concurrently is a single point on the memory plane, which point reads out the memory sequentially.

A reset circuit 4' including the clearing button 4 shown in FIG. 1 is a circuit for clearing all the memories stored in the memory circuit 6. A monitoring portion 10 comprises a color CRT. The monitor 10 employs an ordinary scanning system of a color television. However, the color signals of R, G and B are supplied as input signals independently of each other. Further, the synchronizing signal is also supplied independently. This is a so-called monitoring television.

One form of the arrangement of an output signal controlling circuit 11 is shown in FIG. 9*a*. This circuit

11 comprises two shift register circuits 111 and 112, a monostable circuit 115, R-S flip-flop circuit 117, five AND gates 113, 114, 118, 119 and 120, and a recording switch 116. The recording switch 116 is opened and closed in interlinkage with the image transcription button 5 shown in FIGS. 1 and 6. The shift register circuits 111 and 112 are respectively identical in construction with the shift register circuits 8 and 9 shown in FIGS. 2 and 3. Their first stage output signals are supplied to the AND gate circuit 113 and their last stage output signals are supplied to the AND gate circuit 114. The output signal from the monostable multivibrator circuit 115 is also applied to the input terminal of the AND gate 113. When the recording switch 116 is closed, the monostable multivibrator circuit 115 produces an output and maintains it during a period of time in which the memory circuit 6 scanned for a single frame. The R-S flip-flop circuit 117 receives the output signal of the AND gate circuit 113 at its set terminal and the output signal of the AND gate circuit 114 at its reset terminal. The output signal of the R-S flip-flop circuit 117 is applied to one of the two input terminals of each of the AND gate circuits 118, 119 and 120 so that it is used by the gate circuits 118, 119 and 120 to control the gating of the color signals from the memory circuit 6, and also it is used to control the recording operation of the recording device 12.

The output signal controlling circuit 11 operates as follows. After the pattern stored in the memory circuit 6 is checked with the monitoring portion 10 including a color CRT and it is assured that there is contained no error in the pattern, the recording switch 116 is closed. This triggers the monostable multivibrator circuit 115 causing it to produce an output signal. If, at that time, the scanning of the memory circuit 6 by the shift register circuits 8 and 9 is under way, no set pulse is supplied from the AND gate circuit 113 to the R-S flip-flop circuit 117. When the memory circuit 6 is read out starting at the first memory position for a frame, the AND gate circuit 113 receives input signals to all of the input terminals thereof and consequently the AND gate circuit 113 applies a set pulse to the R-S flip-flop circuit 117 to put it in its "set" state. Upon receiving an output signal from the R-S flip-flop circuit 117, the AND gate circuits 118, 119 and 120 supply three color signals read from the memory circuit 6 to the recorder 12. Simultaneously, by the output signal of the R-S flip-flop circuit 117 the recorder 12 is caused to store the three color signals supplied from the AND gate circuits 118, 119 and 120. When the reading-out operation of the memory circuit 6 is performed successively and eventually comes to the final memory position for a frame, the output signals of the shift register circuits 111 and 112 are simultaneously applied to the input terminals of the AND gate circuit 114, thereby supplying a reset pulse to the R-S flip-flop circuit 117. When this occurs, the AND gate circuits 118, 119 and 120 are closed to block the passage of color signals, and the recording operation of the recorder 12 is simultaneously stopped. In this manner, one frame of the pattern stored in the memory circuit 6 is recorded.

FIG. 9*b* shows a modified form of the output signal controlling circuit 11 shown in FIG. 9*a*, in which the X-axis shift register circuit 8 and the Y-axis shift register circuit 9 are used in common in place of the shift register circuits 111 and 112. The modified circuit in FIG. 9*b* operates in the following manner. When the recording switch 116 is closed, the shift register circuits 8 and 9 are reset and the R-S flip-flop circuit 117 is also set. Consequently, the memory circuit 6 is scanned by the shift register circuits 8 and 9 starting from the beginning of a frame. In response to this, the recorder 12 starts its recording operation and successively records three color signals from the AND gate circuits 118, 119 and 120. When the scanning of the memory circuit 6 reaches the end of a frame, the output signals of the Y-axis shift register circuit 9 causes a reset pulse to be produced by an AND gate circuit 121 to thereby reset the R-S flip-flop circuit 117. This resetting of the R-S flip-flop circuit 117 causes the recorder 12 to stop its recording operation and closes the AND gate circuits 118, 119 and 120.

When this circuit construction is employed, the reproduced picture in the monitoring portion 10 is subjected to disturbance only when the recording switch 116 is operated. Thus, according to the occurrence of such "disturbance," it is possible to decide whether a recording operation has been started normally. Thus, while the memory circuit 6 is repeatedly scanned for display on the CRT 10, the control circuit 11 takes out one frame from the repetitive signals for magnetic tape recording, and produces at the output one of the repetitive signals, corresponding to an interval from one vertical synchronizing signal to the succeeding vertical synchronizing signal. The outside recording device 12 records video signals representing every pattern in synchronized relation to its feeding rate so that every pattern may be recorded continuously. A magnetic recording and reproducing device or a tape punch device may be employed as the recorder.

A data recorder employing a multichannel head is suitable for this recorder. The above-mentioned signals are recorded per one figure in parallel with one another on this recorder. The tape thus prepared is reproduced by a tape player for use in a separate large-sized display system. The details of the separate large display system are described in U. S. Pat. No 3,611,024.

The details of the color switching portion 3 and the memory circuit 6 are described with reference to FIG. 3. Memory circuit 6 is composed of AND gates 13, flip-flop circuits 14, AND gates 15 and OR gates 16. The AND gates 13 are gages for selecting a color. By the AND operation on the outputs of 1 and 3, the output pulse of 1 is supplied only to the trigger terminal of the flip-flop circuit for a color selected by 3, and therefore, only the selected color is stored at the selected position. Numeral 15 designates AND gate circuits for reading out the stored signals. The outputs of the shift registers 8 and 9 sequentially scan the memory circuit 6 to read out stored color information.

FIG. 3 shows the state where red is selected by the switch R of the color switching portion 3. When SW_1 on the keyboard 1 is depressed, for example, the pulses pass through only the AND gate 13 R_1 and are applied to the trigger input of the flip-flop circuit 14 R_1. Namely, the output Q of 14 R_1 becomes high, but the AND gates 13 G_1, 13 B_1 are shut, so that the pulse output of SW_1 does not reach flip-flop circuits 14 G_1 and 14 B_1. Namely, the outputs Q of 14 G_1 and 14 B_1 are low at this time. The high output signal of 14 R_1 passes through a specified AND gate 15 R_1 corresponding to SW_1 and gives an output signal of the memory circuit 6 via the OR gate 16 R. Conversely, if G and B of the color switching portion 3 become high and R is low, the

output of SW_1 is supplied to the trigger terminals of the flip-flops **14** G_1 and **14** B_1. In this case, scanning is effected in the similar way to produce output signals of the memory circuit **6** via the OR gates **16** G and **16** B, respectively and cyan is displayed on the CRT **10.**

The details of the clearing button **4** are also shown in FIG. **3.** The output of the reset circuit **4'** is connected commonly with the reset terminals of the flip-flop circuits **14.** Therefore, upon switching the circuit **4'** on, all of the flip-flop circuits **14** are reset and their outputs become low, so that no output signal is generated from the memory circuit **6** and the monitoring panel becomes black.

The waveforms of signals to and from the AND gates **15** are shown in FIGS. **5***a* to **5***d*. FIG. **5***a* shows the output waveform of the flip-flop **14** R_1 when the output level is high ("") FIG. **5***b* shows the output waveform of the register **8**; FIG. **5***c* shows the output waveform of the register **9**; and FIG. **5***d* shows the output waveform of the AND gate **15** R_1.

The outputs of the memory circuit can be sequentially read out by scanning with the signals shown in FIGS. **5***b* and **5***c*. Such a scanning method is already known as disclosed in U. S. Pat. No. 3,021,387.

The waveforms at the time of TV displaying are shown in FIGS. **7***a* to **7***c*. FIG. **7***a* shows the pulses to be supplied from the line counter of the circuit **7** to the shift register **8** as indicated by (a) in FIG. **6**; FIG. **7***b* shows the pulses to be supplied from the shift register **8** to **10** and **11** as indicated by (b) in FIG. **6**; and FIG. **7***c* shows the pulses to be supplied from the line counter of the circuit **7** to the shift resister **9** as incidated by (c) in FIG. **6.**

In FIG. **7***c*, it will be seen that the pulses are generated for every three pulses in FIG. **7***b*. This is an example in which the line counter of the circuit **7** counts the pulses in three stages to display one mosaic pattern by three horizontal scanning operations.

When the button **5** in FIG. **6** is switched to the recording position, the control circuit **11** reads out the signals for only one figure from the momory circuit **6,** converts them to have a frequency adapted for recording, and records them in a recorder **12.** It also generates a control signal to start or stop the operation of the recorder **12** and supplies the same thereto.

The waveforms of the output signals of the control circuit **11** are shown in FIGS. **8***a* to **8***h*. FIG. **8***a* shows a command signal for recording, and recording is effected while the signal is high; FIG. **8***b* shows a signal to start or stop the recorder **12,** and the recorder is running while the signal is high; FIG. **8***c* shows a horizontal synchronizing signal; FIG. **8***d* shows a vertical synchronizing signal; FIG. **8**e shows a red color signal; FIG. **8***f* shows a green color signal; and FIG. **8***g* shows a blue color signal. The signal shown in FIGS. **8***c* to **8***g* are to be recorded on a magnetic tape, and these five signals are recorded side by side in parallel with one another on the magnetic tape. FIG. **8***h* shows a clock signal, illustrating switching between the cases of TV displaying and recording.

In the operation, firstly, a desired color is selected by an operator depressing the buttons of the color switching portion **3,** and then, a pattern is formed by his watching the monitoring panel **2** and depressing the switching buttons on the keyboard **1** which correspond to desirable buttons on the monitoring panel **2.** As each switching button on the keyboard **1** corresponds to its respective element in the memory circuit **6,** when a switching button on the keyboard **1** is depressed, the selected color is stored in the element in the memory circuit **6** corresponding to the switching button.

On the other hand, the memory circuit **6** is scanned with the reference synchronizing signals generated by the reference synchronizing signal generating circuit **7** so that output signals may be obtained. A frame of the pattern is extracted from these repetitive signals by the output signal controlling circuit **11**; this function is accomplished by depressing the button **5,** whereby the pattern is converted into a signal suitable for magnetic tape recording.

When the pattern thus produced is not needed, it is cleared by the reset circuit **4'**.

When a part of the pattern is desired to be amended, in the case where flip-flops are used as a memory circuit, the part can be cleared by depressing again the switching buttons on the keyboard **1** corresponding to the part to be amended, and after selecting the color switch corresponding to the desired color, the identical switching buttons on the keyboard are depressed again. On the other hand, in the case where memory cells are used as a memory circuit, after selecting the color switch corresponding to a desired color, the identical switching buttons on the keyboard are depressed again, whereby any picture element on the CRT can be corrected to have a desired color without the necessity of being once cleared off as in the former case. FIG. **3** illustrates an embodiment to perform the amendment, in which the parts identical to those in FIG. **2** are indicated by identical numerals.

Firstly, suppose that a red color is displayed at the position of SW_1. When it is desired to change the color to black, the color selection switch in the color switching portion **3** is turned to red and SW_1 is closed once again, where the flip-flop circuit **14** R_1 is inverted and the output Q becomes low; thus the color is changed to black.

When it is desired to change the red color to another color, the color selection switch is selected for the desired color and thereafter SW_1 is depressed, whereby the other desired color can be displayed. In this way it is possible to change the color at each one point. By repeating this operation it is possible to change the colors of a portion of the figure in a simple manner and then to proceed to processing of the next figure.

When a switching button SW_1 on the keyboard **1** is depressed, a pulse is generated, and the outputs of the switch SW_1 and the color switching portion **3** are connected to an AND gate **13** to control the input to a flip-flop circuit **14** depending upon the state of the color switching portion **3.** The flip-flop circuits **14** are all uniderectionally reset by the reset circuit **4'**, and each of them is inverted by a pulse from one of the AND gates **13** thereby to store the information of the relevant picture element and its color. Further, when the switching buttons once depressed are again depressed, the corresponding flip-flop circuits **14** are also again inverted so that the former colors of the picture elements re-appear.

In addition, the AND gates **15** shown in FIG. **3** are adapted to pass the outputs of the flip-flop circuits **14** only upon the simultaneous application of both scanning pulses from the X-axis shift register circuit **8** and the Y-axis shift register circuit **9.** The OR gates **16** sum

up all the outputs of red, green and blue colors, respectively, to produce outputs.

FIGS. 4*a* to 4*e* illustrates the output waveforms. FIGS. 4*a*, 4*b* and 4*c* show the signals of red, green and blue colors, respectively, FIG. 4*d* shows the synchronizing signal and FIG. 4*e* shows the synchronizing signal shown in FIG. 4*d* with the time-axis compressed so as to show the interval from one vertical synchronizing signal to the following one.

It is always possible to display any pattern which is formed by applying such signals as shown in FIG. 4 to the monitoring portion **10**.

As described above, in order to from a colored mosaic pattern by this invention, switches equal in number and respectively corresponding to the picture elements of the pattern to be formed are provided for storing and clearing in the memory element. By means of the switches, the memory composes an electrical pattern, and by scanning the memory, the pattern signal can be displayed on a monitoring CRT. Therefore, it is possible to form a pattern electrically by depressing switching buttons rather than by picking up, with an image pickup tube, a painted picture as done in the prior art, for example, and the pattern is easily taken out as the picture signals. Further, when another pattern similar to an original one is desired to be easily formed, the new pattern can be made by modifying only a part of the original one and it is not necessary to paint again every similar picture. This feature will be explained further in detail. The content of the memory circuit is not cleared unless the memory circuit is reset, and therefore, after the recording of a frame of the stored pattern is finished, the frame is still retained in the memory circuit. Thus, the monitoring portion can monitor it repeatedly. When another new frame is desired to be formed, it is scarce that the previously formed frame has to be wholly changed to form a new frame. Whereas, in most instances, such a new frame is one similar to the previous frame which may be formed by partially modifying the previously formed frame. Accordingly, it would be very inefficient to once reset the storage of the previous frame and then store another new frame. In the device of the present invention, partial modification of the stored information of a picture can be accomplished by the alteration of the contents of only those memory elements corresponding to the picture elements to be altered, which alteration may be effected by the selective operation of any corresponding keyboard switch and any corresponding switch of the color switching portion 3 for selecting any of red, green and blue colors. Accordingly, once a picture is formed, another similar picture may be formed by simply altering a part of the original picture to be modified. Thus, by successively recording modified pictures as such modification is effected, it is possible to obtain a series of picture signals for forming pictures of animation.

We claim:

1. A pattern generating device comprising: a keyboard including an equal number of switches respectively corresponding to picture elements which form output signals of colored mosaic patterns; and including a color switching portion for selecting any of red, green and blue colors to compose a color in said picture elements, the output signals of said keyboard being fed to a memory circuit having memory elements each corresponding to a picture element, said memory circuit storing each of the output signals from said keyboard supplied through said color switching portion in an element corresponding to the keyboard switch which has given rise to said output signals; a scanning circuit for scanning said memory circuit at a speed determined independently of the speed of writing in said memory circuit; and a display means for displaying patterns in synchronized relation to an output of said memory circuit scanned by said scanning circuit.

2. A pattern generating device as claimed in claim **1**, in which the memory circuit comprises three memory portions for storing red, green and blue color signals, each of said portions having memory elements equal to in number and respectively corresponding to the picture elements for forming colored mosaic patterns.

3. A pattern generating device as claimed in claim **2**, each of said memory portions further having gate circuits equal in number and respectively corresponding to the picture elements for forming colored mosaic patterns, said color switching portion connected to the inputs of said gate circuits.

4. A pattern generating device as claimed in claim **2**, further comprising, reset circuit means connected to said memory elements for clearing said memory circuit.

5. A pattern generating device as claimed in claim **1**, in which the memory circuit comprises as memory elements flip-flop circuits equal to in number and respectively corresponding to the picture elements for forming mosaic patterns and means connecting the inputs of said flip-flop circuits to said switches.

6. A pattern generating device as claimed in claim **1**, further comprising gate circuits connected to said memory circuit, said gate circuits being equal to in number and respectively corresponding to the picture elements for forming mosaic patterns, and means for switching the outputs of said memory circuit in sequence through said gate circuits, wherein said outputs of said memory circuit are successively read out for display on a CRT synchronized with the output of said scanning circuit.

7. A pattern generating device as claimed in claim **1**, wherein said display means comprises a color CRT synchronized with the output of said scanning circuit.

8. A pattern generating device as claimed in claim **1**, further comprising a recorder and means connecting said recorder to the memory circuit for recording signals read out of said memory circuit by the scanning circuit in synchronized relation to the scanning rate of said scanning circuit.

9. A pattern generating device comprising: a keyboard including an equal number of switches respectively corresponding to picture elements which form output signals of colored mosaic patterns; and including a color switching portion for selecting any of red, green and blue colors to compose a color in said picture elements, the output signals of said keyboard being fed to a memory circuit including three memory portions of identical structure each having memory elements equal in number and respectively corresponding to a picture element, said memory circuit storing each of the output signals from said keyboard supplied through said color switching portion in an element corresponding to the keyboard switch which has given rise to a corresponding output signal; a reset circuit for resetting the elements of said memory circuit so as to

clear the memories; a scanning circuit for scanning in synchronized relation said memory portions of said memory circuit comprising three identical portions, each storing signals of red, green and blue colors, respectively; a color CRT for displaying patterns in synchronized relation to the output of said memory circuit scanned by said scanning circuit; and a recorder for recording said output signals.

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