(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 March 2019 (07.03.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/043124 A1

(51) International Patent Classification:
H02H 7/12 (2006.01) *H02H 7/125* (2006.01)
H02M 1/32 (2007.01)

(21) International Application Number:
PCT/EP2018/073401

(22) International Filing Date:
30 August 2018 (30.08.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/692,451 31 August 2017 (31.08.2017) US

(71) Applicant: **EATON INTELLIGENT POWER LIMITED** [IE/IE]; 30 Pembroke Road, Dublin, 4 (IE).

(72) Inventors: **LI, Huaqiang**; W182 N4906 Green Crane Drive, Menomonee Falls, Wisconsin 53051 (US). **O'BRIEN, Seth**; 1640 Rivers Bend Lane, Apt.# 108, Wauwatosa, Wisconsin 53226 (US). **RUCHTI, Thomas M.**; W232 N3211 Greenbriar Road, Pewaukee, Wisconsin 53072 (US).

(74) Agent: **EMDE, Eric C.** et al.; Wagner & Geyer Partnerschaft mbB, Gewürzmühlstr. 5, 80538 Munich (DE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) Title: ADJUSTABLE SPEED DRIVE WITH INTEGRATED SOLID-STATE CIRCUIT BREAKER AND METHOD OF OPERATION THEREOF

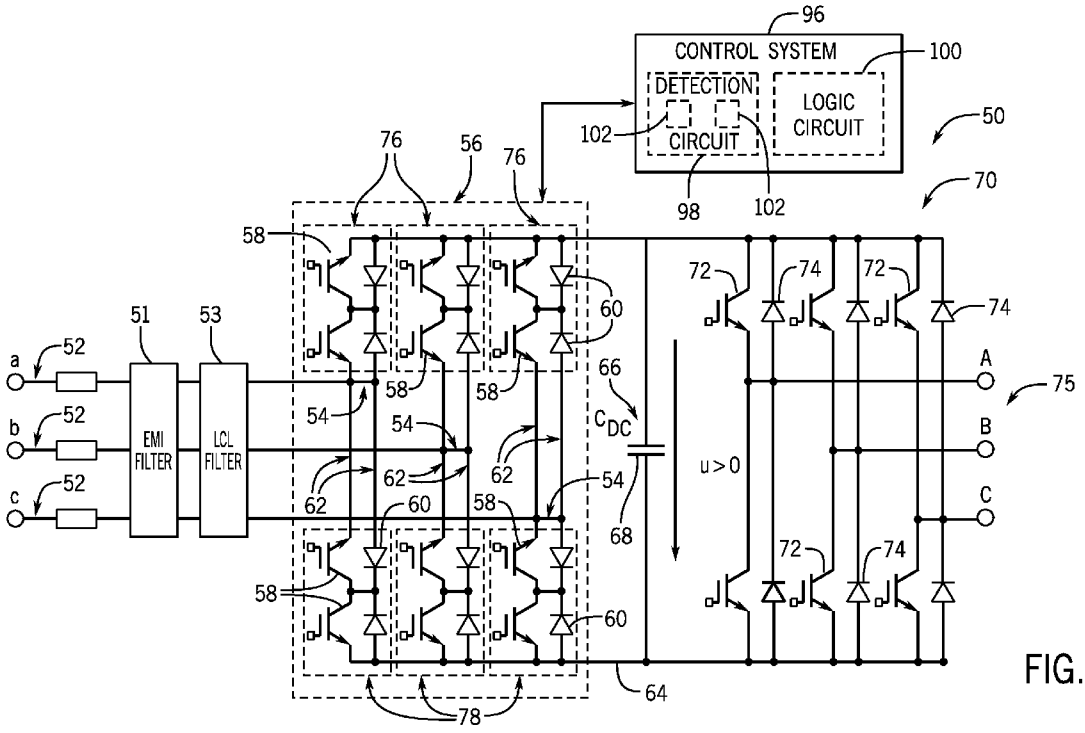


FIG. 3

(57) Abstract: A power conversion circuit (50) having a solid-state circuit breaker (76, 78) integrated therein is disclosed. With a disconnect switch between a utility source and the power conversion apparatus described for meeting UL489, the power conversion circuit includes an input connectable to an AC source, a rectifier circuit (56) connected to the input to convert an AC power input to a DC power, and a DC link (64) coupled to the rectifier circuit (56) to receive the DC power therefrom. The rectifier circuit (56) comprises a plurality of phase legs (62) each including thereon an upper switching unit (76) and a lower switching unit (78), wherein at least one of the upper and lower switching units (76, 78) on each phase leg (62) comprises a bi-directional switching unit that selectively controls current and withstands voltage in both directions, so as to provide a circuit breaking capability that selectively interrupts current flow through the rectifier circuit, while maintaining original power conversion functionalities.

WO 2019/043124 A1

[Continued on next page]

SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

ADJUSTABLE SPEED DRIVE WITH INTEGRATED SOLID-STATE CIRCUIT BREAKER AND METHOD OF OPERATION THEREOF

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to adjustable speed drive (ASD) circuits and, more particularly, to an ASD having a solid-state circuit breaker integrated therein and method of operation thereof.

[0002] One type of system commonly used in industry that performs power conversion is an ASD circuit, also known as a variable frequency drive (VFD) circuit. An ASD is an industrial control device that provides for variable frequency, variable voltage operation of a driven system, such as an AC induction motor. A typical ASD circuit 10 is illustrated in FIG. 1. ASD or VFD circuit 10 includes an electromagnetic interference (EMI) filter 12 provided between a drive input 14 and input rectifier terminals 16. The terminals are connected to a rectifier bridge 18 that converts an AC input power provided at drive input 14 into a DC power, with the rectifier bridge 18 being in the form of an "uncontrolled" rectifier bridge that includes an arrangement of six diodes 20 – with a pair of diodes 20 arranged in series on each of the three input phases. The ASD circuit 10 additionally includes a DC link 22 that receives the DC power from rectifier bridge 18; a DC link capacitor bank 24 having one or more capacitors 26, 28 across DC link 22; two inductors 30 (i.e., a DC choke) coupled in series with and on either side of the rectifier bridge 18 on DC link 22; a brake chopper 32 to discharge the DC link capacitor bank 24; an inverter 34 to convert the DC power to AC power; an output 36 coupled to the inverter 34; and resistors 38 arranged in parallel with capacitors 26, 28 across the DC link 22 in order to balance voltages of the capacitors 26, 28 and discharge them after power-off. While not shown in FIG. 1, it is known that the ASD circuit may also include a pre-charge circuit to control and limit inrush current into DC link capacitor bank 24 during power up.

[0003] With regard to the operation of ASD circuits, it is recognized that a number of tests and standards are set forth regarding the safety and functionality of the ASD circuit, and that such tests must be passed in order to judge the circuit as being compliant with such standards. Standard UL61800-5-1 is the governing safety standard

for ASD circuits in the United States and is used to validate any claimed short circuit rating for the drive, such as 100 kA for example. Standard UL61800-5-1 requires that an ASD circuit under a breakdown of components test not catch fire or experience another unacceptable failure. That is, it is recognized that a breakdown of components test may cause a short circuit across a capacitor that will cause the ASD circuit to fail and, if power is allowed to continue to flow to the capacitor bank when one capacitor has a short circuit, an overvoltage condition will exist on the non-shorted capacitor. This overvoltage condition may, in electrolytic capacitors, cause the non-shorted capacitor to catch on fire and possibly explode.

[0004] Traditionally, a breakdown of components test of an ASD circuit for determining compliance with UL61800-5-1 has been performed using either a fuse or a circuit breaker 40 external to the ASD circuit 10 (i.e., external to a housing 42 thereof), along with a separate switch (e.g., contactor) 41 used specifically for the test, as shown in FIG. 1. In the event that a short circuit occurs during testing, the contactor 41 functions to short out the +/- DC link in order to introduce the fault as required in UL61800-5-1. However, it is recognized that traditional circuit breakers having a finite response time and will let through energy from the source to the ASD circuit when a component short circuit inside the drive occurs. Accordingly, even with the presence of a circuit breaker, it is possible that a damage to the ASD circuit may occur due to overstressed components such as rectifier diode or capacitor failures, as the additional energy that flows to the drive during the circuit breaker response time may be enough to cause such component failure.

[0005] More recently, solid-state circuit breakers have been developed to replace traditional circuit breakers, with such solid-state circuit breakers beneficially having a shorter response time as compared to traditional circuit breakers. The use of a solid-state circuit breaker in a breakdown of components test of an ASD circuit for determining compliance with UL61800-5-1 thus presents an improvement over tests performed with a traditional circuit breaker. However, it is recognized that use of solid-state circuit breakers for providing protection to an ASD circuit still does not prevent an optimal solution. That is, as the solid-state circuit breaker is still external to the ASD circuit, introducing higher cabling and installation costs, as well as more real estate.

Additionally, existing solid-state circuit breakers may not provide protection at higher sustained current levels, such as might occur with in-rush current that is present during start-up of the motor/load, as the solid-state switches in the breaker are always fully gated On and may experience overlong thermal stresses. Accordingly, the solid-state circuit breaker may not be suitable to protect against sustained inrush currents in motor starting applications, which may be 6-7x higher than the rated current.

[0006] As described above, it is recognized that existing electro-mechanical circuit breaker designs external to the ASD circuit fail to provide adequate and comprehensive protection to the ASD circuit during a breakdown of components, during ongoing operation of the drive. Furthermore, the existing solid state circuit breakers fail to provide adequate protection during a motor starter application. Furthermore, it is recognized that the architecture of the ASD circuit 10 itself lacks the means to provide sufficient protection against a short circuit across DC capacitor(s) 26, 28 in DC capacitor bank 24 that could damage ASD circuit and against other various internal and external fault conditions. That is, controlling of the fault current or overvoltage condition in the ASD circuit 10 is not possible, as diodes 20 of rectifier bridge 18 cannot be controlled to turn off, such that power can continue to pass through rectifier bridge 18 to DC capacitor bank 24 while a capacitor is shorted, as illustrated in FIG. 1 via a path along which a short circuit current flows through the ASD circuit 10, i.e., through diode rectifier circuit 18 and then through capacitor bank 24. In another fault situation, the overvoltage condition on the non-shorted capacitor 26, 28 will cause ASD circuit 10 to be damaged, such that the damaged ASD circuit 10 will not be useable and a user will have to make costly repairs to the ASD circuit or replace the ASD circuit. The user will incur additional economic losses during the downtime period when ASD circuit 10 is not in use. While the ASD circuit architecture of FIG. 1 may be modified to replace the passive diode rectifier circuit 18 with an active rectifier circuit 44 that includes solid-state switches 46 therein in addition to diodes 20, such as shown in the embodiment of FIG. 2, the active rectifier circuit 44 still cannot prevent fault current from traveling through diodes 20, as shown in the short circuit current path illustrated therein.

[0007] It would therefore be desirable to provide a system and method for protecting an ASD circuit during a breakdown of components test, to prevent the circuit from catching fire or experiencing other failures due to a fault condition therein, according to the requirements of Standard UL61800-5-1. It would also be desirable for such a system and method to protect the ASD circuit against fault conditions that could damage the ASD circuit during transient and/or steady state operation thereof.

BRIEF DESCRIPTION OF THE INVENTION

[0008] Embodiments of the invention are directed to an ASD circuit with an integrated solid-state circuit breaker and method of operation thereof. The ASD circuit and integrated solid-state circuit breaker removes the need for installing an external circuit breaker, achieving system flexibility, providing increased protection, and reducing total cost of ownership.

[0009] In accordance with one aspect of the invention, a power conversion circuit includes an input connectable to an AC source, a rectifier circuit connected to the input to convert an AC power input to a DC power, and a DC link coupled to the rectifier circuit to receive the DC power therefrom. The rectifier circuit comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit, wherein at least one of the upper and lower switching units on each phase leg comprises a bi-directional switching unit that selectively controls current and withstands voltage in both directions, so as to provide a circuit breaking capability that selectively interrupts current flow through the rectifier circuit.

[0010] In accordance with another aspect of the invention, a method of providing circuit breaking in a power conversion circuit includes receiving an AC power at an input of the power conversion circuit and measuring or determining, via a detection circuit and logic circuit of the power conversion circuit, one or more current and voltage parameters of power provided to the power conversion circuit or present in the power conversion circuit. The method also includes comparing, via the detection circuit or logic circuit, the one or more current and voltage parameters to one or more respective current and voltage thresholds, and identifying, via the logic circuit, a fault condition in the power conversion circuit if the one or more measured or determined current and

voltage parameters exceed the one or more respective current and voltage thresholds. The method further includes controlling, via the logic circuit, a solid-state circuit breaker integrated into the power conversion circuit to interrupt current flow through the power conversion circuit upon identification of the fault condition.

[0011] In accordance with yet another aspect of the invention, an ASD circuit includes an input connectable to an AC source, a rectifier bridge with integrated solid-state circuit breaker connected to the input to convert an AC power input to a DC power, and a DC link coupled to the rectifier bridge to receive a DC link voltage therefrom. The rectifier bridge with integrated solid-state circuit breaker comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit, wherein at least one of the upper and lower switching units on each phase leg is configured to control current and withstand voltage in both directions and allow for the selective interruption of current flow through the respective switching unit.

[0012] Various other features and advantages of the present invention will be made apparent from the following detailed description and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The drawings illustrate preferred embodiments presently contemplated for carrying out the invention.

[0014] In the drawings:

[0015] FIG. 1 is a schematic diagram of an ASD circuit and external circuit breaker, illustrated under a breakdown of components test configuration with the DC link shorted out, as known in the prior art.

[0016] FIG. 2 is a schematic diagram of another ASD circuit, illustrated under a breakdown of components test configuration with the DC link shorted out, as known in the prior art.

[0017] FIG. 3 is a schematic diagram of an ASD circuit with an integrated solid-state circuit breaker, according to an embodiment of the invention.

[0018] FIGS. 4A and 4B are schematic diagrams illustrating current flow paths through the ASD circuit of FIG. 3 during normal operation and a fault condition (illustrated in one of the three phases), respectively, based on selective operation of the integrated solid-state circuit breaker, according to embodiments of the invention.

[0019] FIG. 5 is a schematic diagram of an ASD circuit with an integrated solid-state circuit breaker, according to another embodiment of the invention.

[0020] FIG. 6A is a schematic diagram of an ASD circuit with an integrated solid-state circuit breaker, according to another embodiment of the invention.

[0021] FIG. 6B is a schematic diagram of an ASD circuit with an integrated solid-state circuit breaker, according to another embodiment of the invention.

[0022] FIG. 7 is a flowchart illustrating a technique for controlling the ASD circuit of FIG. 3, according to an embodiment of the invention.

[0023] FIGS. 8A-8D are schematic diagrams of various solid-state switch and/or diode configurations and arrangements that may be implemented in the ASD circuit of FIG. 3, according to embodiments of the invention.

DETAILED DESCRIPTION

[0024] Embodiments of the invention relate to a system and method for preventing component failure and damage in a power conversion circuit responsive to a fault condition. A solid-state circuit breaker is integrated into the power conversion circuit to provide protection thereto, with the solid-state circuit breaker interrupting a fault current in the power conversion circuit upon detection of a fault condition. The integrated solid-state circuit breaker therefore acts to limit the damage to components in the power conversion circuit, such as during a shortage in a capacitor bank on the DC link thereof.

[0025] While embodiments of the invention are described and illustrated herebelow as being directed to ASD or VFD circuit and the integration of a solid-state circuit

breaker into such circuits, it is recognized that embodiments of the invention are not meant to be limited to such circuits. That is, embodiments of the invention may be extended more generally to power/energy conversion circuits of varying constructions and implementations, including uninterruptible power supplies (UPS), DC-AC power converters, and power/energy conversion circuits for driving non-motor loads, for example. Accordingly, the following discussion of the integration of a solid-state circuit breaker into ASD/ VFD circuits is not meant to limit the scope of the invention.

[0026] Referring to FIG. 3, an ASD or VFD circuit 50 with integrated solid-state circuit breaker is illustrated according to an exemplary embodiment of the invention. The ASD circuit 50 includes a drive input 52 and input rectifier terminals 54, with an EMI filter 51 and LCL filter 53 (optional, depending on circuit topologies) connected between the input 52 and terminals 54. The terminals are connected to a front-end AC-DC rectifier bridge or circuit 56 comprising an arrangement of solid-state switches 58 and diodes 60 provided on phase legs 62 of the bridge corresponding to each of the three input phases. The rectifier circuit 56 converts an AC input power provided at drive input 52 (such as, for example, from a utility grid) into a DC power and also functions as a solid-state circuit breaker to interrupt current flow through the ASD circuit 50, as will be explained in greater detail below.

[0027] ASD circuit 50 additionally includes a DC link or bus 64 that receives the DC power from rectifier circuit 56 and a DC link capacitor bank 66 comprised of one or more capacitors 68 across DC link 64 to provide smoothing to the DC link voltage, with this smoothed voltage then being provided to an inverter 70. While capacitor bank 66 is shown with one capacitor 68, capacitor bank 66 may include additional capacitors connected in series or parallel arrangements, as needed. While not shown in FIG. 3, it is recognized that inductors could be included in ASD circuit 50 coupled in series with and on either side of rectifier circuit 56, as well as a pre-charge circuit coupled in series with one of the inductors to control and limit inrush current into the DC link capacitor bank 66 during power up (when drive input 14 is initially coupled to an AC input power). Still further, a brake chopper may be included in ASD circuit 50 to discharge the DC link capacitor 68 in a controlled manner, with the voltage from the brake chopper then being provided to inverter 70 coupled to the DC link 64. The inverter 70

is composed of an arrangement of solid state switching devices 72 and anti-parallel diodes 74, that collectively form a PWM inverter that synthesizes AC voltage waveforms with a variable frequency and amplitude for delivery to output 75 of inverter 70, so as to provide a controlled three-phase power to a load driven thereby (e.g., AC motor).

[0028] As shown in the embodiment of FIG. 3, the rectifier circuit 56 is comprised of six switching units 76, 78 arranged on the three input phases 52, i.e., a pair of switching units in series on each phase – an upper switching unit 76 and a lower switching unit 78. Each of the switching units 76, 78 is formed of a pair of unidirectionally conducting solid-state semiconductor switches 58 and a pair of diodes 60. While the solid-state semiconductor switches 58 are shown as insulated-gate bipolar transistor (IGBTs) in FIG. 3, it is recognized that other solid-state semiconductor switches could be used instead, including metal oxide semiconductor field effect transistors (MOSFETs) or integrated gate-commutated thyristors (IGCTs), for example, although other solid-state semiconductor switches may also be suitable, and thus embodiments of the invention are not meant to be limited to the specific switch types set forth above. Furthermore, the switches 58 (and diodes 60) can be made with Silicon (Si), Silicon Carbide (SiC), Gallium Nitride (GaN), or any suitable Wide Bandgap (WBG) material, with exemplary embodiments having the switches made of GaN or SiC.

[0029] As shown in FIG. 3, each of the IGBTs 58 in a respective switching unit 76, 78 is arranged in anti-parallel with an associated diode 60. The IGBTs 58 in each switching unit 76, 78 are further arranged and connected with one another in anti-series in a common collector (CC) configuration – referred to hereafter simply as "reverse-blocking IGBTs." The diodes 60 are arranged in opposing directions (i.e., anti-series) relative to one another, so as to block current flow in differing directions through the rectifier circuit 56. Based on the arrangement of diodes 60 and reverse-blocking IGBTs 58, each switching unit 76, 78 thus provides a bi-directional switching unit that is able to control current and withstand voltage in both directions and allow for the selective interruption of current flow within ASD circuit 50. With regard to the switching units 76, 78 illustrated in FIG. 3, it is noted that while the IGBTs 58 (and diodes 60) are

shown therein as being connected in anti-series in a common collector configuration, the IGBTs 58 and diodes 60 could instead be connected in other configurations while still providing the desired current controls and voltage protection. FIGS. 8A-8D illustrate alternate IGBT and diode arrangements/configurations that could be used as alternatives to the common collector configuration shown in FIG. 3. FIG. 8A shows a diode bridge configuration where a single IGBT 58 is arranged with four diodes 60. FIG. 8B shows IGBTs 58 connected in anti-series in a common emitter (CE) configuration, while still functioning as reverse-blocking IGBTs (with the orientation of each of diodes 60 then being flipped) able to control current and withstand voltage in both directions and allow for the selective interruption of current flow within ASD circuit 50. FIG. 8C shows two IGBTs 58 arranged/connected in anti-parallel as a reverse blocking (RB) IGBT. Each of the above IGBT and diode arrangements provides distinct advantages and disadvantages, and thus the exact construction of each switching unit 76, 78 can be determined based on the implementation of ASD circuit and the needs/requirements thereof. FIG. 8D illustrates another reverse blocking (RB) IGBT arrangement where each IGBT 58 and diode are integrated in one die, with two such dies being connected as shown to control current and withstand voltage in both directions and allow for the selective interruption of current flow within ASD circuit 50.

[0030] Referring now to FIGS. 4A and 4B, the selective allowance and interruption of current flow along one phase 52 of the ASD circuit 50 based on functioning of rectifier circuit 56 is shown for purposes of illustration/explanation. First, as illustrated in FIG. 4A, under normal operating conditions of ASD circuit 50, current flow is provided along input 52 from an AC power source and passes through diode 60 of an upper switching unit 76 in an uncontrolled fashion. Under normal operating conditions of ASD circuit 50, IGBT 58 of upper switching unit 76 is in an On or conducting state, and thus current also passes through IGBT 58 and to DC capacitor bank 66 connected across DC link 64. Current then flows back through diode 60 of lower switching unit 78, again in an uncontrolled fashion, with current then continuing to flow through IGBT 58 of lower switching unit 78 when in an On or conducting state.

[0031] Next, as illustrated in FIG. 4B, under a fault condition such as shorting out of the +/- DC link 64 or other fault condition, current flow is provided along input 52 from

an AC power source and passes through diode 60 of upper switching unit 76 in an uncontrolled fashion. Under a fault condition, IGBT 58 of upper switching unit 76 is caused to operate in an Off or non-conducting state (as indicated by the "X" marking in FIG.4B), with switching of the IGBT 58 to the Off or non-conducting state being responsive to any of a number of sensed faults or parameters associated with the ASD circuit 50, as will be explained in greater detail below. Upon switching of IGBT 58 of upper switching unit 76 to the Off or non-conducting state, current flow is blocked by IGBT 58 and current flow to the DC link 64 and capacitor bank 66 is terminated. According to one embodiment, and as shown in FIG. 4B, IGBT 58 of lower switching unit 78 is also caused to operate in the Off or non-conducting state, thus providing a redundant blocking of current flow in ASD circuit 50.

[0032] While not shown in FIGS. 4A and 4B, it is to be understood that controlling of IGBTs 58 in switching units 76, 78 on the other phases 52 would be performed in similar fashion to selectively allow and interrupt current flow on the other phases in the ASD circuit 50 during normal operating and fault conditions therein.

[0033] In addition to functioning as a solid-state circuit breaker and providing protection to ASD circuit, it is recognized that rectifier bridge 56 also provides flexibility regarding operation thereof as either an active front end rectifier bridge or an uncontrolled diode front end rectifier bridge. That is, it is recognized that IGBTs 58 of rectifier bridge 56 may be selectively controlled so as to provide active or passive rectification in ASD circuit 50. In operation as an uncontrolled diode front end rectifier bridge, IGBTs 58 may be left gated On during normal operation of the ASD circuit 50, such that current flows through IGBTs (and diodes 60) in an uncontrolled manner. In operation as an active front end rectifier bridge, IGBTs 58 may be selectively gated On and Off during normal operation of the ASD circuit 50, such that current flows through IGBTs 58 in a controlled manner. The operation of rectification circuit 56 in an active or passive/uncontrolled fashion (based on operation of IGBTs 58) can be determined based on the implementation of ASD circuit and the needs/requirements thereof, and appropriate associated components would be included in the circuit if operated as an active front end rectifier - LCL filter 53 (FIG. 3) would be included in the ASD circuit

50 for an active rectifier circuit, but is not required in an uncontrolled front end rectifier configuration.

[0034] Referring now to FIGS. 5 and 6, additional ASD circuits are illustrated according to other embodiments of the invention. As first shown in FIG. 5, an ASD circuit 80 is provided that includes an AC-DC rectifier circuit 82 that is modified as compared to the AC-DC rectifier circuit 56 of FIG. 3. That is, each of a number of upper switching units 76 in rectifier circuit 82 have an identical construction to the switching units 76 shown and described previously in FIG. 3 – with each upper switching unit 76 including a pair of IGBTs 58 arranged in anti-parallel with an associated diode 60, and with the IGBTs 58 arranged such that they function as reverse-blocking IGBTs 58 in the switching unit 76 and the diodes 60 also being arranged in opposing directions, so as to block current flow in differing directions through the rectifier circuit. However, the lower switching units 84 in rectifier circuit 56 are modified as compared to the upper switching units 76, with each of the lower switching units 84 including only a single IGBT 58 arranged in anti-parallel with an associated diode 60 (i.e., no reverse-blocking IGBT and associated blocking diode).

[0035] With regard to the ASD circuit 80 of FIG. 5, it is recognized that lower switching units 84 may have a simpler construction (i.e., removal of reverse-blocking IGBT and associated blocking diode) as compared to upper switching units 76, as the lower switching units 84 provide only a redundant blocking of current flow in ASD circuit 80. That is, the controlling of IGBTs 58 in each of upper switching units 76 should be sufficient to block current flow current flow through the switching units 76 and prevent current from continuing to flow to the DC link capacitor bank 66, so as to provide protection thereto. The ASD circuit 80 may be provided at a lower cost as compared to ASD circuit 50 of FIG. 3, while still providing adequate protection to the ASD drive 80. Additionally, because of device number reduction, the system losses are decreased with efficiency gains.

[0036] As shown in FIGS. 6A and 6B, an ASD circuit 90 is provided that includes additional protection devices therein as compared to the ASD circuits 50, 80 of FIGS. 3 and 5. In the embodiment illustrated embodiment of FIGS. 6A and 6B, the additional

protection devices include a galvanic isolation disconnect switch 92 and a snubber circuit 94, although it is recognized that just one of these two devices could be included in ASD circuit 90. The disconnect switch 92 is located between the drive input 52 and input rectifier terminals 54 and may provide additional protection to the circuit, with the inclusion of disconnect switch 92 allowing the circuit 90 to meet the UL 489 standard, thereby enabling use of the circuit in service entrance, feeder, branch circuit, and other building applications, for example. The disconnect switch 92 functions when all solid-state semiconductor devices in ASD circuit 90 are in their Off or non-conducting state. The snubber circuit 94 is connected to rectifier circuit 82 and functions to absorb transients in the ASD circuit 90, as well as provide electromagnetic interference filtering in the ASD circuit 90.

[0037] While the rectifier circuit 82 of ASD circuit 90 is shown in FIG. 6A as having an identical AC-DC rectifier circuit construction to that of the AC-DC rectifier circuit 82 in the ASD circuit of FIG. 5, it is recognized that protection devices could be added to ASD circuits having various rectifier circuit constructions. In the embodiment of FIG. 6A, each upper switching unit 76 includes a pair of IGBTs 58 arranged in anti-parallel with an associated diode 60, and with the IGBTs 58 arranged such that they function as reverse-blocking IGBTs in the switching unit 76 and the diodes 60 also being arranged in opposing directions, so as to block current flow in differing directions through the rectifier circuit 82, while each lower switching unit 84 includes only a single IGBT 58 arranged in anti-parallel with an associated diode 60. However, the construction of upper and lower switching units 76, 84 could be reversed, as shown in FIG. 6B, with the upper switching units 76 having a simplified construction of only a single IGBT 58 arranged in anti-parallel with an associated diode 60 and the lower switching units 84 including multiple IGBTs 58 and diodes 60 arranged that function as reverse-blocking IGBTs and diodes. Still further, the construction of rectifier circuit 82 could be modified so as to be identical to that of rectifier circuit 56 of FIG. 3.

[0038] Referring now collectively to FIGS. 3 and 5-7, it is seen that each of the ASD circuits 50, 80, 90 illustrated therein further includes a control system 96 that functions to control On/Off switching of the IGBTs 58 of a rectifier circuit. As referred to herein, the control system 96 is defined as including a detection circuit 98 and a logic circuit

100 in operative communication with one another – i.e., the logic circuit 100 receives in input signals from the detection circuit 98. The detection circuit 98 operates to measure or determine voltage or current measurements in ASD circuit 50, 80, 90, while the logic circuit 100 operates to sense a short circuit or other fault condition in the ASD circuit 50, 80, 90 and control switching of the IGBTs 58 of rectifier circuit 56, 82 during normal operation of the ASD circuit and upon detection of a fault condition in the ASD circuit. While each of detection circuit 98 and logic circuit 100 is shown as a single circuit in FIGS. 3, 5, and 6, it is recognized that each of the circuits may in fact comprise a number of separate and distinct controllers or processors, and that embodiments of the invention are not meant to be limited in such regard. For example, separate logic circuits may be provided for sensing a short circuit or other fault condition in the ASD circuit 50, 80, 90 and controlling switching of the IGBTs 58 of rectifier circuit 56, 82. Still further, while control system 96 is shown as being part of ASD circuit 50, 80, 90, it is recognized that the control system 96 – i.e., one or both of the detection circuit 98 and logic circuit 100 thereof - could instead be provided as separate from ASD circuit 50, 80, 90 but operably connected thereto.

[0039] As shown in the figures, detection circuit 98 may include one or more voltage or current sampling or sensing circuits or sensors 102 configured to measure or determine voltage and/or current at one or more locations in the ASD circuit 50, 80, 90. Thus, while shown as being incorporated in detection circuit 98, it is recognized that sampling or sensing circuits 102 could be dispersed throughout ASD circuit 50, 80, 90. According to embodiments of the invention, the detection circuit 98 may operate to measure one or more of the following voltage/current parameters in the ASD circuit 50, 80, 90, including: three phase input currents or voltages, current at the switch level of rectifier circuit, DC link current, and/or load output currents or voltages, for example. A number of examples of exemplary operation of the detection circuit will be set forth here below, according to embodiments of the invention, along with the operation of logic circuit 100 tied to detection circuit 98.

[0040] In a first example of operation of detection circuit 98, detection circuit 98 may include a voltage sampling circuit 102 (i.e., voltage sensors) positioned on capacitor 68 to measure the voltage thereacross. While not shown, it is recognized that

an additional capacitor 68 could be included in capacitor bank 66 and have an additional voltage sampling circuit 102 thereon so that the voltage across the additional capacitor may be measured as well. In detecting a short circuit in capacitor bank 66, logic circuit 100 compares the voltage across capacitor 68 received from voltage sampling circuit 102 to a voltage threshold or limit such as, for example, an overvoltage threshold or an undervoltage threshold. If the voltage across capacitor 68 crosses or passes the voltage threshold, logic circuit 100 detects a shorted capacitor in capacitor bank 66. In some embodiments, logic circuit 100 compares the voltage across capacitor 68 to both an overvoltage voltage threshold and an undervoltage threshold. The overvoltage and undervoltage thresholds may be set approximately 50-100 volts (V) from a nominal capacitor bank voltage and a short circuit voltage, respectively. For example, in an embodiment where capacitor bank 66 includes two capacitors 68, if the nominal voltage across capacitor bank 66 is 650V, both capacitors 68 should have 325V thereacross. If a first capacitor is shorted, then the entire 650V drop would be across the second capacitor, and the overvoltage threshold could be set to about 550-600V, while the voltage then across the first capacitor would drop to 0V, and the undervoltage threshold could be set to about 50-100V. In another embodiment, the voltage across both capacitors 68 may be measured by voltage sampling circuit 102, with the logic circuit 100 calculating the difference between the voltage across the capacitors and comparing that difference to a voltage threshold.

[0041] In operation, if the voltage across capacitor 68 crosses or passes the voltage threshold (or if a difference between the voltage across multiple capacitors 68 is greater than a voltage threshold), logic circuit 100 detects a shorted capacitor in capacitor bank 66 and thus identifies a fault condition in ASD circuit 50, 80, 90. Upon such detection/identification, logic circuit 100 then functions to implement a circuit breaking operation via selective switching of IGBTs 58 in the rectifier circuit 56, 82 of ASD circuit 50, 80, 90, with the logic circuit 100 being operably connected to the IGBTs 58 of rectifier circuit 56, 82 to control switching thereof. When the logic circuit 100 detects a shorted capacitor, the logic circuit 100 transmits gating signals to selective IGBTs 58 in the rectifier circuit 56, 82, such as the IGBTs 58 as illustrated in FIG. 4B, so as to cause the two IGBTs 58 to turn off and become non-conductive – thereby

terminating current flow therethrough and preventing additional current from flowing through capacitor bank 66. Similar gating signals would be transmitted to selective IGBTs 58 in each of the other switching units 76, 78 by logic circuit 100 to control current flow on other phase legs 62 of the rectifier circuit 56, 82.

[0042] In a second example of operation of detection circuit 98, detection circuit 98 functions to sense a current across at the switch level of rectifier circuit, i.e., current across IGBTs 58 in rectifier circuit 56, 82. In one embodiment, the detection circuit 98 may include a voltage sampling or sensing circuit 102 that senses the emitter/source voltage of each IGBT 58 in rectifier circuit 56, 82. For each IGBT 58, the detection circuit 98 may then, after a temperature compensation step being performed, calculate the conduction current across the IGBT 58 based on the voltage. In another embodiment, the detection circuit 98 may include a current sampling or sensing circuit 102 that directly senses the conduction current across each IGBT 58 in rectifier circuit 56, 82. In either embodiment, the calculated/measured current value may then be compared to a pre-determined current threshold by logic circuit 100, and logic circuit 100 will detect a fault condition in ASD circuit 50, 80, 90 if the current value is above the threshold value. Upon such detection/identification, logic circuit 100 then functions to implement a circuit breaking operation via the selective switching of IGBTs 58 in the rectifier circuit 56, 82, with the logic circuit 100 transmitting gating signals to selective IGBTs 58 in the rectifier circuit 56, 82, such as the IGBTs 58 as illustrated in FIG. 4B, so as to cause the two IGBTs 58 to turn off and become non-conductive – thereby interrupting current flow therethrough and terminating current flow through rectifier circuit 56, 82. Similar gating signals would be transmitted to selective IGBTs 58 in each of the other switching units 76, 78 by logic circuit 100 to control current flow on other phase legs 62 of the rectifier circuit 56, 82.

[0043] In another example of operation of detection circuit 98, detection circuit 98 functions to sense a current and/or voltage on each of the three input phases 52 to ASD circuit 50, 80, 90. The detection circuit 98 may thus include a current/voltage sampling or sensing circuit 102 that senses the current and/or voltage on each phase 52. The three-phase current/voltage measured by detection circuit 98 may then be compared to one or more respective current/voltage thresholds by logic circuit 100 to detect the

presence of a fault. In one embodiment, the three-phase current is compared to the input current rating of the ASD circuit 50, 80, 90 to see if any of the phase currents exceeds a maximum rated current value. In another embodiment, the voltage imbalance of the three phase supply may be compared to a pre-determined imbalance threshold. In either embodiment, logic circuit 100 may detect a fault condition in ASD circuit 50, 80, 90 if the current/voltage value is above the threshold value. Upon such detection/identification, logic circuit 100 then functions to implement a circuit breaking operation via the selective switching of IGBTs 58 in the rectifier circuit 56, 82, with the logic circuit 100 transmitting gating signals to selective IGBTs 58 in the rectifier circuit 56, 82, such as the IGBTs 58 as illustrated in FIG. 4B, so as to cause the two IGBTs 58 to turn off and become non-conductive – thereby interrupting current flow therethrough and terminating current flow through rectifier circuit 56, 82. Similar gating signals would be transmitted to selective IGBTs 58 in each of the other switching units 76, 78, by logic circuit 100 to control current flow on other phase legs of the rectifier circuit 56, 82.

[0044] Referring now to FIG. 7, and with reference back to FIG. 3, a technique 110 for controlling ASD circuit 50 is shown, with the technique being performed by the detection circuit 98 and logic circuit 100 of ASD circuit 50, as described above. Process 110 starts at STEP 112 when an AC input power is applied at drive input 52 of ASD circuit 50. The providing of AC input power at STEP 112 may be performed as part of a normal operation of ASD circuit 50 or may be as part of a breakdown of components testing of ASD circuit 50.

[0045] Upon a supplying of AC input power at drive input 50, one or more measured/determined voltage and/or current values are acquired via detection circuit 98 at STEP 114. As previously described, voltage/current parameters that may be measured or determined in the ASD circuit 50, including: three phase input currents or voltages, current at the switch level of rectifier circuit, DC link current, and/or DC link capacitor current, for example. Upon acquisition of such values, a determination is made at STEP 116 regarding whether the one or more measured/determined voltage and/or current values within the ASD circuit 50 are normal and within an acceptable range - with such determination being made via detection circuit 98 and/or logic circuit

100. The determination at STEP 116 is either based on whether any measured voltage/current has exceeded a pre-determined limit/threshold or based on whether a difference between respective voltage/current measurements has exceeded a limit/threshold, as defined in logic circuit 100. If it is determined at STEP 116 that any of the voltage/current parameters are abnormal, as indicated at 118, logic circuit 100 operates to control switching of solid-state switches 58 in the rectifier circuit 56 in a manner that causes the rectifier circuit 56 to operate as a solid-state circuit breaker and interrupt current flow through ASD circuit 50 at STEP 120. That is, at STEP 120, logic circuit 100 functions to implement a circuit breaking operation via the selective switching of IGBTs 58 in the rectifier circuit 56, with the logic circuit 100 transmitting gating signals to selective IGBTs 58 in the rectifier circuit 56, such as the IGBTs 58 as illustrated in FIG. 4B, so as to cause the two IGBTs 58 to turn off and become non-conductive – thereby interrupting current flow through ASD circuit 50. Similar gating signals would be transmitted to selective IGBTs 58 in each of the other switching units 76, 78 by logic circuit 100 to control current flow on other phase legs 62 of the rectifier circuit 56. As one example of protection provided by switching of IGBTs 58, interruption of the current flow prevents additional current from passing through DC link capacitor 68, thereby eliminating the risk of the capacitor 68 exploding or starting on fire due to an uncontrolled overvoltage therethrough.

[0046] Referring still to FIG. 7, if detection circuit 98 instead determines at STEP 116 that all of the measured voltage/current parameters are normal, as indicated at 122, it is then considered that ASD circuit 50 is operating in a normal state/condition (and that input voltages/currents are acceptable), and that ASD circuit 50 may thus be safely operated. Accordingly, technique 110 returns to STEP 114 and continues to monitor the aforementioned voltage/current parameters for identification of any future fault.

[0047] Beneficially, embodiments of the invention thus provide a power conversion circuit, such as an ASD circuit, having circuit breaker capability and functionality built-in thereto to protection against short circuits and other fault conditions that might be present in the power conversion circuit. The incorporation of a solid-state circuit breaker into the power conversion circuit thus provides an effective solution to limit damage to the power conversion circuit from a capacitor short or other fault condition,

with the protection circuit allowing for the power conversion circuit to meet the requirements of the UL61800-5-1 breakdown of components test.

[0048] The ASD circuit and integrated solid-state circuit breaker removes the need for installing an external circuit breaker, achieving system flexibility, providing increased protection (via improved response/switching time – e.g., in the order of microseconds vs. milliseconds with a traditional external circuit breaker), and reducing total cost of ownership. The integrated solid-state circuit breaker also provides protection during both steady state operation of the power conversion circuit and during transient operation of the power conversion circuit. Still further, the structure of the front end rectifier circuit and its integrated solid-state circuit breaker is such that the front end rectifier bridge is selectively operable as an active front end rectifier bridge or an uncontrolled diode front end rectifier bridge.

[0049] Therefore, according to one embodiment of the present invention a power conversion circuit includes an input connectable to an AC source, a rectifier circuit connected to the input to convert an AC power input to a DC power, and a DC link coupled to the rectifier circuit to receive the DC power therefrom. The rectifier circuit comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit, wherein at least one of the upper and lower switching units on each phase leg comprises a bi-directional switching unit that selectively controls current and withstands voltage in both directions, so as to provide a circuit breaking capability that selectively interrupts current flow through the rectifier circuit.

[0050] According to another embodiment of the present invention, a method of providing circuit breaking in a power conversion circuit includes receiving an AC power at an input of the power conversion circuit and measuring or determining, via a detection circuit and logic circuit of the power conversion circuit, one or more current and voltage parameters of power provided to the power conversion circuit or present in the power conversion circuit. The method also includes comparing, via the detection circuit or logic circuit, the one or more current and voltage parameters to one or more respective current and voltage thresholds, and identifying, via the logic circuit, a fault condition in the power conversion circuit if the one or more measured or determined

current and voltage parameters exceed the one or more respective current and voltage thresholds. The method further includes controlling, via the logic circuit, a solid-state circuit breaker integrated into the power conversion circuit to interrupt current flow through the power conversion circuit upon identification of the fault condition.

[0051] According to yet another embodiment of the present invention, an ASD circuit includes an input connectable to an AC source, a rectifier bridge with integrated solid-state circuit breaker connected to the input to convert an AC power input to a DC power, and a DC link coupled to the rectifier bridge to receive a DC link voltage therefrom. The rectifier bridge with integrated solid-state circuit breaker comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit, wherein at least one of the upper and lower switching units on each phase leg is configured to control current and withstand voltage in both directions and allow for the selective interruption of current flow through the respective switching unit.

[0052] The present invention has been described in terms of the preferred embodiment, and it is recognized that equivalents, alternatives, and modifications, aside from those expressly stated, are possible and within the scope of the appending claims.

CLAIMS

What is claimed is:

1. A power conversion circuit comprising:

an input connectable to an AC source;

a rectifier circuit connected to the input to convert an AC power input to a DC power;

a DC link coupled to the rectifier circuit to receive the DC power therefrom; and

wherein the rectifier circuit comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit, wherein at least one of the upper and lower switching units on each phase leg comprises a bi-directional switching unit that selectively controls current and withstands voltage in both directions, so as to provide a circuit breaking capability that selectively interrupts current flow through the rectifier circuit.

2. The power conversion circuit of claim 1 wherein the at least one of the upper and lower switching units on each phase leg comprises:

a first solid-state switch operable in a conducting state and a non-conducting state;

a first diode in anti-parallel with the first solid-state switch;

a second solid-state switch operable in a conducting state and a non-conducting state, the second solid-state switch arranged relative to the first solid-state switch so as to comprise a reverse-blocking solid-state switch; and

a second diode in anti-parallel with the second solid-state switch and providing current blocking in an opposite direction from the first diode;

wherein the upper and lower switching units are selectively operable to interrupt current flow through the rectifier circuit, so as to provide a circuit breaking capability in the power conversion circuit.

3. The power conversion circuit of claim 2 wherein either:

each of the upper switching units and each of the lower switching units in the rectifier circuit comprises the first solid-state switch, the first diode, the second solid-state switch, and the second diode; or

one of the upper and lower switching units on each phase leg comprises the first solid-state switch, the first diode, the second solid-state switch, and the second diode, and wherein the other of the upper and lower switching units on each phase leg comprises a solid-state switch and a diode arranged in anti-parallel.

4. The power conversion circuit of claim 2 further comprising a control system comprising:

a detection circuit configured to measure or determine at least one of a voltage value and a current value at one or more locations in the power conversion circuit; and

a logic circuit operably connected to the detection circuit and configured to:

receive an input signal from the detection circuit comprising the at least one of the voltage value and the current value measured or determined thereby; and

control switching of the first and second solid-state switches between the conducting and non-conducting states based on the input so as to interrupt current flow through the rectifier circuit.

5. The power conversion circuit of claim 4 wherein, in control switching of the first and second solid-state switches, the logic circuit is configured to:

compare the at least one of the voltage value and the current value to one or more voltage or current thresholds;

identify a fault condition in the power conversion circuit if the at least one of the voltage value and the current value crosses a respective one of the one or more voltage or current thresholds; and

switch one of the first and second solid-state switches to the non-conducting state upon identification of the fault condition, so as to interrupt current flow therethrough;

wherein one of the first and second solid-state switches is switched to the non-conducting state in at least one of the upper and lower switching units on each phase leg.

6. The power conversion circuit of claim 5 wherein the logic circuit is configured to identify the fault condition in the power conversion circuit during both steady state operation of the power conversion circuit and during transient operation of the power conversion circuit, with the logic circuit switching one of the first and second solid-state switches to the non-conducting state upon identification of the fault condition to provide the circuit breaking capability in the power conversion circuit during both steady state operation and transient operation thereof.

7. The power conversion circuit of claim 4 wherein the detection circuit is configured to measure or determine at least one of three phase input currents, a current at the switching units of the rectifier circuit, a DC link current, and three phase output currents or voltages.

8. The power conversion circuit of claim 2 wherein the first and second solid-state switches comprise one of insulated-gate bipolar transistor (IGBTs), metal oxide semiconductor field effect transistors (MOSFETs), or integrated gate-commutated thyristors (IGCTs), and wherein the first and second solid-state switches are composed of silicon carbide (SiC) or gallium nitride (GaN).

9. The power conversion circuit of claim 1 wherein the rectifier circuit is selectively operable as an active front end rectifier circuit or an uncontrolled front end rectifier circuit.

10. The power conversion circuit of claim 1 further comprising at least one of:

a galvanic isolation disconnect switch located between the input and the rectifier circuit; and

a snubber circuit connected to the rectifier circuit and configured to absorb surge current in the power conversion circuit, so as to increase solid-state switch reliability and reduce electromagnetic interference.

11. A method of providing circuit breaking in a power conversion circuit, the method comprising:

receiving an AC power at an input of the power conversion circuit;

measuring or determining, via a detection circuit and logic circuit of the power conversion circuit, one or more current and voltage parameters of power provided to the power conversion circuit or present in the power conversion circuit;

comparing, via the detection circuit or logic circuit, the one or more current and voltage parameters to one or more respective current and voltage thresholds;

identifying, via the logic circuit, a fault condition in the power conversion circuit if the one or more measured or determined current and voltage parameters exceed the one or more respective current and voltage thresholds; and

controlling, via the logic circuit, a solid-state circuit breaker integrated into the power conversion circuit to interrupt current flow through the power conversion circuit upon identification of the fault condition.

12. The method of claim 11 wherein controlling the solid-state circuit breaker comprises controlling switching of a plurality of solid-state switches included in switching units positioned on a plurality of phase legs of a rectifier bridge of the power conversion circuit; and

wherein the switching units comprise an upper switching unit and a lower switching unit positioned on each phase leg of the rectifier bridge, with at least one of the upper and lower switching units on each phase leg comprising:

a pair of solid-state switches connected with one another in anti-series; and

a pair of diodes each connected in anti-parallel with a respective one of the pair of the solid-state switches, with the pair of diodes further connected in anti-series with one another.

13. The method of claim 12 wherein controlling switching of the plurality of solid-state switches comprises causing one of the pair of solid-state switches connected with one another in anti-series to become non-conductive, such that current flow through the respective switching unit is interrupted.

14. The method of claim 11 wherein the one or more current and voltage parameters comprises at least one of three phase input currents, a current at the switching units of the rectifier bridge, a DC link current, and three phase load output currents or voltages.

15. The method of claim 11 wherein controlling of the solid-state circuit breaker to interrupt current flow through the power conversion circuit is performable during both of a steady state operation of the power conversion circuit and a transient operation of the power conversion circuit.

16. The method of claim 11 wherein the power conversion circuit is operated as part of a breakdown of components test.

17. An adjustable speed drive (ASD) circuit comprising:

an input connectable to an AC source;

a rectifier bridge with integrated solid-state circuit breaker connected to the input to convert an AC power input to a DC power; and

a DC link coupled to the rectifier bridge to receive a DC link voltage therefrom;

wherein the rectifier bridge with integrated solid-state circuit breaker comprises a plurality of phase legs each including thereon an upper switching unit and a lower switching unit; and

wherein at least one of the upper and lower switching units on each phase leg is configured to control current and withstand voltage in both directions and allow for the selective interruption of current flow through the respective switching unit.

18. The ASD circuit of claim 17 wherein the at least one of the upper and lower switching units on each phase leg comprises an arrangement of one or more solid-state switches, with or without accompanying diodes, that form a bi-directional switching unit that controls current and withstands voltage in both directions and allows for the selective interruption of current flow through the respective switching unit.

19. The ASD circuit of claim 17 further comprising:

a detection circuit configured to measure or determine at least one of a voltage value and a current value at one or more locations in the ASD circuit; and

a logic circuit operably connected to the detection circuit and configured to:

receive an input signal from the detection circuit comprising the at least one of the voltage value and the current value measured or determined thereby;

compare the at least one of the voltage value and the current value to one or more voltage or current thresholds;

identify a fault condition in the ASD circuit if the at least one of the voltage value and the current value crosses a respective one of the one or more voltage or current thresholds; and

causing one of the one or more solid-state switches to become non-conductive upon identification of the fault condition, such that current flow through the respective switching unit is interrupted.

20. The ASD circuit of claim 18 wherein the at least one of the current and voltage values comprises at least one of three phase input currents, a current at the switching units of the rectifier bridge, a DC link current, and three phase load output currents or voltages.

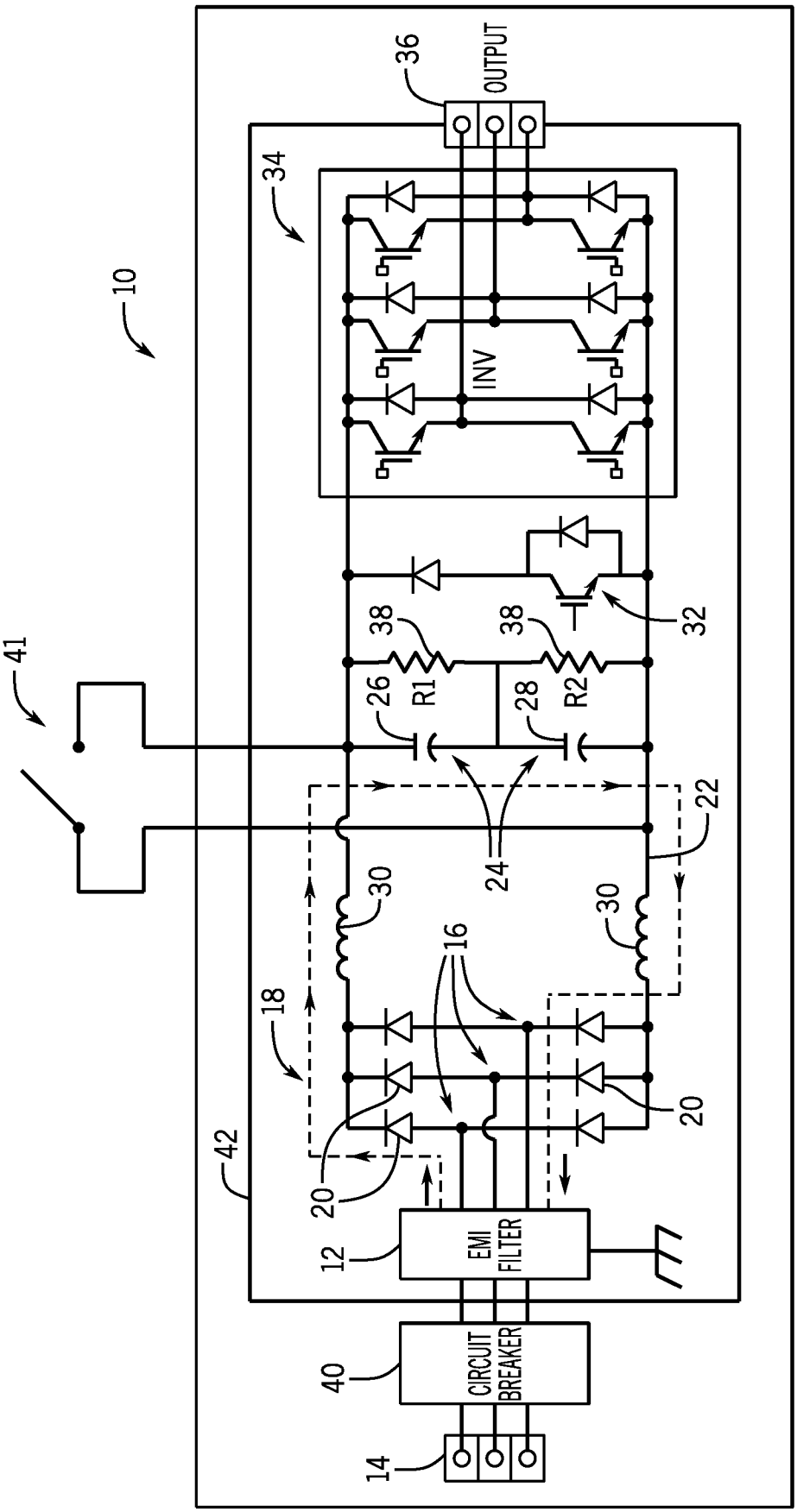


FIG. 1
PRIOR ART

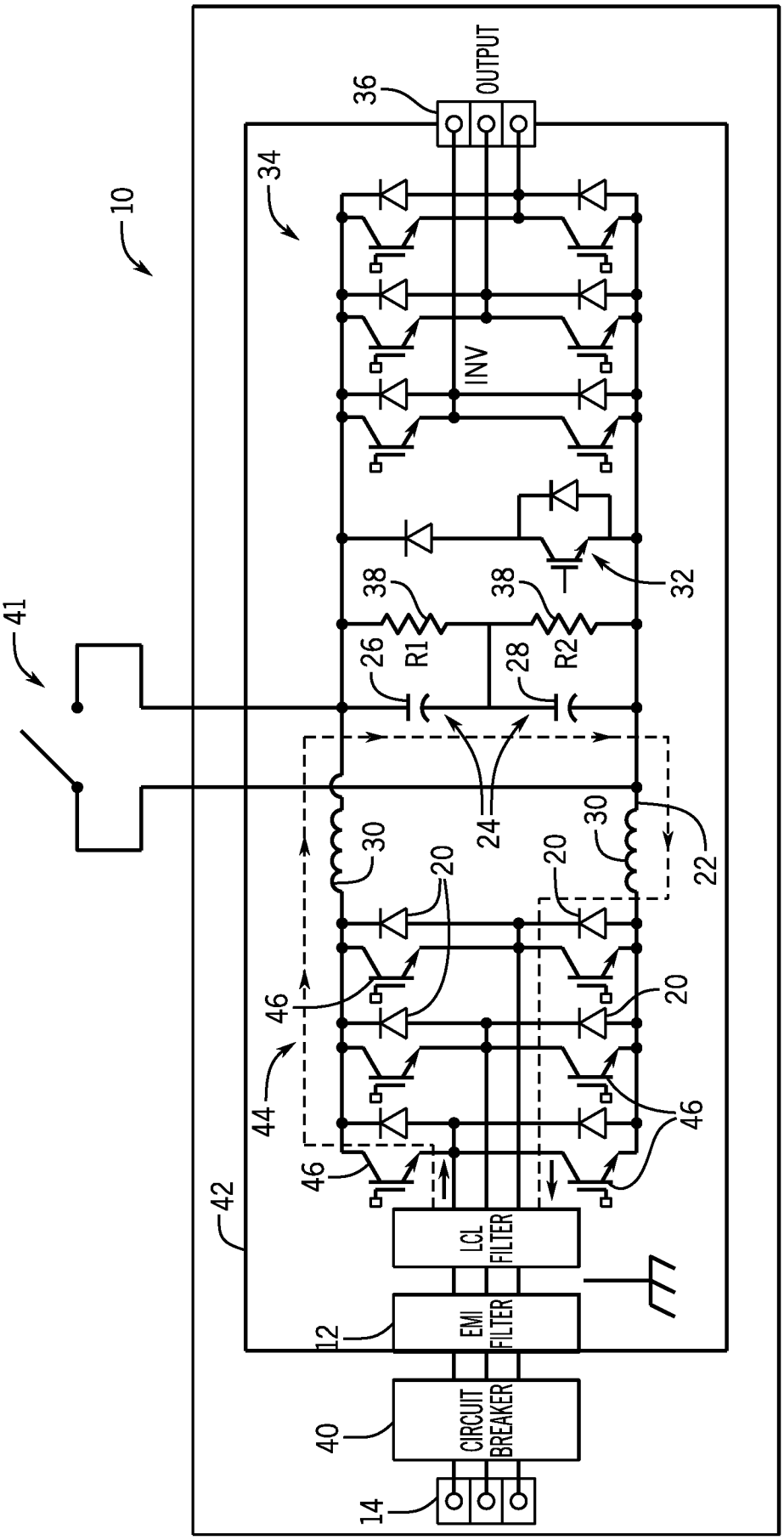


FIG. 2
PRIOR ART

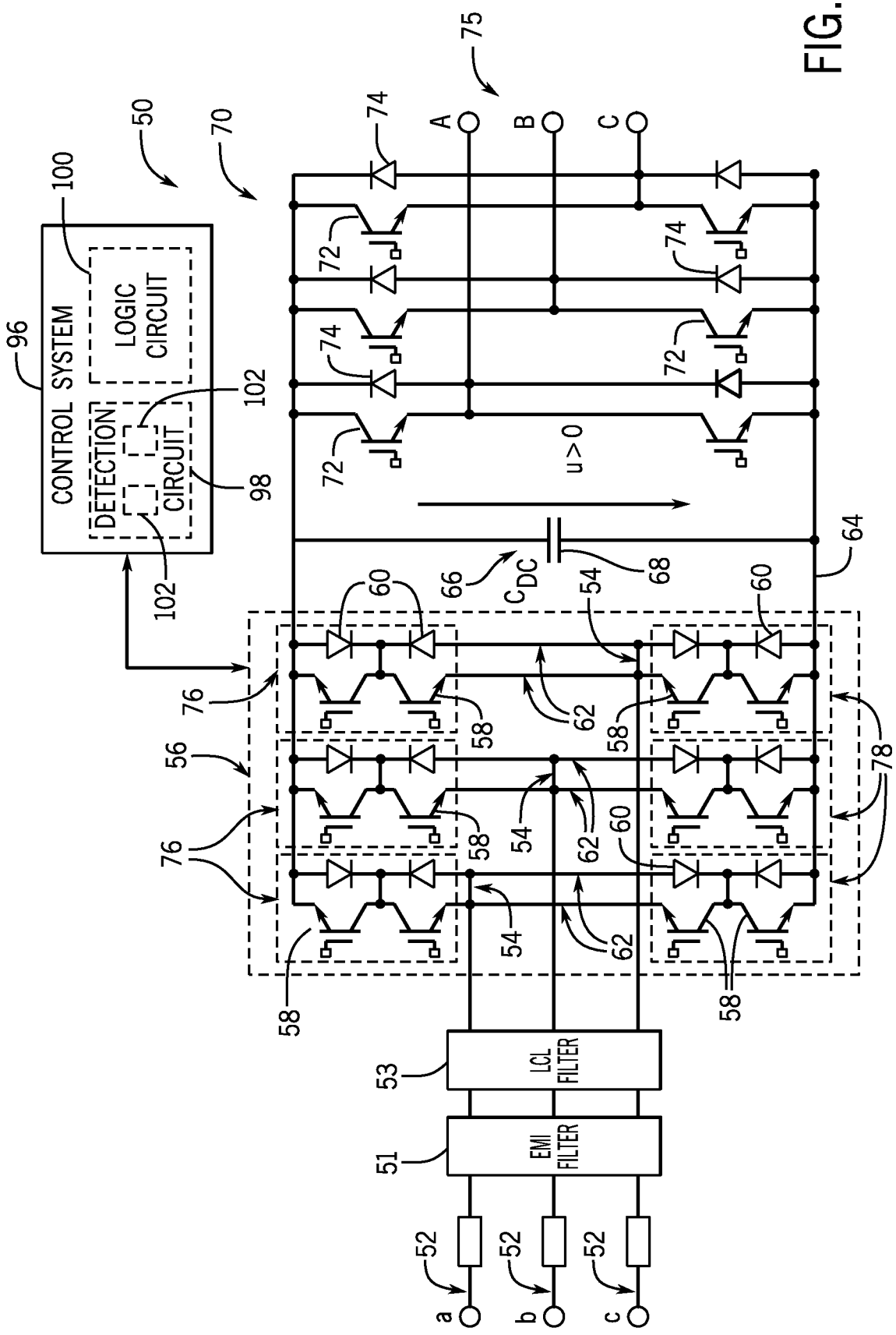

CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
u > 0
LCL FILTER
EMI FILTER
A
B
C
a
b
c

FIG. 3

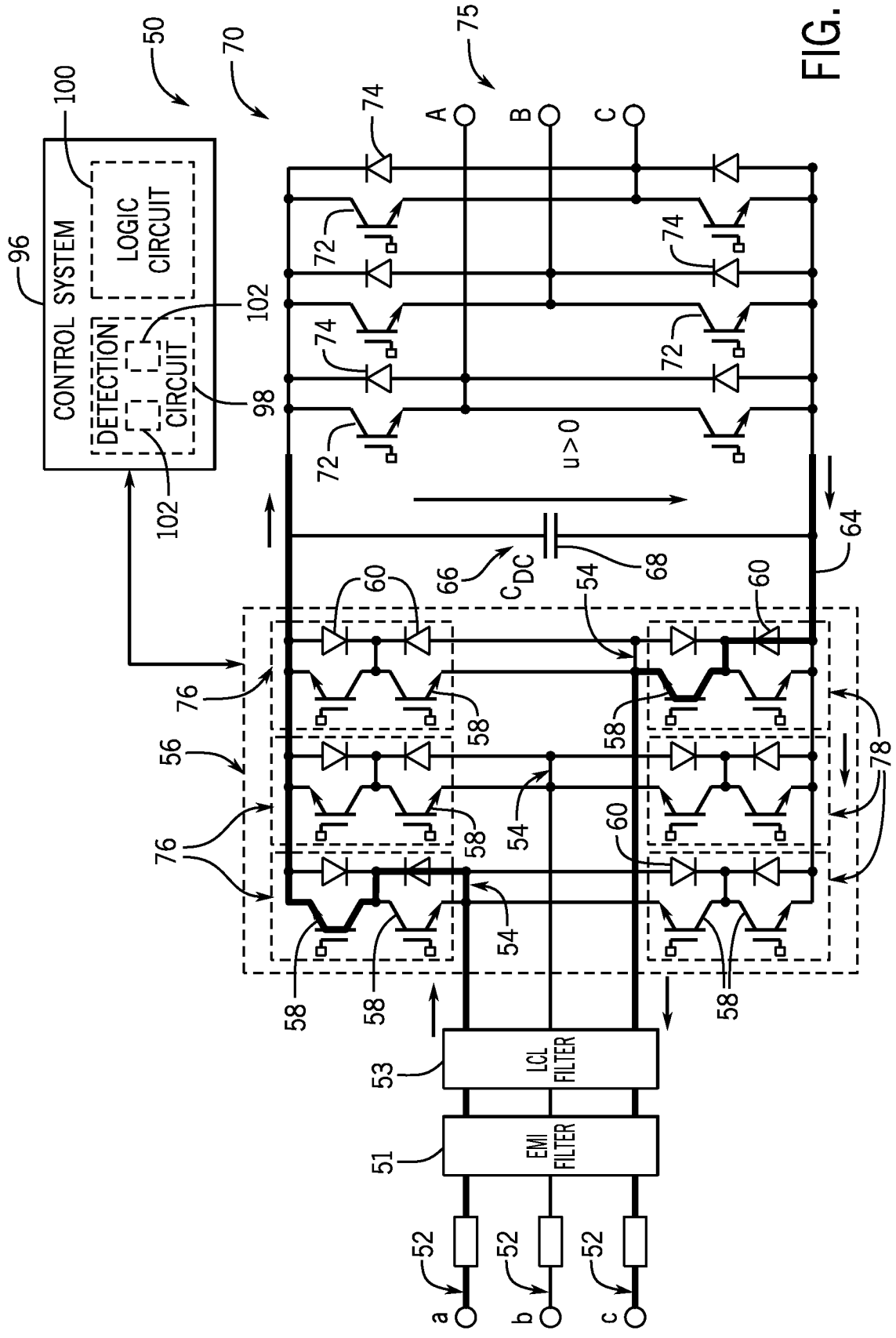

CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
LCL FILTER
EMI FILTER
u > 0
A
B
C
a
b
c

FIG. 4A

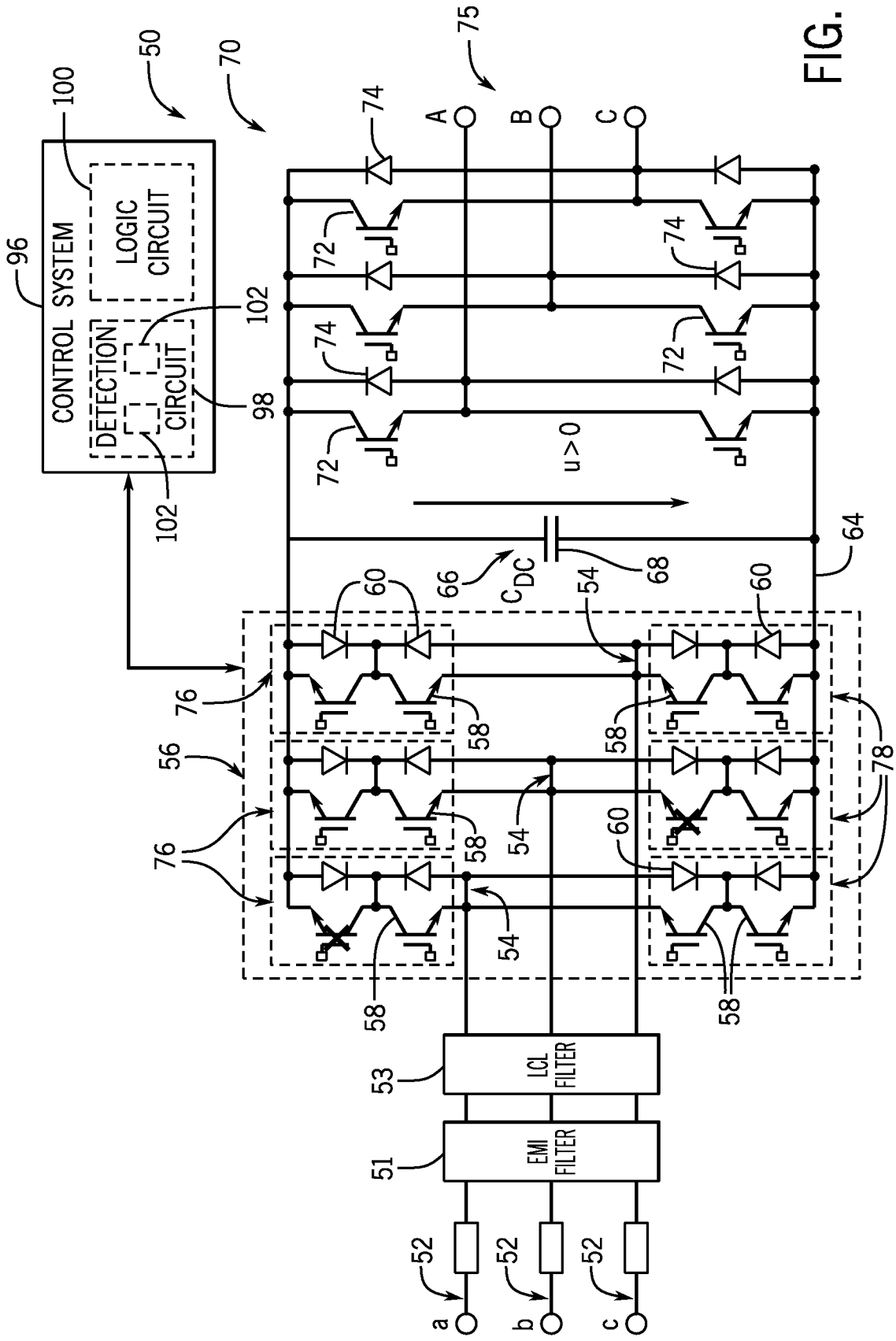

CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
u>0
C_{DC}
LCL FILTER
EMI FILTER
A
B
C
a
b
c

FIG. 4B

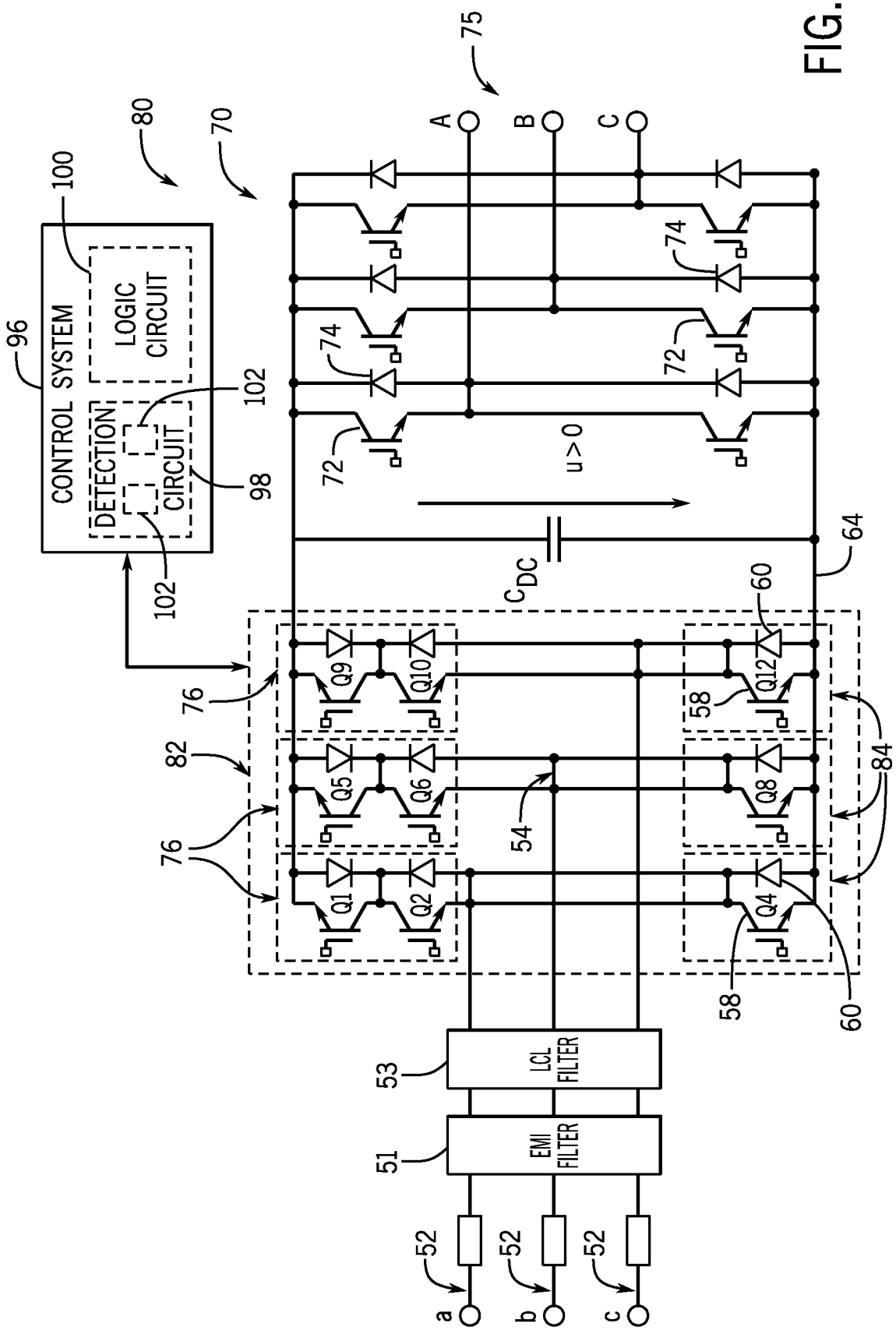

CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
u > 0
C_{DC}
LCL FILTER
EMI FILTER
A
B
C
a
b
c
Q1
Q2
Q4
Q5
Q6
Q8
Q9
Q10
Q12
72
74
75
76
80
82
84
96
98
100
102
51
52
53
54
58
60
64

FIG. 5

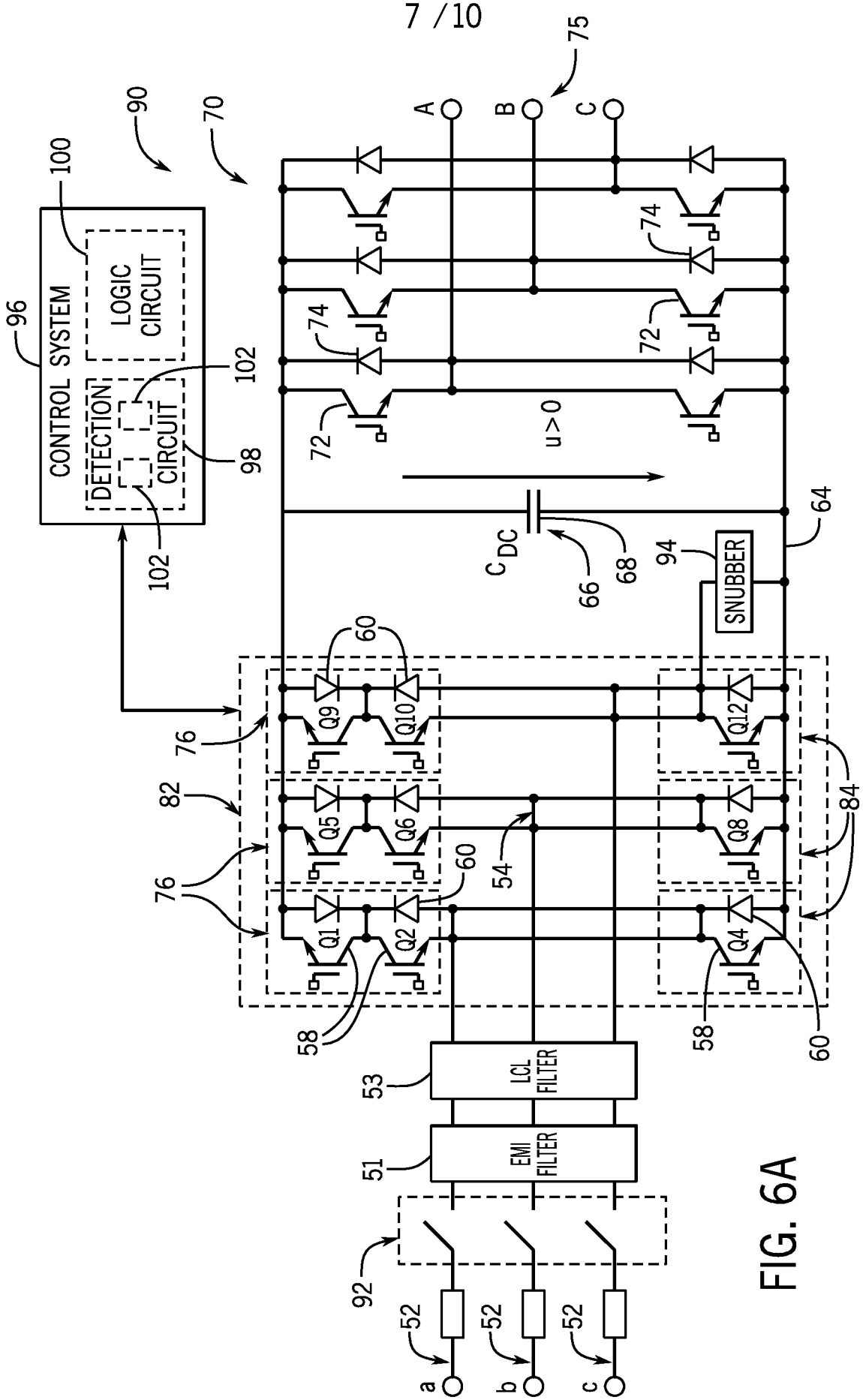

90
70
75
A
B
C
100
96
CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
102
98
102
74
72
u>0
64
C_{DC}
66
68
94
SNUBBER
60
Q9
Q10
Q12
76
82
Q5
Q6
Q8
84
54
Q1
Q2
Q4
58
53
LCL FILTER
51
EMI FILTER
92
52
a
b
c

FIG. 6A

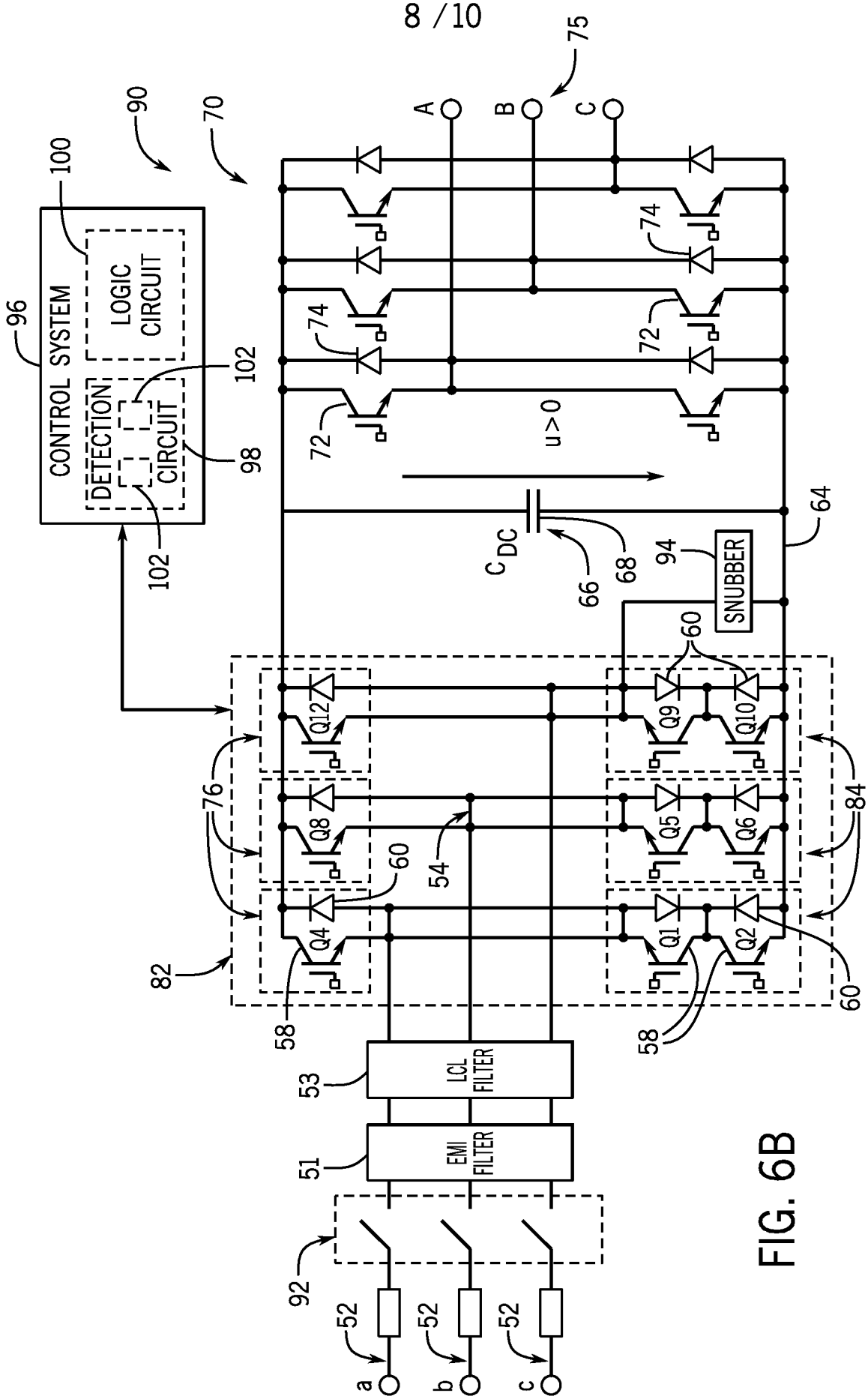

CONTROL SYSTEM
LOGIC CIRCUIT
DETECTION CIRCUIT
A
B
C
u > 0
SNUBBER
LCL FILTER
EMI FILTER
a
b
c

FIG. 6B

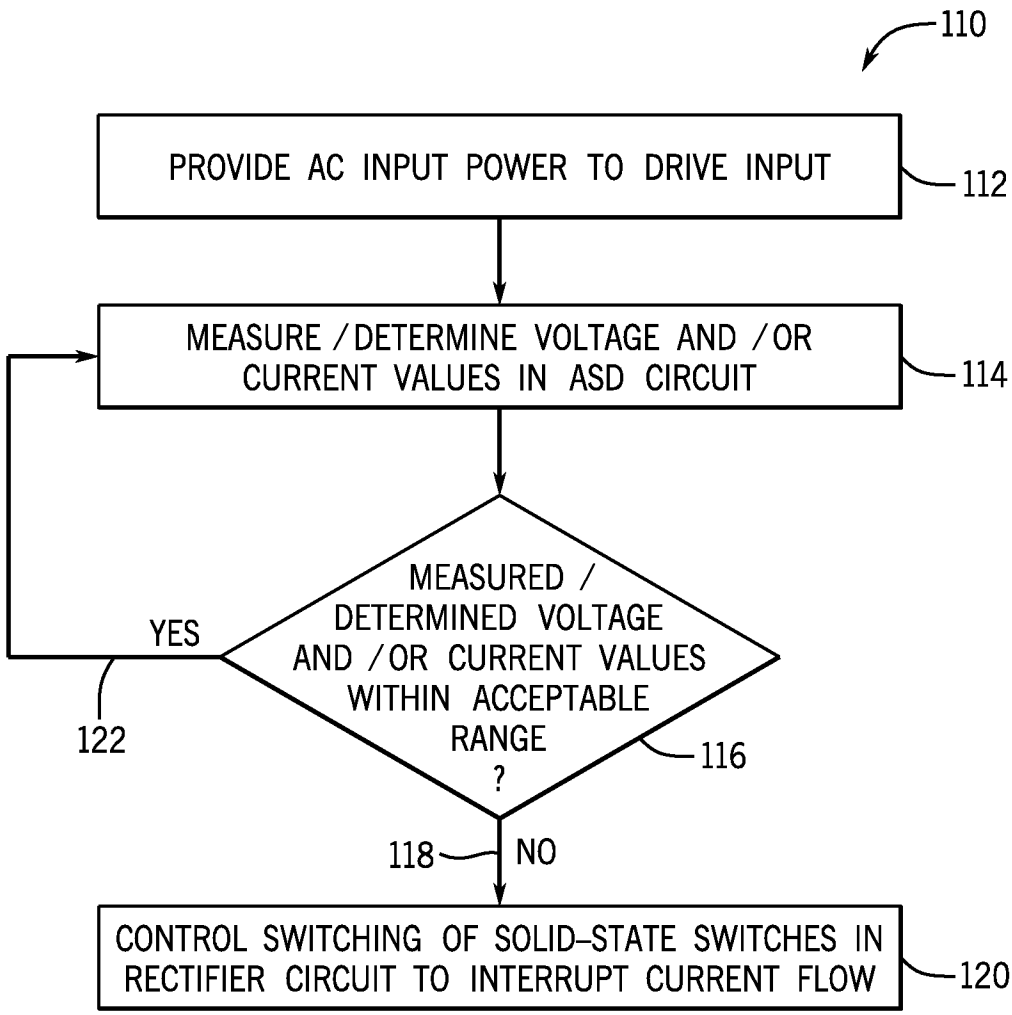

110
PROVIDE AC INPUT POWER TO DRIVE INPUT
112
MEASURE /DETERMINE VOLTAGE AND /OR CURRENT VALUES IN ASD CIRCUIT
114
MEASURED / DETERMINED VOLTAGE AND /OR CURRENT VALUES WITHIN ACCEPTABLE RANGE ?
116
YES
122
118
NO
CONTROL SWITCHING OF SOLID-STATE SWITCHES IN RECTIFIER CIRCUIT TO INTERRUPT CURRENT FLOW
120

FIG. 7

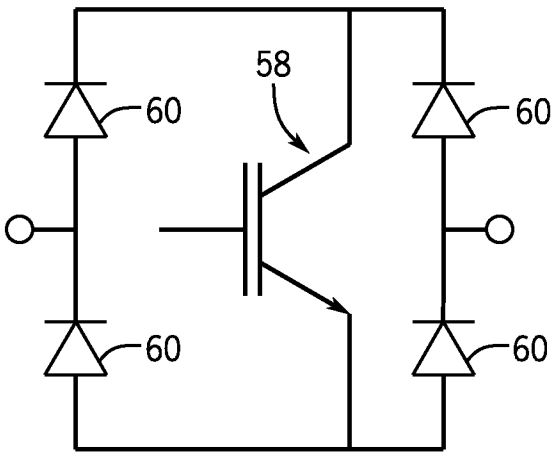


FIG. 8A

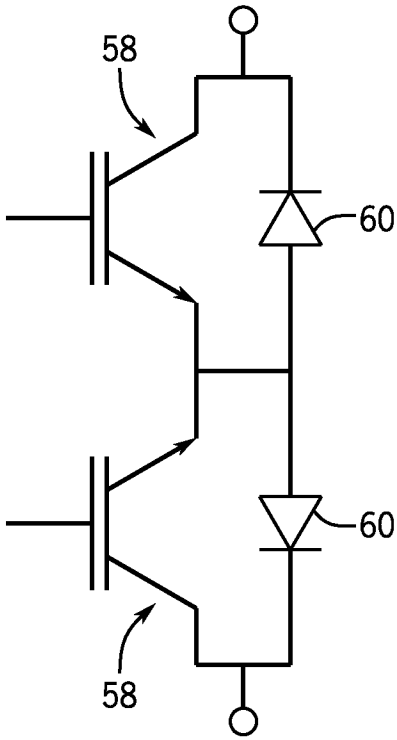


FIG. 8B

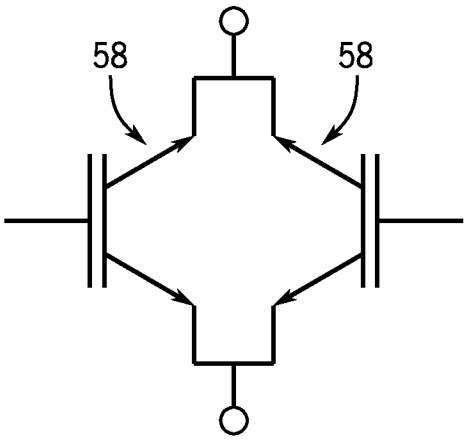


FIG. 8C

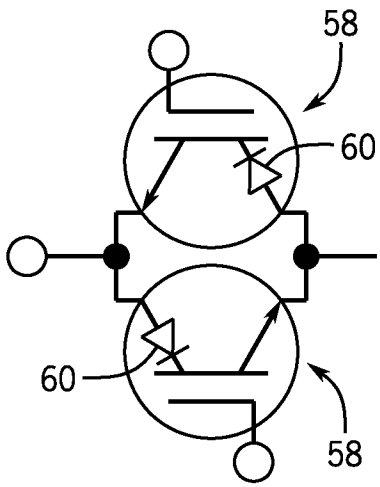


FIG. 8D

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/073401

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02H7/12 H02M1/32 H02H7/125
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02H H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 2008/137276 A1 (JOHNSON CONTROLS TECH CO [US]; SCHNETZKA HAROLD R [US]) 13 November 2008 (2008-11-13) abstract; figures 4,5,7,8 paragraphs [0002], [0312] - [0015], [0022] - [0026] -----	1,9-11, 17-20 4-7, 12-16
X	CN 105 897 005 A (UNIV NANJING AERONAUTICS & ASTRONAUTICS) 24 August 2016 (2016-08-24) abstract; figure 1 -----	1-7,9, 11-15
X	WO 2016/177398 A1 (ABB TECHNOLOGY LTD [CH]) 10 November 2016 (2016-11-10) abstract; figures 1,9-11 page 21, lines 16-23 page 22, line 25 - page 23, line 11 ----- -/--	1,9-11

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 November 2018	05/12/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Palukova, Mila

2

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/073401

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2016/024223 A1 (INESC PORTO INST DE ENGENHARIA DE SIST S E COMPUTADORES DO PORTO [PT]) 18 February 2016 (2016-02-18)	1-3,8
Y	page 9, line 15 - page 11, line 11; figures 1-5	4-7, 12-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/073401

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2008137276 A1	13-11-2008	TW 200913424 A	16-03-2009
		US 2010229580 A1	16-09-2010
		WO 2008137276 A1	13-11-2008
CN 105897005 A	24-08-2016	NONE	
WO 2016177398 A1	10-11-2016	CN 107580751 A	12-01-2018
		EP 3292624 A1	14-03-2018
		US 2018091038 A1	29-03-2018
		WO 2016177398 A1	10-11-2016
WO 2016024223 A1	18-02-2016	EP 3180849 A1	21-06-2017
		JP 2017528102 A	21-09-2017
		US 2017229972 A1	10-08-2017
		WO 2016024223 A1	18-02-2016