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[54] ELECTRONIC LOCK SYSTEM

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Related U.S. Application Data

[63] Continuation of Ser. No. 132,671, April 9, 1971, abandoned.

[52] **U.S. Cl.** ..... **340/149 A,** 340/149 R
[51] **Int. Cl.** **H04q 9/00**
[58] **Field of Search** ..... 340/149 A

[56] **References Cited**

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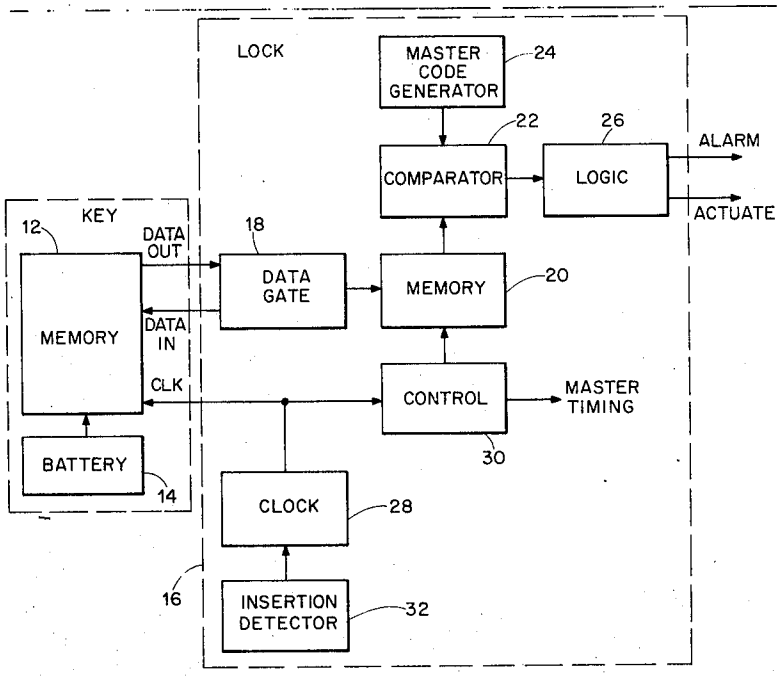
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[57] **ABSTRACT**

An electronic lock system in which a coded data word is stored in a key and, upon insertion of the key into a lock, compared with a master code, a positive comparison providing actuation of the lock. Lack of correspondence between the key code and the master code causes actuation of an alarm and can also cause seizure of the key in the lock. Digital circuitry is employed in both the key and lock and is configured to permit easy alteration of the stored code to greatly enhance system security. Only four interconnections need couple the key to the lock and the stored key code can be selectively altered to further enhance system security.

23 Claims, 5 Drawing Figures



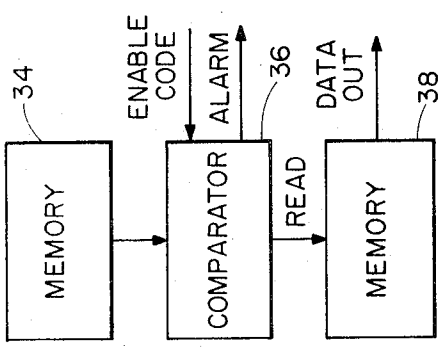


Fig. 2.

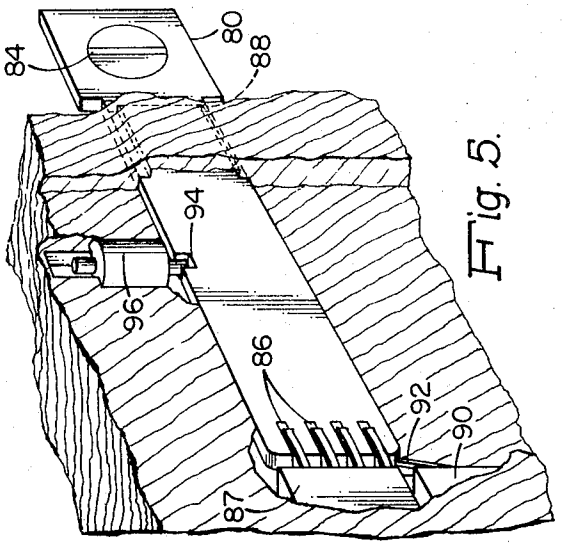


Fig. 5.

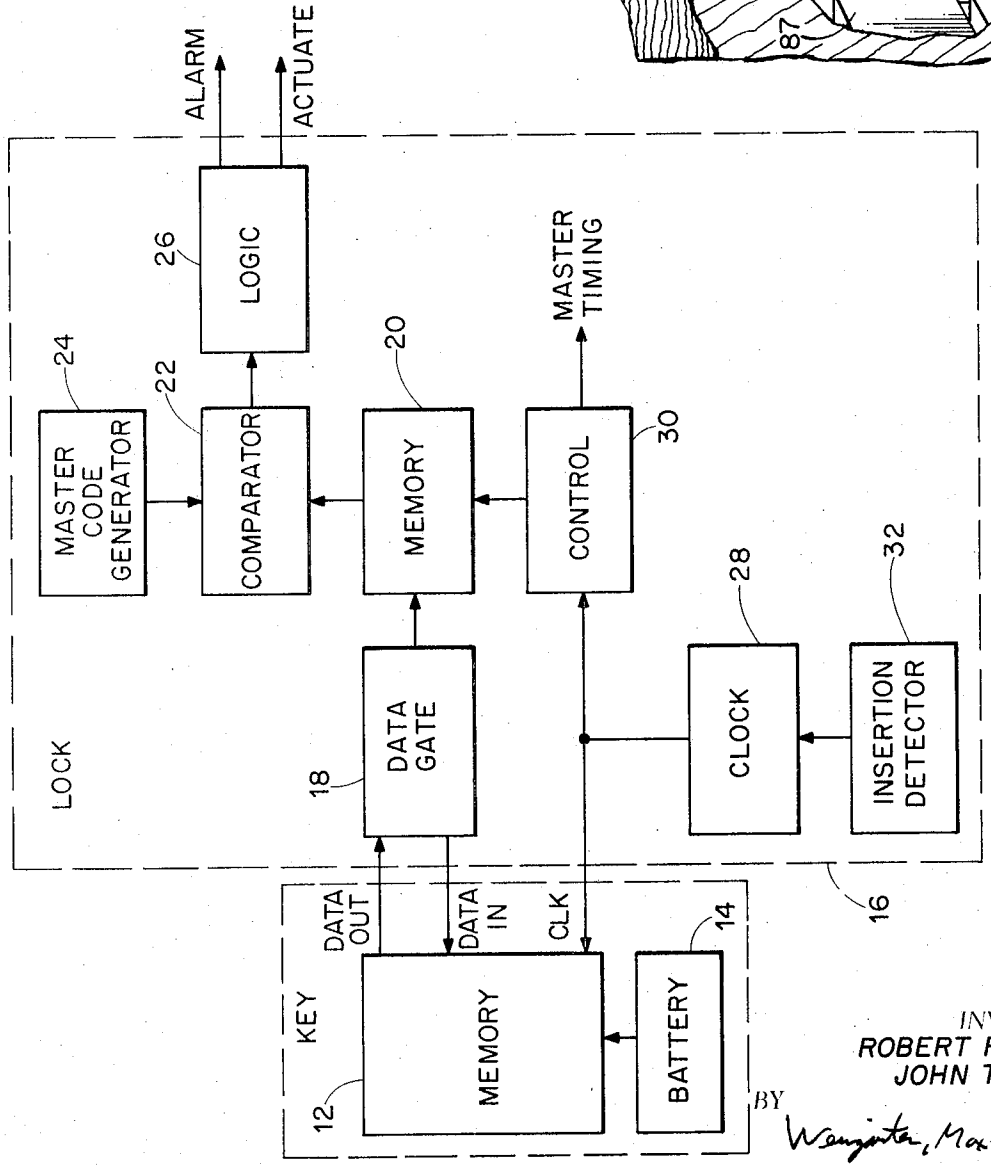


Fig. 1.

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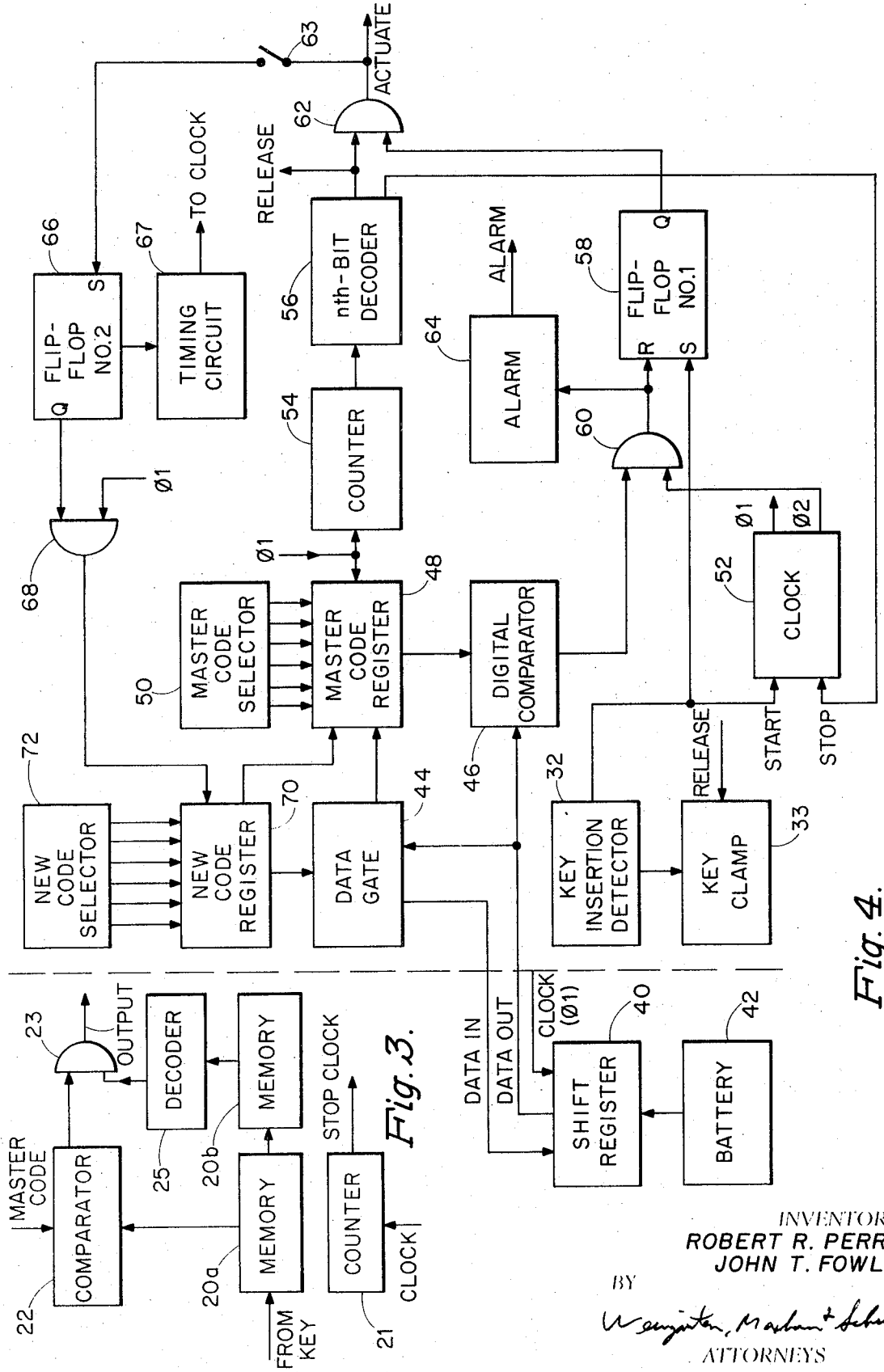


Fig. 3.

Fig. 4.

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ELECTRONIC LOCK SYSTEM

REFERENCE TO RELATED APPLICATIONS

This application is a continuation of Ser. No. 132,671 filed Apr. 9, 1971 and now abandoned.

FIELD OF THE INVENTION

This invention relates to lock systems and more particularly to an electronic lock system employing active digital electronic circuitry in both the key and lock.

BACKGROUND OF THE INVENTION

Electronic locks have been proposed in which an electronic circuit in a lock is energized to activate the lock by use of a key containing circuitry cooperative with the lock circuit. The circuitry employed in a key has generally been of a type in which a plurality of coded interconnections are provided to appropriately energize an associated lock circuit. Such key circuitry, however, usually contains a fixed code which is alterable only by rewiring of the key circuit. There is little versatility of coding in such conventional systems. In addition, the configuration of the key circuit can be ascertained by appropriate analysis and the code thereby duplicated. As a further disadvantage, such keys usually require a relatively large number of interconnections with the lock, with attendant increase in system cost and complexity.

SUMMARY OF THE INVENTION

In accordance with the present invention, a highly reliable and secure electronic lock system is provided in which active data storage means are provided within a key containing a readily alterable coded data word corresponding to a master code stored in an associated lock circuit. Upon insertion of the key into the lock, the data stored in the key is compared with a master code in the lock, identity therebetween causing actuation of the lock. In the event that there is not exact comparison between the master code and the key code, an alarm can be actuated and the key seized within the lock to prevent its removal therefrom. By immediate actuation of an alarm in the event of detection of one or more incorrect bits of the key code, there is little opportunity to attempt duplication of the key code and thereby materially enhancing the security of the system. Analysis of the data storage circuitry within the key will not reveal the data code stored therein and even if the stored data were read out by interrogation of the key, the data can be selectively coded such that it would be, in practice, substantially impossible to analyze and decode the data content thereof.

In a typical embodiment of the invention, the key contains a multiple bit shift register for storing the key code and is typically of the integrated circuit type having extremely low energy requirements. Power is provided by a small battery source located within the key. Alternatively, the shift register can be of the nonvolatile type requiring no external power, in which case no battery need be employed. Only four connections are required between the key and the associated lock; one for transferring data from the key to the lock, one for transferring data from the lock back into the key, a ground connection and a clock line. Such connection can be made by various electrical contact elements

suited to particular system requirements or, as an alternative, connection can be made inductively.

DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. **1** is a simplified block diagram representation of a lock system according to the invention;

FIG. **2** is a block diagram of an alternative key circuit embodying the invention;

FIG. **3** is a partial block diagram of an alternative lock circuit embodying the invention;

FIG. **4** is a more detailed block diagram of a lock system according to the invention; and

FIG. **5** is a pictorial view, partly in section, illustrating a typical key configuration embodying the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1** there is shown an electronic key **10** having a memory **12** powered by a suitable energy source such as a battery **14.** The memory is typically a shift register of the low power type constructed by monolithic integrated circuit techniques and is, therefore, of extremely small physical configuration capable of being readily mounted in a small key member. The battery is typically a low power mercury battery also adapted for mounting in the key member and capable of energizing memory **12** for a long period of time. The power requirements of an integrated circuit shift register are sufficiently small that the effective life of battery **14** is determined more from the shelf life thereof rather than the power drain. The key **10** is cooperative with an electronic lock **16** and is coupled thereto by three lines, labeled data out, data in and clock. The data out line carries data from memory **12** to the lock circuit, the data in line carries data from the lock circuit back into memory **12,** and the clock line carries clock pulses for shifting of data in and out of memory **12.** In actual implementation, a ground line would also interconnect key **10** and lock **16.**

The lock circuit **16** includes a data gate **18** connected to a memory **20,** and operative to couple data from memory **12** to memory **20,** and to recirculate data from memory **12** back into memory **12** for restorage of a key code therein. The memory **20** has an output thereof coupled to a comparator **22** which also receives data from a master code generator **24.** The output of comparator **22** is connected to logic circuitry **26** which provides a first output signal for actuation of associated utilization means, and a second output signal for providing an alarm indication in the event that an improper key code is employed.

Memory **20** and associated components of the lock **16** can also be typically implemented by integrated circuits. Timing of data from the key to the lock circuit is accomplished by means of a clock **28** providing clock signals to memory **12** and to a control circuit **30** which governs operation of memory **20** and also provides master timing signals to the lock system. An insertion detector **32** is provided in the lock for sensing the presence of key **10** therein and for providing in response to key detection a start signal to clock **28** for initiation of the key identification process. As will be described, the insertion detector **32** can also cause mechanical clamping of the key within the lock to prevent its premature withdrawal during the code recognition cycle and also

to capture the key in the event that an improper key code is detected.

In operation, a multiple bit data word specifying a key code is stored in memory **12** representative of a unique key identity, this code being identical to a master code provided by generator **24** located in the lock circuitry. The key code contained within memory **12** is compared with the master code, positive identity between the two codes enabling actuation of the lock. Non-correspondence between one or more bits of the key code and the master code causes actuation of an alarm indicating an attempt to utilize an improper key. Upon insertion of key **10** into lock **16,** the presence of the key as determined by insertion detector **32** causes enabling of clock **28.** Clock pulses from clock **28** are applied to memory **12** and cause readout of the data stored therein to data gate **18** and thence to memory **20.**

The data being shifted out of memory **12** is also recirculated via data gate **18** back into memory **12** to reload the key code for subsequent use. Upon loading of the data word into shift register **20,** comparator **22** is operative to compare the data contents of register **20** with that of master code generator **24** and to provide output signals to logic **26** indicative of whether or not the coded data from key **10** is identical to the master code pattern. Comparison of the key code with the master code can be accomplished on a bit by bit basis or on the entire code word after it is shifted into comparator **22.** If upon comparison between the master code and the key code there is identical correspondence of all bits therebetween, logic **26** provides an output signal to actuate the associated lock or other utilization means. It will be appreciated that the lock **16** can be associated with any utilization means which is to be key operated, such as a locking mechanism for a door, vault or the like, or electrical apparatus. If there is a lack of correspondence between one or more bits of the master code and the key code, logic **26** provides an alarm signal indicative of an erroneous key code. The alarm signal can immediately actuate an alarm indicator or can be employed with suitable counting circuitry to permit a selected number of decoding attempts before an alarm is actuated. Delayed alarm actuation is useful, for example, to prevent a transient condition such as momentary contact loss from causing an alarm.

The security of the present system is considerably enhanced by the feature wherein any attempt to employ an incorrect key code will serve to actuate an alarm. There is thus no opportunity to try different possible key codes in an attempt to actuate the lock, as the first wrong code will cause an alarm indication. It is possible to cause readout of data stored in memory **12** to ascertain its data content and thereby reproduce the key code. However, a key code can be employed as part of the data in memory **12** such that interrogation thereof will not reveal the key code. For example, data stored in memory **12** can be configured such that the code itself is contained at predetermined bit positions within a longer stored word and coding schemes can be selected which are extremely difficult if not practically impossible to decode. The length of the data word stored in memory **12** also serves to enhance security of the system; for example a 32 bit memory permits 2^{32} possible coding combinations.

System security can be further enhanced by use of a key which communicates data to the lock circuit only upon receipt by the key of a proper interrogation code. Such a technique is illustrated in FIG. **2** which shows a first memory **34** coupled to a comparator **36** which, in turn, is coupled to a second memory **38.** Each of the memories **34** and **38** are typically integrated circuit shift registers as described above. The memory **34** contains a predetermined code word which is compared in comparator **36** with an enable code which can be provided by the lock circuit. Upon detection by comparator **36** of identity between the enable code and the code stored in memory **34,** a read command is provided to memory **38** to cause readout of a different code stored in memory **38.** The code word from memory **38** is operative to actuate the lock after identity is established between this code and the master code stored in the lock circuit, as described above.

Upon interrogation of the key by an enable code which does not compare with the preprogrammed data in memory **34,** comparator **36** can provide an alarm signal to the associated lock circuit. An alarm indication can also be provided as above upon non-identity between the master code in the lock and the code from memory **38.** The technique of FIG. **2** thus affords a dual encoding arrangement which is of a higher order of security than the coding arrangement of FIG. **1.** Additional levels of coding can also be readily provided according to the principles of this invention since small, low power digital circuitry can achieve the key function.

In addition to storage in the key of a key identification code for gaining access to the associated lock, the key can also contain additional data representing the identity of the particular key, an account number or the like. The system disclosed in FIG. **1** can be modified as indicated in FIG. **3** to accommodate such additional identification data. Referring to FIG. **3,** data from a key is composed of a first word representing the key code and a second word representing other data such as a key number. This data is applied from the key to a pair of memory stages. The key code word is stored in memory **20***a* while the other identification code is stored in **20***b*. The key code is compared with the master code in comparator **22** in the same manner as described hereinabove.

The output of the comparator is applied to one input of an AND gate **23.** The output of memory **20***b* is applied to a decoder **25,** the output of which is applied to the second input of AND gate **23.** The code processing cycle is governed by a counter **21** operative in response to clock signals from clock **28,** the counter providing a timing sequence sufficient for loading data from the key into memories **20***a* and **20***b*. Upon identification of the key code in comparator **22,** an output signal is provided by AND gate **23** for actuation of the lock. Failure to detect a proper key code will prevent a lock actuation output. In the embodiment of FIG. **3** failure to detect a proper code in memory **20***b* will also prevent lock actuation. It is evident that an output signal from decoder **25** representative of the additional identity code stored in the key can be employed to record such key identity, for example to denote the time that a particular key was employed with the associated lock.

A more particular embodiment of the invention is illustrated in FIG. **4.** The key includes and has disposed therein a shift register **40** typically of the monolithic integrated circuit type and capable of storing a predetermined number of data bits which comprise a key code.

Register **40** is powered by a suitable battery **42** which is also of small physical size to fit within a key element. Data from shift register **40** is communicative with the lock circuit by way of a data gate **44** operative to recirculate data back into shift register **40** to retain the same key code, or to load register **40** with new data to provide a new key code, as will be described.

Data from register **40** is applied to a digital comparator **46** which also receives information from a master code register **48.** Register **48** contains a master code word as provided by a master code selector **50,** which is used for comparison with the key code contained in the shift register **40.** System timing is governed by a clock **52** which is started upon receipt of a start signal from a key insertion detector **32,** such as described above. Detector **32** also energizes key clamp **33** which captures the key in the lock during the identification cycle. A clock provides two output signals, labeled respectively ϕ_1 and ϕ_2, which are clock pulses recurring at the same clock rate but shifted in phase one from the other by a predetermined amount, typically 180°. The clock pulses ϕ_1 are advanced in phase from the clock pulses ϕ_2 and are employed to control data bit transitions, while the delayed clock pulses ϕ_2 are employed to control bit comparisons. Thus it will be appreciated that bit comparisons are accomplished at the midpoint of a bit interval to assure that such comparisons are performed after transients which may occur during bit transitions.

The clock pulses ϕ_1 are applied to register **48** and also to a counter **54** operative to count the number of bits shifted out of register **48.** By means of a counter decoder **56,** the last bit shifted out of register **48** is recognized to denote the end of the code comparison process. The key insertion detector **32** is operative to clamp the key in the lock to prevent its premature removal prior to completion of the decoding process. Detector **32** also provides a signal to flip-flop **58** to set the flip-flop to one logical state, the output signal thereof being applied to one input of an AND gate **62.** Data in key register **40** and master register **48** are clocked out bit by bit by clock pulses ϕ_1 and are compared bit by bit in comparator **46.** The comparator is operative to provide a first output, say zero, if the bit from the key register is identical to the bit from the master register, and to provide a second output, say one, if there is not correspondence between the received data bits. The output of comparator **46** is coupled to an AND gate **60** which also receives the clock pulses ϕ_2, the output of gate **60** being applied to the reset input of flip-flop **58.** The output of flip-flop **58** is coupled to one input of an AND gate **62,** the other input of which is the output signal from counter decoder **56** for enabling gate **62.**

Upon correspondence between a data bit from key register **40** and a date bit from master register **48,** AND gate **60** will remain disabled and no reset signal will be applied to flip-flop **58.** Thus, flip-flop **58** remains in its set state so long as there is identity between the key code and the master code providing an output signal to gate **62.** Upon detection of the last bit of the master code by decoder **56,** an output signal is provided therefrom to AND gate **62** to enable the gate and cause a signal for lock actuation. The signal from decoder **56** is also employed to release key clamp **33** to permit removal of the key from the lock. The output signal from gate **62** is the system output signal for activating the associated lock or other utilization means upon detection of a proper key code.

If, during comparison of any bit of the key code, a lack of identity is found between this bit and the associated bit of the master code in register **48,** the output signal from comparator **46** will cause enabling of AND gate **60** and consequent resetting of flip-flop **58** which causes removal of the flip-flop output signal to gate **62.** No actuation signal can be provided by reason of the disabling of gate **62.** An output signal from gate **60** is provided only upon detection of an error between a bit of the key code and a corresponding bit of the master code, and this output signal is also employed to activate an alarm circuit **64** to indicate detection of an erroneous key code. Upon sensing of an alarm condition, a stop signal can be generated by alarm circuitry **64** to stop clock **52** and discontinue the decoding process and to prevent release of the key clamped in the lock by clamp **33.**

In one mode of operation, the master code stored in register **48** is recirculated back into this register so that the code is available for subsequent data comparison. Similarly, the code in shift register **40** is recirculated therein by means of data gate **44** so that the same key code can later be employed. To further enhance the security of the novel lock system, however, the invention is also operative in another mode wherein the code residing in shift register **40** and master code register **48** is replaced with a new code. Such new code can be replaced on a regular basis or from time to time depending on particular security requirements.

To employ such a new code, the output signal of gate **62** provided upon identity between the key code and the master code, is applied via a switch **63** to set a flip-flop **66,** one output of which is employed to energize a timing circuit **67** which, in turn, provides a start signal to clock **52.** The other output of flip-flop **66** is applied to an AND gate **68** which also receives clock signals ϕ_1. The output of gate **68** is applied to the clock input of a new code register **70** which has stored therein a new data code provided by a new code selector **72.** The output of new code register **70** is applied to data gate **44** for coupling of such new data into key shift register **40.** The new data is also applied to the master code register **48** for use in a subsequent data comparison. In this latter mode of operation, clock **52** is enabled for only a sufficient period of time determined by timing circuit **67** to permit shifting in the new code data into the key shift register **40** and to prevent reinstitution of the digital comparison process until the key is again inserted into the lock at a subsequent time.

The new code selector **72** can be implemented in several different ways and can include a binary word generator which is manually actuable such as by an array of switches, or automatically actuable for example by means of a computer. By use of a digital computer a new key code can be provided from a random number sequence generated by the computer such that the code is readily identifiable only in computer memory and need not be known to operating personnel in order to alter the key code. The master code can be updated immediately after completion of a particular decoding process or, alternatively, can be updated on a periodic basis. For example, in some circumstances it is desirable to reprogram the key code immediately after use of the key and to reprogram the master code on a daily basis to permit use of the key only once per day.

The key can be implemented in a variety of mechanical configurations to suit particular operating requirements. The key can, for example, be in a form much like an ordinary mechanical key as illustrated in FIG. **5.** In this instance the key **80** is formed of a nonconductive material such as an epoxy and has the storage register **82** encapsulated therein. The battery in the form of a small button cell is contained within a battery compartment located in the handle portion of key **80,** access thereto being provided by a removable cover **84.** Electrical connection is provided at the distal end of key **80** by means of four conductive bands **86** provided on the end thereof each being of generally U-shaped configuration as illustrated.

The key is inserted within a keyway **88** of an associated lock, the contact bands **86** being cooperative with an electrical connector **87** disposed at the inner end of the keyway to provide connection between the key and the lock circuitry. Also disposed at the inner end of the keyway is a microswitch **90** which includes an actuation arm **92** disposed for actuation by the end of key **80** upon its insertion into the lock. The switch **90** is part of insertion detector **32** (FIG. **1**) and is operative to provide a key insertion signal to the system clock for commencement of the key decoding process. A notch **94** is provided in one side of key **80** and is cooperative with a rod **94** associated with solenoid **96** to prevent removal of the key during the decoding process. The solenoid **96** is typically energized by a signal from key insertion detector **32.**

As described hereinabove, an alarm signal is provided by the invention in the event that there is lack of comparison between the key code and the master code of the lock. Premature withdrawal of the key could also cause an alarm condition and to prevent such an occurrence, the key is clamped within the lock by solenoid **96** until completion of the decoding cycle. The key can also be retained in the lock in the event that an erroneous code is detected to prevent its removal in such event. The key code can be arranged such that the first bit to be read out of the key is always of ground potential such that ground potential exists on all terminal contacts **86** when the key is not in use, to thereby prevent accidental shorting of the key which could destroy the stored data. The key terminals could alternatively be deactivated when the key is not in use by a suitable switch arrangement.

From the foregoing it will be evident that an electronic lock system has been provided which is both reliable and highly secure and which can be constructed in an efficient and commerically realistic manner. Various modifications and alternative implementations will occur to those versed in the art without departing from the spirit and true scope of the invention. For example, data can be conveyed from the key memory to the lock in a parallel rather than a serial manner, and various levels of coding can be provided to suit the desired level of security. The electronic circuitry and its mechanical housing can take a wide variety of forms adapted to specific installation requirements. Accordingly, it is not intended to limit the invention by what has been particularly shown and described, except as indicated in the appended claims.

We claim:

1. An electronic lock system comprising:

a key including a structural member adapted for engagement with an associated lock and an electronic data memory therein having a plurality of interconnected stages operative to store an electrically alterable multiple bit key code and terminal means for coupling said key to an associated lock by which said key code can be conveyed from said electronic data memory in response to a clock signal;

a lock adapted for operation with said key and including a receptacle for receiving the structural member of said key in operative engagement therewith;

an electronic data memory for storing a multiple bit master code;

means for comparing said key code stored in said key data memory with said master code stored in said master code memory;

clock means for providing a clock signal to said key data memory to cause readout of said key code to said comparison means for comparison of said key code with said master code;

said comparison means being operative to provide an output indication upon receipt of a key code from said key data memory corresponding to said master code; and

logic means receiving said output indication from said comparison means and operative in response thereto to provide an output signal.

2. An electronic lock system according to claim **1** wherein:

said comparison means is also operative to provide a second output indication upon receipt of a key code from said key data memory which does not correspond to said master code;

and said logic means is operative in response to said second output indication to provide a second output signal.

3. An electronic lock system according to claim **1** wherein said lock includes means operative after comparison of said key code with said master code for reentering a key code into the electronic data memory of said key.

4. An electronic lock system according to claim **1** wherein said lock includes:

means for detecting the presence of said structural member in operative position with said lock receptacle and for providing a signal indication of key presence; and

means operative in response to said key presence signal indication to initiate comparison of said key code with said master code.

5. An electronic lock system according to claim **2** wherein said lock includes means within said receptacle for preventing removal of said key therefrom during comparison of said key code with said master code.

6. An electronic lock system according to claim **5** wherein said removal preventing means is operative in response to said second output indication from said comparison means to capture said key in said lock receptacle upon non-identity between said key code and master code.

7. An electronic lock system according to claim **2** wherein said comparison means is operative to compare said key code and said master code on a bit by bit basis and to provide said second signal indication upon detection of a bit of said key code which does not compare with the corresponding bit of said master code.

8. An electronic lock system according to claim 1 wherein said key data memory is of a data capacity to store predetermined data in addition to said key code;

and wherein said lock includes:
a second electronic data memory for storing said predetermined additional data received from said key;

decoding means coupled to said second data memory and operative to provide an output signal in response to said predetermined data in said second data memory; and
gate means operative in response to the presence of both said output indication from said comparison means and said output signal from said decoding means to provide a utilization signal.

9. An electronic lock system comprising:
a key having a structural member adapted for engagement with an associated lock and including therein:
a first electronic data memory having a plurality of interconnected stages operative to store an electrically alterable multiple bit key code;
a second electronic data memory having a plurality of interconnected stages operative to store a predetermined multiple bit code different than said key code; and
comparator means coupled to said first and second electronic data memories and operative to compare said predetermined code in said second data memory with an enable code provided by said lock and to provide in response to correspondence between said enable code and said predetermined code a command signal to said first data memory to cause readout of said key code stored therein to said lock;
a lock adapted for operation with said key and including:
a receptacle for receiving the structural member of said key in operative engagement therewith;
an electronic data memory for storing a multiple bit master code;
means for comparing said key code with said master code and to provide a signal indication upon receipt of a key code which corresponds to said master code; and
logic means receiving said signal indication from said lock comparing means and operative to provide an output signal in response thereto.

10. An electronic lock system according to claim 9 wherein:
said lock comparing means is also operative to provide a second signal indication upon receipt of a key code from said key data memory which does not correspond to said master code;
and said logic means is operative in response to said second signal indication to provide a second output signal.

11. An electronic lock system according to claim 10 wherein said lock comparing means is also operative to provide said second signal indication in response to non-comparison between said enable code and said predetermined code.

12. An electronic lock system comprising:
a key adapted for insertion into an associated lock;
a multiple bit shift register within said key operative to store an electrically alterable multiple bit key code representing key identity and operative in response to clock signals from said lock to convey said key code from said shift register to said lock and to receive a key code from said lock;
a lock adapted for operation with said key and including
a receptacle for receiving said key in operative engagement therewith;
circuitry operative to provide an output signal upon correspondence between said key code and a master code, said circuitry comprising:
means for detecting the presence of said key in operative engagement with said lock receptacle and for providing a signal indication of key presence;
timing means operative in response to said signal indication of key presence for providing clock pulses for controlling operation of said circuitry;
a master code register for storing a multiple bit master code;
digital comparator means operative to compare said key code received from said shift register and said master code received from said master code register and to provide a signal indication upon correspondence between said key code and master code; and
logic means operative in response to said signal indication from said digital comparator means to provide an output signal.

13. An electronic lock system according to claim 12 wherein:
said digital comparator means is also operative to provide a second signal indication upon receipt of a key code from said key data memory which does not correspond to said master code;
and said logic means is operative in response to said second signal indication to provide a second output signal.

14. An electronic lock system according to claim 13 wherein said logic means includes:
a first AND gate coupled to the output of said digital comparator and to said timing means and operative to provide an output signal upon detection of non-correspondence between said master code and said key code;
a second AND gate;
a flip-flop maintained in one binary state by the presence of a signal derived from said key detection means and providing in this binary state an output signal to said second AND gate;
said flip-flop being operative in response to the output signal from said first AND gate to switch to its second binary state causing removal of the flip-flop output signal to said second AND gate;
alarm circuitry operative upon detection of the output signal of said first AND gate to provide an output indication of non-correspondence between said master code and said key code; and
decoding means for recognizing the last bit of said master code to denote the end of the code comparison process and to provide an enabling signal for said second AND gate to cause production of said logic means output signal.

15. An electronic lock system according to claim 14 wherein said timing means includes means for providing first clock pulses and second clock pulses delayed

with respect to said first clock pulses by a predetermined amount, said first clock pulses being employed to control data bit transitions in said logic circuitry, said second clock pulses being employed to control data bit comparisons in said logic circuitry.

16. An electronic lock system according to claim **14** wherein said lock includes:

means for storing a new master code; and

means for transferring said new master code to said key shift register and to said master code register.

17. An electronic lock system according to claim **14** wherein said lock includes:

means for storing a new master code;

a second flip-flop coupled to the output of said second AND gate and operative to remain in one binary state in the presence of an output signal from said second AND gate and an opposite binary state in the absence of an output signal from said second AND gate; and

a third AND gate coupled to the output of said second flip-flop and to said timing means and operative to provide a gating signal to said new code storage means to transfer said new master code to said master code register and to said key shift register.

18. An electronic lock system according to claim **12** wherein said key shift register is of a data capacity to store a multiple bit code longer than said key code, said key code being stored in said shift register as part of the stored code.

19. An electronic lock system comprising:

a key having a structural member adapted for insertion into an associated lock;

an electronic data memory within said structural member and having plural interconnected stages each operative to store a bit of an electrically alterable multiple bit code representing key identity;

a plurality of first terminals on said structural member connected to said electronic data memory and operative to couple said member to an associated lock;

a lock adapted for operation with said key and including:

a receptacle for receiving the structural member of said key therein;

a plurality of second terminals within said receptacle for coupling to respective ones of said first terminals of said key with said key in said receptacle;

logic circuitry coupled to said second terminals and having an electronic data memory for storing a multiple bit master code;

first logic means operative with said key inserted in said receptacle to compare the key code stored in said key data memory, and to provide an output indication of correspondence between said key code and master code; and

second logic means operative in response to said output indication from said first logic means to provide an output signal.

20. An electronic lock system according to claim **19** wherein:

said first logic means is also operative to provide a second output indication upon receipt of a key code from said key data memory which does not correspond to said master code;

and said second logic means is operative in response to said second output indication to provide a second output signal.

21. An electronic lock system comprising:

a key including

a structural member adapted for engagement with an associated lock;

an electronic shift register disposed in said structural member and operative to store an alterable multiple bit code representing key identity and to read out said code in response to clock pulses from said lock; and

a plurality of first terminals disposed in predetermined disposition on said structural member and connected to said shift register, said first terminals including a clock terminal, a data input terminal and a data output terminal;

a lock including

a receptacle for receiving the structural member of said key and having a plurality of second terminals operative to couple to respective ones of said first terminals of said key;

means in said receptacle for detecting the presence of a key and for providing an output indication of key presence; and

circuitry for decoding said key code and including

clock means operative in response to an output indication from said key detection means for providing clock pulses for controlling the key decoding process;

a master code register for storing a multiple bit master code;

a digital comparator operative in response to said clock pulses to receive said master code and said key code and to provide a signal indication upon detection of correspondence between said key code and master code; and

logic means operative in response to said signal indication from said digital comparator to provide an output signal.

22. An electronic lock system according to claim **21** wherein:

said comparator is also operative to provide a second signal indication upon receipt of a key code from said key shift register which does not correspond to said master code;

and said logic means is operative in response to said second signal indication to provide a second output signal.

23. An electronic lock system comprising:

a key adapted for use with an associated lock and having an electronic data memory therein with a plurality of interconnected stages operative to store an electrically alterable multiple bit key code and terminal means for coupling said key to an associated lock by which said key code can be conveyed from said electronic data memory in response to a command signal;

a lock adapted for operation with said key and including receptacle means for receiving said key in operative association therewith;

an electronic data memory for storing a multiple bit master code;

means for providing a command signal to said key data memory to cause readout of said key code to comparison means for comparison of said key code with said master code;

means operative to compare said key code stored in said key data memory with said master code stored in said master code memory and to provide a signal indication upon receipt of a key code from said key data memory corresponding to said master code; and

logic means operative in response to said signal indication from said comparison means to provide a utilization signal upon correspondence between said key code and said master code.

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