(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 February 2012 (09.02.2012)

PCT

(10) International Publication Number
WO 2012/018975 A2

(51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 29/78* (2006.01)

(21) International Application Number:
PCT/US2011/046539

(22) International Filing Date:
4 August 2011 (04.08.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/850,097 4 August 2010 (04.08.2010) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 12/850,097 (CON)
Filed on 4 August 2010 (04.08.2010)

(71) Applicant *(for all designated States except US)*: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku Tokyo, 160-8366 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KIRKPATRICK, Brian, K.** [US/US]; 1007 Biscayne Court, Allen, TX 75013 (US). **CHAMBERS, James, J.** [US/US]; 5511 McCommas Boulevard, Dallas, TX 75206 (US).

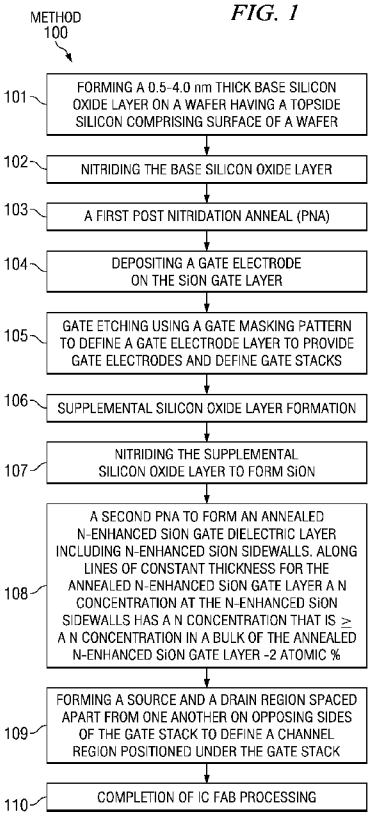
(74) Agents: **FRANZ, Warren L.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU,

[Continued on next page]

(54) Title: MOS TRANSISTORS INCLUDING SION GATE DIELECTRIC WITH ENHANCED NITROGEN CONCENTRATION AT ITS SIDEWALLS

FIG. 1



(57) Abstract: A method (100) of forming an integrated circuit having at least one MOS device includes forming a SiON gate dielectric layer (101, 102, 103) on a silicon surface, depositing a gate electrode layer (104) over the SiON gate layer and then patterning (105) to form a gate stack and expose gate dielectric sidewalls. A supplemental silicon oxide layer is then formed (106) over the exposed SiON sidewalls, followed by nitriding (107) and a post-nitridation anneal (108). This results in an annealed N-enhanced SiON gate dielectric layer including N-enhanced SiON sidewalls, wherein, along lines of constant thickness, a nitrogen concentration at the N-enhanced SiON sidewalls is > the nitrogen concentration in a bulk of the annealed N-enhanced SiON gate layer -2 atomic %.

WO 2012/018975 A2

SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

MOS TRANSISTORS INCLUDING SiON GATE DIELECTRIC WITH ENHANCED NITROGEN CONCENTRATION AT ITS SIDEWALLS

[0001] Disclosed embodiments relate to integrated circuits (ICs) including MOS transistors having SiON gate dielectrics.

BACKGROUND

[0002] Replacing conventional silicon oxide (e.g., SiO_2) gate dielectrics with silicon oxynitride (SiON) layers for MOS transistors is known to reduce gate dielectric leakage and boron (B) penetration from the gate electrode (for P^+ polysilicon gate for PMOS) into the underlying semiconductor surface which can result in threshold voltage (Vt) shifts. A conventional method to form a SiON gate dielectric layer includes thermal oxidation of a silicon comprising surface to form a silicon oxide "base" dielectric, followed by a plasma nitridation to incorporate nitrogen (N) throughout the silicon oxide dielectric, and then a thermal post nitridation anneal in O_2/N_2 at a temperature around 1,100 ºC.

[0003] The higher the nitrogen concentration in the SiON dielectric, the higher its dielectric constant which allows the use of a thicker dielectric film for a given equivalent oxide thickness (EOT). The thickness of the SiON layer may be expressed as an EOT which is a parameter used to compare the performance of MOS transistors having a high-k dielectric layer with the performance of MOS transistors having a silicon dioxide gate dielectric layer. The EOT is defined as the thickness of a silicon dioxide gate dielectric needed to obtain the same gate capacitance as that obtained with a gate dielectric having a higher dielectric constant k as compared to silicon dioxide (the k of SiO_2 is about 3.9). For example, an EOT of 1 nm would result from the use a 10 nm thick high-k dielectric that has a k value of 39.

[0004] With ever increasing nitrogen concentrations within the gate dielectric, the process has become susceptible to reduced Gate Oxide Integrity (GOI) and/or increased Early Failure Rates (EFR), notable along gate dielectric edges. Within the wafer fab engineering community, this is referred to as elevated polysilicon finger failures when similarly sized (area) polysilicon block structures fail at a reduced rate compared to polysilicon fingers which are structures with a higher ratio of polysilicon edge area per total unit area. Most work to address

this problem has been directed at improving the silicon oxide base dielectric quality, or reducing the gate etch depletion effect (e.g., by changing the etch conditions).

SUMMARY

[0005] Disclosed embodiments are based on the Inventors' recognition that conventional gate-first process flows inherently expose the sidewalls of the SiON gate dielectric once the gate (e.g., polysilicon) etch has been performed, and the exposure leads to significant nitrogen loss at the sidewalls as a function of exposure time. Further, the Inventors have recognized that promptly capping the exposed SiON sidewalls with a capping layer is not practical since such a capping layer cannot be put in place until after the wafer surface is cleaned following gate etch, thus being too late to avoid significant nitrogen loss along the SiON sidewalls.

[0006] Disclosed embodiments do not require minimizing the nitrogen loss along the exposed SiON sidewalls following gate etch. Instead, disclosed embodiments comprise processing that adds nitrogen by a supplemental oxidation and nitridation to replace (and in some embodiments provide enough nitrogen to more than replace) the nitrogen lost at the exposed SiON sidewall following gate etch. In a typical embodiment, a supplemental silicon oxide layer is formed on the exposed SiON sidewalls, and the supplemental silicon oxide layer is then nitrided.

[0007] The supplemental silicon oxide layer can formed by a solution-based chemical oxidation, such as provided by a post gate etch clean, or by deposition or thermal growth that can follow the post gate etch clean. The nitridation of the supplemental silicon oxide layer can comprise a plasma nitridation process such as Decoupled-plasma nitridation (DPN). A post-nitridation anneal (PNA) follows the nitridation to form an annealed N-enhanced SiON gate dielectric layer including N-enhanced SiON sidewalls. The PNA can include oxygen and include conditions that form up to 20 Å of additional SiON. The PNA can stabilize the nitrogen added and repair defects induced in the SiON gate layer along the SiON sidewalls that can result from the plasma nitridation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a flow chart that shows steps in an example method for forming an IC comprising MOS transistors including a N-enhanced SiON gate dielectric having N-enhanced SiON sidewalls, according to an embodiment of the invention.

[0009] FIG. 2 is graphical representation of a nitrogen concentration profile as a function of lateral position from one sidewall to the other sidewall under the gate electrode along a line of constant thickness for example N-enhanced SiON gate dielectric layers having N-enhanced SiON sidewalls according to disclosed embodiments as compared to a conventional "prior art" SiON gate dielectric layer having N-depleted SiON sidewalls.

[0010] FIG. 3 is a simplified cross-sectional view of a portion of an IC including a substrate having a top silicon comprising surface shown including at least one MOS device that includes a N-enhanced SiON gate dielectric layer having an N-enhanced SiON sidewalls, according to a disclosed embodiment.

[0011] FIG. 4 is a graphical representation of a nitrogen concentration profile in the thickness dimension for a bulk region (away from the SiON sidewalls) of an example SiON gate dielectric layer according to a disclosed embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] FIG. 1 is a flow chart that shows steps in an example method 100 for forming an IC comprising MOS transistors including a N-enhanced SiON gate dielectric having N-enhanced SiON sidewalls, according to an embodiment of the invention. Step 101 comprises forming a 0.5-4.0 nm thick base silicon oxide layer, such as by thermally or chemically oxidizing an exposed top silicon surface of a wafer. When the steps 106-108 are configured to form as much as 10 to 20 Å of SiON, the base silicon oxide layer formed during step 101 is generally 5 to 15 Å thick, typically from 6 to 10 Å thick.

[0013] As used herein and unless otherwise specified, the term "silicon" refers to all forms of silicon, including but not limited to, single crystalline, polycrystalline and amorphous silicon, and certain compounds (alloys) of silicon, including but not limited to, silicon germanium (SiGe) and silicon carbide (SiC). In one embodiment the thickness of the silicon oxide layer is 1.0 to 3.0 nm. For example, the base silicon oxide layer can be grown by oxidation in ambients such as O_2, O_2+H_2, N_2O, N_2O+H_2, H_2O, in a temperature range of 800-1100 °C, at a pressure of 0.001-100 Torr, for a time of 1-60s. Reduced pressure (i.e. sub-atmospheric pressure) oxidation reduces the oxidation rate to limit the thickness of the resulting base silicon oxide layer.

[0014] Step 102 comprises nitriding the base silicon oxide layer to form SiON. Those skilled in the art will appreciate that different plasma methods can be used for introducing

nitrogen into a silicon oxide layer. For example, plasma-enhanced-chemical-vapor-deposition (PECVD) methods can be used in which substrates are subjected to a plasma atmosphere in a conventional CVD apparatus. For example, nitridation can be performed in NH_3 or NH_3 containing ambient gas at a temperature of 500-1000 ºC, at a pressure of 0.001-100 Torr, for a time of 1 to 60s. Further, parallel plate plasma deposition systems can also be used to introduce nitrogen into a dielectric material. A DPN may also be used. DPN uses inductive coupling for plasma formation. In DPN, radio frequency (RF) power is transferred to the plasma via an RF magnetic field, which, in turn, generates an ionizing electric field. The plasma environment can comprise N_2, N_2+He,N_2+ noble gas or NH_3.

[0015] As used herein, "SiON" refers to a dielectric material comprising silicon (Si), oxygen (O) and nitrogen (N) that comprises a nitrogen concentration of 6 to 35 at. % SiON for layers having uniform nitrogen concentration along their thickness dimension and a maximum nitrogen concentration of 8 to 35 at. % nitrogen for SiON layers having non-uniform nitrogen concentration along their thickness dimension. The Si concentration can range from 34 to 40 at. %, and the O concentration can range from 26 to 60 at. %.

[0016] In one embodiment, the nitridation performed in step 102 is used to set the basic shape of the nitrogen concentration profile over its thickness, such that the maximum nitrogen concentration in the SiON gate layer away from the silicon interface is sufficiently high, for example at least 10 at. %. A sufficiently high nitrogen concentration away from the silicon interface in the SiON layer provides leakage current (Jg) reduction and B blocking (for B doped polysilicon gates), while being shallow enough to prevent nitridation of the silicon interface and resulting mobility/delta Vt degradation.

[0017] Step 103 comprises a first PNA. The first PNA can comprise a multi-step PNA. The multi-step PNA can comprise a first anneal 103(a) in a non-oxidizing ambient that can remove weakly bonded nitrogen and stabilize the remaining nitrogen in the SiON gate layer such that it is less likely to diffuse out during subsequent thermal processing. In one embodiment the first anneal 103(a) is performed in a N_2 or a noble gas ambient at a temperature from 500-1100 ºC, at a pressure of 0.001 to 760 Torr, for a time of 0.1 to 60s.

[0018] For the multi-step PNA, the first anneal 103(a) is followed by a second anneal 103(b) in an oxidizing ambient. The second (oxidizing) anneal 103(b) can heal remaining defects in the SiON gate layer without subjecting the SiON gate layer at the silicon interface to

additional oxidation in order to prevent degradation of the EOT of the SiON gate layer. The second anneal 103(b) can also reduce the nitrogen concentration at the top portion of the SiON gate layer (near the gate electrode interface) which the Inventors have discovered can be helpful for polysilicon gates in order to reduce the N-content in order to avoid an increase in polysilicon depletion that can result from BN formation for P^+ polysilicon gates. The second anneal 103(b) generally grows 1 or 2 Å of SiON. In one embodiment the second anneal 103(b) is performed in an oxygen containing gas including pure O_2 gas at 500 to 1100 ºC, at a pressure of 0.001 to 100 Torr, for a time of 0.1 to 120s. In another embodiment, the first anneal 103(a) and the second anneal 103(b) of the PNA are performed in a common chamber (e.g. single wafer rapid thermal annealer (RTA)).

[0019] Step 104 comprises depositing a gate electrode layer on the SiON gate layer. In one embodiment, the gate electrode layer can comprise polysilicon. Polysilicon can be deposited using a silicon comprising gas, such as SiH_4, Si_2H_6, Si_2Cl_6 or SiH_2Cl_2, etc., at a temperature of 500-800 °C, at a pressure of 1 to 100 Torr, for a time from 10 to 300 s. In other embodiments, the gate electrode layer can comprise a metal to provide a metal gate, such as W/TiN, Mo, Ta, TaN, TiN or $TaSi_xN_y$ in the case of a replacement gate process.

[0020] In one embodiment, reduced pressure is maintained between step 102 and step 104 at a level below 300 Torr, such as a level below 100 Torr. The Inventors have found that performing such steps in reduced pressure prevents uncontrolled N-loss due to reaction of the SiON gate layer with ambient oxygen and also prevents the SiON layer from being contaminated from adventitious carbon both of which can degrade device performance for MOS devices in terms of EOT and Vt control. Maintaining reduced pressure allows the SiON gate layer to be essentially carbon free (e.g. < 0.2 atomic % C). For example, in one embodiment, forming the silicon oxide layer (step 101) takes place in a first chamber, the wafer is transferred under reduced pressure to a second chamber, wherein the nitriding (step 102) takes place in the second chamber. The wafer is transferred under reduced pressure to a third chamber, wherein the first anneal 103(a) takes place. The wafer is transferred under reduced pressure to a fourth chamber, wherein the second anneal 103(b) takes place. The wafer is transferred at step 104 under reduced pressure to a fifth chamber, wherein the gate electrode layer is deposited.

[0021] Step 105 comprises a gate etch using a gate masking pattern to define the gate electrode layer to provide gate electrodes and thus define gate stacks, and optionally gate

electrode lines and other gate electrode layer features (e.g., capacitor plates). An optional hard-mask layer (e.g., silicon nitride with a SiON cap) can be added between step 104 and 105. The finite gate electrode layer to SiON gate layer selectivity during gate etch combined with the nominal overetch during the gate etch at step 105 results in the formation of exposed SiON sidewalls which the Inventors have recognized leads to nitrogen loss while the SiON sidewall is exposed to the ambient.

[0022] Step 106 comprises supplemental silicon oxide formation. In one embodiment forming the supplemental silicon oxide layer comprises a solution-based chemical oxidation which can oxidize the exposed gate electrode sidewall when the gate electrode comprises polysilicon including along at its interface with the SiON sidewall which can increase the thickness of the gate dielectric layer several Å along its exposed sidewall. The silicon oxide formed by the solution-based chemical oxidation is typically a low density and is typically 6 to 12 Å thick, that upon annealing would condense in a non-oxidizing ambient down to <2 Å. In the particular case of a solution-based chemical oxidation, the wet chemistry can comprise use of solutions such as SC1 (i.e., NH_4OH, H_2O_2, and deionized water (DNI) mixture). Typical SC1 conditions comprising NH_4OH: H_2O_2: DIW 1:1:5 to 1:2:100, such as at 1:1:20 to 1:1:50, at a T of 25 to 70 ºC, for 1 to 10 minutes. Alternatively, sulfuric acid/hydrogen peroxide (H_2SO_4, H_2O_2) can be used; typically in a 2:1 to 20:1 ratio, in a temperature range of 85 to 180 ºC, for 1 to 15 minutes may be used. In yet another embodiment, SC2 conditions comprising HCl/H_2O_2/DIW at 1:1:5 to 1:2:500, 1 to 2 minutes, 25 to 80 ºC may be used.

[0023] In another embodiment forming the supplemental silicon oxide layer comprises a deposition, such as LPCVD. In the case of a deposition, the supplemental oxide is deposited on top of the exposed SiON sidewall. In another embodiment the supplemental silicon oxide layer is grown by thermal oxidation, such as at a temperature of 800-1100 ºC, a pressure of 0.001-10 Torr, for a time of 1-60s. Thermal oxidation can proceed from the top silicon comprising surface as well as from the exposed gate electrode sidewall when the gate electrode comprises polysilicon. Like the solution-based chemical oxidation, thermal oxidation can increase the thickness of the SiON gate layer several Å along its exposed sidewall.

[0024] Step 107 comprises nitriding the supplemental oxide layer to form SiON. Step 107 can generally utilize any of the various plasma processes disclosed above relative to step 102, and in one embodiment comprises DPN.

[0025] Step 108 comprises a second PNA to form an annealed N-enhanced SiON gate dielectric layer including N-enhanced SiON sidewalls, wherein along lines of constant thickness for the annealed N-enhanced SiON gate layer a nitrogen concentration at the N-enhanced SiON sidewalls is ≥ the nitrogen concentration in a bulk (away from the sidewalls) of the annealed N-enhanced SiON gate layer -2 atomic %. The thickness of the annealed N-enhanced SiON gate layer following the second PNA is generally from 12 to 30 Å. Three (3) example PNA variants are described below, and are referred to herein as type A, type B and type C PNAs.

[0026] A type "A" PNA can be based on the multi-step PNA described above relative to step 103, with the first anneal performed in a N_2 or a noble gas ambient at a temperature from 500 to1100 ºC, at a pressure of 0.001-760 Torr, for a time of 0.1-60s, and the second anneal performed in an oxygen containing gas including pure O_2 gas at 500 to 1100 ºC, at a pressure of 0.001 to 100 Torr, for a time of 0.1 to 120s. The type A PNA typically grows 0.5 to 2.0 Å of SiON, but can grow as much as 6 to 8 Å.

[0027] The type "B" PNA comprises a time from 5 to 30s, a temperature from 1,000 to 1,105 °C, a pressure from 0.1 to 3.0 Torr, a rotation rate range from 120 to 360 RPM, in an oxidizing ambient comprising O_2 from 1.2 to 3.6 slm, O_2/N_2 from 1.2/3.6 to 3.6/1.2, or O_2/N_2 from 0.4/2.0 to 2.0/0.4. The type B PNA typically grows 7 to 9 Å of SiON, but can grow from 4 to 19 Å. In one particular embodiment the type B PNA comprises a time of 15s, a temperature of 1100 °C, a pressure of 0.48 Torr, a rotation rate of 240 RPM, and an oxidizing ambient comprising 2.4 slm O_2.

[0028] The type "C" PNA is generally is accompanied by Step 106 comprising the solution-based chemical oxidation embodiment, but can include other oxidations. The type C PNA comprises a time from 8 to 15s, a temperature from 750 to 900 °C, a pressure from 5 to 40 Torr, and an oxidizing ambient comprising N_2O and H_2 with N_2O from 5 to 10 slm, and H_2 from 0.1 to 0.5 slm. In one particular embodiment the type C PNA comprises 8 slm N_2O/0.2 slm H_2. The type C PNA typically grows 0.5-2.0 Å of SiON, but can grow from 6 to 8 Å.

[0029] Step 109 comprises forming a source and a drain region spaced apart from one another on opposing sides of the gate stack to define a channel region positioned under the gate stack, and step 110 comprises completion of IC fab processing. A spacer process as known in the art may be added between steps 108 and 109. Conventional processing can generally be used for steps 109 and 110.

[0030] FIG. 2 is graphical representation of a nitrogen concentration profile as a function of lateral position from one sidewall to the other sidewall under the gate electrode along a line of constant thickness (e.g., 6 Å from the gate electrode interface, along a lateral distance of 50 nm from one sidewall to the other sidewall) for an example N-enhanced SiON gate dielectric layer having an N-enhanced SiON sidewalls as compared to a conventional "prior art" SiON gate dielectric layer having N-depleted SiON sidewalls. The "prior art" SiON gate dielectric layer 215 is shown having a 17 at. % nitrogen concentration in its bulk region defined herein to be away from the left and right SiON sidewalls, and a nitrogen concentration < 8 at. % at both its left and right SiON sidewalls. As described above, SiON gate dielectric layer 215 has nitrogen depletion at its sidewalls compared to the nitrogen concentration in its bulk away from the sidewalls due to exposure of the sidewalls of the SiON gate dielectric to the ambient once the gate etch has been performed.

[0031] In contrast, nitrogen concentration profiles 220 and 225 represent N-enhanced SiON gate dielectric layers having N-enhanced SiON sidewalls that result from performing additional processing to conventional SiON gate dielectric layer 215 comprising step 106 (supplemental silicon oxide formation), step 107 (nitriding the supplemental silicon oxide to form SiON), and step 108 (a second PNA to form an annealed N-enhanced SiON gate dielectric layer including N-enhanced SiON sidewalls). Steps 106-108 provide N-enhanced SiON gate layers having a nitrogen concentration at the N-enhanced SiON sidewalls that is ≥ a nitrogen concentration in the bulk (away from the left and right SiON sidewalls) of the N-enhanced SiON gate layer -2 atomic %. For example, nitrogen concentration profile 220 is shown having a 17 at. % nitrogen concentration in its bulk away from the left and right SiON sidewalls, and a nitrogen concentration between 16 and 17 at. % at both its left and right SiON sidewalls. Nitrogen concentration profile 225 is shown having a 17 at. % nitrogen concentration in its bulk away from the left and right SiON sidewalls, and a nitrogen concentration higher than that away from the left and right SiON sidewalls of about 18 at. % at both its left and right SiON sidewalls.

[0032] FIG. 3 is a simplified cross-sectional view of a portion of an IC 300 including a substrate 305 having a top silicon comprising surface 307 shown including at least one MOS device 310 that includes a N-enhanced SiON gate dielectric layer 320 having an enhanced N-enhanced SiON sidewalls 320(a), according to a disclosed embodiment. The top silicon interface 308 shown in FIG. 3 represents the interface between the N-enhanced SiON gate layer 320 and

the top silicon comprising surface 307, while gate electrode interface 326 represents the interface between the N-enhanced SiON gate layer 320 and the gate electrode 330.

[0033] Gate electrode 330 is shown as a polysilicon electrode, and as such, is N-enhanced along its sidewall 330(a) $\geq$ 10 at. % due to the nitridation during the nitridation processes described above (steps 107 and 108). Along lines of constant thickness for the annealed N-enhanced SiON gate layer 320 a nitrogen concentration at the N-enhanced SiON sidewalls 320(a) is $\geq$ the nitrogen concentration in a bulk of the annealed N-enhanced SiON gate layer -2 atomic %, such as shown by representations 220 and 225 provided in FIG. 2.

[0034] As described above, substrate 305 can comprise any one of a bulk silicon substrate, SiGe substrate, strained silicon substrate, an SOI substrate, or other single crystal substrate. The MOS device 310 is shown in a highly simplified form and as shown includes a source region 311 and a drain region 312 spaced apart to define a channel region 313. Features such as LDDs, spacers and additional implants (e.g. halo implants) are not shown to avoid obscuring inventive details. In one embodiment, the gate electrode 330 comprises polysilicon, such as P^+ (e.g. B) doped for PMOS devices and N+ doped for NMOS devices. In other embodiments, the gate electrode 330 comprises a metal gate, such as when a replacement metal gate process is employed, so that the gate electrode 330 can comprise metal gates such as W/TiN, Mo, Ta, TaN, TiN or $TaSi_xN_y$.

[0035] Although not shown in FIG. 3, IC 300 generally includes other active circuitry, comprising circuit elements that generally include other transistors including bipolar transistors, diodes, capacitors, and resistors, as well as signal lines and other conductors that interconnect these various circuit elements.

[0036] FIG. 4 is a graphical representation of a nitrogen concentration profile in the thickness dimension for a bulk region (away from the SiON sidewalls) for an example SiON gate dielectric layer according to a disclosed embodiment. For example, method 100 described above can provide the concentration profile shown in FIG. 4. The average nitrogen concentration can be seen to be $\geq$ 8 at. %, such as $\geq$ 10 at. %, a maximum nitrogen concentration of least 15 at. %, and a nitrogen concentration at an interface 308 between the N-enhanced SiON gate layer and the top silicon comprising surface shown as the semiconductor interface to be $\leq$ 2 at. %.

[0037] Embodiments of the invention can be integrated into a variety of process flows to form a variety of devices and related products. The semiconductor substrates may include various elements therein and/or layers thereon. These can include barrier layers, other dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, embodiments of the invention can be used in a variety of processes including bipolar, CMOS, BiCMOS and MEMS processes.

[0038] Those skilled in the art will appreciate that other embodiments and variations are possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A method of forming an integrated circuit including at least one MOS device on a wafer having a top surface including silicon, comprising:

forming a SiON gate dielectric layer on said top surface;

depositing a gate electrode layer on said gate dielectric layer;

patterning said gate electrode layer to form a gate stack, whereby SiON sidewalls and gate electrode sidewalls are exposed by said patterning;

forming a supplemental silicon oxide layer over said exposed SiON sidewalls;

nitriding said supplemental layer;

after said nitriding, performing an anneal, thereby forming an annealed N-enhanced SiON gate dielectric layer including N-enhanced SiON sidewalls; wherein, along lines of constant thickness for said annealed N-enhanced SiON gate layer, a nitrogen concentration at said N-enhanced SiON sidewalls is $\geq$ a nitrogen concentration in a bulk of said annealed N-enhanced SiON gate layer -2 atomic %; and

forming a source and a drain region spaced apart from one another on opposing sides of said gate stack to define a channel region under said gate stack.

2. The method of claim 1, where said supplemental silicon oxide layer is formed by thermal oxidation at a temperature of 800-1100 ºC at a pressure of 0.001 to 10 Torr for a time of 1 to 60 seconds.

3. The method of claim 1, wherein said post-nitridation anneal comprises a first anneal performed in a N_2 or a noble gas ambient at a temperature of 500 to 1100 ºC and a pressure of 0.001 to 760 Torr for a time of 0.1 to 60 seconds; and a second anneal performed in an oxygen containing gas including pure O_2 gas at 500 to 1100 ºC at a pressure of 0.001 to 100 Torr for a time of 0.1 to 120 seconds.

4. The method of claim 1, wherein said post-nitridation anneal is performed for a time of 5 to 30 seconds at a temperature of 1,000 to 1,105 °C and a pressure of 0.1 to 3.0 Torr in

an oxidizing ambient comprising O_2 from 1.2 to 3.6 slm, O_2/N_2 from 1.2/3.6 to 3.6/1.2, or O_2/N_2 from 0.4/2.0 to 2.0/0.4.

5. The method of claim 1, wherein said supplemental silicon oxide layer is formed using a solution-based chemical oxidation and said post-nitridation anneal is performed for a time from 8 to 15 seconds at a temperature from 750 to 900 °C and a pressure from 5 to 40 Torr in an oxidizing ambient comprising N_2O from 5 to 10 slm and H_2 from 0.1 to 0.5 slm.

6. The method of claim 1, wherein said gate electrode layer comprises polysilicon that is deposited using a silicon containing gas at a temperature of 500-800 °C and a pressure of 1 to 100 Torr for a time of 10 to 300 seconds.

7. The method of claim 1, wherein forming said supplemental silicon oxide film takes place in a first chamber; said nitriding takes place in a second chamber after transferring said wafer under a pressure of 0.001 Torr to 100 Torr to the second chamber; and said post-nitridation anneal takes place in a third chamber after transferring said wafer to said third chamber.

8. An integrated circuit device, comprising:

a substrate having a top surface comprising silicon and including at least one MOS device, said MOS device comprising:

a source and a drain region spaced apart to define a channel region;

a N-enhanced SiON gate dielectric layer on said top silicon comprising surface including over said channel region, wherein said N-enhanced SiON gate layer includes N-enhanced SiON sidewalls, wherein along lines of constant thickness for said N-enhanced SiON gate layer a nitrogen concentration at said N-enhanced SiON sidewalls is $\geq$ a nitrogen concentration in a bulk of said SiON layer -2 atomic %;

a gate electrode on said N-enhanced SiON gate layer including over said channel region.

9. The device of claim 8, wherein said nitrogen concentration at said N-enhanced SiON sidewalls is ≥ a nitrogen concentration in said bulk of said SiON layer.

10. The device of claim 9, wherein an average nitrogen concentration in said bulk of said N-enhanced SiON gate layer is ≥ 8 at. %, a maximum nitrogen concentration in said bulk of said N-enhanced SiON gate layer is at least 15 at. %, and a nitrogen concentration in said bulk of said N-enhanced SiON gate layer at an interface between said N-enhanced SiON gate layer and said top silicon comprising surface is ≤ 2 at. %.

11. The IC of claim 10, wherein said gate electrode layer comprises polysilicon.

12. The IC of claim 11, wherein a maximum nitrogen concentration in the SiON gate layer is at least 10 at. %; and a thickness of said N-enhanced SiON gate layer is from 12 to 30 Å.

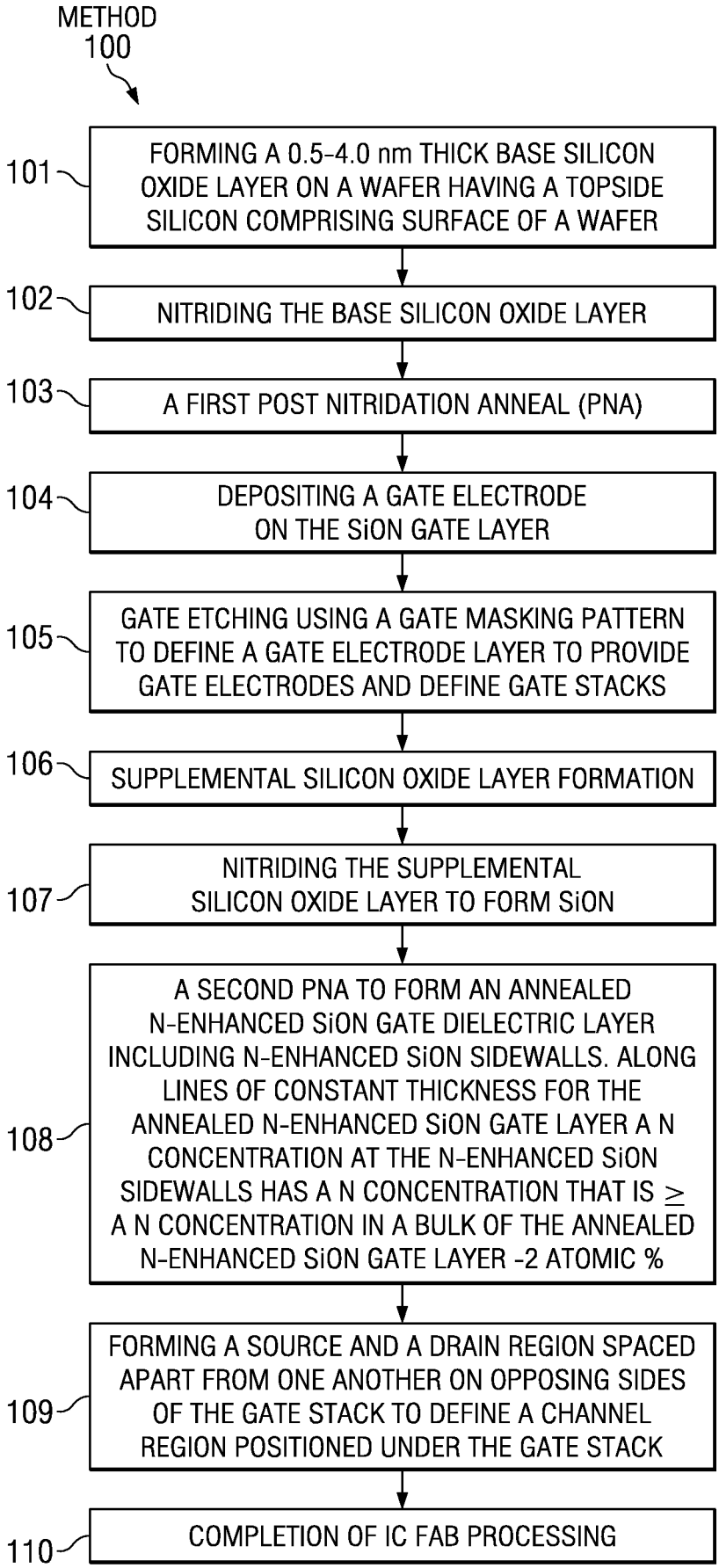

METHOD
100
101
FORMING A 0.5-4.0 nm THICK BASE SILICON OXIDE LAYER ON A WAFER HAVING A TOPSIDE SILICON COMPRISING SURFACE OF A WAFER
102
NITRIDING THE BASE SILICON OXIDE LAYER
103
A FIRST POST NITRIDATION ANNEAL (PNA)
104
DEPOSITING A GATE ELECTRODE ON THE SiON GATE LAYER
105
GATE ETCHING USING A GATE MASKING PATTERN TO DEFINE A GATE ELECTRODE LAYER TO PROVIDE GATE ELECTRODES AND DEFINE GATE STACKS
106
SUPPLEMENTAL SILICON OXIDE LAYER FORMATION
107
NITRIDING THE SUPPLEMENTAL SILICON OXIDE LAYER TO FORM SiON
108
A SECOND PNA TO FORM AN ANNEALED N-ENHANCED SiON GATE DIELECTRIC LAYER INCLUDING N-ENHANCED SiON SIDEWALLS. ALONG LINES OF CONSTANT THICKNESS FOR THE ANNEALED N-ENHANCED SiON GATE LAYER A N CONCENTRATION AT THE N-ENHANCED SiON SIDEWALLS HAS A N CONCENTRATION THAT IS ≥ A N CONCENTRATION IN A BULK OF THE ANNEALED N-ENHANCED SiON GATE LAYER -2 ATOMIC %
109
FORMING A SOURCE AND A DRAIN REGION SPACED APART FROM ONE ANOTHER ON OPPOSING SIDES OF THE GATE STACK TO DEFINE A CHANNEL REGION POSITIONED UNDER THE GATE STACK
110
COMPLETION OF IC FAB PROCESSING

FIG. 1

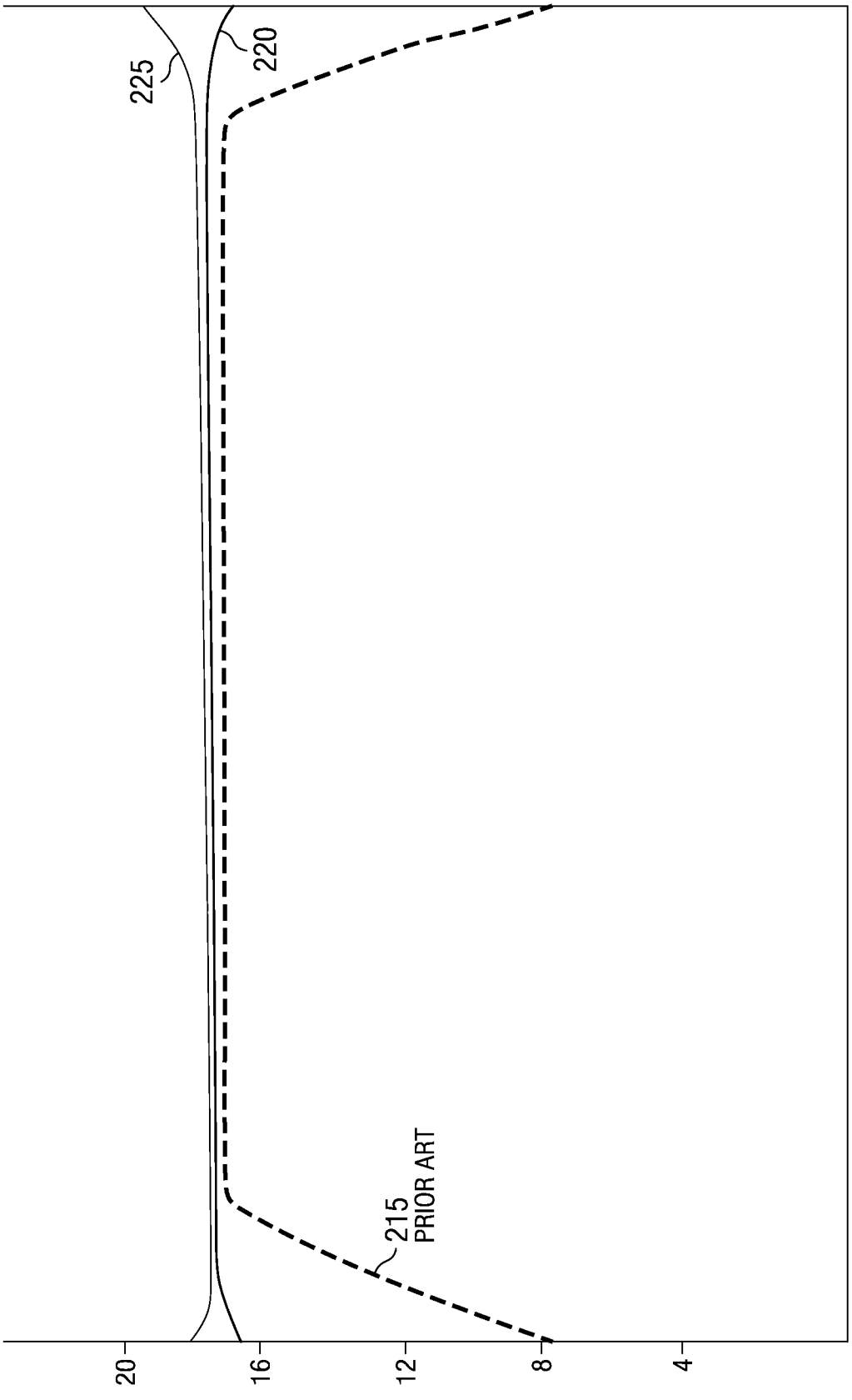

225
220
215
PRIOR ART
20
16
12
8
4
TOMIC % N
IN SiON
ATE LAYER
LEFT SiON
SIDEWALL
LATERAL POSITION UNDER GATE ELECTRODE
RIGHT SiON
SIDEWALL

FIG. 2

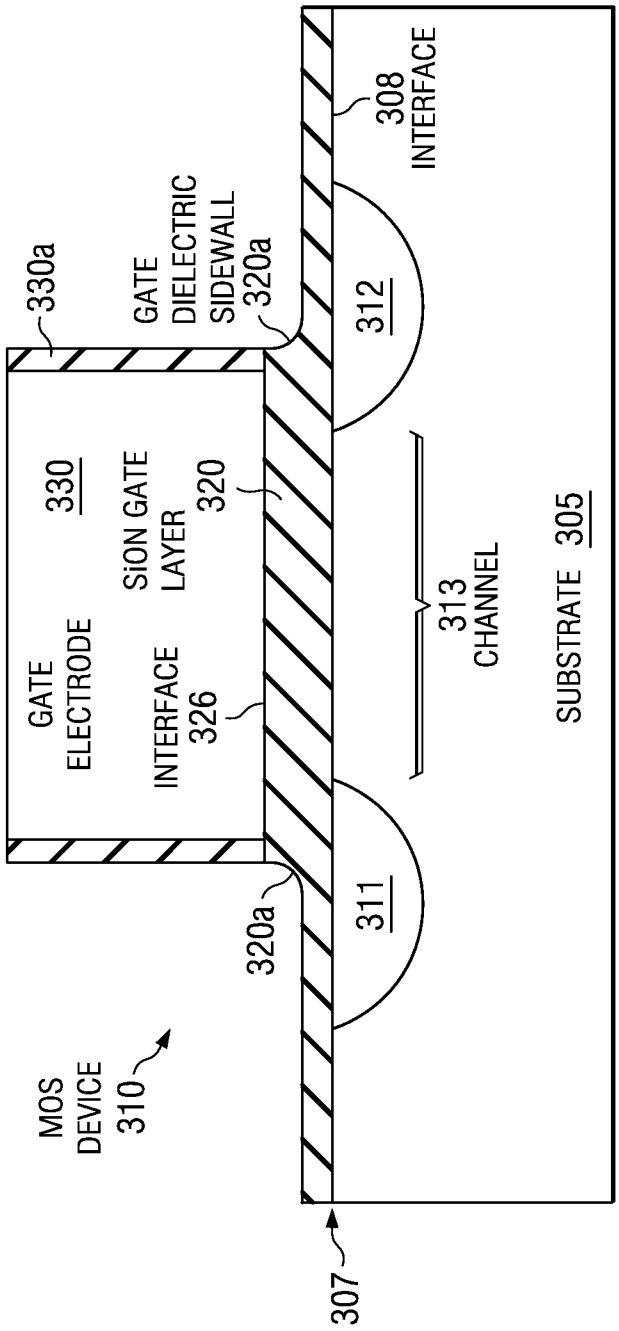

MOS DEVICE 310
300 IC
307
330a
GATE DIELECTRIC SIDEWALL 320a
308 INTERFACE
GATE ELECTRODE 330
SiON GATE LAYER 320
INTERFACE 326
312
311
320a
313 CHANNEL
SUBSTRATE 305

FIG. 3

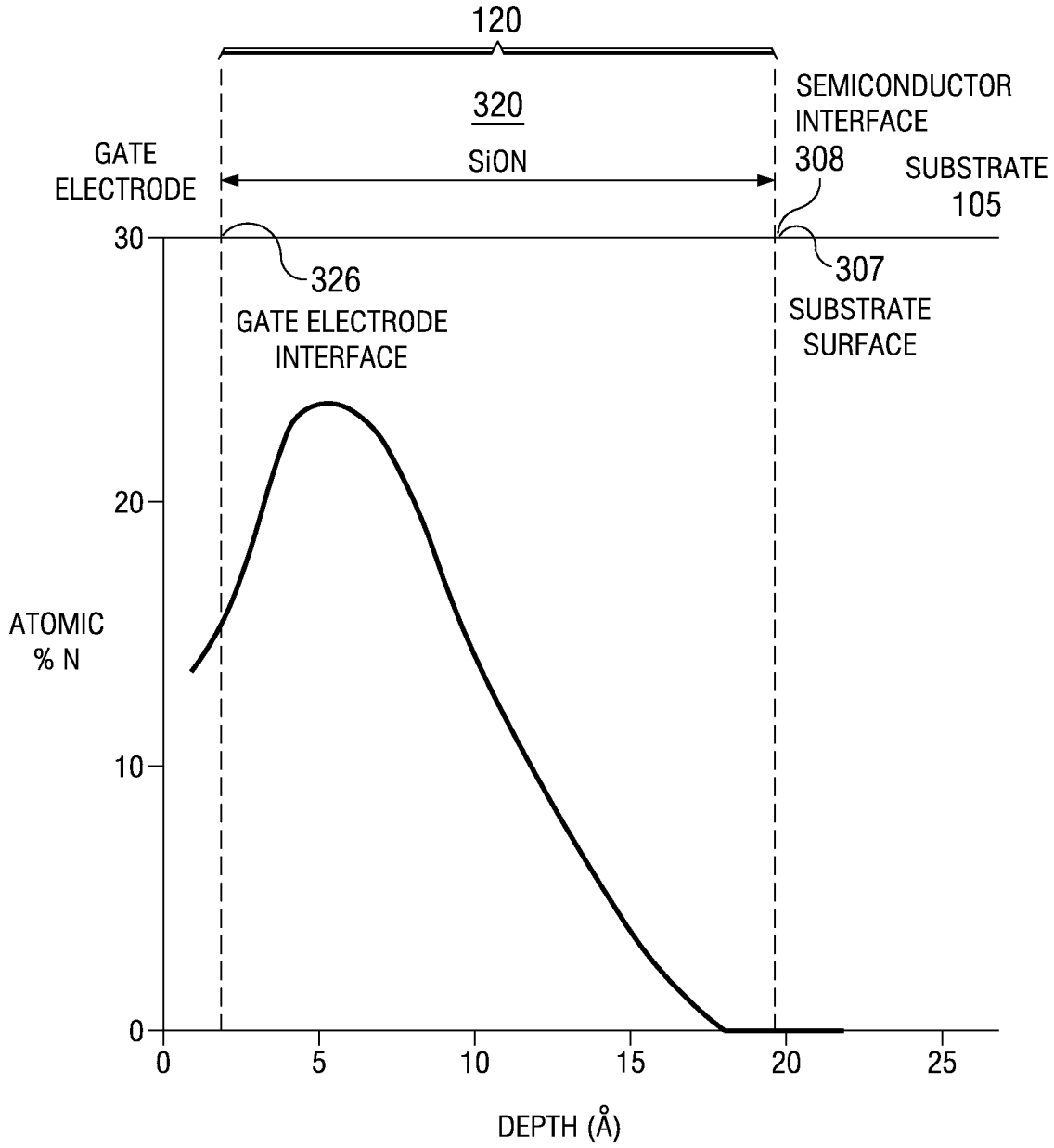

120
320
SiON
GATE
ELECTRODE
SEMICONDUCTOR
INTERFACE
308
SUBSTRATE
105
30
326
GATE ELECTRODE
INTERFACE
307
SUBSTRATE
SURFACE
20
ATOMIC
% N
10
0
0
5
10
15
20
25
DEPTH (Å)

FIG. 4