

[54] SOLENOID DRIVE CIRCUIT

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317/141 S; 307/270; 192/84

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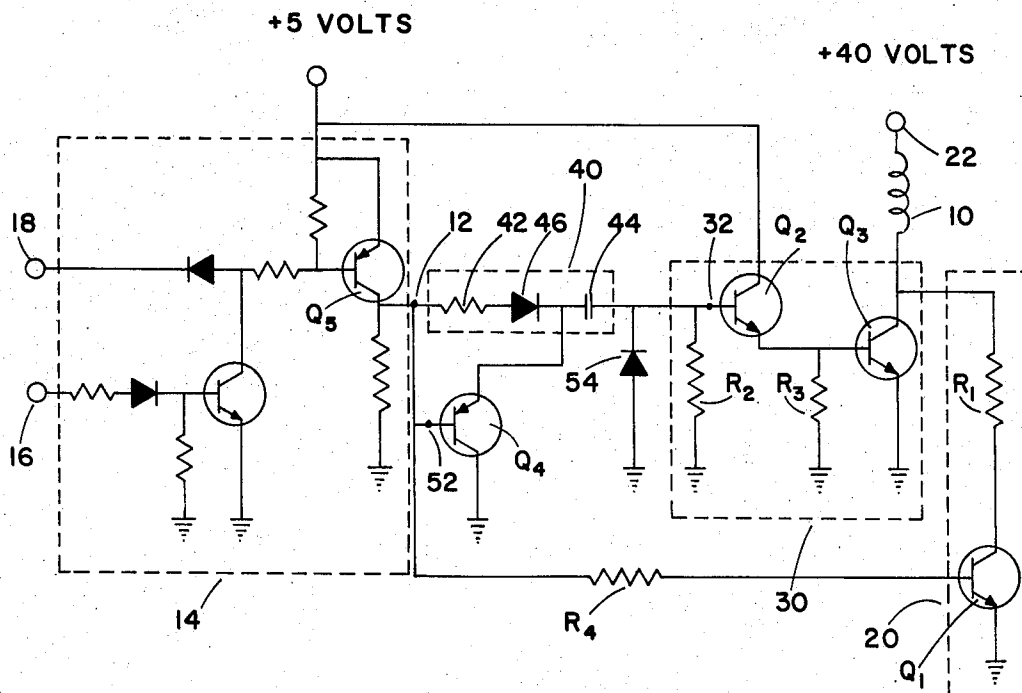
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[57]

ABSTRACT

A circuit for initially applying an unusually large drive voltage to a solenoid coil and for subsequently reducing the applied voltage during the travel of the solenoid plunger. The solenoid coil is serially connected to a first transistor circuit operating as an on-off switch and to a second transistor circuit connected parallel to the first transistor circuit and operating to variably control the voltage applied to the solenoid. A capacitor-charge timing circuit controls the variable transistor and thereby gradually reduces the voltage applied to the solenoid.

5 Claims, 2 Drawing Figures



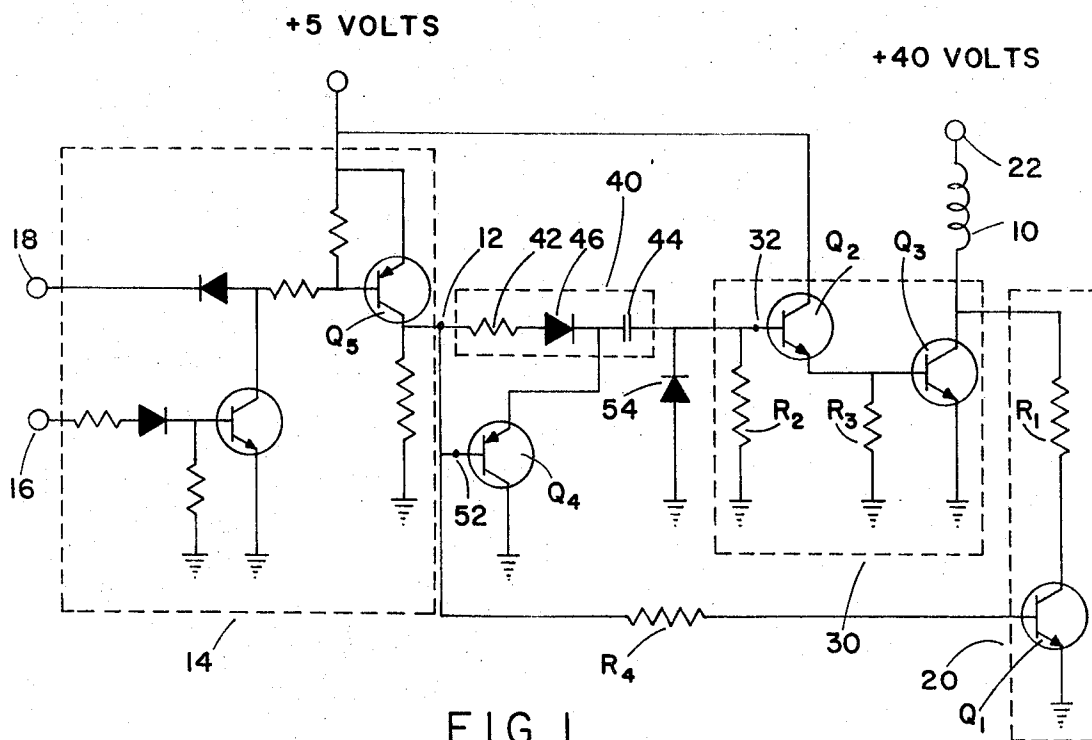


FIG. 1

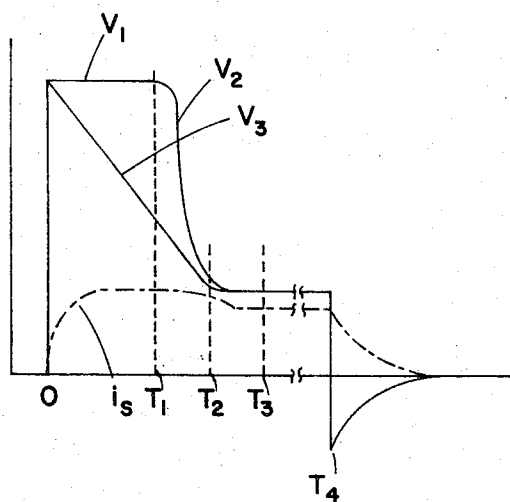


FIG. 2

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SOLENOID DRIVE CIRCUIT

BACKGROUND OF THE INVENTION

This invention is an improvement in the invention described in my copending application, Ser. No. 98,627, filed on Dec. 16, 1970, "Solenoid Drive Circuit" by Edwin E. Mason, control systems and more particularly relates to an electronic circuit for applying a desired voltage waveform to a solenoid coil.

The solenoid is an old and well established electro-mechanical device. It is used in diverse applications for changing electrical energy to mechanical energy. For example, I am interested primarily in the uses of solenoids for operating an input-output typewriter in response to remotely originated electrical signals in the manner disclosed in my copending application, Ser. No. 79,202, filed on Oct. 8, 1970, for "Input-output Typewriter Apparatus," by Edwin E. Mason, and assigned to the same assignee as the instant application.

The conventional manner of operating a solenoid is to apply to the solenoid a voltage which is slightly larger than or equal to the minimum voltage necessary to actuate the solenoid. Usually this voltage is continuously applied to the solenoid until the solenoid is de-energized. To de-energize a solenoid, the voltage is lowered to a value below the minimum holding voltage and ordinarily to zero volts.

There are several undesirable consequences of this conventional operation which my invention overcomes. With all solenoids, a minimum actuation voltage is necessary to overcome the inertia of the solenoid and to begin the movement of its plunger. However, with the continued application of the same voltage, the plunger will accelerate until its travel is abruptly ended by a mechanical stop. At the instant the plunger strikes the mechanical stop, it is traveling at its maximum velocity and consequently has its maximum momentum. The sudden stopping of the plunger produces a sudden slamming or hammering of the plunger into the mechanical parts of the solenoid. This hard slamming of the plunger tends to jar all the equipment with which the solenoid is associated and in particular tends to weaken, wear, and eventually damage the solenoid.

Because a lower voltage can be utilized to hold the solenoid in its actuated position after the plunger comes to rest, the continued application of the higher actuation voltage functions only to waste electrical power and to cause the dissipation of excess heat into the associated equipment.

There is a need, therefore, for a solenoid drive circuit which will initially overdrive the solenoid by applying a voltage to the solenoid which is considerably greater than its minimum actuation voltage. This will hasten the change in momentum of the plunger and similarly will more rapidly raise the solenoid current to the actuating current by more quickly overcoming the high initial reactance of the solenoid. There is also a need for a circuit which will automatically reduce the voltage applied to the solenoid during the plunger travel after the solenoid current has risen to a desired value, and yet will continue to maintain the solenoid current slightly above or equal to the minimum holding current of the solenoid.

SUMMARY OF THE INVENTION

The invention is a solenoid drive circuit for energizing and for de-energizing a solenoid in response to suitable signals at a drive circuit input. The solenoid drive circuit has a first electronic switch means which is in series with a solenoid and a source of driving electrical power. The first electronic switch means switches the current to the solenoid and has its control input connected to the drive circuit input for controlling the first electronic switch.

An electronic control valve means is connected parallel to the first switch means and is used for variably controlling a portion of the current to the solenoid. The electronic valve means also has a control input.

A timing means is provided for providing a time changing current for controlling the valve means. The timing means comprises serially connected timing resistance, capacitance and a diode connected to permit current flow turning on said valve means and charging the capacitance. The timing means is connected between the control input of the valve means and the drive circuit input. Discharge means for at times discharging the capacitance is also provided. The discharge means comprises a second electronic switch means connected to discharge the capacitance when turned on. The control input of the second electronic switch is connected to have at least the voltage across the diode applied to the control input of the second electronic switch.

OBJECTS OF THE INVENTION

It is an object of the invention to provide an improved solenoid drive circuit.

Another object of the invention is to provide an improved solenoid drive circuit which will initially overdrive the solenoid until the solenoid is driven at approximately its minimum holding current.

Another object of the invention is to speed up the actuation and complete operation of a solenoid and at the same time reduce the momentum of the solenoid plunger as it arrives at its actuated position.

Another object of the invention is to provide a solenoid drive circuit which will exhibit an improved duty cycle so that solenoid operation may be improved while heat generation and power losses minimized.

Another object of the invention is to avoid use of a high voltage PNP transistor.

Further objects and features of the invention will be apparent from the following specification and claims when considered in connection with the accompanying drawings illustrating the invention.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of the preferred embodiment of the invention; and

FIG. 2 is a graph illustrating solenoid voltage and current.

In describing the preferred embodiment of the invention illustrated in the drawings, specific terminology will be resorted to for the sake of clarity. However, it is not intended to be limited to the specific terms so elected and it is to be understood that each specific term includes all technical equivalents which operate in a similar manner to accomplish a similar purpose.

DETAILED DESCRIPTION

FIG. 1 illustrates a solenoid drive circuit for energizing and de-energizing a solenoid 10 in response to suitable signals at a drive circuit input 12. The drive circuit input terminal 12 is preceded by a logic circuit, indicated generally by 14, which permits either a positive logic level at the terminal 16 or a negative logic level at the terminal 18 to cause actuation of the solenoid drive circuit by raising the terminal 12 from ground level to the positive logic level.

The solenoid 10 is connected in series with a first electronic switch means, indicated generally as 20, and a source of driving power connected at the terminal 22. The first electronic switch means 20 comprises a bipolar junction transistor Q_1 series connected to a current limiting resistor R_1 . The function of the first electronic switch means 20 is to switch the current through the solenoid 10. The first electronic switch means 20 is controlled at the base of the transistor Q_1 which is connected through a resistor R_4 to the drive circuit input 12. The occurrence of the positive logic voltage at the drive circuit input 12 turns on the transistor Q_1 to permit at least a minimum holding current to flow through the solenoid 10.

An electronic valve means, indicated generally as 30, is connected parallel to the first switch means 20. The function of the electronic valve means 30 is to provide a time changing current through the solenoid 10. The valve means 30 has a control input at the base of the emitter follower-connected transistor Q_2 . The output of the transistor Q_2 is connected to the input of the transistor Q_3 which controls the time changing portion of the current through the solenoid 10.

A timing means, indicated generally as 40, is connected between the control input 32 of the valve means 30 and the drive circuit input 12. The function of the timing means 40 is to provide a time changing current for controlling the valve means 30 and for thereby controlling the time changing voltage applied to the solenoid 10. The timing means 40 comprises a serially connected timing resistance 42, a capacitance 44, and a diode 46. The diode 46 is connected in a polarity to permit current flow in a direction which turns on the valve means 30 and charges the capacitance 44.

A capacitance discharge means is also provided for at times discharging the capacitance 44. For this purpose, a second electronic switch means which is a transistor Q_4 is connected to discharge the capacitance when the transistor Q_4 is turned on and is therefore conducting. The control input of this second electronic switch is at its base terminal 52 and is connected to the drive circuit input 12. As will be seen, return of the drive circuit input 12 to ground potential results in turning on the transistor Q_4 . This will occur when the diode 46 is reverse biased.

Instead of transistor Q_4 , a diode could be inserted at the base and emitter connections in the circuit in the same polarity as the base emitter junction. However, this would result in a much slower discharge of the capacitor 44 through the resistor R_4 . The transistor Q_4 is preferred in order to speed up the discharge of capacitor 44 by utilizing the current gain of a transistor Q_4 .

Although the transistor Q_4 could discharge the capacitance 44 through the leakage resistance R_2 , a diode 54 is provided to further speed up the discharge of the capacitance 44. As will be seen below, the diode 54 is

reverse biased during charging of the capacitance and actuation of the solenoid and is forward biased only during discharge of the capacitance 44. Thus, the effect of this second diode 54 is to very substantially decrease the discharge time constant.

The preferred discharging transistor Q_4 is a PNP type junction transistor having its emitter connected to a common node between the capacitance 44 and the diode 46. Its base is connected to the drive circuit input 12 and its collector is connected to the second diode 54, at ground reference.

The operation of the circuit may be described with reference to the circuit diagram of FIG. 1 and the graph of FIG. 2. Prior to time zero on the graph of FIG. 2, the circuit is de-energized with all transistors being cut off and with the solenoid plunger at rest. At time zero, a positive logic signal is applied to the input terminal 16 or a negative logic signal is applied to the input terminal 18. The input logic signal brings the transistor Q_5 into conduction thereby applying a positive voltage to the drive circuit input terminal 12. The capacitor 44 of the timing circuit means 40, which was initially discharged, now begins charging in the polarity illustrated. Charging current flows primarily through the bases of the transistors Q_2 and Q_3 . The charging current begins at its maximum current and because it flows through the bases of the transistors Q_2 and Q_3 it immediately turns on the valve means 30 to its maximum conducting condition.

Simultaneously the occurrence of the positive voltage at the drive circuit input 12 immediately turns on the transistor Q_1 so that the first electronic switch 20 immediately provides a parallel current path for the solenoid 10. Thus, initially at time zero in FIG. 2, the maximum voltage of, for example, nearly 40 volts is applied to the solenoid 10.

As time progresses, the timing capacitance 44 begins to accumulate charge and therefore the current through the timing circuit means 40 decreases. This decrease in timing circuit current means a decrease in base current in the valve means 30 and therefore results in a decrease of the voltage applied to the solenoid 10 as time continues. Eventually, at a time such as T_2 in FIG. 2, the timing circuit current through the transistors Q_2 and Q_3 will decrease until the transistor Q_3 no longer conducts. At this point, only the current flowing through the transistor Q_1 , continues in the solenoid 10. With proper design, the remaining current through the transistor Q_1 will be the minimum holding current required to maintain the solenoid in an energized condition.

It should be noted however, that an alternative embodiment of the invention may be constructed by eliminating the transistor Q_1 and its current limiting resistance R_1 . Such a modification would result in a maximum voltage initially being applied to the solenoid 10 with the voltage thereafter decreasing to zero. This modified circuit would be useful where it is desired to energize the solenoid for a brief instant of time and to immediately de-energize the solenoid automatically.

Proper selection of the value of the timing resistance 42 and the value of the capacitance 44 and of the other resistances effecting current flow in the timing circuit means 40 will permit the design engineer to select the rate and the waveform according to which the voltage on the solenoid decreases as time progresses. If, for example, the timing resistance 42 is made relatively small,

and if the circuit is designed so that the initial voltage applied at the base 32 of the transistor Q_2 is in the saturation region well above the transistors linear region, then a waveform, such as that illustrated as V_1 and V_2 , can be applied to the solenoid 10. If however, the timing resistance 42 is made relatively large and the initial current in the base of the transistor Q_2 is on the edge of the linear region, then a nearly linear ramp function such as that illustrated as V_3 can be applied to the solenoid 10. Of course, the continuous family of solenoid drive voltage waveforms exist. A designer can select the waveform which meets the mechanical and electrical characteristics of the solenoid. For example, a quicker acting lower momentum solenoid would utilize a waveform more like that indicated as V_3 .

Returning now to the operation of the circuit illustrated in FIG. 1, when the capacitance 44 becomes charged, the electronic valve means 30 will cease conducting and the minimum holding current will be conducted through the transistor Q_1 and the solenoid 10, so long as the positive voltage continues to exist at the drive circuit input 12.

When the logic signal is removed from the input terminal 16 or the input terminal 18, the input terminal 16 or 18 is returned to the ground level. This causes the transistor Q_3 to cease conducting thereby bringing the drive circuit input terminal 12 to the ground level. The discharging transistor Q_4 will now begin conducting through the diode 54 which is forward biased by the charge on the capacitance 44. The transistor Q_4 will continue discharging the capacitance until the capacitance 44 is entirely discharged. In addition, the grounding of the drive circuit input 12 will cut off the transistor Q_1 therefore depriving the solenoid 10 of any current. The plunger of the solenoid 10 will immediately begin its return to the de-energized condition. In this manner, the circuit returns to its initial de-energized condition and awaits actuation at a later time.

The circuit values chosen by the designer, are selected also with the consideration of the time needed for the plunger of the solenoid to complete its travel. Solenoid travel could end near time T_1 , T_2 or T_3 , although I prefer to end near time T_2 . For example, in the preferred circuit illustrated, a time in a range of 8 to 14 milliseconds as T_2 has given desirable results.

Many of the improved results obtainable by the solenoid drive circuit are described in connection with the above cited copending application. In addition to these, this circuit is an improvement over the previous circuit because costs are significantly reduced. In the circuit illustrated in the application, there is no need for a costly, high voltage PNP transistor.

It is to be understood that while the detailed drawings and specific examples given described preferred embodiments of the invention therefore the purpose of illustration only that the apparatus of the invention is not limited to the precise details and conditions disclosed and that various changes may be made therein without departing the spirit of the invention which is defined in the following claims.

What is claimed is:

1. A solenoid drive circuit for energizing and de-energizing a solenoid in response to suitable signals at a drive circuit input, said circuit comprising:

- a. a first electronic switch means in series with said solenoid and a source of driving power for switching a current through said solenoid, the first switch means having a control input connected to and being controlled at said drive circuit input;
- b. an electronic valve means connected parallel to said first switch means for providing a time changing current through said solenoid, the valve means having a control input;
- c. a timing means for providing a time changing current for controlling said valve means and comprising serially connected timing resistance, capacitance and a diode connected to permit current flow in a direction to turn on said valve means and to charge said capacitance, said timing means connected between the control input of the valve means and said drive circuit input; and
- d. capacitance discharge means for at times discharging the capacitance and comprising a second electronic switch means connected to discharge said capacitance when turned on and a second diode connected in series with the second electronic switch means and said capacitance in a polarity to be reverse biased except during discharge of the capacitance.

2. A drive circuit according to claim 1 wherein: said first electronic switch means includes a bipolar junction transistor and said valve means includes a bipolar junction transistor having timing circuit charging current flowing through the base-emitter junction of the valve means.

3. A drive circuit according to claim 2 wherein: the capacitance and diode share a common node and said second electronic switch means is a bipolar junction transistor having its emitter connected to said common node, its base connected to said drive circuit input, and its collector connected to said second diode.

4. A drive circuit according to claim 2 wherein: said valve means comprises a first transistor in an emitter follower configuration and a second bipolar junction transistor connected to the output of the emitter follower, and the emitter follower is connected to the logic level power supply and said second transistor and said first electronic switch are NPN devices and are the only transistors subject to collector voltages above the logic level.

5. A drive circuit according to claim 4 wherein: said second electronic switch is a PNP junction transistor having its emitter connected between the first diode and the capacitance, having its base connected to the drive circuit input and having its collector connected to the anode of said second diode, the cathode of said second diode being connected to the opposite side of said capacitance.

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