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(54) Loss-of-signal detector.

(57) A digital loss-of-signal ("LOS") detector comprises a trough circuit(20) and a smearing circuit(30). The trough circuit generates a logic output whenever an incoming communication signal is within a predefined voltage range. The output of the trough circuit(20) is applied to the smearing circuit(30), which will generate an LOS output whenever the output of the trough circuit(20) remains at a given logic level for a predetermined length of time.

A state machine(110) can be coupled to the output of the smearing circuit(30), to the trough circuit(20) and to the clock signal, the state machine(110) generating the LOS indication if the output from the smearing circuit(30) remains at a logic level for at least a predetermined number of clock cycles. The LOS detector of both embodiments can respond very quickly to a loss of the signal and can also be constructed as a single integrated circuit.

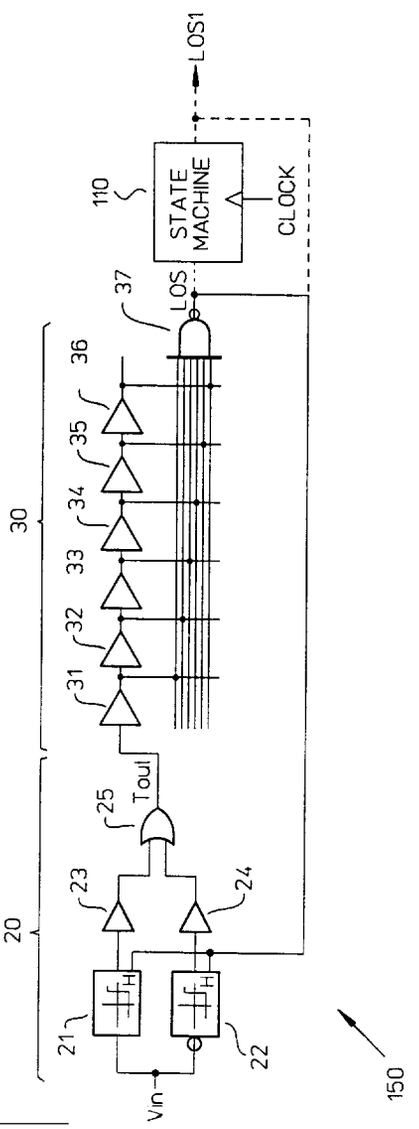

FIG. 2

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The present invention relates to a system and method for determining the loss of an incoming signal, for example for the fiber optic detection of a loss-of-signal ("LOS") event in a fiber-optic communications system.

In most, if not all digital communications systems, the receiver must be able to detect the presence or absence of an incoming signal. Rapid detection of an LOS event permits equally rapid restarting of the system.

In high speed fiber optic communications systems, a signal is transmitted as a series of laser light pulses over an optical fiber. If a break in the fiber is undetected, laser light could strike someone in the eye, with serious consequences. In many known duplex systems, when the receiver detects an LOS event, the receiver shuts down its own laser light, which in turn causes the transmitter to shut down. This prevents possible eye injury.

Although the receiver must respond quickly and correctly to a true LOS event, it must not shut down because of small variations in the strength of the incoming signal. Avoiding unnecessary shutdowns due to these signal variations requires very precise control of the threshold of the receiver's level detector. Also, given that some noise in the communications channel is unavoidable, the receiver must not react instantaneously to every possible LOS event. Multiple indications of LOS over a period of time should be necessary to trigger an LOS indication and to shut down the system.

Known LOS detection circuits generally use a peak detector to determine when the incoming signal has fallen below a preset threshold. These peak detectors convert the incoming A.C. signal to a D.C. signal using rectifiers such as diodes. The rectified signal is then applied to an external capacitor. The output of the peak detector is applied to a voltage comparator, which determines if the rectified signal is above or below a predefined reference voltage. The reference voltage is usually set using an external resistor.

In functional terms, known LOS detection circuits first detect a peak voltage level, measure the duration of the pulse using a resistor-capacitor time constant, and compare the detected peak voltage with the predefined threshold voltage.

There are several drawbacks with these known circuits. As the detector is a peak detector, it detects the maximum voltage level of the incoming signal. As the typical incoming signal is a square wave, the peak detector measures the initial rising voltage of the signal, which frequently overshoots and exceeds the signal's intended maximum. It is possible that this initial overshoot will trigger the peak detector and prevent the generation of an LOS indication, despite the fact that the true signal amplitude is below the LOS threshold. Failing to shut the system down in such a case is just as undesirable as shutting it down too often.

The external capacitor which maintains the voltage level during pulse transitions introduces a slow analog component into the circuit, which can cause some uncertainty in the circuit's response time, and increases the cost of the circuit. At high bit rates (above 500M-bits/s,) parasitic capacitances and inductances in the peak detector integrated circuit's ("IC"s) package, bond wires, and the external capacitor can trigger a false LOS indication.

The threshold voltage in known systems is defined by an external resistor. The sheet resistance of the IC which comprises the peak detector forms part of the voltage expression with the external resistor to ensure that the results of both the equation and the resulting circuit are in the proper units. As the sheet resistance varies from part to part, the threshold voltage will drift unless the external resistor is repeatedly trimmed to maintain it.

The present invention seeks to provide improved loss of signal detection.

According to an aspect of the present invention, there is provided a system for determining the loss of an incoming signal as specified in claim 1.

According to another aspect of the present invention, there is provided a method of determining the loss of a signal as specified in claim 9.

In some embodiments, it is possible to provide a LOS detector having a very precisely controlled threshold voltage which will only respond to a true LOS event but which will also not miss a LOS event due to a voltage overshoot. A completely digital LOS detector can also be provided which can cope with the increasing transmission rates used in fiber-optic communications channels and which can be fabricated as a single IC. It is also possible to eliminate the need to trim an external resistance to maintain the proper threshold voltage.

A first embodiment comprises a completely digital LOS detector in which an incoming digital communication signal is supplied to a herein-called "trough" circuit, which has a user defined threshold voltage("V_{TH}") set by 2 external resistors. The trough circuit generates a logic-I signal whenever the incoming voltage is above or below the V_{TH} and a logic-0 signal whenever the incoming voltage is within +/- V_{TH}. The output of the trough circuit represents the presence or absence of the input signal. This output is supplied to a digital "smearing" circuit. The purpose of the smearing circuit is to ensure that the output from the LOS detector reliably indicates the presence or absence of an LOS event, and not a brief voltage fluctuation or similar transient.

To further ensure that a true LOS event has occurred, a second embodiment includes a digital state machine coupled to the output of the smearing circuit. This state machine can be used in systems having a clock signal. By using the clock signal, the state ma-

chine monitors the output of the smearing circuit and only generates an LOS signal after the smearing circuit has been at a sustained level for a predetermined number of clock cycles.

An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a known LOS detector;

Fig. 2 is a block diagram of an embodiment of LOS detector;

Fig. 3 shows the transfer function of an upper threshold unit of the detector circuit shown in Fig. 2;

Fig. 4 is a circuit diagram of the detector shown in Fig. 2;

Fig. 5 is a state diagram of a state machine of the detector of Fig. 2;

Fig. 6 is a logic diagram showing one realisation of the state machine of Figure 5; and

Fig. 7 is a timing diagram showing how the detector of Fig. 2 in response to a LOS event.

For purposes of the description of the preferred embodiments, a LOS event is defined as the receiver no longer detecting incoming light of sufficient intensity for a sufficient period of time. The receiver for the described embodiments includes a light-to-electricity converter as well as amplifiers which amplify the converted signal prior to that signal's transmission to the LOS detector.

Fig. 1 is a block diagram of a known LOS detector 10. A differential incoming communication signal 11 is supplied to peak detector 13, which is comprised of internal diodes and a resistor, and external capacitor 12. The output of peak detector 13 and the output of trigger level generator 14 are supplied to voltage comparator 16, the output of which is used to indicate an LOS event. The trigger level generator's output voltage includes the D.C. bias voltage of signal 11 and the preset threshold voltage at which the LOS is triggered. Often, this threshold voltage is set by R_{ext} 15. The trigger level is adjusted depending on the state of the LOS signal to give the system necessary hysteresis.

The output from the peak detector 13 is a D.C.voltage with at least a slight ripple caused by the charging and discharging of capacitor 12. Because of the output signal's decay from peak detector 13 caused by the discharge of capacitor 12, the level of the output signal is somewhat ambiguous and depends on the number of consecutive 0s and 1s that occur(the greater the number of 0s, the longer capacitor 12 discharges). Additionally, the presence of external capacitor 12 increases the cost of the circuit. The use of a peak detector may also result in the failure to generate an LOS indication in those cases where the incoming signal overshoots its intended voltage momentarily.

Fig. 2 is a block diagram of an embodiment of LOS detector. Digital LOS detector 150 includes a trough circuit 20 and a smearing circuit 30. State machine 110 can be coupled to the output of smearing circuit 30 in any environment where a clock signal is available. The state machine uses the clock signal to insure further that the output of smearing circuit 30 remains at the same logic level for a sufficiently long time to verify that the presence or absence of a LOS condition has occurred. The preferred is shown in Fig. 2, indicated by dotted lines. Instead of the output of gate 37 being coupled to trough circuit 20, it is instead coupled to state machine 110, the output of which is coupled back to trough circuit 20.

The transfer function of trough circuit 20 is shown in Fig. 3. The incoming communications signal is a digital communication square wave with finite rise and fall times. When $|V_{in}|$ of this signal is less than V_{TH}, T_{out} of trough circuit 20 is logic-0. When $|V_{in}|$ is greater than V_{TH}, T_{out} of trough circuit 20 is logic-1. In this embodiment of the present invention, trough circuit 20 is further comprised of upper threshold detector 21, lower threshold detector 22, amplifiers 23 and 24 and OR gate 25.

Fig. 4 is a circuit diagram of upper threshold detector 21. Detector 21 includes an amplifier section 82 which comprises two differential current amplifiers 85 and 87, variable current source 84, and output stage buffers 86. As the construction and operation of lower threshold detector 22 is identical to that of upper threshold detector 21, with the exception that the input signal to lower threshold detector 22 is inverted with respect to threshold detector 21's input, only the design and operation of upper threshold detector 21 will be discussed in detail.

The two differential amplifiers 85 and 87 have different gains. Establishing the gains of differential amplifiers 85 and 87 is done in a known manner by properly selecting the value of their collector and emitter resistances. The collectors of amplifiers 85 and 87 share the same load resistors 49 and 50. This arrangement creates the functional equivalent of a voltage amplifier with two different gains. Depending on the state of the LOS output (LOS or LOS1, Fig. 2, depending upon whether state machine 110 is present or not), either amplifier 85 or amplifier 87 is activated and the other amplifier is tri-stated. When the output of smearing circuit 30 or state machine 110 indicates an LOS condition, the amplifier with the lower gain is turned on. This in turn requires that V_{in} reach a higher level before the LOS condition will be removed. Alternatively, if there is no LOS, the higher gain amplifier turns on. V_{in} must fall further in this case before an LOS condition is triggered. This provides the desired hysteresis.

As the gain ratio of the two amplifiers is very well defined, the hysteresis in dB is a constant, independent of the threshold voltage V_{TH}. Note that Fig. 3 shows the transfer function of trough circuit 30 when

the higher gain differential amplifier is on. If the lower gain differential amplifier is on, the transfer function is similar, with a different V_{TH}.

V_{TH} is determined by applying the current generated by the adjustable D.C. current source 84 to load resistor 50. This creates a D.C. offset in the trigger voltage for the trough circuit, which gives rise to half the transfer function shown in Fig. 3. The other half of the transfer function is generated by the lower threshold detector 22.

Adjustable current source 84 comprises a current source and a steering circuit. The current source is comprised of transistors 70 and 71 and resistors 69 and 72. The values of these components are selected to provide the desired temperature coefficient to compensate for gain variations in amplifiers 85 and 87, as well as in the amplifiers whose output is provided to LOS detector 150. The current generated by the current source is steered by a steering circuit comprised of transistors 65 and 66 and resistors 63,64,67,68 and external resistors 79 and 80.

The difference in the voltages applied to the bases of transistors 65 and 66 steers a variable amount of the current generated by adjustable current source 84 through resistor 50, which in turn determines the offset voltage of differential amplifiers 85 and 87.

As the voltage difference is determined by the ratio of the internal resistors 63 and 64 to external resistors 79 and 80, the absolute value of the IC's sheet resistance is decoupled from that of the external resistors, allowing an even more precise setting of V_{TH}. Although it is more difficult to fabricate resistors of a precise value using known IC fabrication techniques, the ratio of their values can easily be very tightly controlled.

Output stage 86 buffers the differential signals generated by amplifiers 85 or 87 and is coupled in turn to amplifier 23 (Fig. 2) which sharpens the signal, and finally to OR gate 25. The design and construction of amplifier 23 is known. The design and operation of the logic circuitry needed to generate a logic signal whenever detectors 21 and 22 detect a transition in voltage level going through V_{TH} is known.

Transitions in V_{in} detected by trough circuit 20 generate a short logic-0 output. However, individually these short pulses are not indicative of a LOS event. Only if the output of trough circuit 20 remains at a logic-0 level for at least a certain minimum of time should an LOS signal be generated. As the transitions in V_{in} and the consequent pulses generated by trough circuit 20 cannot exceed the bit width of V_{in}, the width of the pulses generated by trough circuit 20 in normal, non-LOS operation is less than one bit period of V_{in}.

Smearing circuit 30 (Fig. 2) performs the necessary filtering of the output of trough circuit 20. Circuit 30 functions by successively delaying the input pulses and recombining these delayed input pulses with the original input pulse. Only if the output of trough 20 remains low for at least the same amount of time as the total delay path is a high output generated by smearing circuit 30. As this total delay path time exceeds the maximum pulse width generated by trough circuit 20 in a non-LOS situation, smearing circuit 30 will only generate a positive output when a definite LOS condition has occurred. Thus the output of smearing circuit 30 is the true indication of an LOS event. The exact number of delay elements will vary depending upon the bit rate of the incoming signal. In a system using a 500M-bit data rate, the signal's period is 2 nanoseconds. Therefore, the total length of the delay is 2 nanoseconds. In such a system, only if the output from trough circuit 20 has been at logic-0 for at least 2 nanoseconds will the output of smearing circuit 30 be a logic-1. The illustrated preferred embodiment uses 6 delay elements 31 through 36. The output of each delay element is supplied to the next delay element and to NAND logic gate 37 to generate the final output. Other logic gates could be used and the implementation of this circuit function with such gates would be routine. If the bit rate of the incoming signal was changed, changes in the number of delay elements might also be necessary. Such changes would be a routine matter.

In systems where a clock signal is available and the clock frequency is less than or equal to the data rate of V_{in}, a state machine 110 (see Figs. 2 and 6) can be incorporated into the described embodiment to enhance the output of the smearing circuit, making it even more robust. This state machine monitors the input signal from smearing circuit 30 more closely to ensure that only true LOS events of a certain minimum duration trigger a high output .

The state diagram shown in Fig. 5 indicates how state machine 110 monitors the input signal from smearing circuit 30 and does not change state unless the input signal is sustained for four consecutive clock cycles. Fig. 6 shows one logic circuit embodying the state diagram of Fig. 5, the circuit being readily understandable from Fig. 6 without the need for a detailed description herein. The generation of a logic circuit from a state diagram is a known process and the logic circuit shown in Fig. 6 is only one embodiment of the state diagram of Fig. 5. Many others could be used and their design would be known to one of skill in the art. Indeed, even an analog output stage such as a capacitor could be coupled to the output of smearing circuit 30 to perform the same function as state machine 110.

The performance of the example in operation is illustrated in Fig. 7. V_{in} is the signal applied to trough circuit 20, T_{out} is the output of trough circuit 20, LOS is the output of smearing circuit 30, A,B, and L are outputs generated within state machine 110, and LOS1 is the output of state machine 110. As shown by Fig. 7, trough circuit 20 generates a short pulse every time V_{in} transitions between a first and second state. LOS

from smearing circuit 30 is not generated until T_{out} has been low for a minimum period T. LOS1 does not go to its logic-1 state until 5 clock cycles have passed since LOS has gone to its logic-1 state.

The disclosures in United States patent application no. 08/195,243, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. A system for determining the loss of an incoming signal, comprising a trough circuit (20) coupled to a signal input for determining when an incoming signal varies between a first voltage level and a second voltage level and operative to generate a first output signal whenever the incoming signal varies from a first threshold level to a second threshold level and from the second threshold level to the first threshold level; and a smearing circuit (30) coupled to the trough circuit and operative to generate a second output signal if the first output signal is generated for longer than a first predefined period of time, the second output signal being indicative of the loss of an incoming signal.

2. A system according to claim 1, comprising a state machine (110) coupled to the smearing circuit (30) and to a first clock signal, the state machine (110) being operative to generate a third ouput signal if the second output signal remains above a third voltage level for at least a predefined number of clock cycles, the third output signal being indicative of the loss of an incoming signal.

3. A system according to claim 1 or 2, wherein the smearing circuit (30) includes delay means (31-36) operative to generate a plurality of time delay signals each of which delay signals is generated from one of a plurality of successive first output signals from the trough circuit (20), the smearing circuit (30) being operative to generate the second output signal when the first output signal and all the time delay signals are at the same logic state simultaneously.

4. A system according to claim 3, wherein the delay means comprises a plurality of delay units (31-36), each delay unit including an input and an output, the input of a first delay unit (31) being coupled to the output of the trough circuit (20), the output of the first delay unit (31) being coupled to the input of a successive delay unit (32), each successive delay unit being coupled to the output of the previous delay unit, the output of each delay unit being coupled to an NAND gate (37) operative to generate the second output signal if the outputs of all the delay units are at the same logic state simultaneously.

5. A system according to claim 4, wherein the total time delay from when a logic signal is received by the first delay unit (31) to the time delayed logic signal is generated by the last delay unit (36) exceeds the time required for the incoming signal to switch between the first and second voltage levels.

6. A system according to any preceding claim, wherein the trough circuit (20) comprises first differential amplifier means (85) coupled to the signal input and the second or third output signal for generating a logic signal in response to a first state of the second or third output signal; second differential amplifier means (87) coupled to the signal input and the second or third output signal for generating a logic signal in response to a second state of the second or third output signal; a current source for generating a constant current (84); and steering circuit means (84) coupled to the current source and to the first and second differential amplifier means for steering a variable amount of the constant current through a load resistor (15) to determine a threshold voltage of the first and second differential amplifier means.

7. A system according to claim 6, wherein the first and second differential amplifier means are coupled respectively to a first and second output buffer circuit (86).

8. A system according to claim 6 or 7, wherein the trough circuit (20) comprises two identical trough circuit units (20), the first trough circuit unit being coupled to receive the incoming signal, the second trough circuit unit being coupled to receive an inversion of the incoming signal.

9. A method of determining the loss of a signal, the signal including a first and second voltage level, the method comprising the steps of: detecting when the signal varies between the first and second voltage levels;
generating a first logic signal whenever a transition between the first and second voltage levels is detected;
applying the first logic signal to a delay network (30); and
generating a second logic signal from the delay network if the first logic signal is applied to the delay network for a predetermined period of time.

10. A method according to claim 9, comprising the steps of applying the second logic signal to a

state machine (110), the state machine (110) generating a third logic signal if the second logic signal is applied to the state machine for a predetermined number of clock cycles.

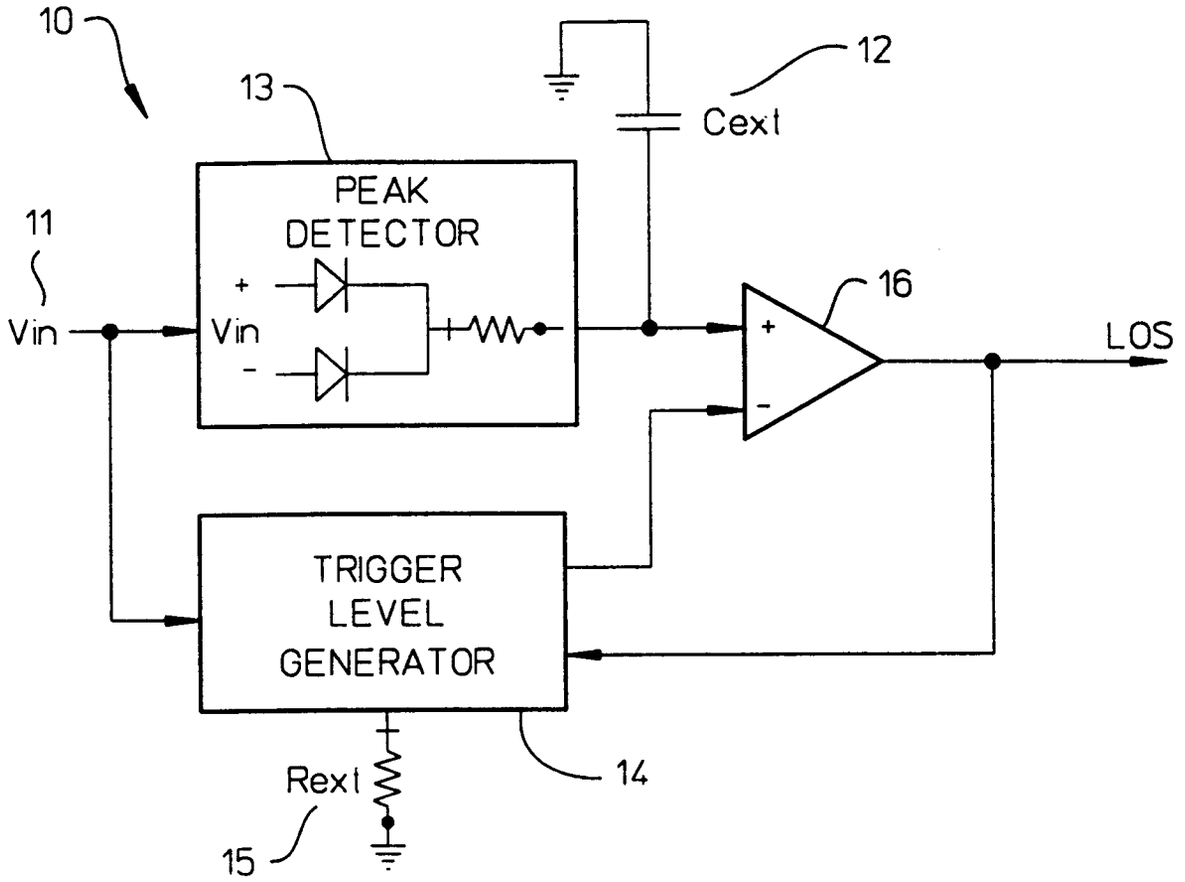
10
13
12
Cext
PEAK
DETECTOR
11
Vin
+
Vin
-
16
LOS
TRIGGER
LEVEL
GENERATOR
Rext
14
15

FIG. 1

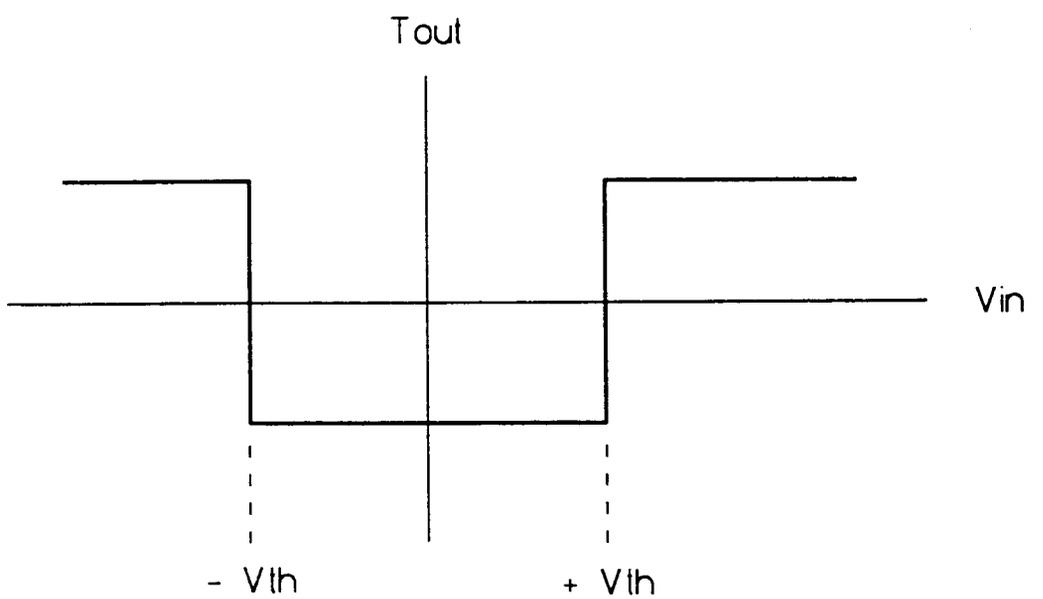
Tout
Vin
- Vth
+ Vth

FIG. 3

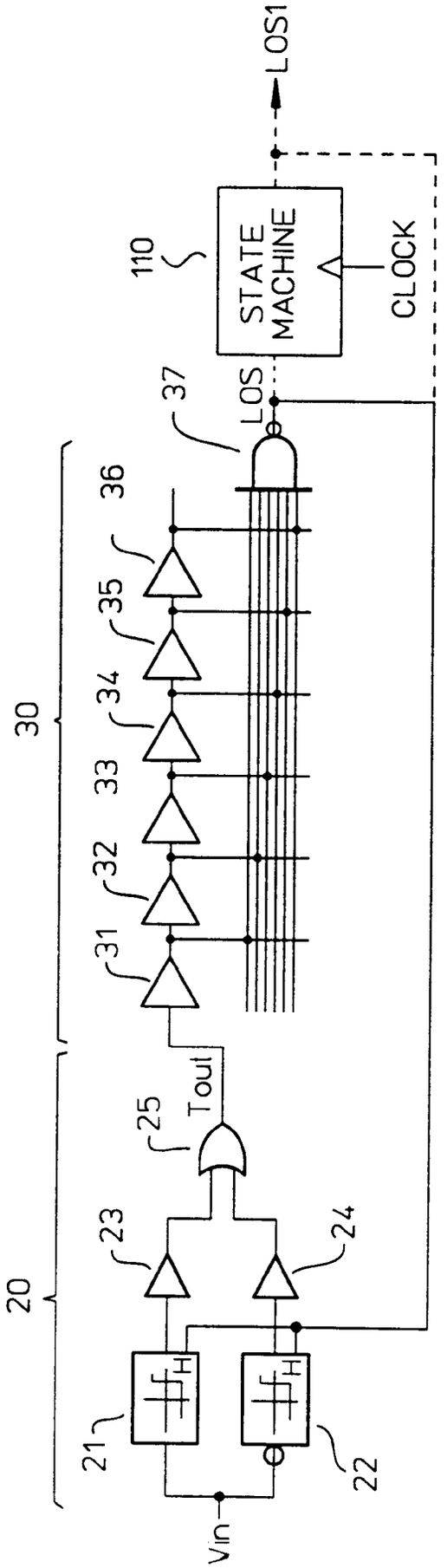
LOS1
110
STATE MACHINE
CLOCK
37
LOS
36
35
34
33
32
31
30
25
Tout
23
24
20
21
22
Vin
150

FIG. 2

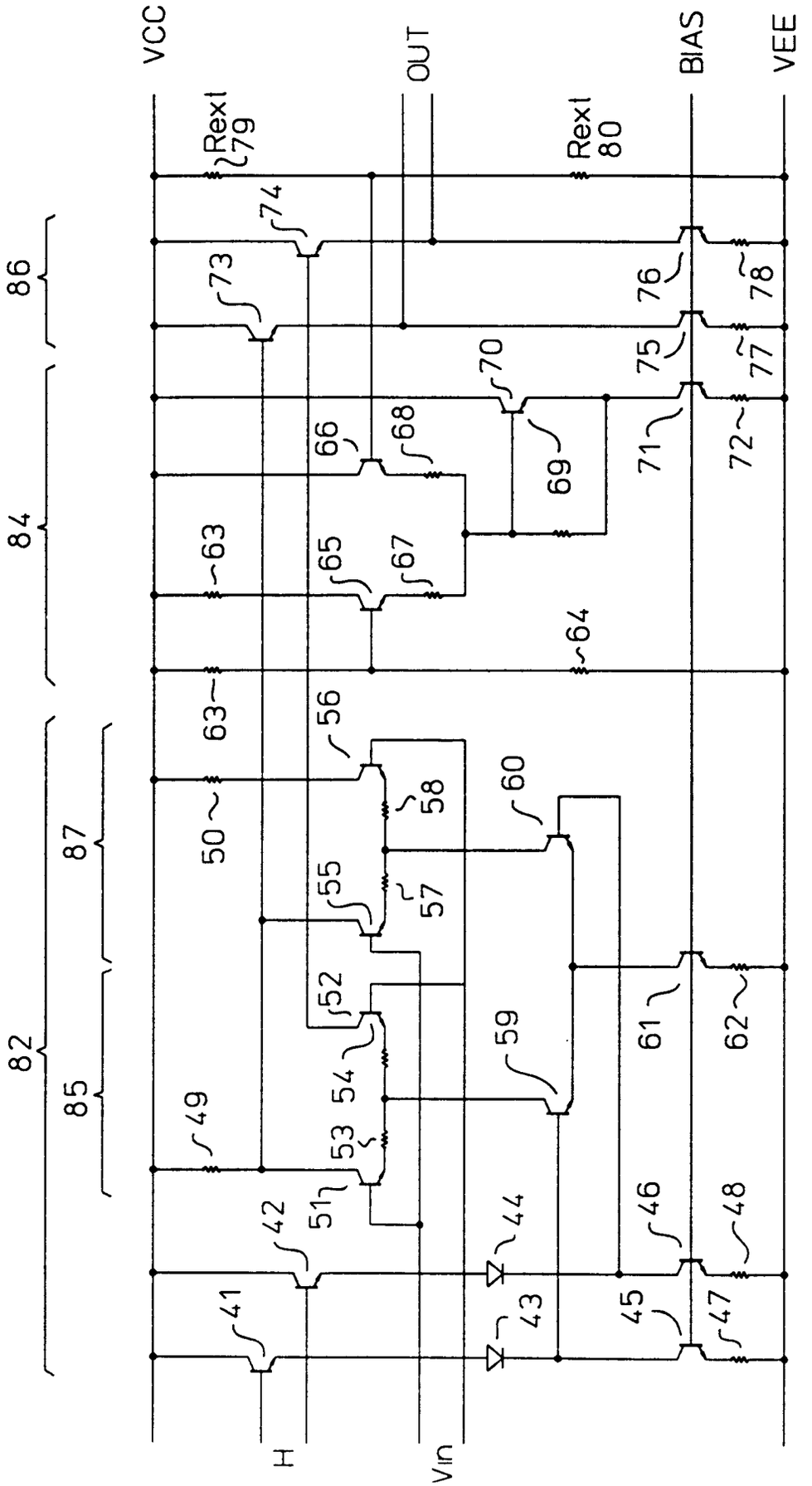
VCC
Rext
79
OUT
Rext
80
BIAS
VEE
86
84
82
87
85
74
73
76
78
75
77
70
66
68
71
72
69
63
65
67
64
63
56
50
58
60
55
57
52
54
59
61
62
49
53
51
42
44
46
48
41
43
45
47
H
Vin

FIG. 4

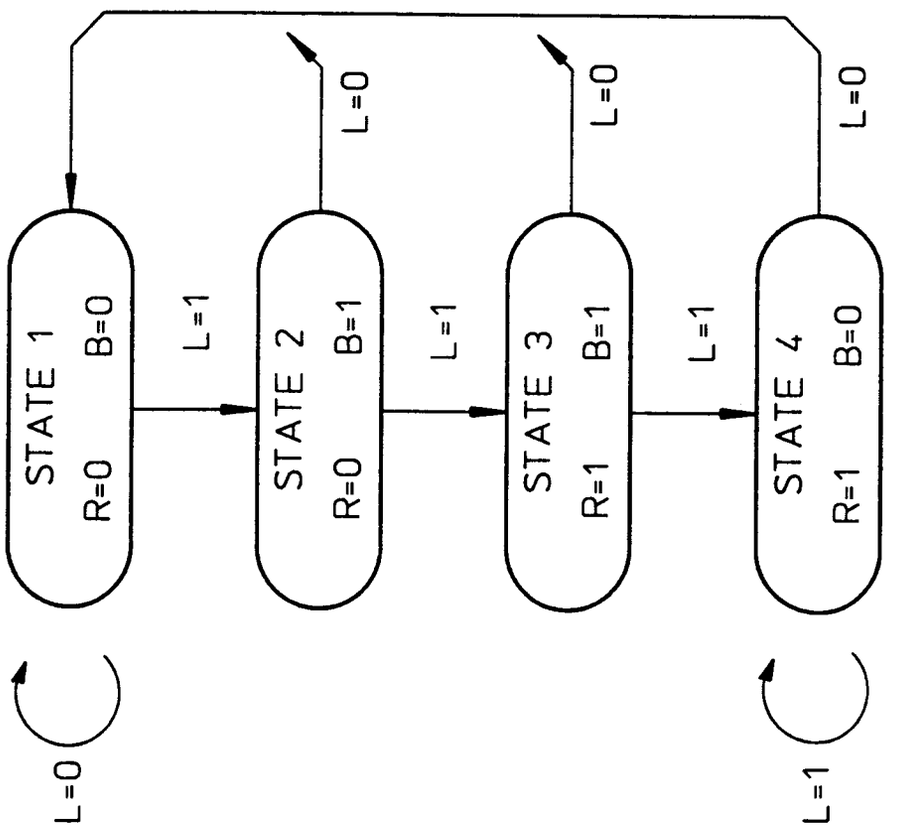
STATE 1
R=0 B=0
STATE 2
R=0 B=1
STATE 3
R=1 B=1
STATE 4
R=1 B=0
L=1
L=1
L=1
L=0
L=0
L=0
L=0
L=1

FIG. 5

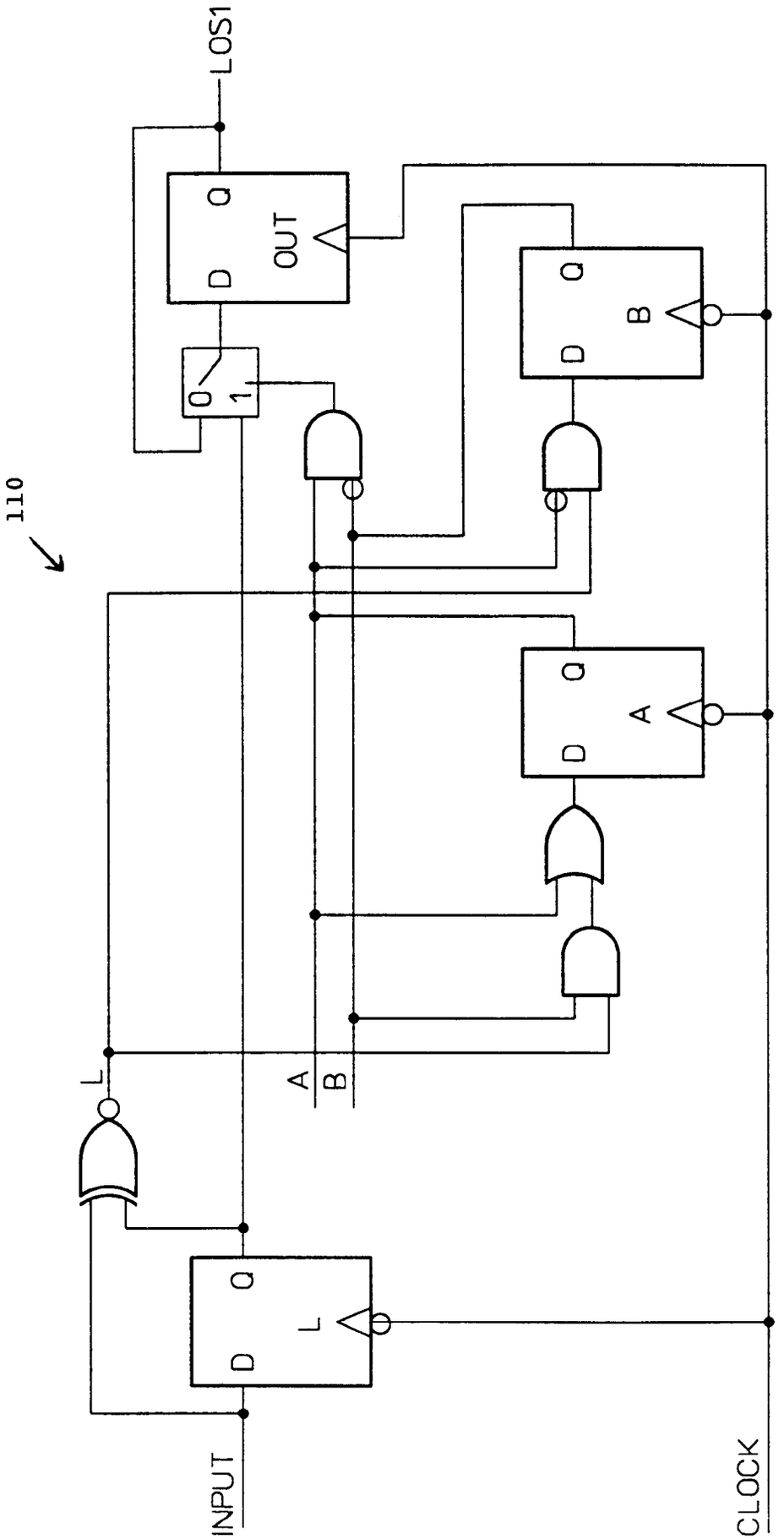

FIG. 6

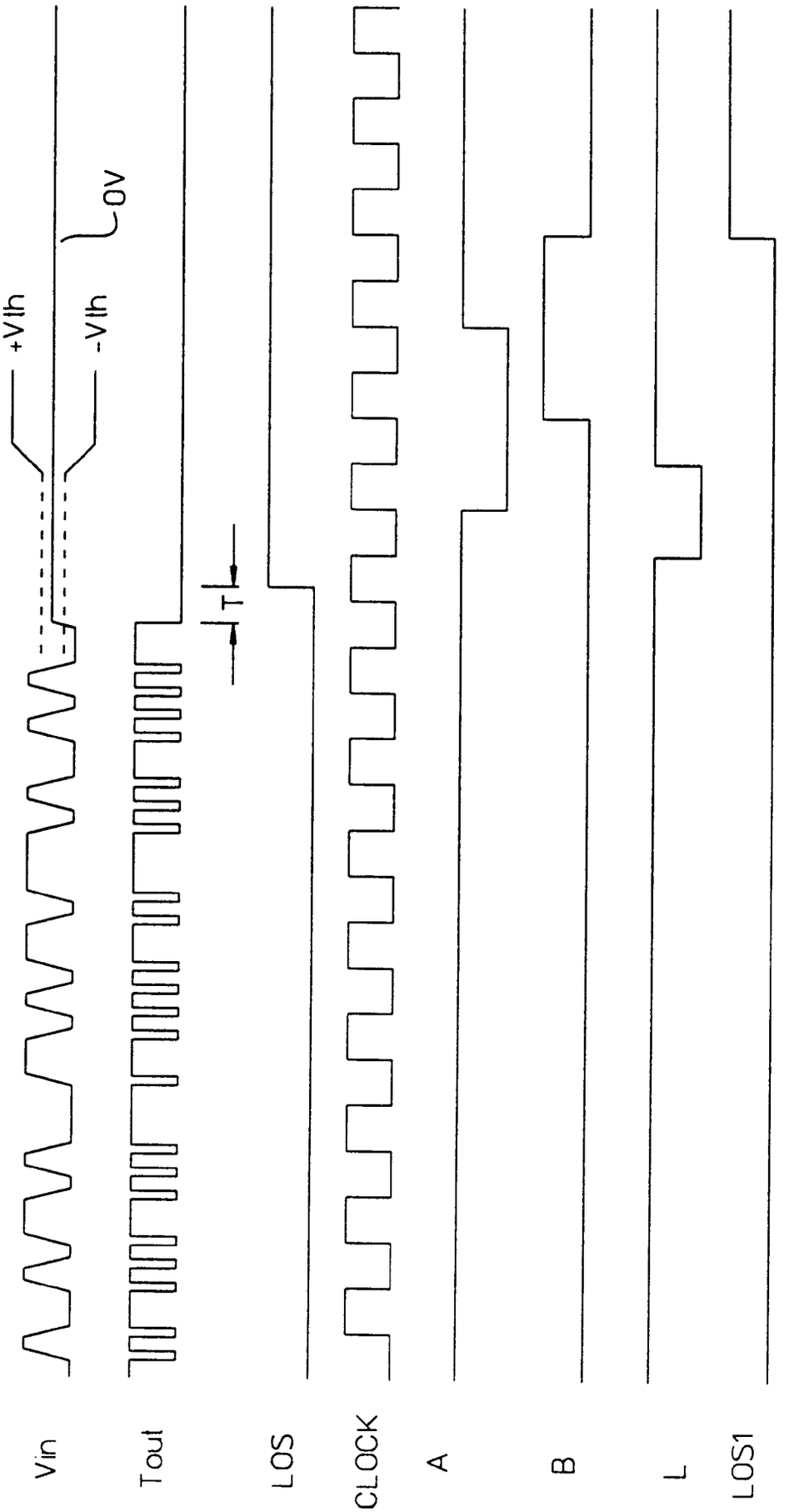

FIG. 7