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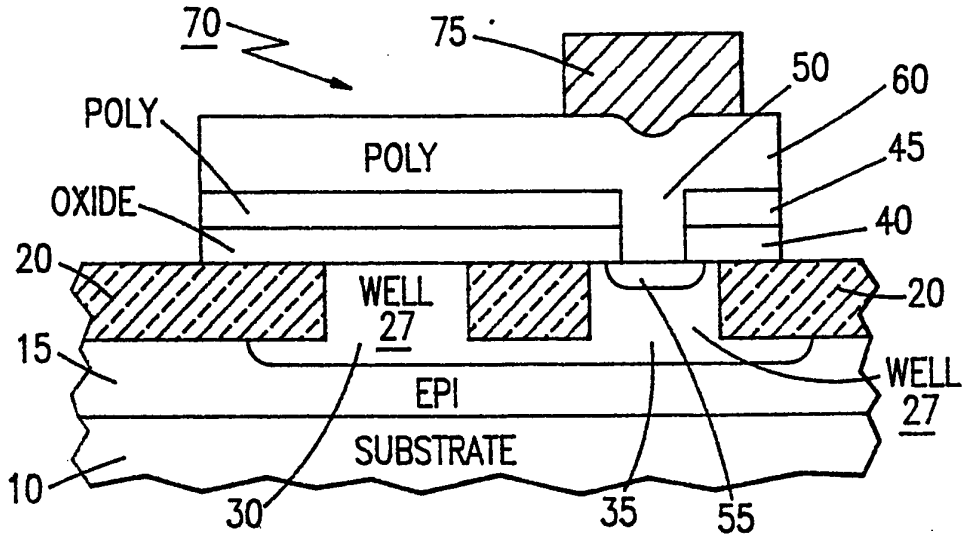
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(54) Title: MOS DEVICE HAVING PROTECTION AGAINST ELECTROSTATIC DISCHARGE



(57) Abstract

A MOS device having protection against electrostatic discharge includes a protection diode formed below the MOS device so that excess charge buildup in the MOS device is conducted away from the MOS device by the protection diode.

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MOS DEVICE HAVING PROTECTION AGAINST ELECTROSTATIC DISCHARGE

TECHNICAL FIELD

The present invention relates generally to MOS devices and, more particularly, to a MOS device having protection against electrostatic discharge and, even more particularly, to a MOS device having protection against electrostatic discharge during manufacturing.

BACKGROUND OF THE INVENTION

In recent years, electrostatic discharge (ESD) has become an increasingly critical factor in the yield and reliability of MOS-type integrated circuits. Specifically, ESD has been known to result in the destruction of MOS devices to the inputs and/or outputs of the completed integrated circuit of which the MOS device is a component. In reaction, numerous protection circuits have been developed by circuit designers to solve the problem of damage to MOS devices caused by ESD. Some of these protection circuits have been somewhat effective in protecting input and output MOS devices during an ESD transient. However, the problem of ESD has not yet been effectively addressed in regard to protecting MOS devices during early stages of manufacturing or processing of MOS-type integrated circuits, i.e., prior to completion of the MOS-type integrated circuit.

As a specific example, protection against ESD damage is particularly important for today's MOS

transistors which utilize very thin gate oxides and shallow source/drain junctions. For instance, present day MOS transistor gate oxides can have a thickness of approximately 100 Angstroms or less, and source/drain junctions of 2000 Angstroms or less. Such very thin gate oxides and shallow source/drain junctions are highly vulnerable to being damaged by ESD. By way of example, some dry etching techniques implemented during manufacturing, such as reactive ion etching or plasma etching, can create electrostatic charge on a gate which exceeds the dielectric field strength of the gate oxide, thereby causing breakdown of the gate oxide and destruction of the MOS transistor. See, for example, "Dielectric Breakdown of Gate Insulator Due to Reactive Ion Etching", by T. Watanabe and Y. Yoshida, Solid State Technology, April, 1984, pp. 263-266. Generally, the dielectric field strength of a 100 Angstrom gate oxide is approximately 10MV/cm, and electrostatic charge of 10V would exceed this dielectric field strength so as to cause breakdown of the gate oxide.

Thus, there remains a need for protection against damage to MOS-type devices, such as, MOS transistors, caused by ESD. Such protection is more particularly required during the manufacturing of integrated circuits having MOS devices integrated therein.

SUMMARY OF THE INVENTION

Broadly speaking, the present invention relates to a MOS device having protection against electrostatic discharge, and a process for fabricating the same. The MOS device includes a semiconductor substrate, and

an epitaxial layer grown on the semiconductor substrate. A tie-down region is formed in the epitaxial layer, and a protection diode is formed in the tie-down region. An insulating layer is grown on the epitaxial layer, and the insulating layer has a buried protection diode window formed therein at a location directly above the protection diode so as to expose the protection diode. A conductive layer is deposited on the insulating layer, such that the conductive layer fills the buried protection diode window and contacts the protection diode. Thus, excess charge buildup in the MOS device is conducted through the conductive layer and away from the MOS device by the protection diode.

In a particular example of the present invention, a MOS transistor has protection against electrostatic discharge by having a buried protection diode formed below the gate of the transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, aspects and advantages will be more readily apparent and better understood from the following detailed description of the invention, in which:

FIGS. 1-5 show consecutive process steps in accordance with the present invention for fabricating a MOS transistor having a buried gate protection diode for protection against ESD during subsequent processing of the MOS transistor; and

FIG. 6 illustrates a specific example of utilization of the present invention in a BiCMOS technology.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although the specific example given hereinafter is of a MOS transistor, it should be fully understood by those skilled in the art that the present invention has applicability and usefulness in any thin oxide MOS device which requires protection against ESD. By way of example, such devices may include on-chip capacitors, trench capacitors, polysilicon resistors, or the like.

Referring initially to FIG. 1A, there is shown a semiconductor substrate 10 having an epitaxial layer 15 grown thereon by conventional methods. Depending upon whether an NMOS or PMOS transistor is being fabricated, the epitaxial layer 15 can either be N-type or P-type. Isolations 20 are formed in the epitaxial layer 15. In conjunction with the gate, the isolations 20 define the source and drain regions of the MOS transistor. The isolations 20 can be formed by conventional methods, such as by local oxidation of silicon (LOCOS), trench/refill (CVD SiO_2), or the like.

A photoresist mask 25 is applied and an impurity having a conductivity opposite to the conductivity of the epitaxial layer 15 is implanted into the epitaxial layer 15 so as to form a well 27 having well regions 30,35. Those skilled in the art will understand that the advantages associated with having one integrated well 27 for each MOS transistor fabricated is related to layout density and conservation of real estate. As described hereinbelow, well region 30 will be used to form the source and drain regions of the MOS

transistor, and drain regions of the MOS transistor, and well region 35 will be used to form a buried diode for protection of the MOS transistor. In this way, the buried diode is integrated as part of the MOS transistor structure.

As an example, if an NMOS transistor is being fabricated, then an P-type impurity, such as boron, can be implanted into the N-type epitaxial layer 15 so that the well regions 30,35 will be P-type regions; and if a PMOS transistor is being fabricated, then a N-type impurity, such as phosphorous, can be implanted into the P-type epitaxial layer 15 so that the well regions 30,35 will be N-type regions.

FIG. 1B shows a top view of the structure of FIG. 1A, but without the photoresist mask 25 applied thereto. As described hereinbelow, well region 30 is used to form the active source and drain regions of the MOS transistor, and well region 35 is used to form a tie-down region which will be included as part of the protection circuit in accordance with the present invention.

As shown in FIG. 2, after formation of the well regions 30,35, a layer of oxide 40 is grown on the epitaxial layer 15 using conventional methods. The layer of oxide 40 is used for formation of a gate, and those skilled in the art will appreciate that other insulating material can be used in lieu of oxide, such as nitride, a composite of oxide and nitride, or the like. As mentioned in the Background of the Invention, in today's technology this layer of gate oxide 40 can have a thickness of approximately 100 Angstroms or less.

Optionally, some processes may require there to be a layer of protective polysilicon 45 deposited on

the layer of gate oxide 40. Generally, the protective polysilicon layer 45 has a thickness of approximately 600 Angstroms. The protective polysilicon layer 45 functions to protect the gate oxide 40 from contamination during further processing. However, it should be understood that the protective polysilicon layer 45 may not be required for fabrication of the MOS transistor, and is not essential to the practice of the present invention. As shown in FIG. 3, the layer of gate oxide 40 and the protective polysilicon layer 45 (if included) are then etched so as to form a buried protection diode window 50. For reasons explained hereinbelow, it is important that the buried protection diode window 50 be located substantially directly above the well region 35 for forming the protection circuit. A layer of gate polysilicon 60 is then deposited over the protective polysilicon layer 45. It should be understood that another layer of conductive material, such as metal, single crystal Si, or the like can be substituted for the layer of gate polysilicon 60.

The gate polysilicon 60 must fill the buried protection diode window 50 so as to cover and contact the tie-down region 35. An impurity of a conductivity opposite the conductivity of the well 35 is then implanted into the well region 35 and gate polysilicon 60 so as to form the source/drain regions of the MOS transistor and gate polysilicon dopant. Preferably, subsequently, a buried diode region 55 is formed by the out-diffusion of dopant impurities from the gate polysilicon 60 utilizing conventional MOS annealing heat treatments. Alternatively, the buried diode region 55 can be formed by a separate step of ion implantation prior to deposition of the gate

polysilicon 60. It should be important to understand that the buried diode region 55 can be contacted through the buried protection diode window 50.

The buried diode region 55 and the well region 35 form a buried diode. Illustratively, the gate polysilicon layer 60 can have a thickness over the gate oxide 40 and protective polysilicon 45 of approximately 0.1 micrometers. A photoresist mask 65 is then applied over the gate polysilicon 60 for formation of the gate.

Referring now to FIG. 4, the gate polysilicon layer 60, protective polysilicon layer 45 and gate oxide layer 40 are then etched so as to form gate 70. Conventionally, metal is then deposited and etched to form a gate contact 75 so as to complete the MOS transistor. A layer of thin-film insulation (not shown), such as tetraethoxysilane (TEOS), CVD SiO_2, PSG, etc, can then be applied over the transistor for isolation of metallization levels. Thus, the transistor or, more specifically, the gate polysilicon 60 is tied down so as to form a protection circuit. Advantageously, the protection circuit is formed at a very early stage of chip manufacture, and no metallization layers are utilized for such formation. The protection circuit protects the transistor during subsequent manufacturing steps. For example, if electrostatic charge on the gate 70 was to exceed the dielectric field strength of the gate oxide 40, the excess charge build-up would be conducted through the gate polysilicon 60 and away from the MOS transistor either by the forward operation or by the reverse saturation current of the diode formed by the buried diode region 55 and the well region 35. Accordingly, damage to the transistor is prevented.

As can be seen in FIG. 5, the buried diode region 55 is located directly below the gate 70 of the transistor. Thus, advantageously, no additional real estate or silicon area on the surface of the wafer is required for addition of the protection circuit. In other words, the buried diode is situated within the same silicon area that the gate 70 of the MOS transistor occupies so that no additional real estate is required for the addition of the buried diode.

Furthermore, since no additional silicon area is required by the addition of the buried protection diode, no metallization wiring channels are blocked by the protection circuit. This holds true for either used or unused MOS transistors.

Additionally, it should be noted that this protection circuit is particularly desirable and easily implemented in most BiCMOS technologies since the photoresist mask for forming the buried protection diode window 50 is already available. For example, this would be the case if the gate conductive material of the MOS transistor is the same as the base conductive material of the bipolar transistor being utilized in the BiCMOS technology; or, alternatively, this would also be the case if the gate conductive material of the MOS transistor is the same as the emitter conductive material of the bipolar transistor being utilized in the BiCMOS technology. Formation of the buried protection diode window 50 would then be "free".

More specifically, the same photoresist mask used in the formation of either the opening for the base or emitter, whichever the case may be, of the bipolar device can be altered to include, an opening for the buried protection diode window 50, and these

openings can then be formed in the same step. In this manner, no additional photoresist mask and/or process step is required to form the buried protection diode window 50, and its formation is thus considered to be "free". As such, no additional step is required to form the protection circuit of the present invention.

A specific example of a BiCMOS technology involving an NMOS transistor 85 and an NPN transistor 90 is shown in FIG. 6. In this example, the material of the gate polysilicon 60′ of the NMOS transistor 85 is the same as the material of the base polysilicon 95 of the NPN transistor 90. The opening for the base of the NPN transistor 90 is referenced generally by the reference numeral 100. By altering the photoresist mask used to form the base opening of the NPN transistor 90, the buried protection diode window 50′ can be formed in the same etch step required to form the base opening of the NPN transistor 90. The gate polysilicon 60′ and the base polysilicon 95 can then also both be deposited in one process step. Thus, since the photoresist mask and etch step used for forming the buried protection diode window 50′ are already required for forming the base opening of the NPN transistor 90, formation of the buried protection diode window 50′ is considered to be "free". Those skilled in the art will realize that this concept of forming the buried protection diode window for "free" can be extended to other technologies in which thin oxide devices are susceptible to ESD-like transients. For example, a protection diode window may also be formed for the devices mentioned hereinabove, specifically, such devices may include

on-chip capacitors, trench capacitors, polysilicon resistors, or the like.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Thus, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the appended claims.

What is claimed is:

1. A MOS device having protection against electrostatic discharge, comprising:

a semiconductor substrate;

an epitaxial layer grown on said semiconductor substrate;

a tie-down region formed in said epitaxial layer;

a protection diode formed in said tie-down region;

an insulating layer grown on said epitaxial layer, said insulating layer having a buried protection diode window formed therein at a location directly above said protection diode so as to expose said protection diode;

a conductive layer deposited on said insulating layer, said conductive layer filling said buried protection diode window and contacting said protection diode, wherein excess charge buildup in the MOS device is conducted through said conductive layer and away from the MOS device by said protection diode.

2. A MOS device according to claim 1, wherein said insulating layer comprises oxide.

3. A MOS device according to claim 1, wherein said insulating layer comprises nitride.

4. A MOS device according to claim 1, wherein said insulating layer comprises oxide and nitride.

5. A MOS device according to claim 1, wherein said conductive layer comprises polysilicon.

6. A MOS device according to claim 1, wherein said conductive layer comprises metal.

7. A MOS device according to claim 1, wherein said conductive layer comprises single crystal silicon.

8. A process for fabricating a MOS device having protection against electrostatic discharge, comprising the steps of:

providing a semiconductor substrate;

growing an epitaxial layer on said semiconductor substrate;

forming a tie-down region in said epitaxial layer;

growing a layer of insulating material on said epitaxial layer;

forming a buried protection diode window in said layer of insulating material at a location directly above said tie-down region so as to expose said tie-down region;

depositing a layer of conductive material over said insulating material, said layer of conductive material filling said buried protection diode window and forming a protection diode in said tie-down region; and

etching said layer of conductive material and said layer of insulating material so as to form a MOS device;

wherein excess charge buildup in the MOS device is conducted through said conductive material and away from the MOS device by said protection diode.

9. A process for fabricating a MOS device according to claim 8, wherein said layer of insulating material comprises oxide.

10. A process for fabricating a MOS device according to claim 8, wherein said layer of insulating material comprises nitride.

11. A process for fabricating a MOS device according to claim 8, wherein said layer of insulating material comprises oxide and nitride.

12. A process for fabricating a MOS device according to claim 8, wherein said layer of conductive material comprises polysilicon.

13. A process for fabricating a MOS device according to claim 8, wherein said layer of conductive material comprises metal.

14. A process for fabricating a MOS device according to claim 8, wherein said layer of conductive material comprises single crystal silicon.

15. A MOS transistor having protection against electrostatic discharge, comprising:

a semiconductor substrate;

an epitaxial layer grown on said semiconductor substrate;

isolations formed in said epitaxial layer;

a source region, a drain region and a tie-down region formed in said epitaxial layer between said isolations, said regions being defined by said isolations;

a protection diode formed in said tie-down region;

a gate insulating layer grown on said epitaxial layer, said gate insulating layer having a buried protection diode window formed therein at a location directly above said protection diode so as to expose said protection diode;

a gate conductive layer deposited on said gate insulating layer, said gate conductive layer filling said buried protection diode window and contacting said protection diode, wherein excess charge buildup in the MOS transistor is conducted through said gate conductive layer and away from the MOS transistor by said protection diode.

16. A MOS transistor according to claim 15, wherein said gate insulating layer comprises oxide.

17. A MOS transistor according to claim 15, wherein said gate insulating layer comprises nitride.

18. A MOS transistor according to claim 15, wherein said gate insulating layer comprises oxide and nitride.

19. A MOS transistor according to claim 15, wherein said gate conductive layer comprises polysilicon.

20. A MOS transistor according to claim 15, wherein said gate conductive layer comprises metal.

21. A MOS transistor according to claim 15, wherein said gate conductive layer comprises single crystal silicon.

22. A MOS transistor according to claim 15, wherein the MOS transistor is a NMOS transistor.

23. A MOS transistor according to claim 15, wherein the MOS transistor is a PMOS transistor.

24. A MOS transistor according to claim 15, further comprising a protective layer between said gate insulating layer and said gate conductive layer.

25. A MOS transistor according to claim 24, wherein said protective layer comprises polysilicon.

26. A MOS transistor according to claim 15, wherein said gate insulating layer has a thickness of less than approximately 100 Angstroms.

27. A MOS transistor according to claim 15, wherein the MOS transistor is implemented in a BiCMOS technology.

28. A MOS transistor according to claim 27, wherein said gate conductive layer of the MOS transistor comprises the same material used to form the base of a bipolar transistor.

29. A MOS transistor according to claim 27, wherein said gate conductive layer of the MOS transistor comprises the same material used to form the emitter of a bipolar transistor.

30. A process for fabricating a MOS transistor having protection against electrostatic discharge, comprising the steps of:

providing a semiconductor substrate;

growing an epitaxial layer on said semiconductor substrate;

forming isolations in said epitaxial layer;

forming a source region, a drain region and a tie-down region in said epitaxial layer between said isolations, said regions being defined by said isolations;

growing a layer of insulating material on said epitaxial layer;

forming a buried protection diode window in said layer of insulating material at a location directly above said tie-down region so as to expose said tie-down region;

depositing a layer of conductive material over said layer of insulating material, said layer of conductive material filling said buried protection diode window and forming a protection diode in said tie-down region; and

etching said layer of conductive and said layer of insulating material so as to form a gate;

wherein excess charge buildup in the MOS transistor is conducted through said conductive material and away from the MOS transistor by said protection diode.

31. A process for fabricating a MOS device according to claim 30, wherein said layer of insulating material comprises oxide.

32. A process for fabricating a MOS device according to claim 30, wherein said layer of insulating material comprises nitride.

33. A process for fabricating a MOS device according to claim 30, wherein said layer of insulating material comprises oxide and nitride.

34. A process for fabricating a MOS device according to claim 30, wherein said layer of conductive material comprises polysilicon.

35. A process for fabricating a MOS device according to claim 30, wherein said layer of conductive material comprises metal.

36. A process for fabricating a MOS device according to claim 30, wherein said layer of conductive material comprises single crystal silicon.

37. A process for fabricating a MOS transistor according to claim 30, wherein said protection diode is formed in said tie-down region by out-diffusion.

38. A process for fabricating a MOS transistor according to claim 30, wherein said protection diode is formed in said tie-down region by ion implantation.

39. A process for fabricating a MOS transistor according to claim 30, wherein the MOS transistor is a NMOS transistor.

40. A process for fabricating a MOS transistor according to claim 30, wherein the MOS transistor is a PMOS transistor.

41. A process for fabricating a MOS transistor according to claim 30, further comprising the step of

depositing a protective layer on said layer of insulating material prior to said step of forming a buried protection diode window, said protective layer protecting said layer of insulating material from contamination during processing.

42. A process for fabricating a MOS transistor according to claim 41, wherein said protective layer comprises polysilicon.

43. A process for fabricating a MOS transistor according to claim 30, wherein said layer of insulating material has a thickness of less than approximately 100 Angstroms.

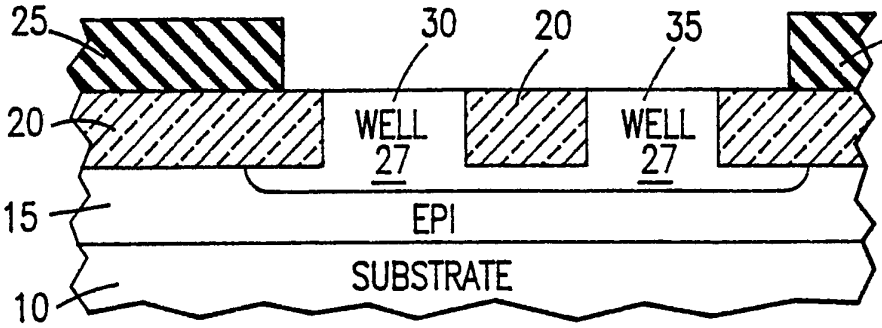


FIG.1A

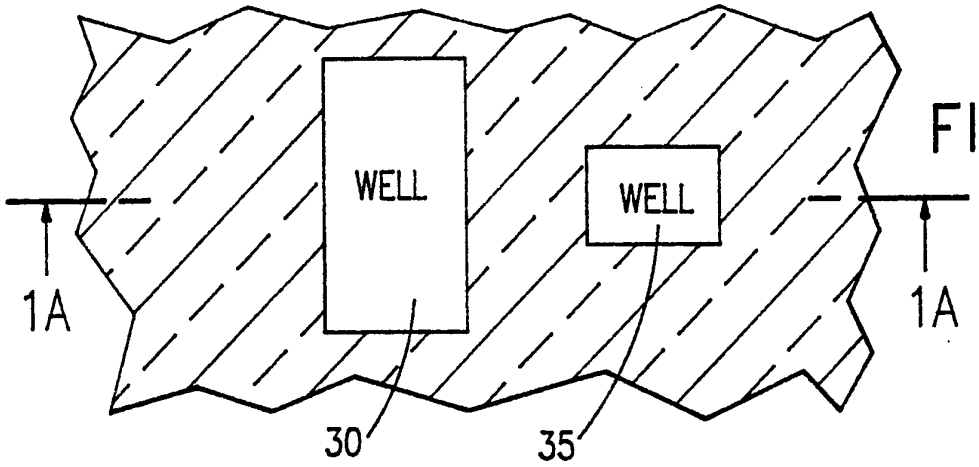


FIG.1B

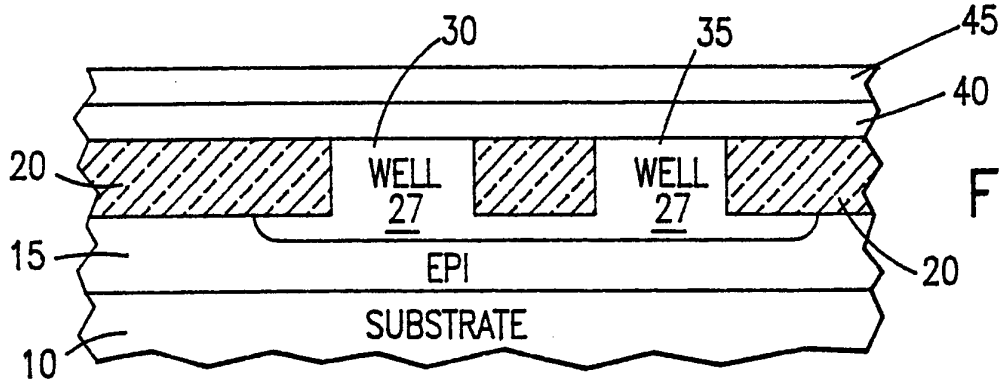


FIG.2

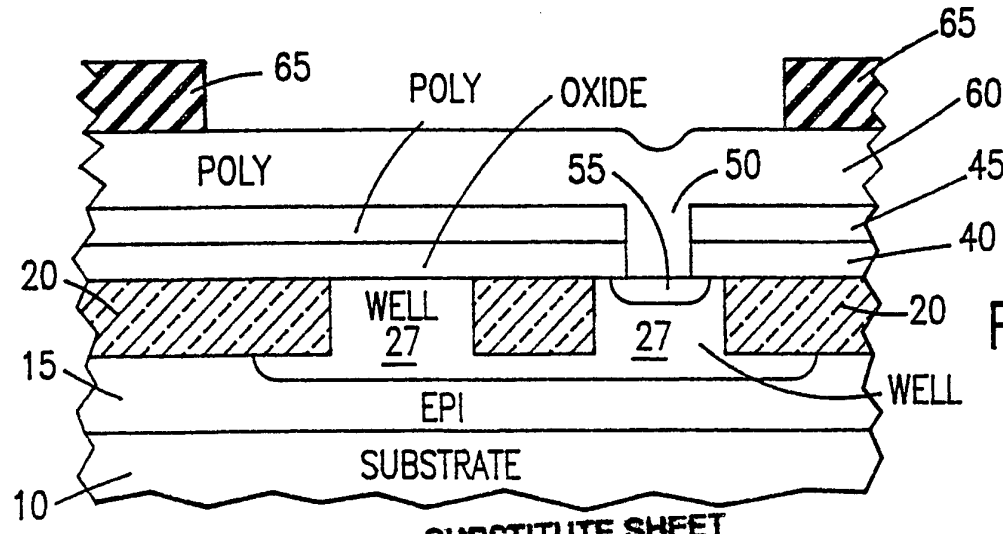


FIG.3

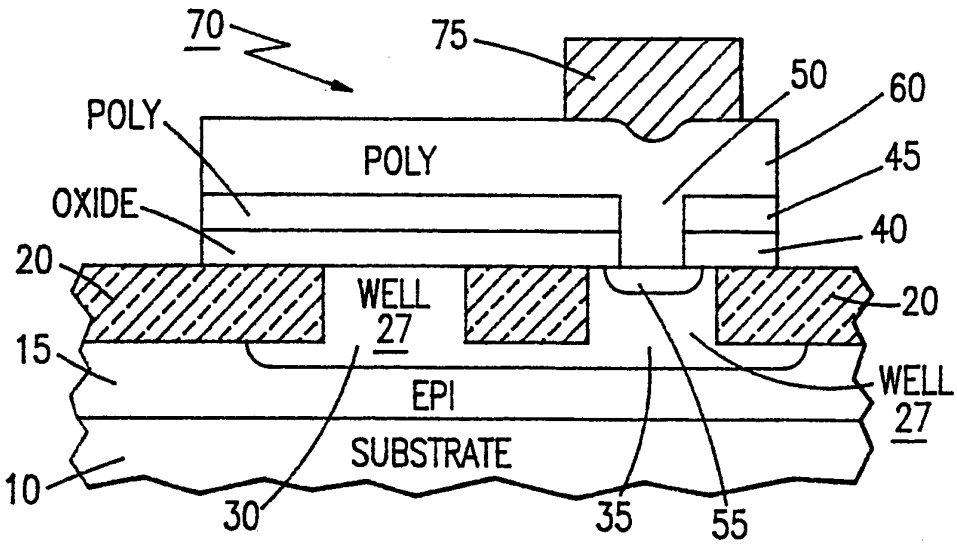


FIG.4

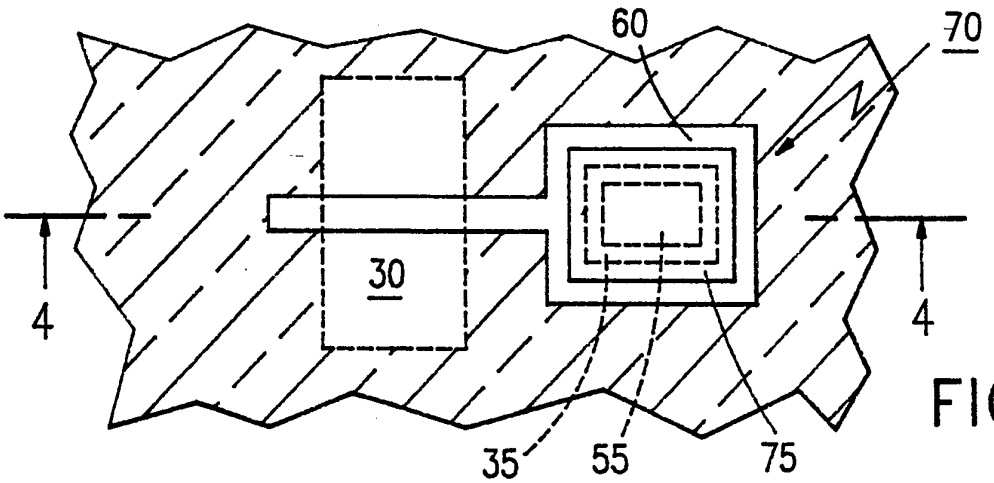


FIG.5

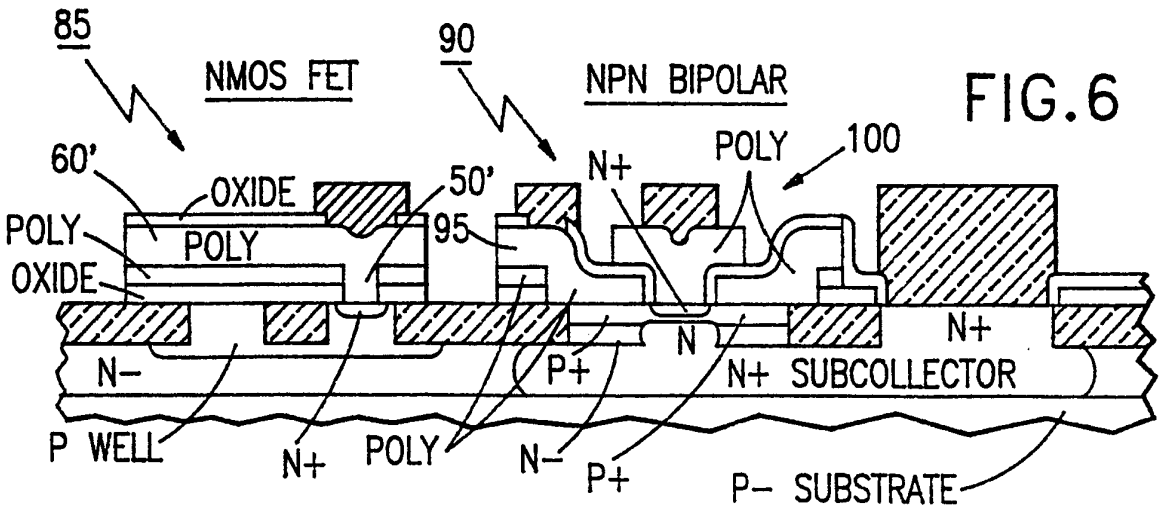


FIG.6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/09404

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L27/02

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 36 (E-227)16 February 1984 & JP,A,58 194 364 (HITACHI) 12 November 1983 see abstract ---	1-43
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 164 (E-410)11 June 1986 & JP,A,61 014 764 (SHINDENGEN KOGYO) 22 January 1986 see abstract ---	1-43
A	US,A,4 119 440 (HILE) 10 October 1978 see column 5, line 56 - column 7, line 63; figures 3-5 ---	1-43

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
05 MARCH 1993	15. 03. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VENDANGE P.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,3 789 503 (NISHIDA) 5 February 1974 see column 2, line 49 - column 4, line 26; figures	1-43
A	DE,A,3 408 285 (TELEFUNKEN) 19 September 1985 see abstract; figures	1-43
A	EP,A,0 387 944 (N. V. PHILIPS) 19 September 1990 see abstract; figures	1-43

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9209404
SA 66819

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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US-A-3789503	05-02-74	None	
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