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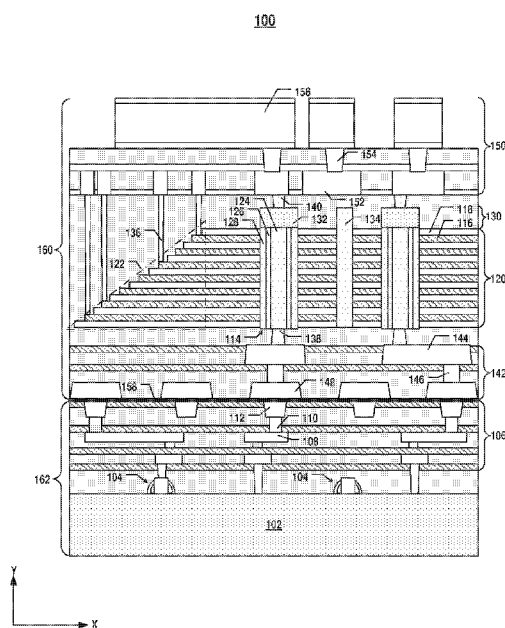


FIG. 1

(57) Abstract: Embodiments of methods for forming three-dimensional (3D) memory devices are disclosed. In an example, a peripheral device is formed on a first substrate. A first interconnect layer is formed above the peripheral device on the first substrate. A dielectric stack including a plurality of dielectric/sacrificial layer pairs and a plurality of memory strings each extending vertically through the dielectric stack is formed on a second substrate. A second interconnect layer is formed above the memory strings on the second substrate. The first substrate and the second substrate are bonded, so that the first interconnect layer is below and in contact with the second interconnect layer. The second substrate is thinned after the bonding. A memory stack is formed below the thinned second substrate and including a plurality of conductor/dielectric layer pairs by replacing, with a plurality of conductor layers, sacrificial layers in the dielectric/sacrificial layer pairs.

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METHODS FOR FORMING THREE-DIMENSIONAL MEMORY DEVICES

BACKGROUND

- [0001] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.
- [0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.
- [0003] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

- [0004] Embodiments of methods for forming 3D memory devices are disclosed herein.
- [0005] In one example, a method for forming a 3D memory device is disclosed. A peripheral device is formed on a first substrate. A first interconnect layer is formed above the peripheral device on the first substrate. A dielectric stack including a plurality of dielectric/sacrificial layer pairs and a plurality of memory strings each extending vertically through the dielectric stack is formed on a second substrate. A second interconnect layer is formed above the memory strings on the second substrate. The first substrate and the second substrate are bonded, so that the first interconnect layer is below and in contact with the second interconnect layer. The second substrate is thinned after the bonding. A memory stack is formed below the thinned second substrate and including a plurality of conductor/dielectric layer pairs by replacing, with a plurality of conductor layers, sacrificial layers in the dielectric/sacrificial layer pairs.
- [0006] In another example, a method for forming a 3D memory device is disclosed. A peripheral device is formed on a first substrate. A first interconnect layer is formed above the peripheral device on the first substrate. A plurality of memory strings each extending vertically are formed on a second substrate. A second interconnect layer is formed above

the memory strings on the second substrate. The first substrate and the second substrate are bonded, so that the first interconnect layer is below and in contact with the second interconnect layer. The second substrate is thinned after the bonding. A memory stack is formed below the thinned second substrate and including a plurality of conductor/dielectric layer pairs. Edges of the conductor/dielectric layer pairs in a staircase structure of the memory stack along a vertical direction away from the first substrate are staggered laterally toward the memory strings.

[0007] In still another example, a method for forming a 3D memory device is disclosed. A plurality of memory strings each extending vertically are formed on a substrate. An interconnect layer is formed above the memory strings. The substrate is flipped upside down so that the substrate is above the memory strings. The substrate is thinned after the flipping. After the thinning, a memory stack is formed below the thinned substrate and including a plurality of conductor/dielectric layer pairs. A plurality of first via contacts are formed, such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0009] FIG. 1 illustrates a cross-section of an exemplary 3D memory device, according to some embodiments.

[0010] FIGs. 2A-2B illustrate a fabrication process for forming an exemplary peripheral device chip, according to some embodiments.

[0011] FIGs. 3A-3D illustrate a fabrication process for forming an exemplary memory array device chip, according to some embodiments.

[0012] FIGs. 4A-4F illustrate a fabrication process for forming an exemplary 3D memory device with a memory array device chip bonded to a peripheral device chip, according to some embodiments.

[0013] FIG. 5 is a flowchart of a method for forming an exemplary peripheral device chip, according to some embodiments.

- [0014] FIG. 6 is a flowchart of a method for forming an exemplary memory array device chip, according to some embodiments.
- [0015] FIG. 7 is a flowchart of a method for forming an exemplary 3D memory device with a memory array device chip bonded to a peripheral device chip, according to some embodiments.
- [0016] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

- [0017] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.
- [0018] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.
- [0019] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended

to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0020] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0021] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0022] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0023] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For

example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0024] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0025] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0026] Various embodiments in accordance with the present disclosure provide a method for forming a 3D memory device with a smaller die size, higher cell density, and improved performance compared with other 3D memory devices. By vertically stacking a memory array device chip above a peripheral device chip, the cell density of the resulting 3D memory device can be increased. Moreover, by decoupling the peripheral device processing and the memory array device processing, the thermal budget associated with processing the memory array device is not limited by performance requirement of the peripheral device. Similarly, the peripheral device performance is not impacted by the memory array device processing. For example, the peripheral device and the memory array device can be separately fabricated on different substrates so that certain high-temperature processes for fabricating the memory array device will not adversely affect the fabrication of the peripheral device (e.g., avoid excess diffusion of the dopants, control the doping concentration and/or thickness of ion implantation, etc.).

[0027] FIG. 1 illustrates a cross-section of an exemplary 3D memory device 100 according to some embodiments of the present disclosure. 3D memory device 100

represents an example of a non-monolithic 3D memory device. The term “non-monolithic” means that the components of 3D memory device 100 (e.g., peripheral devices and memory array devices) can be formed separately on different substrates and then joined to form a 3D memory device. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), or any other suitable materials.

[0028] 3D memory device 100 can include a peripheral device on substrate 102. The peripheral device can be formed “on” substrate 102, where the entirety or part of the peripheral device is formed in substrate 102 (e.g., below the top surface of substrate 102) and/or directly on substrate 102. The peripheral device can include a plurality of transistors 104 formed on substrate 102. Isolation regions (e.g., shallow trench isolations (STIs), not shown) and doped regions (e.g., source regions and drain regions of transistors 104, not shown) can be formed in substrate 102 as well.

[0029] In some embodiments, the peripheral device can include any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100. For example, the peripheral device can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). In some embodiments, the peripheral device is formed on substrate 102 using complementary metal-oxide-semiconductor (CMOS) technology (also known as a “CMOS chip”).

[0030] 3D memory device 100 can include an interconnect layer 106 (referred to herein as a “peripheral interconnect layer”) above transistors 104 to transfer electrical signals to and from transistors 104. Peripheral interconnect layer 106 can include a plurality of interconnects (also referred to herein as “contacts”), including lateral interconnect lines 108 and vertical interconnect access (via) contacts 110. As used herein, the term “interconnects” can broadly include any suitable types of interconnects, such as middle-end-of-line (MEOL) interconnects and back-end-of-line (BEOL) interconnects. Peripheral interconnect layer 106 can further include one or more interlayer dielectric (ILD) layers (also known as “intermetal dielectric (IMD) layers”) in which interconnect lines 108 and via contacts 110 can form. That is, peripheral interconnect layer 106 can

include interconnect lines 108 and via contacts 110 in multiple ILD layers. Interconnect lines 108 and via contacts 110 in peripheral interconnect layer 106 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. The ILD layers in peripheral interconnect layer 106 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low dielectric constant (low-k) dielectrics, or any combination thereof.

[0031] In some embodiments, peripheral interconnect layer 106 further includes a plurality of bonding contacts 112 at the top surface of peripheral interconnect layer 106. Bonding contacts 112 can include conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. The remaining areas at the top surface of peripheral interconnect layer 106 can be formed with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. Conductive materials (of bonding contacts 112) and dielectric materials at the top surface of peripheral interconnect layer 106 can be used for hybrid bonding as described below in detail.

[0032] 3D memory device 100 can include a memory array device above the peripheral device. It is noted that x and y axes are included in FIG. 1 to further illustrate the spatial relationship of the components in 3D memory device 100. Substrate 102 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x -direction (i.e., the lateral or width direction). As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate of the semiconductor device (e.g., substrate 102) in the y -direction (i.e., the vertical or thickness direction) when the substrate is positioned in the lowest plane of the semiconductor device in the y -direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0033] In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND memory strings 114 each extending vertically above the peripheral device (e.g., transistors 104) and substrate 102. The memory array device can include NAND memory strings 114 that extend vertically through a plurality of pairs each including a conductor layer 116 and a

dielectric layer 118 (referred to herein as “conductor/dielectric layer pairs”). The stacked conductor/dielectric layer pairs are also referred to herein as a “memory stack” 120. Conductor layers 116 and dielectric layers 118 in memory stack 120 alternate in the vertical direction. In other words, except the ones at the top or bottom of memory stack 120, each conductor layer 116 can be adjoined by two dielectric layers 118 on both sides, and each dielectric layer 118 can be adjoined by two conductor layers 116 on both sides. Conductor layers 116 can each have the same thickness or different thicknesses. Similarly, dielectric layers 118 can each have the same thickness or different thicknesses. Conductor layers 116 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Dielectric layers 118 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0034] Memory stack 120 can include an inner region (also known as a “core array region”) and an outer region (also known as a “staircase region”). In some embodiments, the inner region is the center region of memory stack 120 where array of NAND memory strings 114 are formed, and the outer region is the remaining region of memory stack 120 surrounding the inner region (including the sides and edges). As shown in FIG. 1, at least on one lateral side, the outer region of memory stack 120 can include a staircase structure 122. The edges of the conductor/dielectric layer pairs in staircase structure 122 of memory stack 120 along the vertical direction away from substrate 102 (the positive y -direction) are staggered laterally toward array of NAND memory strings 114. In other words, the edges of memory stack 120 in staircase structure 122 can be tilted toward the inner region as moving away from substrate 102 (from bottom to top). The slope of staircase structure 122 can face away from substrate 102. In some embodiments, the length of each conductor/dielectric layer pair of memory stack 120 increases from the top to the bottom.

[0035] In some embodiments, each two adjacent conductor/dielectric layer pairs in staircase structure 122 are offset by a nominally same distance in the vertical direction and a nominally same distance in the lateral direction. Each offset thus can form a “landing area” for word line fan-out in the vertical direction. Some of conductor layers 116 in the conductor/dielectric layer pairs can function as the word lines of 3D memory device 100 and extend laterally into staircase structure 122 for interconnection. As shown

in FIG. 1, the offset of the edges of each adjacent conductor/dielectric layer pairs in staircase structure 122 is nominally the same, according to some embodiments.

[0036] As shown in FIG. 1, each NAND memory string 114 can extend vertically through the inner region of memory stack 120 and include a semiconductor channel 124 and a dielectric layer (also known as a “memory film”). In some embodiments, semiconductor channel 124 includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, the memory film is a composite layer including a tunneling layer 126, a storage layer 128 (also known as a “charge trap/storage layer”), and a blocking layer (not shown). Each NAND memory string 114 can have a cylinder shape (e.g., a pillar shape). Semiconductor channel 124, tunneling layer 126, storage layer 128, and the blocking layer are arranged radially from the center toward the outer surface of the pillar in this order, according to some embodiments. Tunneling layer 126 can include silicon oxide, silicon oxynitride, or any combination thereof. Storage layer 128 can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof.

[0037] In some embodiments, NAND memory strings 114 further include a plurality of control gates (each being part of a word line). Each conductor layer 116 in memory stack 120 can act as a control gate for each memory cell of NAND memory string 114. Each NAND memory string 114 can include a source select gate at its upper end and a drain select gate at its lower end. As used herein, the “upper end” of a component (e.g., NAND memory string 114) is the end farther away from substrate 102 in the y-direction, and the “lower end” of the component (e.g., NAND memory string 114) is the end closer to substrate 102 in the y-direction. For each NAND memory string 114, the drain select gate can be disposed below the source select gate in 3D memory device 100.

[0038] In some embodiments, 3D memory device 100 further includes a semiconductor layer 130 disposed above and in contact with NAND memory strings 114, for example, on the upper end of each NAND memory string 114. Memory stack 120 can be disposed below semiconductor layer 130. Semiconductor layer 130 can be a thinned substrate on which memory stack 120 is formed. In some embodiments, semiconductor layer 130 includes a plurality of semiconductor plugs 132 electrically separated by isolation regions (e.g., STIs). In some embodiments, each semiconductor plug 132 is disposed at the upper

end of corresponding NAND memory string 114 and functions as the source of corresponding NAND memory string 114 and thus, can be considered as part of corresponding NAND memory string 114. Semiconductor plug 132 can include a single crystalline silicon. Semiconductor plug 132 can be un-doped, partially doped (in the thickness direction and/or the width direction), or fully doped by p-type or n-type dopants. In some embodiments, semiconductor plug 132 can include SiGe, GaAs, Ge, or any other suitable materials. In some embodiments, the thickness of semiconductor layer 130 (and semiconductor plug 132 therein) is between about 0.1 μm and about 50 μm , such as between 0.1 μm and 50 μm . In some embodiments, the thickness of semiconductor layer 130 (and semiconductor plug 132 therein) is between about 0.2 μm and about 5 μm , such as between 0.2 μm and 5 μm (e.g., 0.2 μm , 0.3 μm , 0.4 μm , 0.5 μm , 0.6 μm , 0.7 μm , 0.8 μm , 0.9 μm , 1 μm , 2 μm , 3 μm , 4 μm , 5 μm , any range bounded by the lower end by any of these values, or in any range defined by any two of these values).

[0039] In some embodiments, 3D memory device 100 further includes a gate line slit (“GLS”) 134 that extends vertically through memory stack 120. GLS 134 can be used to form the conductor/dielectric layer pairs in memory stack 120 by a gate replacement process. In some embodiments, GLS 134 is firstly filled with dielectric materials, for example, silicon oxide, silicon nitride, or any combination thereof, for separating the NAND memory string array into different regions (e.g., memory fingers and/or memory blocks). Then, GLS 134 is filled with conductive and/or semiconductor materials, for example, W, Co, polysilicon, or any combination thereof, for electrically controlling an array common source (ACS), according to some embodiments.

[0040] In some embodiments, 3D memory device 100 includes local interconnects that are formed in one or more ILD layers and in contact with components in memory stack 120, such as the word lines (e.g., conductor layers 116) and NAND memory strings 114. The interconnects are referred to herein as “local interconnects” as they are in contact with the components in memory stack 120 directly for fan-out. As used herein, the term “interconnects” can broadly include any suitable types of interconnects, including vertical interconnect access (e.g., via) contacts and lateral interconnect lines. The local interconnects can include word line via contacts 136, bit line via contacts 138, and source line via contacts 140. Each local interconnect can include an opening (e.g., a via hole or a

trench) filled with conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof.

[0041] Word line via contacts 136 can extend vertically through one or more ILD layers. Each word line via contact 136 can have its lower end in contact with corresponding conductor layer 116 (e.g., at the landing area) in staircase structure 122 of memory stack 120 to individually address a corresponding word line of 3D memory device 100. In some embodiments, each word line via contact 136 is disposed above corresponding conductor layer 116. Each bit line via contact 138 can be disposed below memory stack 120 and have its upper end in contact with the lower end (the drain end) of corresponding NAND memory string 114 to individually address corresponding NAND memory string 114. Multiple bit line via contacts 138 are disposed below and in contact with multiple NAND memory strings 114, respectively, according to some embodiments. As shown in FIG. 1, word line via contacts 136 and bit line via contacts 138 fan-out the corresponding memory stack components toward opposite vertical directions (the positive and negative y-directions). Source line via contacts 140 can extend vertically through one or more ILD layers. Each source line via contact 140 can have its lower end in contact with corresponding semiconductor plug 132 (e.g., the source) of NAND memory string 114. In some embodiments, each source line via contact 140 is disposed above corresponding NAND memory string 114.

[0042] Similar to the peripheral device, the memory array device of 3D memory device 100 can also include interconnect layers for transferring electrical signals to and from NAND memory strings 114. As shown in FIG. 1, 3D memory device 100 can include an interconnect layer 142 (referred to herein as an “array interconnect layer”) below NAND memory strings 114. Array interconnect layer 142 can include a plurality of interconnects, including interconnect lines 144 and via contacts 146 in one or more ILD layers. In some embodiments, array interconnect layer 142 includes a plurality of bonding contacts 148 at its bottom surface. Interconnect lines 144, via contacts 146, and bonding contacts 148 can include conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. The remaining areas at the bottom surface of array interconnect layer 142 can be formed with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. Conductive materials (of bonding contacts 148) and dielectric materials at the bottom

surface of array interconnect layer 142 can be used for hybrid bonding as described below in detail.

[0043] As shown in FIG. 1, another interconnect layer 150 (referred to herein as a “BEOL interconnect layer”) can be disposed above NAND memory strings 114 and semiconductor layer 130 and can include interconnects, such as interconnect lines 152 and via contacts 154 in one or more ILD layers. BEOL interconnect layer 150 can further include contact pads 156 and a redistribution layer (not shown) at the top surface of 3D memory device 100 for wire bonding and/or bonding with an interposer. BEOL interconnect layer 150 and array interconnect layer 142 can be formed at opposite sides of NAND memory strings 114. In some embodiments, interconnect lines 152, via contacts 154, and contact pads 156 in BEOL interconnect layer 150 can transfer electrical signals between 3D memory device 100 and external circuits. BEOL interconnect layer 150 can be electrically connected to the memory stack components by the local interconnects. As shown in FIG. 1, each word line via contact 136 can have its upper end in contact with BEOL interconnect layer 150. Similarly, each source line via contact 140 can have its upper end in contact with BEOL interconnect layer 150. The arrangement and configuration of staircase structure 122 and semiconductor layer 130 allow direct fan-out of the word lines (e.g., conductor layers 116) and the sources of NAND memory strings 114 through the local interconnects (e.g., word line via contacts 136 and source line via contacts 140) and BEOL interconnect layer 150 without detouring through array interconnect layer 142.

[0044] In some embodiments, 3D memory device 100 further includes one or more through array contacts (TACs, not shown) that extend vertically through memory stack 120. Each TAC can extend through the entirety of memory stack 120, (e.g., all the conductor/dielectric layer pairs therein) and have its upper end in contact with BEOL interconnect layer 150 and its lower end in contact with array interconnect layer 142. TACs can thus make electrical connections between peripheral interconnect layer 106 and BEOL interconnect layer 150 and carry electrical signals from the peripheral device to the BEOL interconnects of 3D memory device 100.

[0045] A bonding interface 158 can be formed between peripheral interconnect layer 106 and array interconnect layer 142. Bonding contacts 112 can be bonded with bonding contacts 148 at bonding interface 158. As shown in FIG. 1, the peripheral device (e.g.,

transistors 104) can be disposed below the memory array device (e.g., NAND memory strings 114) in 3D memory device 100 after bonding. In 3D memory device 100, bonding interface 158 is disposed between the memory array device (e.g., memory strings 114) and the peripheral device (e.g., transistors 104), according to some embodiments. Peripheral interconnect layer 106 can be between bonding interface 158 and the peripheral device (e.g., transistors 104), and array interconnect layer 142 can be between bonding interface 158 and the memory array device (e.g., memory strings 114).

[0046] In some embodiments, a first semiconductor structure (e.g., a memory array device chip 160), including NAND memory strings 114, semiconductor layer 130 (e.g., a thinned substrate), array interconnect layer 142, BEOL interconnect layer 150, and word line via contacts 136, is bonded to a second semiconductor structure (e.g., a peripheral device chip 162), including substrate 102, the peripheral device (e.g., transistors 104), and peripheral interconnect layer 106, in a face-to-face manner at bonding interface 158. Array interconnect layer 142 can contact peripheral interconnect layer 106 at bonding interface 158. Peripheral device chip 162 and memory array device chip 160 can be bonded using hybrid bonding (also known as “metal/dielectric hybrid bonding”), which is a direct bonding technology (e.g., forming bonding between surfaces without using intermediate layers, such as solder or adhesives) and can obtain metal-metal bonding and dielectric-dielectric bonding simultaneously. The metal-metal bonding can be formed between bonding contacts 148 and bonding contacts 112, and the dielectric-dielectric bonding can be formed between the dielectric materials at the remaining areas at bonding interface 158.

[0047] FIGs. 2A-2B illustrate a fabrication process for forming an exemplary peripheral device chip, according to some embodiments. FIGs. 3A-3D illustrate a fabrication process for forming an exemplary memory array device chip, according to some embodiments. FIGs. 4A-4F illustrate a fabrication process for forming an exemplary 3D memory device with a memory array device chip bonded to a peripheral device chip, according to some embodiments. FIG. 5 is a flowchart of a method 500 for forming an exemplary peripheral device chip, according to some embodiments. FIG. 6 is a flowchart of a method 600 for forming an exemplary memory array device chip, according to some embodiments. FIG. 7 is a flowchart of a method 700 for forming an exemplary 3D memory device with a memory array device chip bonded to a peripheral device chip,

according to some embodiments. Examples of the 3D memory device depicted in FIGs. 2-7 include 3D memory device 100 depicted in FIG. 1. FIGs. 2-7 will be described together. It is understood that the operations shown in methods 500, 600, and 700 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIGs. 5-7.

[0048] Referring to FIG. 5, method 500 starts at operation 502, in which a peripheral device is formed on a first substrate. The substrate can be a silicon substrate. As illustrated in FIG. 2A, a peripheral device is formed on a silicon substrate 202. The peripheral device can include a plurality of transistors 204 formed on silicon substrate 202. Transistors 204 can be formed by a plurality of processes including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, chemical mechanical polishing (CMP), and any other suitable processes. In some embodiments, doped regions (not shown) are formed in silicon substrate 202 by ion implantation and/or thermal diffusion, which function, for example, as source regions and/or drain regions of transistors 204. In some embodiments, isolation regions (e.g., STIs, not shown) are also formed in silicon substrate 202 by wet/dry etch and thin film deposition.

[0049] Method 500 proceeds to operation 504, as illustrated in FIG. 5, in which a first interconnect layer (e.g., a peripheral interconnect layer) is formed above the peripheral device. The peripheral interconnect layer can include a first plurality of interconnects in one or more ILD layers. Method 500 proceeds to operation 506, as illustrated in FIG. 5, in which a first plurality of bonding contacts are formed at the top surface of the peripheral interconnect layer.

[0050] As illustrated in FIG. 2B, a peripheral interconnect layer 206 can be formed above transistors 204. Peripheral interconnect layer 206 can include interconnects, including interconnect lines 208 and via contacts 210 of MEOL and/or BEOL of the peripheral device chip in a plurality of ILD layers, to make electrical connections with the peripheral device (e.g., transistors 204). Bonding contacts 212 can be formed at the top surface of peripheral interconnect layer 206 for hybrid bonding. In some embodiments, peripheral interconnect layer 206 includes multiple ILD layers and interconnects therein formed by multiple processes. For example, interconnect lines 208, via contacts 210, and bonding

contacts 212 can include conductive materials deposited by one or more thin film deposition processes including, but not limited to, chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), electroplating, electroless plating, or any combination thereof. Fabrication processes to form interconnect lines 208, via contacts 210, and bonding contacts 212 can also include photolithography, CMP, wet/dry etch, or any other suitable processes. The ILD layers can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. The ILD layers and interconnects illustrated in FIG. 2B can be collectively referred to as an “interconnect layer” (e.g., peripheral interconnect layer 206).

[0051] Referring to FIG. 6, method 600 includes operation 602, in which a dielectric stack is formed on a second substrate. The substrate can be a silicon substrate. The dielectric stack can include a plurality of dielectric/sacrificial layer pairs. As illustrated in FIG. 3A, isolation regions 304 (e.g., STIs) are formed in a silicon substrate 302 by wet/dry etch and thin film deposition to electrically isolate silicon plugs 306 (e.g., single crystalline silicon plugs). Silicon plugs 306 can be patterned and doped with n-type or p-type dopant using ion implantation and/or thermal diffusion processes. In some embodiments, the thickness of isolation regions 304 and silicon plugs 306 is between about 0.1 μm and about 50 μm , such as between 0.1 μm and 50 μm . In some embodiments, the thickness of isolation regions 304 and silicon plugs 306 is between about 0.2 μm and about 5 μm , such as between 0.2 μm and 5 μm (e.g., 0.2 μm , 0.3 μm , 0.4 μm , 0.5 μm , 0.6 μm , 0.7 μm , 0.8 μm , 0.9 μm , 1 μm , 2 μm , 3 μm , 4 μm , 5 μm , any range bounded by the lower end by any of these values, or in any range defined by any two of these values).

[0052] As illustrated in FIG. 3B, pairs of a first dielectric layer 310 and a second dielectric layer (known as a “sacrificial layer”) 312 (together referred to herein as “dielectric layer pairs”) are formed on silicon substrate 302. The stacked dielectric layer pairs can form a dielectric stack 308. Dielectric stack 308 can include an alternating stack of sacrificial layer 312 and dielectric layer 310 that is different from sacrificial layer 312. In some embodiments, each dielectric layer pair includes a layer of silicon nitride and a layer of silicon oxide. In some embodiments, sacrificial layers 312 can each have the same thickness or have different thicknesses. Similarly, dielectric layers 310 can each

have the same thickness or have different thicknesses. Dielectric stack 308 can be formed by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof.

[0053] Method 600 proceeds to operation 604, as illustrated in FIG. 6, in which a plurality of memory strings each extending vertically through the dielectric stack are formed. As illustrated in FIG. 3C, NAND memory strings 314 are formed on silicon substrate 302, each of which extends vertically through dielectric stack 308. In some embodiments, each NAND memory string 314 can be aligned with corresponding silicon plug 306. Silicon plug 306 can be part of NAND memory string 314. In some embodiments, fabrication processes to form NAND memory string 314 include forming a semiconductor channel 316 that extends vertically through dielectric stack 308. In some embodiments, fabrication processes to form NAND memory string 314 also include forming a composite dielectric layer (memory film) between semiconductor channel 316 and the plurality of dielectric/sacrificial layer pairs in dielectric stack 308. The memory film can be a combination of multiple dielectric layers including, but not limited to, a tunneling layer 318, a storage layer 320, and a blocking layer.

[0054] Tunneling layer 318 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. Storage layer 320 can include materials for storing charge for memory operation. The storage layer materials can include, but not limited to, silicon nitride, silicon oxynitride, a combination of silicon oxide and silicon nitride, or any combination thereof. The blocking layer can include dielectric materials including, but not limited to, silicon oxide or a combination of silicon oxide/silicon oxynitride/silicon oxide (ONO). The blocking layer can further include a high-k dielectric layer, such as an aluminum oxide layer. Semiconductor channel 316 and the memory film (including tunneling layer 318 and storage layer 320) can be formed by processes such as ALD, CVD, PVD, any other suitable processes, or any combination thereof.

[0055] Method 600 proceeds to operation 606, as illustrated in FIG. 6, in which a second interconnect layer (e.g., an array interconnect layer) is formed above the memory strings. The array interconnect layer can include a second plurality of interconnects in one or more ILD layers. Method 600 proceeds to operation 608, as illustrated in FIG. 6, in which a second plurality of bonding contacts are formed at the top surface of the array

interconnect layer. As illustrated in FIG. 3D, an array interconnect layer 322 can be formed above dielectric stack 308 and NAND memory strings 314. Array interconnect layer 322 can include interconnects, including interconnect lines 324 and via contacts 326 in one or more ILD layers for transferring electrical signals to and from NAND memory strings 314. In some embodiments, bit line via contacts 321 can be formed in an ILD layer formed above dielectric stack 308 prior to forming array interconnect layer 322, such that each bit line via contact 321 is above and in contact with corresponding NAND memory string 314. Bonding contacts 328 can be formed at the top surface of array interconnect layer 322 for hybrid bonding.

[0056] In some embodiments, array interconnect layer 322 includes multiple ILD layers and interconnects therein formed in multiple processes. For example, interconnect lines 324, via contacts 326, and bonding contacts 328 can include conductive materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Fabrication processes to form interconnect lines 324, via contacts 326, and bonding contacts 328 can also include photolithography, CMP, wet/dry etch, or any other suitable processes. The ILD layers can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. The ILD layers and interconnects illustrated in FIG. 3D can be collectively referred to as an “interconnect layer” (e.g., array interconnect layer 322).

[0057] Referring to FIG. 7, method 700 includes operation 702, in which the second substrate on which the memory strings are formed is flipped upside down. As a result, the second substrate is above the memory strings. Method 700 proceeds to operation 704, as illustrated in FIG. 7, in which the second substrate and the first substrate on which the peripheral device is formed are bonded in a face-to-face manner, so that the peripheral interconnect layer is below and in contact with the array interconnect layer. The bonding can be hybrid bonding.

[0058] As illustrated in FIG. 4A, silicon substrate 302 and components formed thereon (e.g., NAND memory strings 314) are flipped upside down. Array interconnect layer 322 facing down is to be bonded with peripheral interconnect layer 206 facing up, i.e., in a face-to-face manner, so that array interconnect layer 322 can be above and in contact with peripheral interconnect layer 206 in the resulting 3D memory device. In some

embodiments, bonding contacts 328 of array interconnect layer 322 are aligned with bonding contacts 214 of peripheral interconnect layer 206 prior to the bonding. As a result, bonding contacts 328 can be in contact with bonding contacts 214 when silicon substrate 302 is joined with silicon substrate 202. In some embodiments, a treatment process, e.g., a plasma treatment, a wet treatment, and/or a thermal treatment, is applied to the bonding surfaces prior to the bonding. As a result of the bonding, e.g., hybrid bonding, bonding contacts 328 can be inter-mixed with bonding contacts 214, thereby forming a bonding interface 402 between array interconnect layer 322 and peripheral interconnect layer 206, as shown in FIG. 4B.

[0059] Method 700 proceeds to operation 706, as illustrated in FIG. 7, in which the second substrate is thinned. As illustrated in FIG. 4B, silicon substrate 302 becomes a single crystalline silicon layer 404 (including silicon plugs 306 and the surrounding isolation regions) after the thinning. In some embodiments, after the thinning process, single crystalline silicon layer 404 (and silicon plugs 306 therein) has a thickness between about 0.1 μm and about 50 μm , such as between 0.1 μm and 50 μm . In some embodiments, the thickness of single crystalline silicon layer 404 (and silicon plugs 306 therein) is between about 0.2 μm and about 5 μm , such as between 0.2 μm and 5 μm (e.g., 0.2 μm , 0.3 μm , 0.4 μm , 0.5 μm , 0.6 μm , 0.7 μm , 0.8 μm , 0.9 μm , 1 μm , 2 μm , 3 μm , 4 μm , 5 μm , any range bounded by the lower end by any of these values, or in any range defined by any two of these values). Silicon substrate 302 can be thinned by processes including, but not limited to, wafer grinding, dry etch, wet etch, CMP, any other suitable processes, or any combination thereof.

[0060] Method 700 proceeds to operation 708, as illustrated in FIG. 7, in which a staircase structure is formed at an edge of the dielectric stack. The staircase structure can be formed by performing a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs toward the first substrate. As illustrated in FIG. 4C, a staircase structure 406 is formed at the edge of dielectric stack 308. Edges of the dielectric/sacrificial layer pairs in staircase structure 406 of dielectric stack 308 along the vertical direction away from silicon substrate 202 (the positive y -direction) are staggered laterally toward NAND memory strings 314. To form staircase structure 406, a photoresist layer can be patterned to expose portions of the top one of the dielectric/sacrificial layer pairs. The patterned photoresist layer can be used as an etch mask to etch the exposed portions of the top one

of the dielectric/sacrificial layer pairs by wet etch and/or dry etch. Any suitable etchants (e.g., of wet etch and/or dry etch) can be used to remove the entire thickness of the top one of the dielectric/sacrificial layer pairs in the exposed portions (including sacrificial layer 312 and dielectric layer 310 therein). The etched thickness can be controlled by etch-stop at different materials (e.g., silicon nitride and silicon oxide) used in the dielectric/sacrificial layer pair. The etching of the exposed portions of the top one of the dielectric/sacrificial layer pairs can result in the exposure of portions of the one beneath the top one of the dielectric/sacrificial layer pairs.

[0061] The patterned photoresist layer can then be trimmed (e.g., etched incrementally and inwardly, often from all directions) to expose another portion of the top one of the dielectric/sacrificial layer pairs. The amount of the trimmed photoresist layer can be controlled by trim rate and/or trim time and can be directly relevant (e.g., determinant) to the dimensions of the resulting step structure. The trim of the photoresist layer can be performed using any suitable etch process, e.g., an isotropic dry etch or a wet etch. Both the enlarged exposed portions of the top one of the dielectric/sacrificial layer pairs and the exposed portions of the one beneath the top one of the dielectric/sacrificial layer pairs are etched using the trimmed photoresist layer as an etch mask to form one step structure of staircase structure 406. Any suitable etchants (e.g., of wet etch and/or dry etch) can be used to remove the entire thickness of the dielectric/sacrificial layer pair in the exposed portions (including sacrificial layer 312 and dielectric layer 310 therein) toward silicon substrate 202. The trim process of the photoresist layer followed by the etch process of the dielectric/sacrificial layer pair is referred to herein as a trim-etch cycle for the dielectric/sacrificial layer pairs.

[0062] The trim-etch cycle for the dielectric/sacrificial layer pairs can be repeated toward silicon substrate 202 (the negative *y*-direction) until finishing the etching of the bottom one of the dielectric/sacrificial layer pairs. Consequently, staircase structure 406 having a plurality of step structures at the edge of dielectric stack 308 can be formed. Due to the repeated trim-etch cycles for the dielectric/sacrificial layer pairs, dielectric stack 308 can have a tilted side edge and a top dielectric/sacrificial layer pair shorter than the bottom one, as shown in FIG. 4C.

[0063] Method 700 proceeds to operation 710, as illustrated in FIG. 7, in which a memory stack is formed below the thinned second substrate by replacing, with a plurality

of conductor layers, sacrificial layers in the dielectric/sacrificial layer pairs. The memory stack thus includes a plurality of conductor/dielectric layer pairs. In some embodiments, forming the memory stack includes etching an opening through the thinned second substrate and the dielectric/sacrificial layer pairs, etching the sacrificial layers in the dielectric/sacrificial layer pairs through the opening, and depositing the conductor layers in the conductor/dielectric layer pairs through the opening. As a result, a staircase structure can be formed at an edge of the memory stack. The edges of the conductor/dielectric layer pairs in the staircase structure of the memory stack along the vertical direction away from the first substrate can be staggered laterally toward the memory strings.

[0064] As illustrated in FIG. 4D, a GLS 408 is formed through single crystalline silicon layer 404 and the dielectric/sacrificial layer pairs of dielectric stack 308. GLS 408 can be patterned and etched by wet etch and/or dry etch. Each sacrificial layer 312 (shown in FIG. 4C) of dielectric stack 308 then can be etched through GLS 408, and conductor layers 410 can be deposited through GLS 408. That is, each sacrificial layer 312 of dielectric stack 308 can be replaced by conductor layer 410, thereby forming a plurality of conductor/dielectric layer pairs in a memory stack 412. The replacement of sacrificial layers 312 with conductor layers 410 can be performed by wet/dry etch of sacrificial layers 312 selective to dielectric layers 310 and filling the structure with conductor layers 410. Conductor layers 410 can include conductive materials including, but not limited to, W, Co, Cu, Al, doped silicon, polysilicon, silicides, or any combination thereof. Conductor layers 410 can be filled by thin film deposition processes, such as CVD, ALD, any other suitable process, or any combination thereof.

[0065] As a result, NAND memory strings 314 can each extend vertically through memory stack 412. In some embodiments, conductor layers 410 in memory stack 412 are used to form the select gates and word lines for NAND memory strings 314. At least some of conductor layers 410 in memory stack 412 (e.g., except the top and bottom conductor layers 410) can each be used as word lines of NAND memory strings 314. As a result of the gate replacement, a staircase structure 414 can be formed at the edge of memory stack 412. The edges of the conductor/dielectric layer pairs in staircase structure 414 of memory stack 412 along the vertical direction away from silicon substrate 202 (the positive y-direction) can be staggered laterally toward NAND memory strings 314.

[0066] Method 700 proceeds to operation 712, as illustrated in FIG. 7, in which local interconnects of the memory stack and memory strings are formed. The local interconnects can include word line via contacts formed above the staircase structure of the memory stack and include source line via contacts formed above the memory strings. As illustrated in FIG. 4E, an ILD layer 416 can be formed on single crystalline silicon layer 404 by a thin film deposition process, such as CVD, ALD, any other suitable process, or any combination thereof, of a dielectric material. Source line via contacts 418 can be formed through ILD layer 416 and in contact with silicon plugs 306 of memory strings 314, respectively. Each source line via contact 418 can have its lower end in contact with the upper end of corresponding NAND memory string 314. Word line via contacts 420 are formed through one or more ILD layers (including ILD layer 416) and above staircase structure 414 of memory stack 412, according to some embodiments. The lower end of word line via contact 420 can land on a word line of NAND memory strings 314 (e.g., conductor layer 410) in staircase structure 414 of memory stack 412, such that each word line via contact 420 is above and in contact with corresponding conductor layer 410.

[0067] In some embodiments, fabrication processes to form source line via contacts 418 and word line via contacts 420 include forming vertical openings using a dry/wet etch process, followed by filling the openings with conductive materials and other materials (e.g., a barrier layer, an adhesion layer, and/or a seed layer) for conductor filling, adhesion, and/or other purposes. Source line via contacts 418 and word line via contacts 420 can include conductive materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. The openings of source line via contacts 418 and word line via contacts 420 can be filled with conductive materials and other materials by ALD, CVD, PVD, electroplating, any other suitable processes, or any combination thereof. In some embodiments, GLS 408 can be filled with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof, by CVD, PVD, ALD, any other suitable processes, or any combination thereof.

[0068] Method 700 proceeds to operation 714, as illustrated in FIG. 7, in which a third interconnect layer (e.g., a BEOL interconnect layer) is formed above the thinned second substrate. The BEOL interconnect layer can include a third plurality of interconnects in

one or more ILD layers. As illustrated in FIG. 4F, a BEOL interconnect layer 422 can be formed above single crystalline silicon layer 404 and NAND memory strings 314. BEOL interconnect layer 422 can include interconnects, including interconnect lines 424 and via contacts 426 in one or more ILD layers for transferring electrical signals to and from the 3D memory device. In some embodiments, contact pads 428 and a redistribution layer (not shown) can be formed at the top surface of BEOL interconnect layer 422 for wire bonding and/or bonding with an interposer.

[0069] In some embodiments, BEOL interconnect layer 422 includes multiple ILD layers and interconnects therein formed in multiple processes. For example, interconnect lines 424, via contacts 426, and contact pads 428 can include conductive materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Fabrication processes to form interconnect lines 424, via contacts 426, and contact pads 428 can also include photolithography, CMP, wet/dry etch, or any other suitable processes. The ILD layers can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. The ILD layers and interconnects illustrated in FIG. 4F can be collectively referred to as an “interconnect layer” (e.g., BEOL interconnect layer 422).

[0070] Although not shown, in some embodiments, prior to the bonding, a TAC is formed extending vertically through dielectric stack 308 and in contact with the interconnects in array interconnect layer 322. After the bonding, via contacts can be formed extending vertically through one or more ILD layers and in contact with the TAC, so that BEOL interconnect layer 422 can be electrically connected to periphery interconnect layer 206.

[0071] According to one aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A peripheral device is formed on a first substrate. A first interconnect layer is formed above the peripheral device on the first substrate. A dielectric stack including a plurality of dielectric/sacrificial layer pairs and a plurality of memory strings each extending vertically through the dielectric stack is formed on a second substrate. A second interconnect layer is formed above the memory strings on the second substrate. The first substrate and the second substrate are bonded, so that the first interconnect layer is below and in contact with the second interconnect layer. The second

substrate is thinned after the bonding. A memory stack is formed below the thinned second substrate and including a plurality of conductor/dielectric layer pairs by replacing, with a plurality of conductor layers, sacrificial layers in the dielectric/sacrificial layer pairs.

[0072] In some embodiments, a staircase structure is formed at an edge of the dielectric stack after the bonding. To form the staircase structure, a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs are performed toward the first substrate prior to forming the memory stack, according to some embodiments.

[0073] In some embodiments, a plurality of first via contacts are formed, such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs. In some embodiment, a plurality of second via contacts are formed, such that each of the second via contacts is above and in contact with one of the memory strings.

[0074] In some embodiments, a third interconnect layer is formed above the thinned second substrate after forming the memory stack.

[0075] In some embodiments, the bonding includes hybrid bonding. To bond the first substrate and the second substrate, the second substrate is flipped upside down, according to some embodiments.

[0076] In some embodiments, to form the memory stack, an opening is etched through the thinned second substrate and the plurality of dielectric/sacrificial layer pairs; the sacrificial layers in the plurality of dielectric/sacrificial layer pairs are etched through the opening; and the conductor layers in the plurality of conductor/dielectric layer pairs are deposited through the opening.

[0077] According to another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A peripheral device is formed on a first substrate. A first interconnect layer is formed above the peripheral device on the first substrate. A plurality of memory strings each extending vertically are formed on a second substrate. A second interconnect layer is formed above the memory strings on the second substrate. The first substrate and the second substrate are bonded, so that the first interconnect layer is below and in contact with the second interconnect layer. The second substrate is thinned after the bonding. A memory stack is formed below the thinned second substrate and including a plurality of conductor/dielectric layer pairs. Edges of the conductor/dielectric

layer pairs in a staircase structure of the memory stack along a vertical direction away from the first substrate are staggered laterally toward the memory strings.

[0078] In some embodiments, a dielectric stack including a plurality of dielectric/sacrificial layer pairs through which the memory strings extend vertically is formed prior to the bonding. To form the memory stack, the staircase structure is formed at an edge of the dielectric stack; and sacrificial layers in the dielectric/sacrificial layer pairs are replaced by a plurality of conductor layers, according to some embodiments. To replace the sacrificial layers, an opening is etched through the thinned second substrate and the plurality of dielectric/sacrificial layer pairs; the sacrificial layers in the plurality of dielectric/sacrificial layer pairs are etched through the opening; and the conductor layers in the plurality of conductor/dielectric layer pairs are deposited through the opening, according to some embodiments. In some embodiments, to form the staircase structure, a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs are performed toward the first substrate.

[0079] In some embodiments, a plurality of first via contacts are formed, such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs. In some embodiments, a plurality of second via contacts are formed, such that each of the second via contacts is above and in contact with one of the memory strings.

[0080] In some embodiments, a third interconnect layer is formed above the thinned second substrate after forming the memory stack.

[0081] In some embodiments, the bonding includes hybrid bonding. To bond the first substrate and the second substrate, the second substrate is flipped upside down, according to some embodiments.

[0082] According to still another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A plurality of memory strings each extending vertically are formed on a substrate. An interconnect layer is formed above the memory strings. The substrate is flipped upside down so that the substrate is above the memory strings. The substrate is thinned after the flipping. After the thinning, a memory stack is formed below the thinned substrate and including a plurality of conductor/dielectric layer pairs. A plurality of first via contacts are formed, such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs.

- [0083] In some embodiments, a plurality of second via contacts are formed after forming the memory stack, such that each of the second via contacts is above and in contact with one of the memory strings.
- [0084] In some embodiments, a second interconnect layer is formed above the thinned substrate such that the plurality of first and second via contacts are in contact with the second interconnect layer.
- [0085] In some embodiments, a dielectric stack including a plurality of dielectric/sacrificial layer pairs through which the memory strings extend vertically is formed prior to the flipping. To form the memory stack, a staircase structure is formed at an edge of the dielectric stack; and sacrificial layers in the dielectric/sacrificial layer pairs are replaced by a plurality of conductor layers, according to some embodiments. To replace the sacrificial layers, an opening is etched through the thinned substrate and the plurality of dielectric/sacrificial layer pairs; the sacrificial layers in the plurality of dielectric/sacrificial layer pairs are etched through the opening; and the conductor layers in the plurality of conductor/dielectric layer pairs are deposited through the opening, according to some embodiments. In some embodiments, to form the staircase structure, a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs are performed away from the thinned substrate.
- [0086] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.
- [0087] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries

can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0088] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0089] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for forming a three-dimensional (3D) memory device, comprising:
forming a peripheral device on a first substrate;
forming, on the first substrate, a first interconnect layer above the peripheral device;
forming, on a second substrate, a dielectric stack comprising a plurality of dielectric/sacrificial layer pairs and a plurality of memory strings each extending vertically through the dielectric stack;
forming, on the second substrate, a second interconnect layer above the memory strings;
bonding the first substrate and the second substrate, so that the first interconnect layer is below and in contact with the second interconnect layer;
thinning the second substrate after the bonding; and
forming a memory stack below the thinned second substrate and comprising a plurality of conductor/dielectric layer pairs by replacing, with a plurality of conductor layers, sacrificial layers in the dielectric/sacrificial layer pairs.
2. The method of claim 1, further comprising after the bonding, forming a staircase structure at an edge of the dielectric stack.
3. The method of claim 2, wherein forming the staircase structure comprises prior to forming the memory stack, performing a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs toward the first substrate.
4. The method of any one of claims 1-3, further comprising forming a plurality of first via contacts such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs.
5. The method of any one of claims 1-4, further comprising forming a plurality of second via contacts such that each of the second via contacts is above and in contact with one of the memory strings.

6. The method of any one of claims 1-5, further comprising forming a third interconnect layer above the thinned second substrate after forming the memory stack.
7. The method of any one of claims 1-6, wherein the bonding includes hybrid bonding.
8. The method of any one of claims 1-7, wherein forming the memory stack comprises:
 - etching an opening through the thinned second substrate and the plurality of dielectric/sacrificial layer pairs;
 - etching the sacrificial layers in the plurality of dielectric/sacrificial layer pairs through the opening; and
 - depositing the conductor layers in the plurality of conductor/dielectric layer pairs through the opening.
9. The method of any one of claims 1-8, wherein bonding the first substrate and the second substrate comprises flipping the second substrate upside down.
10. A method for forming a three-dimensional (3D) memory device, comprising:
 - forming a peripheral device on a first substrate;
 - forming, on the first substrate, a first interconnect layer above the peripheral device;
 - forming a plurality of memory strings each extending vertically on a second substrate;
 - forming, on the second substrate, a second interconnect layer above the memory strings;
 - bonding the first substrate and the second substrate, so that the first interconnect layer is below and in contact with the second interconnect layer;
 - thinning the second substrate after the bonding; and
 - forming a memory stack below the thinned second substrate and comprising a plurality of conductor/dielectric layer pairs, wherein edges of the conductor/dielectric layer pairs in a staircase structure of the memory stack along a vertical direction away from the first substrate are staggered laterally toward the memory strings.

11. The method of claim 10, further comprising prior to the bonding, forming, on the second substrate, a dielectric stack comprising a plurality of dielectric/sacrificial layer pairs through which the memory strings extend vertically.

12. The method of claim 11, wherein forming the memory stack comprises:
forming the staircase structure at an edge of the dielectric stack; and
replacing sacrificial layers in the dielectric/sacrificial layer pairs by a plurality of conductor layers.

13. The method of claim 12, wherein replacing the sacrificial layers comprises:
etching an opening through the thinned second substrate and the plurality of dielectric/sacrificial layer pairs;
etching the sacrificial layers in the plurality of dielectric/sacrificial layer pairs through the opening; and
depositing the conductor layers in the plurality of conductor/dielectric layer pairs through the opening.

14. The method of claim 12, wherein forming the staircase structure comprises performing a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs toward the first substrate.

15. The method of any one of claims 10-14, further comprising forming a plurality of first via contacts such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs.

16. The method of any one of claims 10-15, further comprising forming a plurality of second via contacts such that each of the second via contacts is above and in contact with one of the memory strings.

17. The method of any one of claims 10-16, further comprising forming a third interconnect layer above the thinned second substrate after forming the memory stack.

18. The method of any one of claims 10-17, wherein the bonding includes hybrid bonding.

19. The method of any one of claims 10-18, wherein bonding the first substrate and the second substrate comprises flipping the second substrate upside down.

20. A method for forming a three-dimensional (3D) memory device, comprising:
forming a plurality of memory strings each extending vertically on a substrate;
forming an interconnect layer above the memory strings;
flipping the substrate upside down so that the substrate is above the memory strings;
thinning the substrate after the flipping;
after the thinning, forming a memory stack below the thinned substrate and comprising a plurality of conductor/dielectric layer pairs; and
forming a plurality of first via contacts such that each of the first via contacts is above and in contact with a conductor layer of one of the conductor/dielectric layer pairs.

21. The method of claim 20, further comprising after forming the memory stack, forming a plurality of second via contacts such that each of the second via contacts is above and in contact with one of the memory strings.

22. The method of claim 21, further comprising forming a second interconnect layer above the thinned substrate such that the plurality of first and second via contacts are in contact with the second interconnect layer.

23. The method of any one of claims 20-22, further comprising prior to the flipping, forming a dielectric stack comprising a plurality of dielectric/sacrificial layer pairs through which the memory strings extend vertically.

24. The method of claim 23, wherein forming the memory stack comprises:
forming a staircase structure at an edge of the dielectric stack; and
replacing sacrificial layers in the dielectric/sacrificial layer pairs by a plurality of conductor layers.

25. The method of claim 24, wherein replacing the sacrificial layers comprises:
etching an opening through the thinned substrate and the plurality of dielectric/sacrificial layer pairs;
etching the sacrificial layers in the plurality of dielectric/sacrificial layer pairs through the opening; and
depositing the conductor layers in the plurality of conductor/dielectric layer pairs through the opening.

26. The method of claim 24, wherein forming the staircase structure comprises performing a plurality of trim-etch cycles for the dielectric/sacrificial layer pairs away from the thinned substrate.

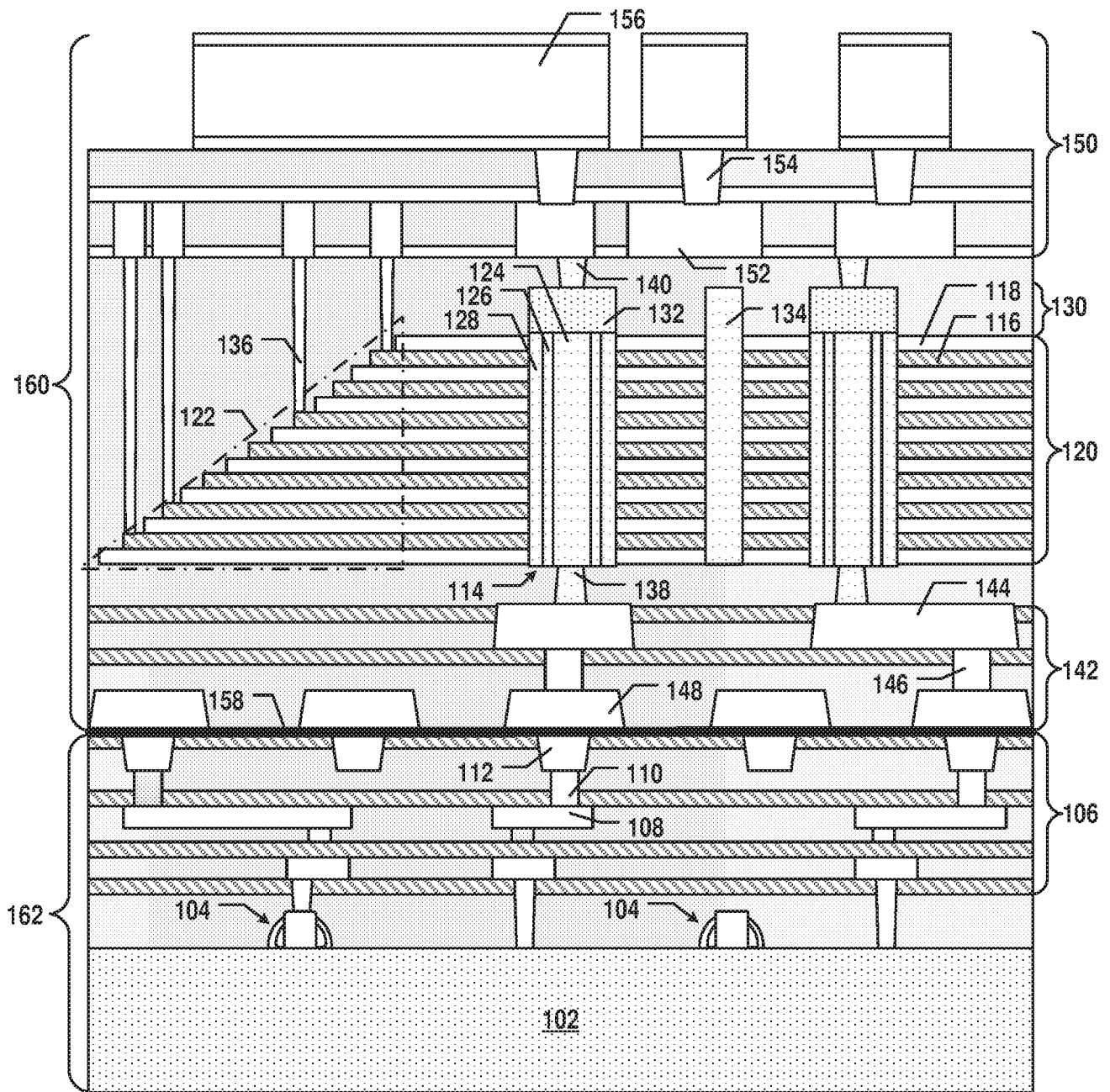
100

FIG. 1

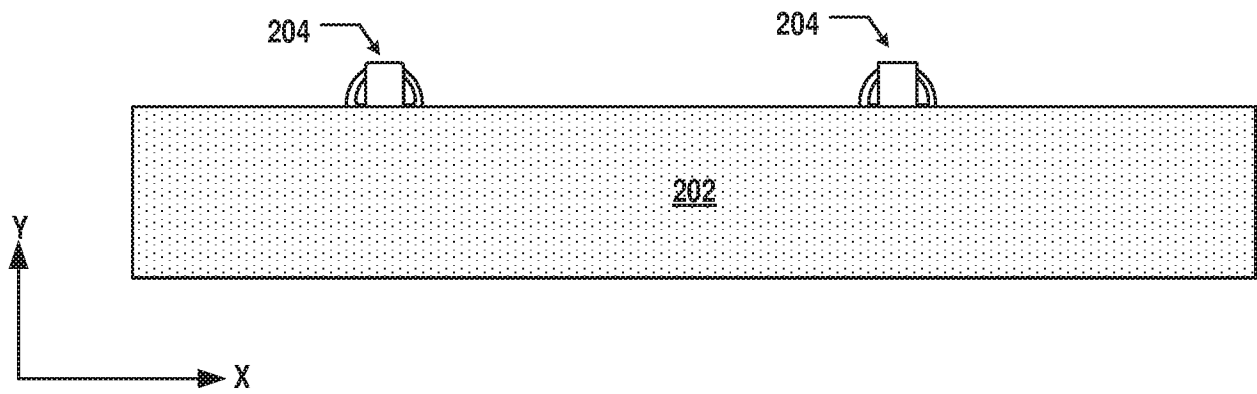


FIG. 2A

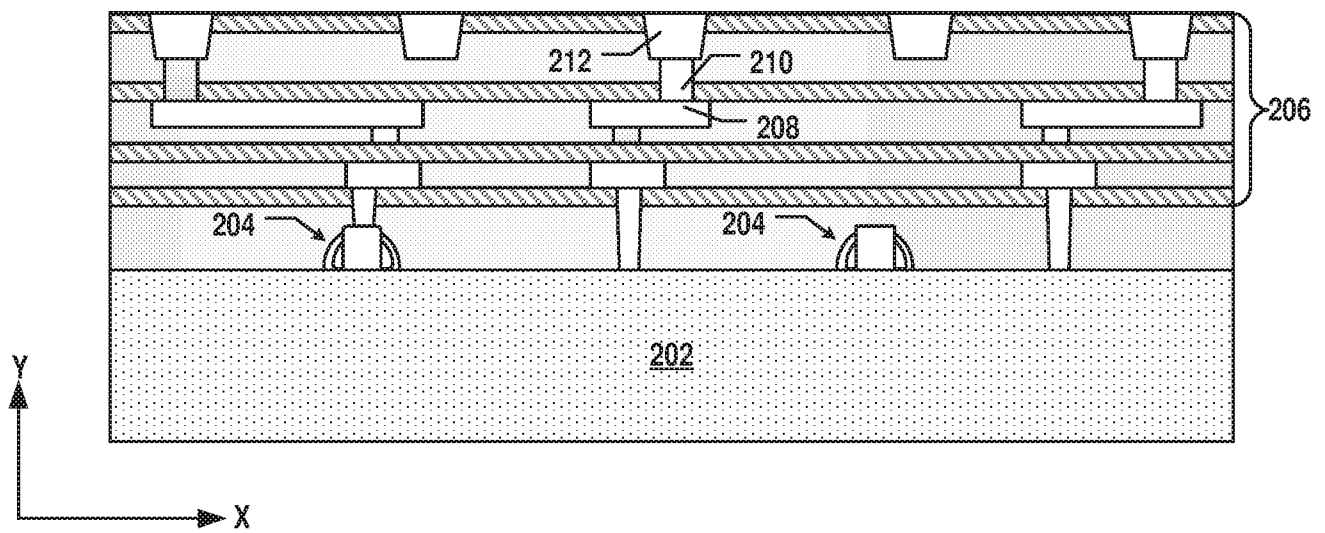


FIG. 2B

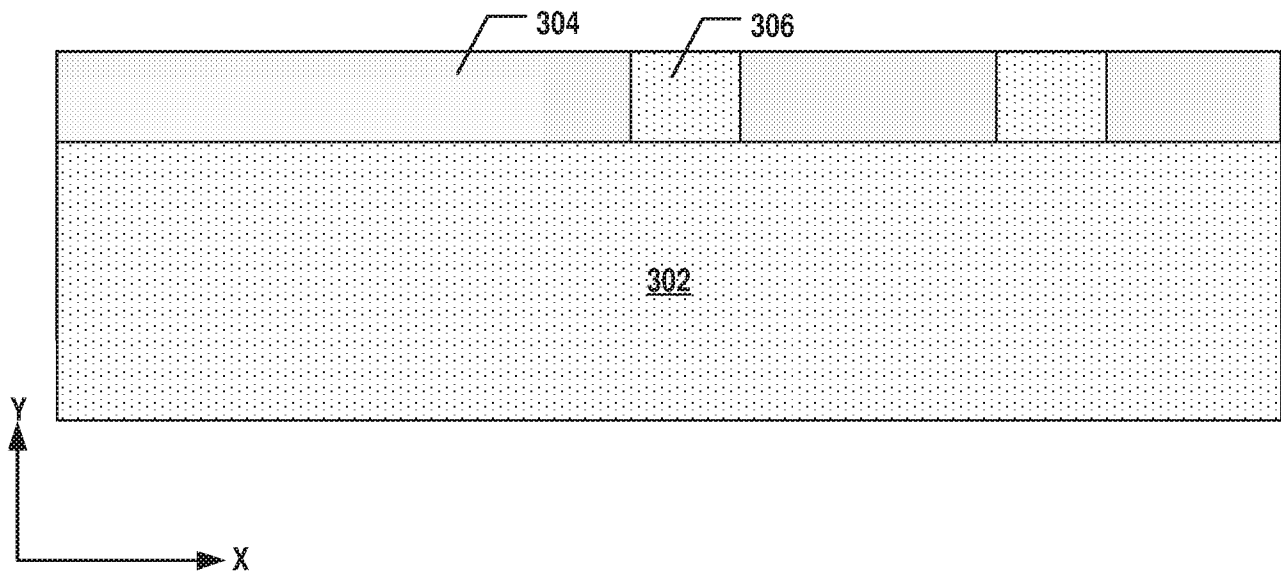


FIG. 3A

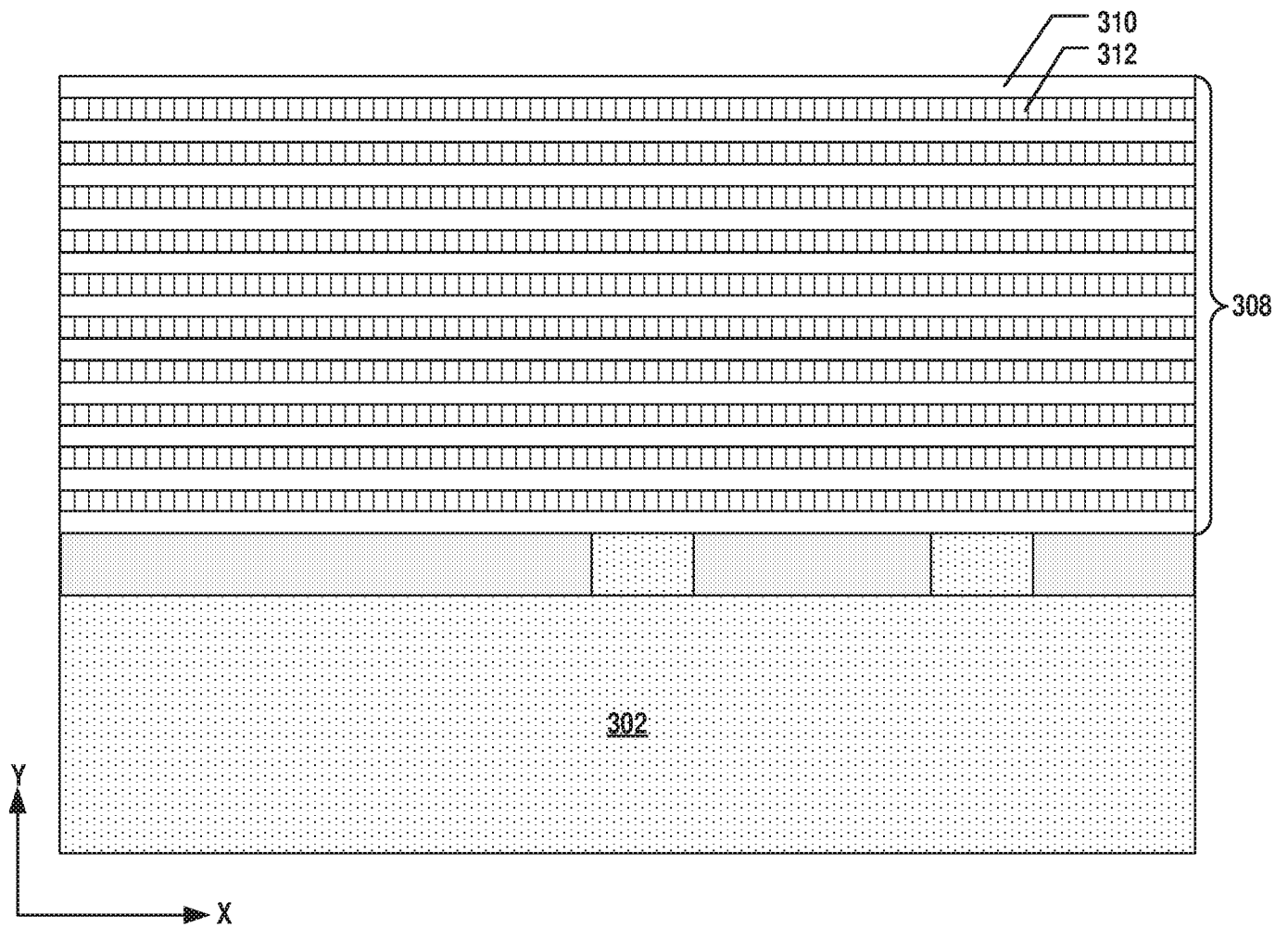


FIG. 3B

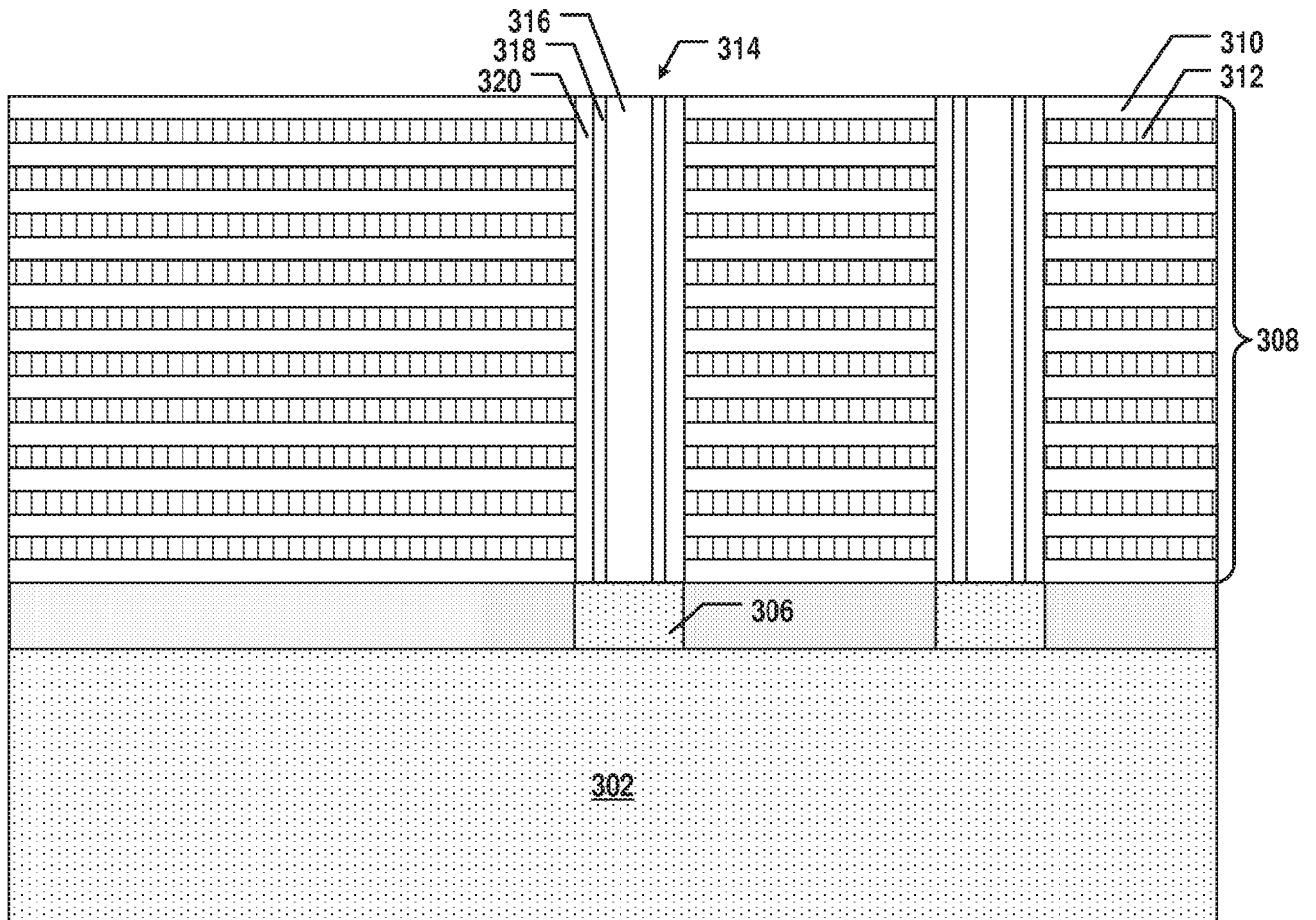


FIG. 3C

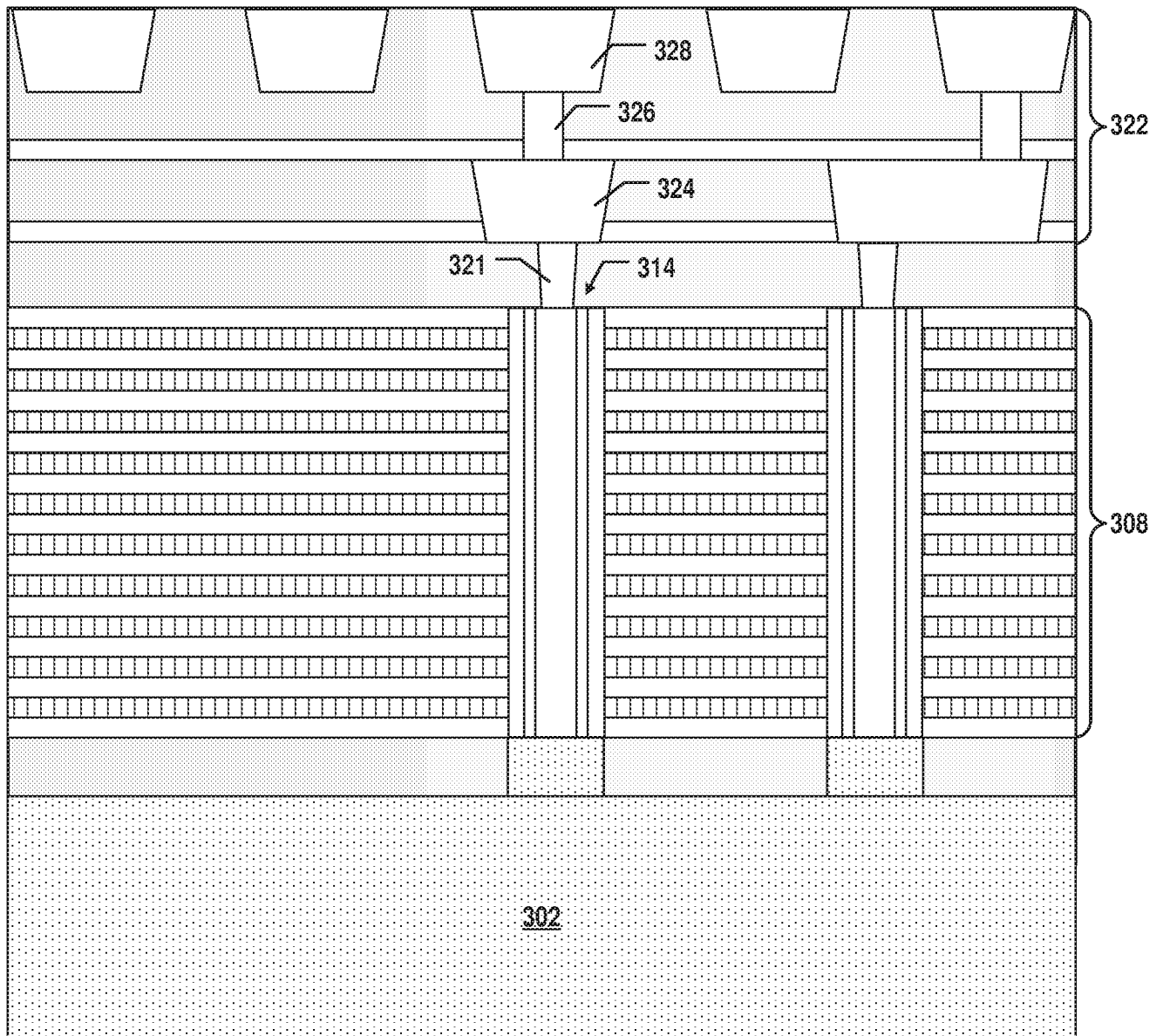


FIG. 3D

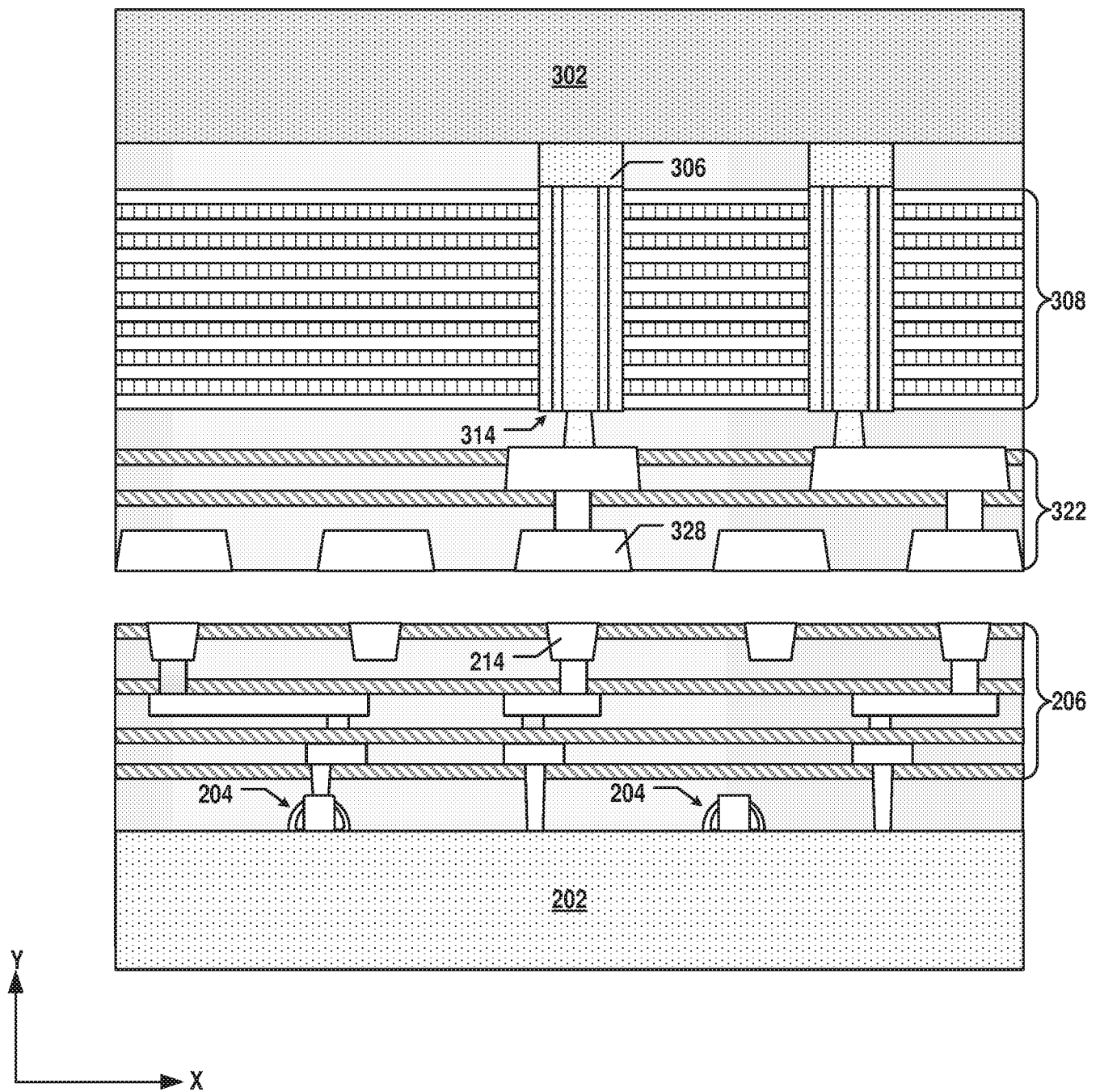


FIG. 4A

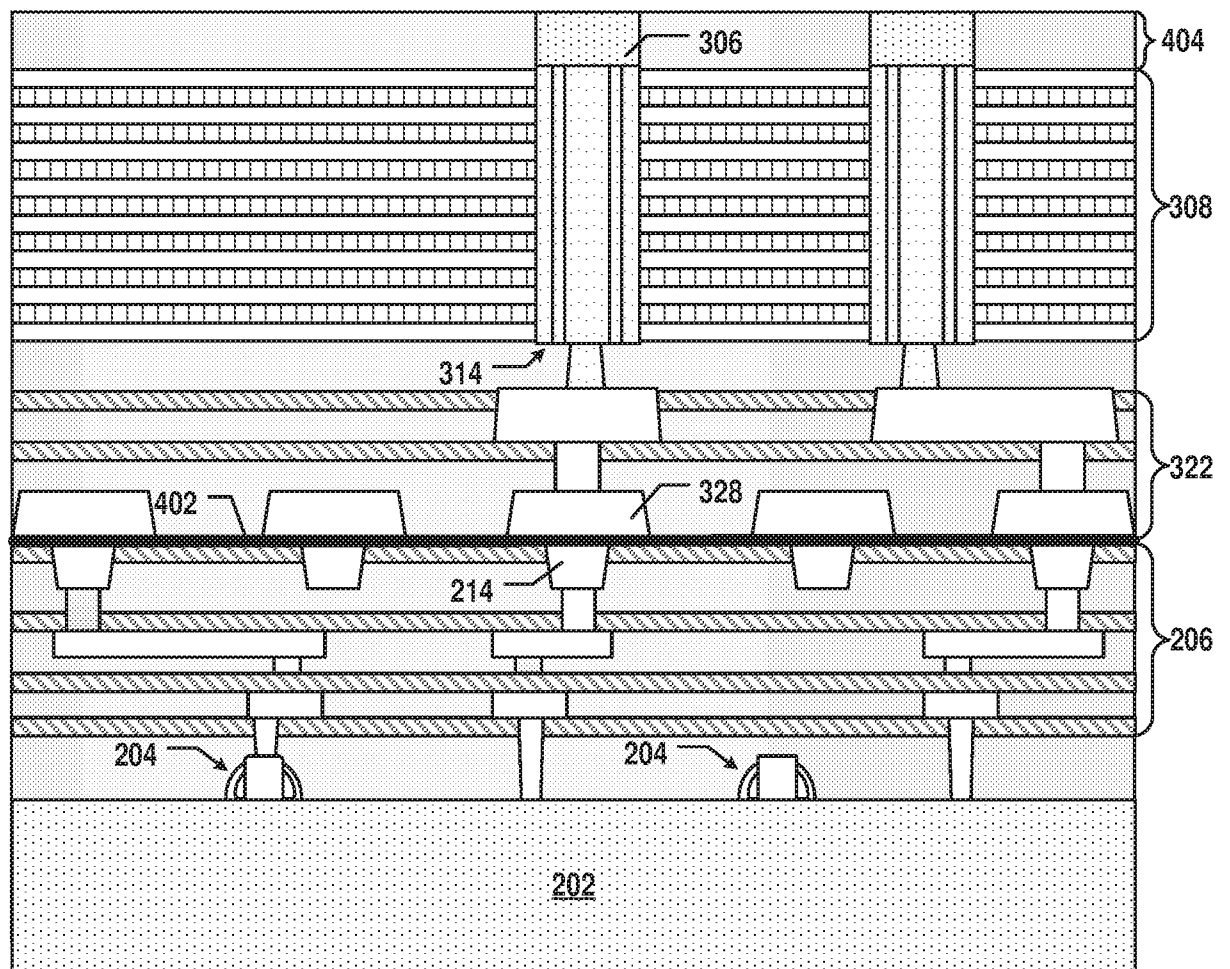


FIG. 4B

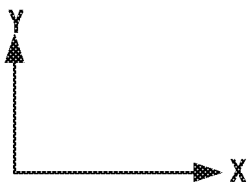
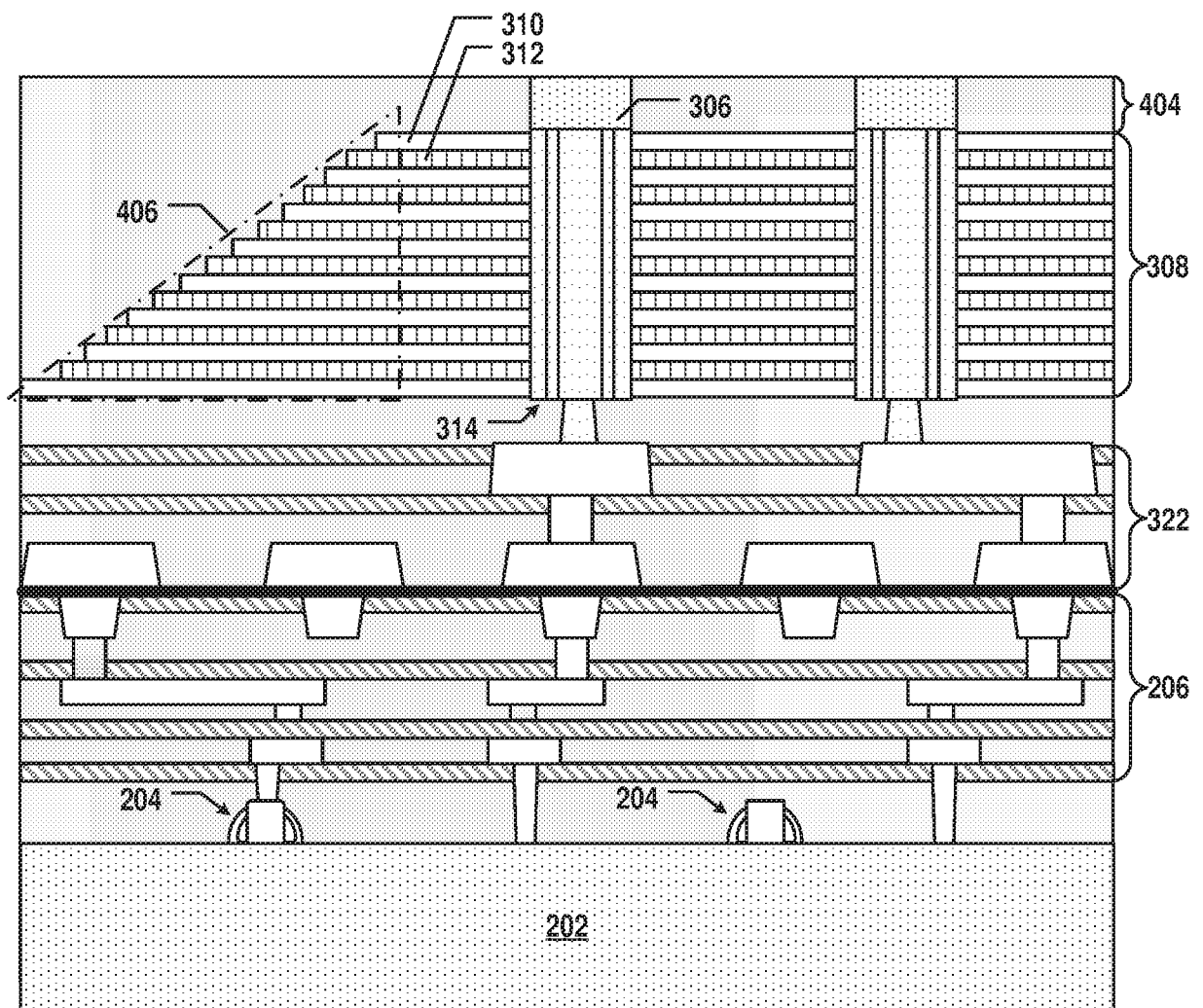


FIG. 4C

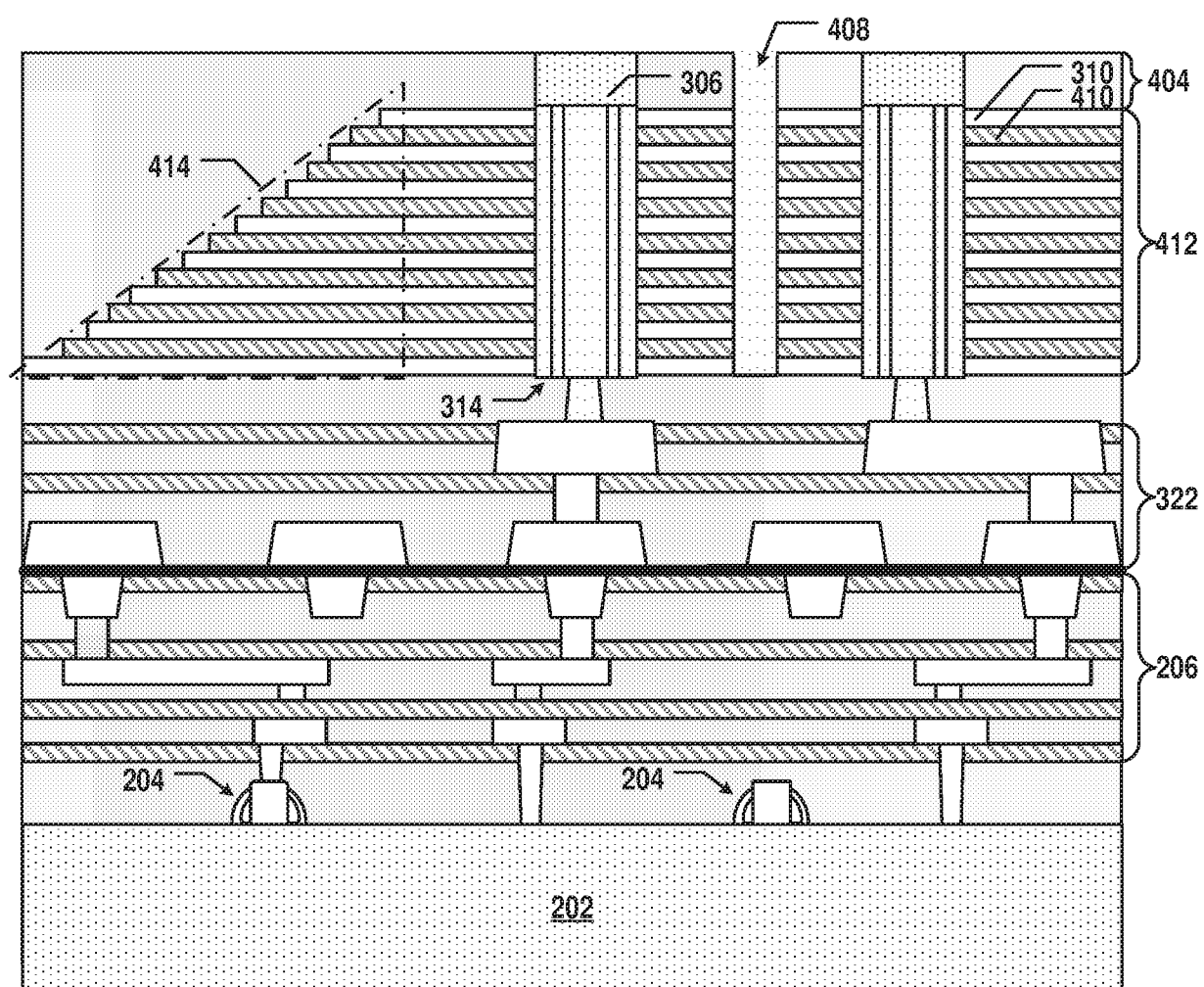


FIG. 4D

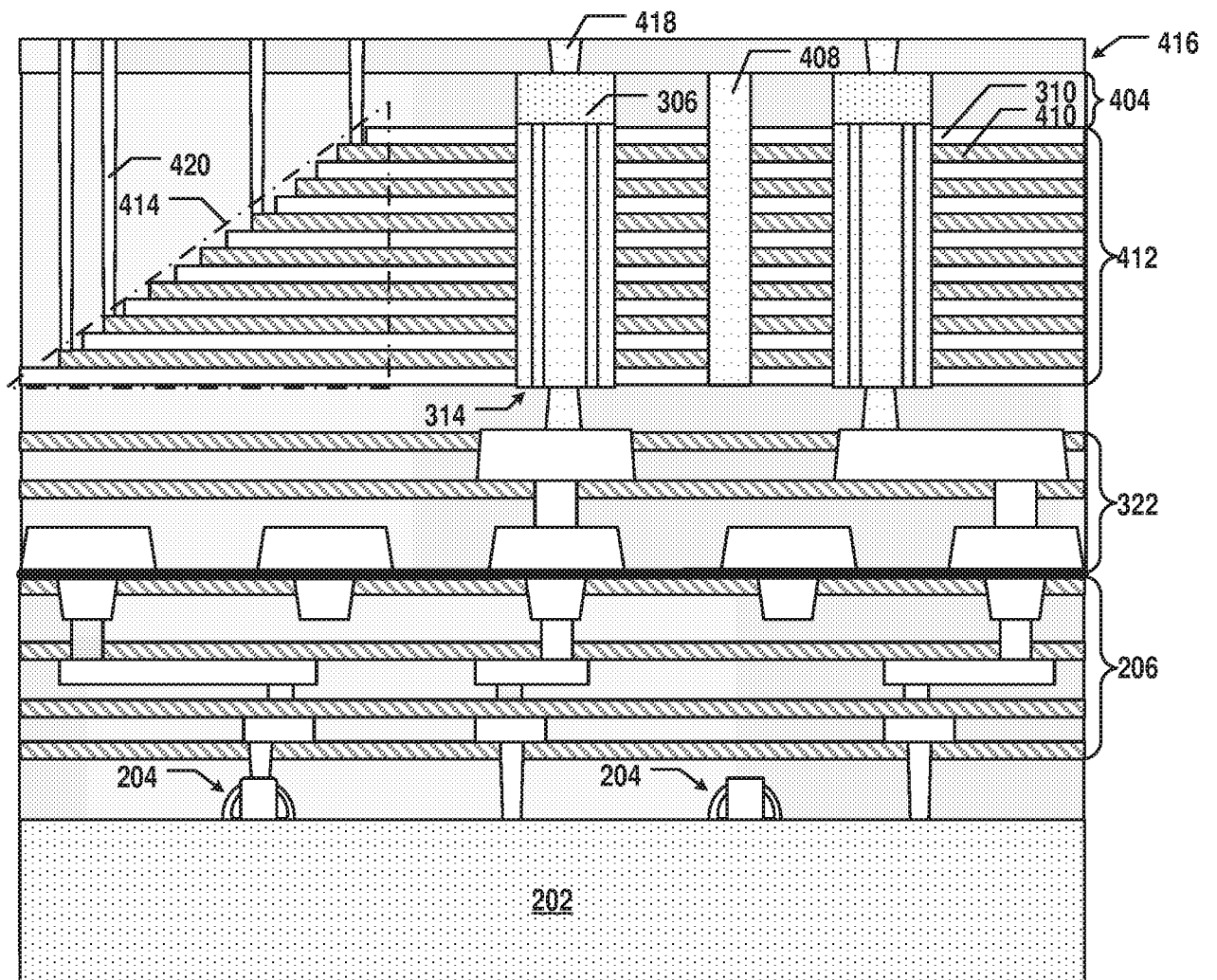


FIG. 4E

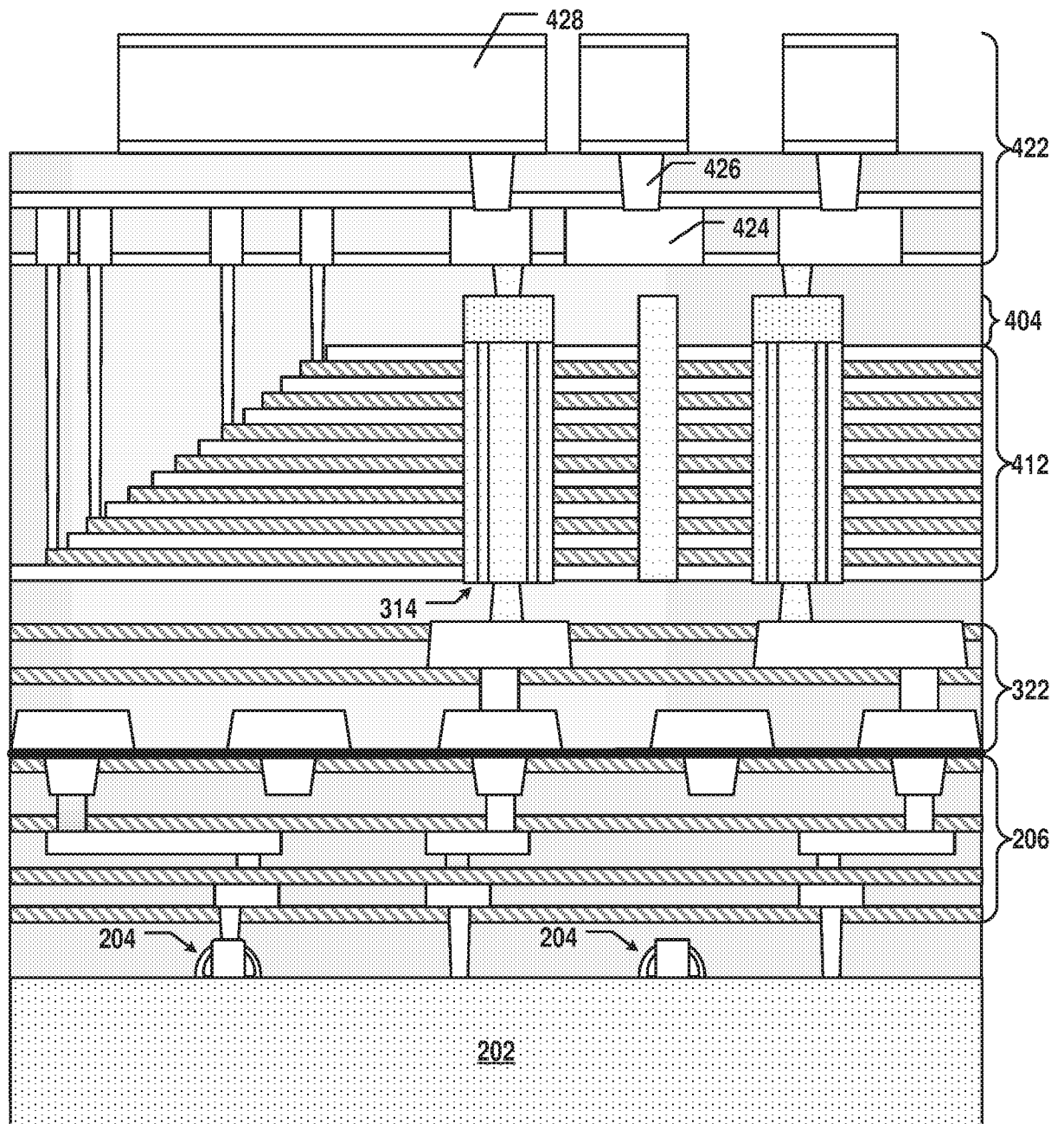


FIG. 4F

500

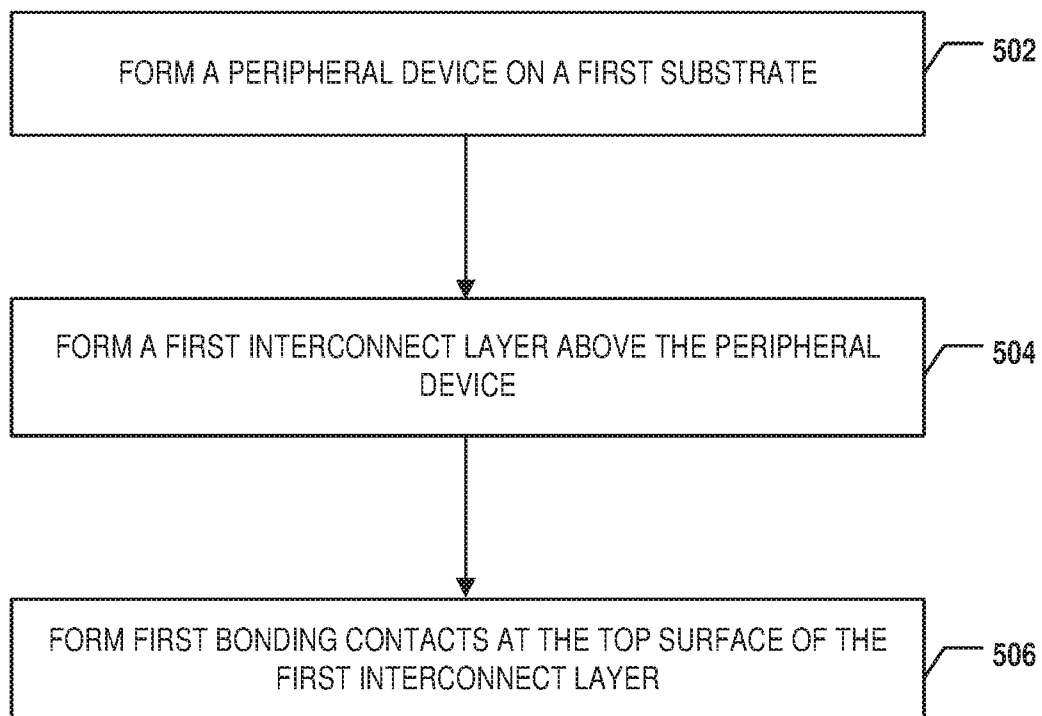


FIG. 5

600

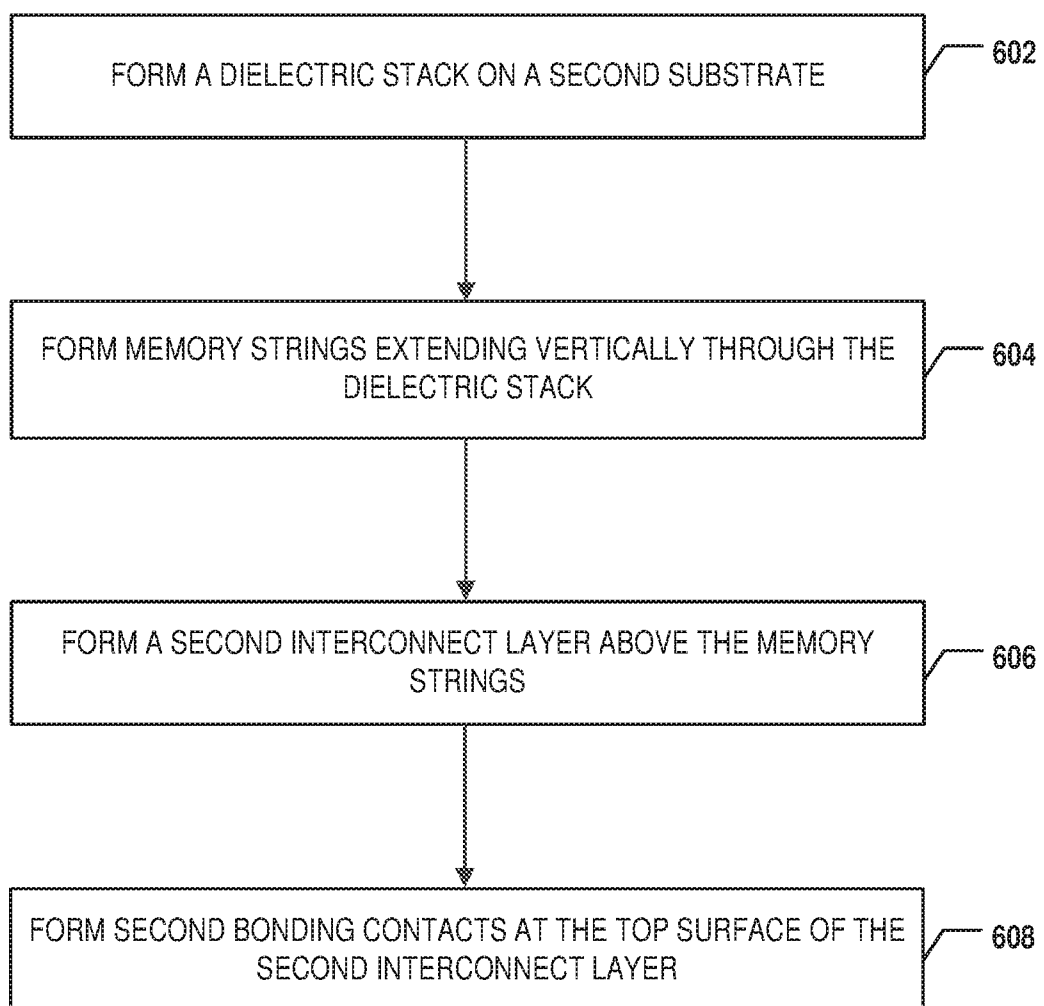


FIG. 6

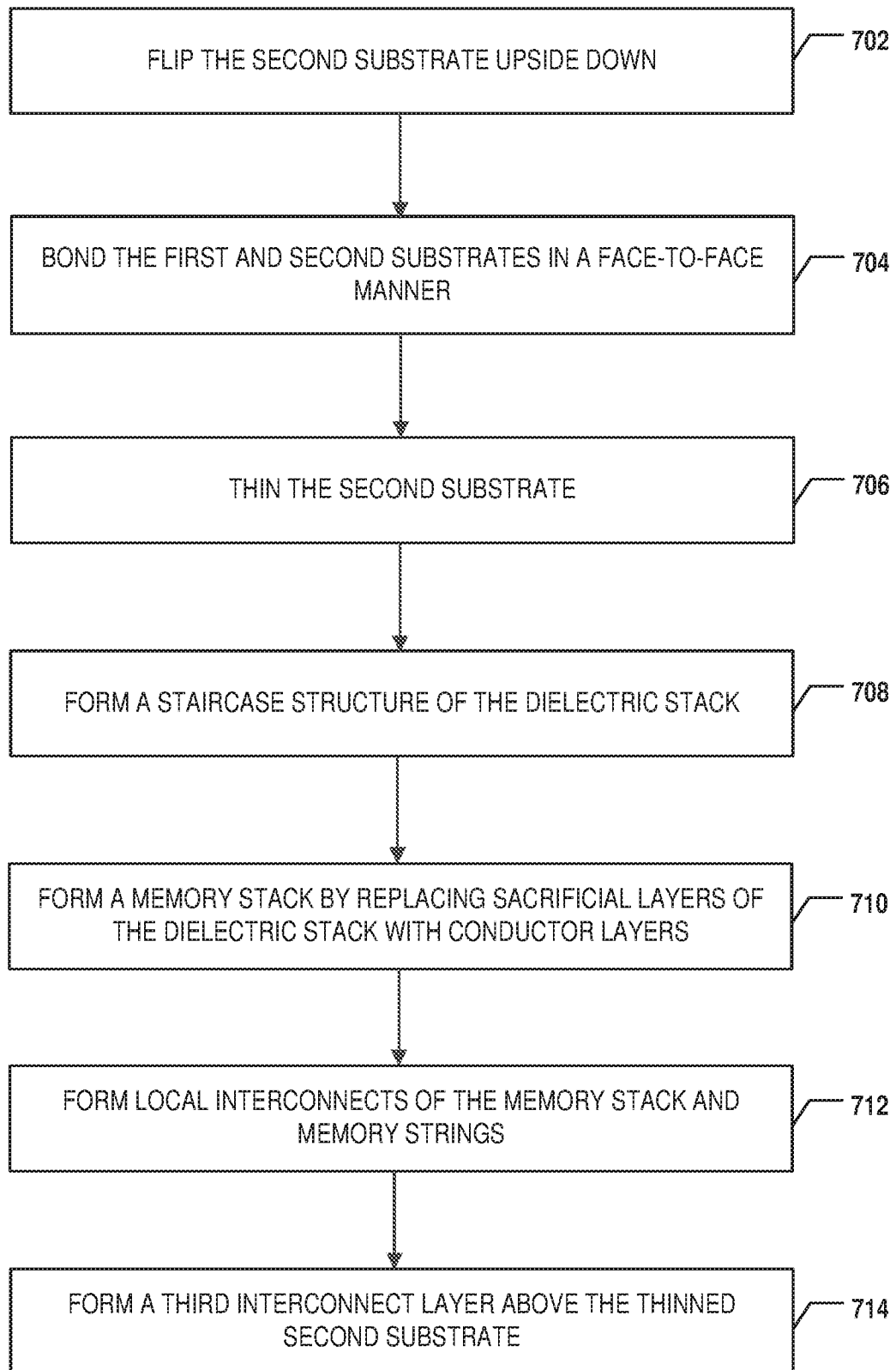
14/14
700

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/096501

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/1157(2017.01)i; H01L 27/11578(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,EPODOC,WPI,CNKI,IEEE: memory, NAND, 3D, three-dimensional, bond+, flip+, thin+, strings, stair+, step, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 107887395 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 06 April 2018 (2018-04-06) description, paragraphs [0058]-[0107], and figures 1-7	1, 4-7, 9, 20-23
Y	CN 107887395 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 06 April 2018 (2018-04-06) description, paragraphs [0058]-[0107], and figures 1-7	2-3, 8, 10-19, 24-26
Y	CN 106910746 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 30 June 2017 (2017-06-30) description, paragraphs [0105]-[0137], and figures 7-10	2-3, 8, 10-19, 24-26
X	CN 107658315 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 02 February 2018 (2018-02-02) description, paragraphs [0063]-[0099], and figures 2-8	1-19
A	US 2018144977 A1 (LAM RES. CORP.) 24 May 2018 (2018-05-24) the whole document	1-26

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

03 April 2019

Date of mailing of the international search report

24 April 2019

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961229

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/096501

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	107887395	A	06 April 2018	CN	107887395	B	14 December 2018
				US	10147732	B1	04 December 2018
CN	106910746	A	30 June 2017	WO	2018161859	A1	13 September 2018
				TW	201834221	A	16 September 2018
				CN	106910746	B	19 June 2018
				US	2019057974	A1	21 February 2019
CN	107658315	A	02 February 2018	US	20190081069	A1	14 March 2019
				WO	2019037403	A1	28 February 2019
US	2018144977	A1	24 May 2018	TW	201832351	A	01 September 2018
				US	10002787	B2	19 June 2018
				WO	2018098197	A1	31 May 2018