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(54) Title: STRESS BUFFER LAYER IN EMBEDDED PACKAGE

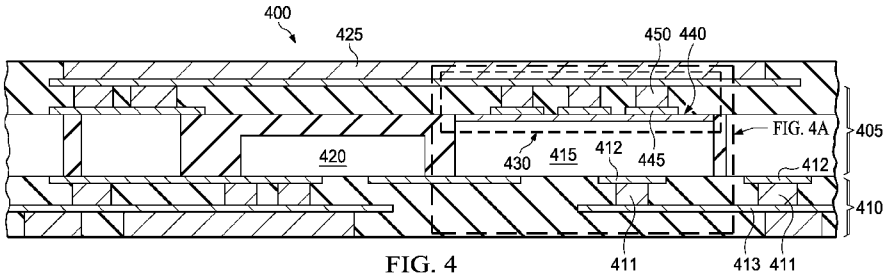


FIG. 4

(57) Abstract: The disclosed principles provide a stress buffer layer (430) between an IC die (415) and heat spreader (425) used to dissipate heat from the die (415). The stress buffer layer (430) comprises distributed pairs of conductive pads (445) and a corresponding set of conductive posts (450) formed on the conductive pads (445). In one embodiment, the stress buffer layer (430) may comprise conductive pads (445) laterally distributed over non-electrically conducting surfaces of an embedded IC die (415) to thermally conduct heat from the IC die (415). In addition, such a stress buffer layer (430) may comprise conductive posts (450) laterally distributed and formed directly on each of the conductive pads (445). Each of the conductive posts (450) thermally conduct heat from respective conductive pads (445). In addition, each conductive post (450) may have a lateral width less than a lateral width of its corresponding conductive pad (445). A heat spreader (425) is then formed over the conductive posts (450) which thermally conducts heat from the conductive posts (450) through the heat spreader (425).

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STRESS BUFFER LAYER IN EMBEDDED PACKAGE

[0001] This relates generally to embedded packages and their manufacturing techniques, and more particularly to the addition of a stress buffer layer in embedded packages and methods for manufacturing such a stress buffer layer.

BACKGROUND

[0002] Integrated circuit (IC) dies are encapsulated in protective packages to allow easy handling and assembly onto printed circuit boards (PCBs) and to protect the dies or related components and devices from damage. A dielectric material, such as a hard plastic, may be used to encapsulate the dies and related components to form the package. A variety of different IC package types exist, and several types include heat spreaders formed on one or more sides (e.g., the top side) of the package. Specifically, heat spreaders are interconnected to the encapsulated dies, and possibly other encapsulated components, to function as a heat sink and thereby assist in drawing heat out of the package.

[0003] The technique for physically (and thus thermo-conductively) connecting the heat spreader to the encapsulated die(s) and other components may help ensure proper heat dissipation. Cracks or other physical failures between the underlying dies and the heat spreader can result in insufficient heat dissipation, which may result in die overheating and in turn, die failure. This may be caused due to a mismatch in the coefficient of thermal expansion (CTE) of the silicon used to form the underlying dies (a CTE of 3ppm/K) and of copper used to form the heat spreader (a CTE of 16ppm/K). Thus, multiple techniques and structures for physically connecting the encapsulated dies with a heat spreader exist; however, even the more popular approaches can suffer catastrophic failure.

[0004] One approach is to directly contact the top (e.g., via a thermal pad) of an encapsulated die with the heat spreader. FIG. 1 is a cross-sectional view of a block diagram of a IC package 100 providing a direct connection between a die and a heat spreader. Specifically, the package 100 is comprised of a circuit layer 105 and a redistribution layer (RDL) 110. The circuit layer 105 includes the IC dies 115, as well as other components such as a drive IC 120. The RDL 110 may include a number of conductive vias 122, such as metal pillars, and interconnects 124, such

as a metal leadframe, to provide electrical connection to electrically conductive bond pads on the die 115 and other components to other underlying circuitry.

[0005] The package 100 also includes a heat spreader 125, which may be composed of copper due to its excellent thermal-conductivity. In order to dissipate the heat from the die 115 to the heat spreader 125, an interface 130 provided by the direct physical connection between the two exists. In some embodiments, a plain metal layer, which may also be copper, may be provided as the direct interface 130 of the die 115 and the heat spreader 125. However, due to the large mismatch in CTE at the direct interface 130 between the silicon of the die 115 and the copper of the heat spreader 125 (or metal layer), cracks may develop at their interface 130 when the package 100 is subjected to high temperatures. For example, embedded packages may be heated to a temperature above the solder melting temperature (e.g., during an infrared (IR) reflow process) to remove moisture the plastic encapsulant may have absorbed during the manufacturing process. During such an IR reflow process, the CTE mismatch between the heat spreader 125 and the top surface of the die 115 can result in such cracking, with this loss in structural integrity often significantly affecting the heat dissipation capabilities of the heat spreader. Such cracking may also occur in response to the high temperatures experienced in extreme operating conditions for the package 100.

[0006] FIG. 2 is an image from a scanning electron microscope (SEM) of a used package 200 employing a direct physical connection between an encapsulated die and a heat spreader. As with FIG. 1, the package 200 in FIG. 2 also includes a circuit layer 205 as well as an RDL 210. An IC die 215 can be seen encapsulated within a dielectric material in the circuit layer 205. The scan also shows a copper heat spreader 225 directly connected to the top of the die 215 for heat dissipation. Over time, a large crack 230 may be formed at the interface between the die 215 and the heat spreader 225 caused by the mismatch in thermal expansion between these two components of the package 200. FIG. 2A provides a close up view of a portion of the package 200 in FIG. 2. In this close up view, the crack 230 proximate to the interface between the die 215 and the heat spreader 225 is shown. Consequently, the ability of the heat spreader 225 of this package 200 to dissipate heat from the die 215 has been compromised.

[0007] FIG. 3 is a cross-sectional view of a block diagram of another IC package 300 providing an indirect connection between a die and a heat spreader. This package 300 again includes a circuit layer 305 and an RDL 310. The circuit layer 305 includes an IC die 315 in

need of heat dissipation using a heat spreader 325. In this approach, thermally conductive vias 335 are used to provide a physical, and thus thermal, connection between the die 315 and the heat spreader 325. To provide good thermal conductivity, the vias 335 may be formed of copper along with the heat spreader 325, again due to copper's good thermal conductivity. In addition, a thin conductive seed layer 340, usually copper as well, may also be formed on top of the die 315 to assist with thermal conductance across the top of the die 315, as well as provide contact with the bottoms of the conductive vias 335.

[0008] Unfortunately, as with the prior approach, this second approach may suffer from structural disadvantages. In particular, although the conductive vias 335 and the seed layer 340 may be formed of copper, the interfaces where the vias 335 contact the seed layer 340 may suffer from mechanical failure. Specifically, the interface between the bottoms of each conductive via 335 and the top of the die 315 may suffer structural failure, again usually in the form of cracks, not due necessarily to CTE mismatch, but instead due to high thermo-mechanical stress resulting from the relatively small diameter for each of the bottoms of the conductive vias 335 even though connected to the similar composition seed layer 340. This may occur when the package 300 undergoes through an IR reflow process. This loss in structural integrity can significantly affect the heat dissipation capabilities of the heat spreader 375.

[0009] FIG. 3A is an SEM image 350 of a used package employing conductive vias between an encapsulated die and a heat spreader. The image 350 shows this embodiment of a package also includes a circuit layer 355 and RDL 360, with a silicon IC die 365 encapsulated in the circuit layer 355. The heat spreader 375 can be seen located above and spaced from the die 365, with copper vias 385 providing physical, and thus thermal, connections between the die 365 and the heat spreader 375. In addition, a thin conductive seed layer 390 can also be seen deposited over the top of the die 365 to assist with heat dissipation, with the copper vias 385 being physically connected to the top of the seed layer 390 at interfaces 380.

[0010] However, as mentioned above, structural failure in the form of cracks still form at the interfaces 380 between the vias 385 and seed layer 390 after the package undergoes an IR reflow process or other cause of similar high temperatures. This is caused by the downwardly tapered sidewalls of the vias 385 that result from the formation process employed to form the conductive vias 385. Specifically, once dielectric material is deposited on and around the circuit layer 355 to encapsulate the die 365 and other components and interconnects in the circuit layer 355, the

encapsulation material is deposited to a predetermined height about the die 365. Then, laser drilling is used to form the vias 385 by drilling down through the encapsulation material to reach the top of the die 365 or the top of the seed layer 390. Metal deposition techniques may then be used to fill the drilled holes with copper to form the vias 385. Thereafter, copper deposition may again be used to form the heat spreader 325 on top of the encapsulation material, and in contact with the tops of the copper vias 385.

[0011] Unfortunately, the laser drilling process creates via openings that are tapered from their tops to their bottoms. As a result, the filled conductive vias 385 have a corresponding downward, cylindrical tapering. This tapering of the vias 385 results in a via structure with a narrow diameter at the interface 380 with the die 365 or seed layer 390. These tapered via 385 structures result in less overall copper surface area conducting heat from the seed layer 390 or die 365, which results is less heat dissipation. In addition, this relatively narrow interface 380 results in a high thermo-mechanical stress at the interface 380 of each via 385, for example, after the package undergoes a reflow process. Consequently, similarly to the direct conductive connection of the other approach described above, the high thermo-mechanical stress at the interfaces 380 will result in cracks being formed their interfaces 380 of the bottom of each via 385, especially in extreme operating conditions for the package 300. Also as before, such cracks result in mechanical failure for the heat dissipation intended to be provided by the conductive vias 385. Furthermore, the inwardly tapered structure of the bottom portions of the vias 385 provides less overall thermal conductive surface contacting the die 365 or a seed layer 390 over the top surface of the die 365

[0012] Accordingly, what is needed in the art is a dissipation structure for encapsulated packages, and related methods for manufacturing such dissipation structures, that do not suffer from the deficiencies of the prior art. The examples provide these and other improvements.

SUMMARY

[0013] Some examples provide for the creation of a stress buffer layer between an embedded IC die and a heat spreader used to dissipate heat from non-electrically conductive surfaces of the IC die. The stress buffer layer is comprised of a distributed set of conductive pads and a corresponding set of conductive posts formed on the conductive pads. In particular, the conductive pads may have a substantially larger width or diameter than the conductive posts. The relatively large diameter of the conductive pads provides a much larger interface between

the conductive pads and either the top of the embedded die directly, or a conductive seed layer if one is used, and thus reduces the thermo-mechanical stress at the interface at the die associated with a CTE mismatch found in some approaches described above. Also, the large diameter of the conductive pads eliminates the high thermo-mechanical stress present when narrow, tapered conductive vias are formed using the laser drilling technique described above.

[0014] Thus, in one aspect, the description is directed to a stress buffer layer for use in dissipating heat within an embedded IC package. For example, a stress buffer layer as disclosed herein may comprise a plurality of conductive pads laterally distributed over an IC die encapsulated in an IC package. Each of the plurality of conductive pads may have a proximal end contacting a non-electrically conductive surface of the IC die, and having a distal end opposite each proximal end of each conductive pad. In addition, such a stress buffer layer may further comprise a plurality of conductive posts laterally distributed and formed directly on each of the plurality of conductive pads. Each of the plurality of conductive posts may have proximal end contacting respective distal ends of each conductive pad, and a distal end opposite each proximal end of each conductive post. Also, each conductive post may have a lateral width less than a lateral width of its corresponding conductive pad. Moreover, the structure for dissipating heat from the die may further comprise a heat spreader formed over the plurality of conductive posts. The heat spreader may have a proximal surface contacting the distal ends of the plurality of conductive posts, and a distal surface exposed from the IC package.

[0015] In another aspect, the disclosure is directed to methods for manufacturing a stress buffer layer that is used in dissipating heat from an embedded IC die from within an IC package. For example, a method may comprise depositing a first mask layer over an IC die, and then removing areas of the first mask layer to create first openings exposing corresponding non-electrically conductive surfaces of the IC die. The method may then include forming a conductive pad in each of the first openings over the exposed corresponding non-electrically conductive surfaces of the IC die and to a height of the first mask layer. An exemplary method may then include depositing a second mask layer over the conductive pads and remaining portions of the first mask layer, and then removing areas of the second mask layer to create second openings, each exposing a portion of a corresponding conductive pad. A conductive post may then be formed in each of the second openings directly on the exposed portion of each corresponding conductive pad. An exemplary method may then include removing the first and

second mask layers, and depositing an encapsulating dielectric material over the IC die, conductive pads, and conductive posts to a height of the conductive posts. Then, a heat spreader maybe formed on the encapsulating dielectric material and the conductive posts, and with a distal surface of the heat spreader exposed from the encapsulating dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The invention and a preferred mode of use are described by reference to the following detailed description of illustrative embodiments and the accompanying drawings, wherein:

[0017] FIG. 1 is a cross-sectional view of a block diagram of an IC package providing a direct connection between a die and a heat spreader;

[0018] FIG. 2 is an image from a scanning electron microscope of a used package employing a direct physical connection between an encapsulated die and a heat spreader;

[0019] FIG. 2A is a close up view of a portion of the package in FIG. 2;

[0020] FIG. 3 is a cross-sectional view of a block diagram of another IC package providing an indirect connection between a die and a heat spreader;

[0021] FIG. 3A is an image from a scanning electron microscope of a used package employing conductive vias between an encapsulated die and a heat spreader;

[0022] FIG. 4 is a cross-sectional view of a block diagram of an embedded IC package having a heat dissipation structure constructed in accordance with the disclosure;

[0023] FIG. 4A is a close up cross-sectional view of the stress buffer layer described with respect to FIG. 4;

[0024] FIG. 4B is a chart providing a summary of the DOE results of the development of thermo-mechanical stress cracks at the interface with an embedded die constructed with a stress buffer layer in accordance with the disclosure;

[0025] FIGS. 5A – 5I are cross-sectional block diagrams of an exemplary process for forming a stress buffer layer for an embedded package in accordance with the disclosure;

[0026] FIG. 6 is a 3D view of an embedded package having one embodiment of a stress buffer layer in accordance with the disclosure; and

[0027] FIG. 7 is an image from a scanning electron microscope of an embedded package employing a stress buffer layer in accordance with the disclosure.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0028] The various embodiments are described with specificity. However, the description

itself does not limit the scope of this patent. The claimed subject matter may also be embodied in other ways, to include different steps or elements similar to the ones described. The components are illustrative and not restrictive. Components that would perform the same or similar functions as the components described herein are included within the scope of the invention.

[0029] As used in the specification and the appended claims, the singular forms "a," "an" and "the" include plural references unless the context clearly dictates otherwise. References to a composition containing "a" constituent is intended to include other constituents in addition to the one named. Also, in describing the preferred embodiments, terminology will be resorted to for the sake of clarity. Each term contemplates its broadest meaning as understood by those skilled in the art and includes all technical equivalents which operate in a similar manner to accomplish a similar purpose.

[0030] Terms such as "having," "has," "including," or "includes" are open-ended and are intended to have the same meaning as terms such as "comprising" or "comprises" and not preclude the presence of other structure, material, or acts. Similarly, while terms such as "can" or "may" are open-ended and reflect that structure, material, or acts are not necessary, use of other terms is not intended to reflect that structure, material, or acts are essential. To the extent that structure, material, or acts are essential, they are identified as such.

[0031] The mention of one or more method steps does not preclude the presence of additional method steps or intervening method steps between those steps expressly identified. Moreover, the term "step" does not imply any particular order among or between various steps unless and except when the order of individual steps is explicitly required.

[0032] Referring now to FIG. 4, illustrated is a cross-sectional view of a block diagram of an embedded IC package 400 having a heat dissipation structure constructed in accordance with the disclosure. The embedded IC package 400 includes a circuit layer 405 and an RDL 410, and may be embodied as Quad Flat No-leads (QFN), Small Outline No-Lead (SON) (e.g., very small outline no-lead (VSON) or very, very small outline no-lead (WSON) packages), Land Grid Array (LGA), or other advantageous package; however, package 400 may include any type of embedded package with a heat spreader or other heat dissipation structure. Within the circuit layer 405, an IC die 415 is encapsulated in a dielectric material, as is a drive IC 420. Within the RDL 410 are electrically conductive vias 411 connected to electrically conductive bond pads 412

formed on an active side of the IC die 415. An electrically conductive leadframe 413 is also shown connected to the conductive vias 411 for distributing electrical signals within the RDL 410.

[0033] Located above the circuit layer 405 is a heat spreader 425, which may be constructed of copper. Physically, and thermally, connecting the embedded die 415 to the heat spreader 425 is a stress buffer layer 430 constructed in accordance with the disclosure. In particular, the design and structure of the stress buffer layer 430 reduces thermo-mechanical stress at the connection to the IC die. The heat dissipation structure may again include an optional seed layer 440 deposited on top of the die 415, which again can improve heat dissipation from the die 415. The unique structure of the stress buffer layer 430 comprises a combination of a thermally conductive pad 445 with a conductive post 450. Specifically, a proximal end of each conductive pad 445 is in contact with non-electrically conductive surface(s) of the die 415 or seed layer 440 over the non-electrically conductive surface(s), while the distal end of each conductive pad 445 is directed away from the die 415. Such non-electrically conductive surface(s) may include any surface of the die 415 not having electrically conductive bond pads used to electrically communicate to or from circuitry within the die 415. Each conductive post 450 has its proximal end in contact with the distal end of each corresponding conductive pad 445, while the distal end of each conductive post 450 is directed away from the conductive pads 445. Then, the distal end of each conductive post 450 is in contact with the heat spreader 425, or an optional seed layer (see FIG. 4A) placed between the heat spreader 425 and each conductive post 450. The heat spreader 425 then includes a distal surface exposed from the IC package 400.

[0034] In an exemplary embodiment, both the pads 445 and posts 450 are formed of the same material to improve their bonding to one another, such as both being formed of copper due to its high thermal conductivity. However, other thermally conductive materials may also be employed. In another embodiment, the conductive pads 445 may have a substantially annular or substantially cylindrical shape, but other shapes for the conductive pads 445 may also be employed. As illustrated, he conductive pads 445 may have a substantially larger width or diameter than the conductive posts 450. Advantageously, the relatively large diameter of the conductive pads 445 provides a much larger interface between the pads 445 and either the top, non-electrically conductive surfaces of the die 415 directly, or a conductive seed layer 440 if present, which reduces the thermo-mechanical stress at the interface at the die 415 associated

with a CTE mismatch found in some approaches. However, the diameters of the conductive pads 445 are not so large as to substantially equate to the contact area of a heat spreader disposed directly on the die 415. Also, the large diameter of the conductive pads 445 eliminates the high thermo-mechanical stress present when narrow, tapered conductive vias are formed using the laser drilling technique described above.

[0035] Turning to FIG. 4A, illustrated is a close up cross-sectional view of the stress buffer layer 430 described with respect to FIG. 4. This close up view more precisely illustrates the shape and proportion of the conductive pads 445 and the conductive posts 450 creating the stress buffer layer 430. Also shown in this view is that an optional seed layer 425a may also be deposited before the heat spreader 425, if desired, with the tops of the conductive posts 450 connected to the seed layer 425a.

[0036] In either embodiment, the description provides for the creation of a stress buffer layer 430 created by a plating process for forming the conductive pads 445 and the conductive posts 450. The conductive pads 445 having a larger diameter than the conductive posts 450 makes a direct contact to the die 415 (or seed layer 440), and the larger diameter of the pads 445 results in stress distribution per unit area on a die 415 that is substantially smaller than the laser drilled vias discuss above. Additionally, the extra volume of copper (or other desirable conductive material) from larger diameter of the conductive pads 445 also improves thermal performance of a package 400 having a stress buffer layer 430 as disclosed herein.

[0037] The design parameters associated with a stress buffer layer 430 as disclosed herein may also be adjusted based on desired thermo-mechanical stress and thermal conductivity performance of the package 400. Dimension (a) is the amount of pull-back from the edge of the die 415 to the outer diameter of an outer conductive pad 445. Dimension (b) is the additional radius from the conductive posts 450 provided by the larger conductive pads 445. Dimension (c) is spacing between the conductive posts 450. Dimension (d) is the diameter of the conductive posts 450. Dimension (e) is the thickness of the heat spreader 425. Dimension (f) is the total height of the conductive pads 445 and the conductive posts 450. Based on these predetermined dimensions, the height of the conductive posts (f) can be selected so as to move the high stress point from the die to a stress buffer layer as disclosed herein. Also, the post diameter (d) combined with the additional lateral radii provided by the larger conductive pad helps to distribute stress to a wider area on the die as compared to narrower conductive vias provide by

structures.

[0038] FIG. 4B illustrates a chart providing a summary of the design of experiments (DOE) results of the development of thermo-mechanical stress cracks at the interface with an embedded die constructed with a stress buffer layer in accordance with the disclosure. More specifically, the DOE results looked at a comparison of the thickness of the heat spreader (e) and the overall height of the conductive posts 450 and conductive pads 445. The results demonstrate the trade-off between the thickness of the heat spreader 425 and the total height of the stress buffer layer 430. For example, the DOE results demonstrated that minimum height of 30 μm for stress buffer layer 430 resulted in no cracks at the die interface for a heat spreader 425 thickness up to about 60 μm. Higher thicknesses for the heat spreader 425 had the tendency to increase the likelihood for cracks to develop. Similarly, if the height of the stress buffer layer 430 is too small, e.g., 15 μm and below, die cracks also tended to develop. Notably, the results proved that the elimination of the stress buffer layer (i.e., 0 μm) with the use of a heat spreader resulted in simply a direct connection of the heat spreader to the embedded die. This is one of the techniques described above, and demonstrated the presence of die cracks that may result with that heat dissipation technique.

[0039] Turning now to FIGS. 5A – 5I, illustrated are cross-sectional block diagrams of an exemplary process for forming a stress buffer layer for an embedded package 500. FIG. 5A illustrates the circuit layer of an exemplary package at an intermediate stage of formation. Specifically, the intermediate structure includes an embedded IC die 505 encapsulated with a dielectric package material 510. On top of this intermediate structure, the process deposits a first mask layer 515. The first mask layer 515 may be a photolithographic mask deposited using photolithographic process; however, other masking technologies, either now existing or later developed, may also be employed. Although not illustrated, a seed layer may also be deposited over the top of the die 505 prior to depositing the first mask layer 515.

[0040] FIG. 5B illustrates a cross-sectional view of the intermediate package structure at a later stage of the manufacturing process of a stress buffer layer. At this stage, the first mask layer 515 is removed at multiple areas to create first openings 520 exposing non-electrically conductive surfaces of the embedded die 505. For example, photolithography processes may again be used to open select portions of the first mask layer 515. The opened areas of the first mask layer 515, which in advantageous embodiments are substantially circular in shape, provide

the locations of the conductive pads for the stress buffer layer. Moreover, the thickness of the first mask layer 515 is used to set the thickness of the conductive pads in this embodiment.

[0041] FIG. 5C illustrates a cross-sectional view of the intermediate package structure at a further stage of the manufacturing process of a stress buffer layer. At this stage of the process, the conductive pads 525 are formed directly on top of corresponding non-electrically conductive surfaces of the die 505. In embodiments where a seed layer is used over the die 505, the conductive pads 525 are formed on the seed layer. To form the conductive pads 525, a plating process may be used, such as a copper plating process. In other embodiments, the conductive pads 525 may be formed using a deposition technique used in semiconductor manufacturing, or any other advantageous process for metal deposition or formation.

[0042] FIG. 5D illustrates a cross-sectional view of the intermediate package structure at an even later stage of the manufacturing process. At this stage of the process, a second mask layer 530 is formed over the finished conductive pads 525, as well as the remaining portions of the first mask layer 515. The second mask layer 530 may again be formed using photolithographic processes, or any other advantageous process. In addition, the second mask layer 530 may be formed using the same process as the first mask layer 515, but no such limitation is required. Moreover, as the thickness of the second mask layer 530 is selected to provide the height of the conductive posts of the stress buffer layer, the second mask layer 530 may be comprised of a different material than the first mask layer 515, and thus be deposited or otherwise formed using a different process.

[0043] FIG. 5E illustrates a cross-sectional view of the intermediate package structure at a further stage of the manufacturing process of a stress buffer layer. At this stage, the second mask layer 530 is removed at multiple areas to create second openings 535 exposing portions of the previously formed conductive pads 525. As before, photolithography processes may again be used to open select portions of the second mask layer 530. The openings 535 of the second mask layer 530, which may again also be substantially circular in shape, provide the precise locations and shapes of the conductive posts 540 with respect to the conductive pads 525, and thus may be centered over the conductive pads 525.

[0044] FIG. 5F illustrates a cross-sectional view of the intermediate package structure at a further stage of the manufacturing process of a stress buffer layer. During this stage of the process, the conductive posts 540 are created within the second openings 535 in the second mask

layer 530. As with the conductive pads 525, the posts 540 may be created using a plating process, such as a copper plating process. In other embodiments, the posts 540 may be formed using a deposition technique used in semiconductor manufacturing or another advantageous process for metal deposition or formation. As illustrated, the height of the posts 540 is determined by the thickness of the second mask layer 530. Moreover, as with the conductive pads 525, the posts 540 may also be formed in a cylindrical shape; however, other shapes for the posts 540 may also be used.

[0045] FIG. 5G illustrates a cross-sectional view of the intermediate package structure at a further stage of the manufacturing process of a stress buffer layer. At this stage, after the formation of the completed stress buffer layer 545 (a combination of the conductive pads 525 and conductive posts 540), the first and second masks 515, 530 are then stripped or otherwise removed from the structure. techniques for removing the masks 515, 530 may be employed. FIG. 5H illustrates a cross-sectional view of the intermediate package structure further in the process. Specifically, this stage comprises the deposition of the encapsulating dielectric material 550 used to embed the die 505 and other components in the circuit layer of the package 500. Any technique for providing the dielectric material 550 may be employed, either now existing or later developed.

[0046] FIG. 5I illustrates a cross-sectional view of the package 500 after the manufacturing process is completed. At this stage of the process, the heat spreader 555 is formed on top of the dielectric material 550. To form the heat spreader 555, a plating process or other material deposition process may be employed. The heat spreader 555 is either placed in direct contact with the tops of the components of the stress buffer layer 545, or alternatively a conductive seed layer 560 may first be deposited over the dielectric material 550 and in contact with the tops of the stress buffer layer 545, and then the heat spreader 555 formed directly on top of the seed layer 560. Moreover, a distal surface of the heat spreader 555 is left exposed from the encapsulating dielectric material 550 so as to transfer heat out of the package 500. In exemplary embodiments, the heat spreader 555 is formed of copper; however, other metallic or conductive material may also be employed, if desired. In addition, the seed layer 560, if present, may also be formed from the same material as the heat spreader 555, or another advantageous material may be employed.

[0047] Turning now to FIG. 6, illustrated is a 3D view of an embedded package 600 having

one embodiment of a stress buffer layer in accordance with the disclosure. The package 600 again includes an RDL 605 and an encapsulated IC die 610 in a circuit layer of the package 600. Also illustrated is a stress buffer layer manufactured as herein to thermally connect the die 610 with a heat spreader 615. The stress buffer layer is formed by pairs of conductive pads 620 and corresponding conductive posts 625, which in this exemplary embodiment are substantially equally spaced above the upper non-electrically conductive surfaces of the die 610. However, other spacing arrangements or layouts for the pairs of conductive pads 620 and conductive posts 625 may also be employed.

[0048] The stress buffer layer is comprised conductive pads 620 formed directly on the top surface of the die 610, such that proximal ends of the conductive pads 620 are in contact with the die 610. As before, an optional seed layer may also be used between the pads 620 and the die 610. The conductive pads 620, in this embodiment, are formed of copper and into a substantially cylindrical shape to a predetermined diameter (d_1) and to a predetermined height (h_1). Formed on top of each conductive pad 620 is a conductive post 625, such that the proximal ends of the conductive posts 625 contact the distal ends of the conductive pads 620. The conductive posts 625 are also formed of copper and have a substantially cylindrical shape. The conductive posts 625 are formed to a predetermined diameter (d_2) and to a predetermined height (h_2). Once each pair of the conductive posts 625 are formed on corresponding conductive pads 620, the overall height (f) of the stress buffer layer is established. Additionally, the spacing (c) of the conductive posts 625 may also be predetermined for the stress buffer layer. In an exemplary embodiment, the overall height (f) of the stress buffer layer may be in the range of 30μm – 60μm, with the height (h_1) of the conductive pads 620 in the range of about 5μm – 20μm and the height (h_2) of the conductive posts 625 in the range of about 10μm – 50μm. In such embodiments, the heat spreader 615 may have a height (e) in the range of 15μm – 60μm. In a more specific embodiment, the overall height (f) of the stress buffer layer may be about 40μm, and the height (e) of the heat spreader 615 may also be about 40μm. In such embodiments, the height (h_1) of the conductive pads 620 may be about 10μm with the height (h_2) of the conductive posts 625 about 30μm. Thus, the ratio for the height (h_1) of the pads 620 as compared to the height (h_2) of the conductive posts 625 may be about 3:1; however, other height ratios for these two components may also be used.

[0049] Turning finally to FIG. 7, provided is an image from a scanning electron microscope of

a portion of an embedded package 700 employing a stress buffer layer in accordance with the disclosure. As before, the package 700 includes a circuit layer 705 and an RDL 710, with an embedded IC die 715 encapsulated in the circuit layer 705. Also within the circuit layer 705 is a stress buffer layer as herein providing a thermal connection between the top non-electrically conductive surface of the die 715 and a heat spreader 720. The heat spreader 720 also has its distal surface exposed from the package 700.

[0050] The stress buffer layer is shown as again comprising pads 725 formed on the die 715, and conductive posts 730 formed on top of the pads 725. In exemplary embodiments, both the pads 725 and posts 730 may again be formed having cylindrical shapes, but other shapes may also be formed for either or both of these components of the stress buffer layer. The image in FIG. 7 was taken after the package 700 had gone through IR reflow, in the manner described above. Notably, the interface 735 of the pads 725 and the non-electrically conductive surface of the die 715 does not have any cracks visible in the SEM image. Consequently, the thermal conductivity of the stress buffer layer can sufficiently dissipate heat from the die 715 due to its maintained structural integrity despite the package 700 having gone through the IR reflow process.

[0051] While this invention has been particularly shown and described with reference to preferred embodiments, various changes in form and detail may be made therein without departing from the spirit and scope of the invention. Accordingly, this invention includes all modifications and equivalents of the subject matter recited in the claims appended hereto. Moreover, any combination of the above-described elements in all possible variations thereof is encompassed by the invention unless otherwise indicated herein or otherwise clearly contradicted by context.

[0052] The various embodiments have been presented by way of example only, and not limitation. Thus, the breadth and scope of this disclosure is not limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the claims and their equivalents. Furthermore, the above advantages and features are provided in described embodiments, but do not limit the application of such issued claims to processes and structures accomplishing any or all of the above advantages.

CLAIMS

What is claimed is:

1. A integrated circuit (IC) package, comprising:

a plurality of conductive pads laterally distributed over an IC die within the IC package, each of the plurality of conductive pads contacting a non-electrically conducting surface of the IC die;

a plurality of conductive posts laterally distributed directly on each of the plurality of conductive pads, wherein each of the plurality of conductive posts has a lateral width less than a lateral width of its corresponding conductive pad of the plurality of conductive pads; and

a heat spreader attached to the plurality of conductive posts, the heat spreader including a surface exposed from the IC package.

2. An IC package according to claim 1, wherein each of the plurality of conductive pads and each of the plurality of conductive posts comprise copper.

3. An IC package according to claim 1, wherein each of the plurality of conductive pads and each of the plurality of conductive posts comprise a substantially cylindrical shape.

4. An IC package according to claim 1, wherein each pair of the plurality of conductive pads and corresponding plurality of conductive posts are substantially equally spaced.

5. An IC package according to claim 1, wherein an overall height of each pair of the plurality of conductive pads and corresponding plurality of conductive posts is in the range of 30μm – 60μm when a height of the heat spreader is in the range of 15μm – 60μm.

6. An IC package according to claim 1, wherein an overall height of each pair of the plurality of conductive pads and corresponding plurality of conductive posts is about 40μm when a height of the heat spreader is about 40μm.

7. An IC package according to claim 1, wherein a ratio for a height of each of the plurality of conductive posts to a height of each corresponding conductive pads is about 3:1.

8. An IC package according to claim 1, further comprising a seed layer formed between the non-electrically conducting surfaces of the IC die and each of the plurality of conductive pads.

9. A method for manufacturing a heat dissipation structure for use in dissipating heat within an integrated circuit (IC) package, the method comprising:

depositing a first mask layer over an IC die within the IC package;

removing areas of the first mask layer to create first openings exposing corresponding

non-electrically conducting surfaces of the IC die;

forming a conductive pad in each of the first openings over the exposed corresponding non-electrically conducting surfaces of the IC die and to a height of the first mask layer;

depositing a second mask layer over each formed conductive pad and remaining portions of the first mask layer;

removing areas of the second mask layer to create second openings, each exposing only a part of a corresponding formed conductive pad;

forming a conductive post in each of the second openings directly on the exposed part of each corresponding conductive pad;

removing the first and second mask layers;

depositing an encapsulating dielectric material over the IC die, conductive pads, and conductive posts to a height of the conductive posts; and

forming a heat spreader on the encapsulating dielectric material and the conductive posts, and with a distal surface of the heat spreader exposed from the encapsulating dielectric material.

10. A method according to claim 9, wherein depositing a first mask layer and removing areas of the first mask layer, and depositing a second mask layer and removing areas of the second mask layer, comprise a photolithographic process.

11. A method according to claim 9, wherein forming a conductive pad in each of the first openings and forming a conductive post in each of the second openings comprises a plating process.

12. A method according to claim 9, wherein the conductive pads and conductive posts comprise copper.

13. A method according to claim 9, further comprising forming a seed layer on the non-electrically conductive surface of the IC die prior to depositing the first mask layer.

14. A method according to claim 9, further comprising forming a seed layer on the encapsulating dielectric material and the conductive posts prior to forming the heat spreader.

15. An integrated circuit (IC) package, comprising:

an IC die having electrically conducting bond pads and non-electrically conducting surfaces distributed on an exterior of the IC die;

electrically conductive vias connected to one or more of the electrically conducting bond pads;

a stress buffer layer, comprising:

a plurality of conductive pads laterally distributed over an IC die encapsulated in an IC package, each of the plurality of conductive pads having a proximal end contacting one of the non-electrically conducting surfaces of the IC die, and having a distal end opposite each proximal end of each the plurality of conductive pads; and

a plurality of conductive posts laterally distributed directly on each of the plurality of conductive pads, each of the plurality of conductive posts having a proximal end contacting respective distal ends of each conductive pad of the plurality of conductive pads, and having a distal end opposite each proximal end of each of the plurality of conductive posts, wherein each conductive post has a lateral width less than a lateral width of its corresponding conductive pad; and

a heat spreader having a proximal surface contacting the distal ends of the plurality of conductive posts, and having a distal surface exposed from the IC package.

16. An IC package according to claim 15, wherein each of the plurality of conductive pads and each of the plurality of conductive posts comprise copper.

17. An IC package according to claim 15, wherein an overall height of each pair of the plurality of conductive pads and corresponding plurality of conductive posts is in the range of 30μm – 60μm when a height of the heat spreader is in the range of 15μm – 60μm.

18. An IC package according to claim 15, wherein an overall height of each pair of the plurality of conductive pads and corresponding plurality of conductive posts is about 40μm when a height of the heat spreader is about 40μm.

19. An IC package according to claim 15, wherein a ratio for a height of each of the plurality of conductive posts to a height of each corresponding conductive pads is about 3:1.

20. An IC package according to claim 15, further comprising a seed layer formed between the non-electrically conducting surfaces of the IC die and each of the plurality of conductive pads.

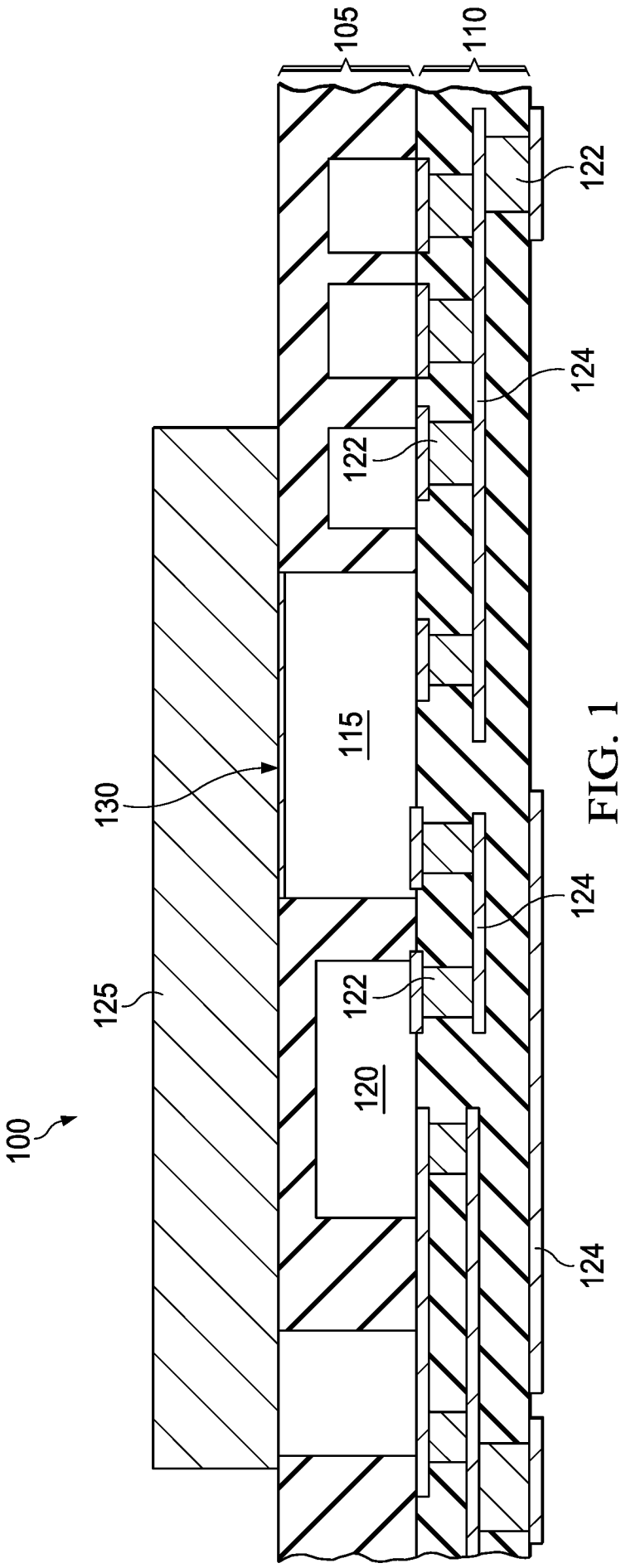


FIG. 1
(PRIOR ART)

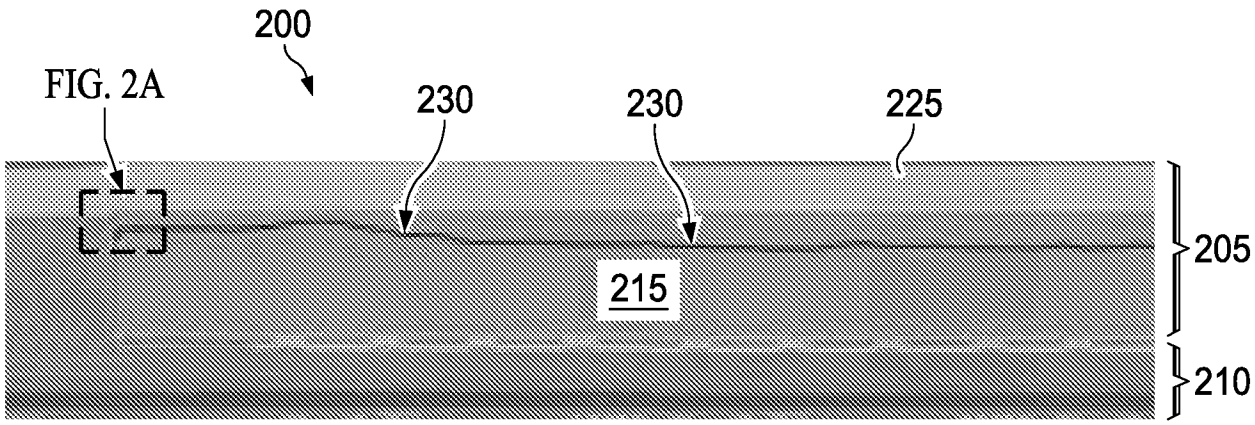


FIG. 2
(PRIOR ART)

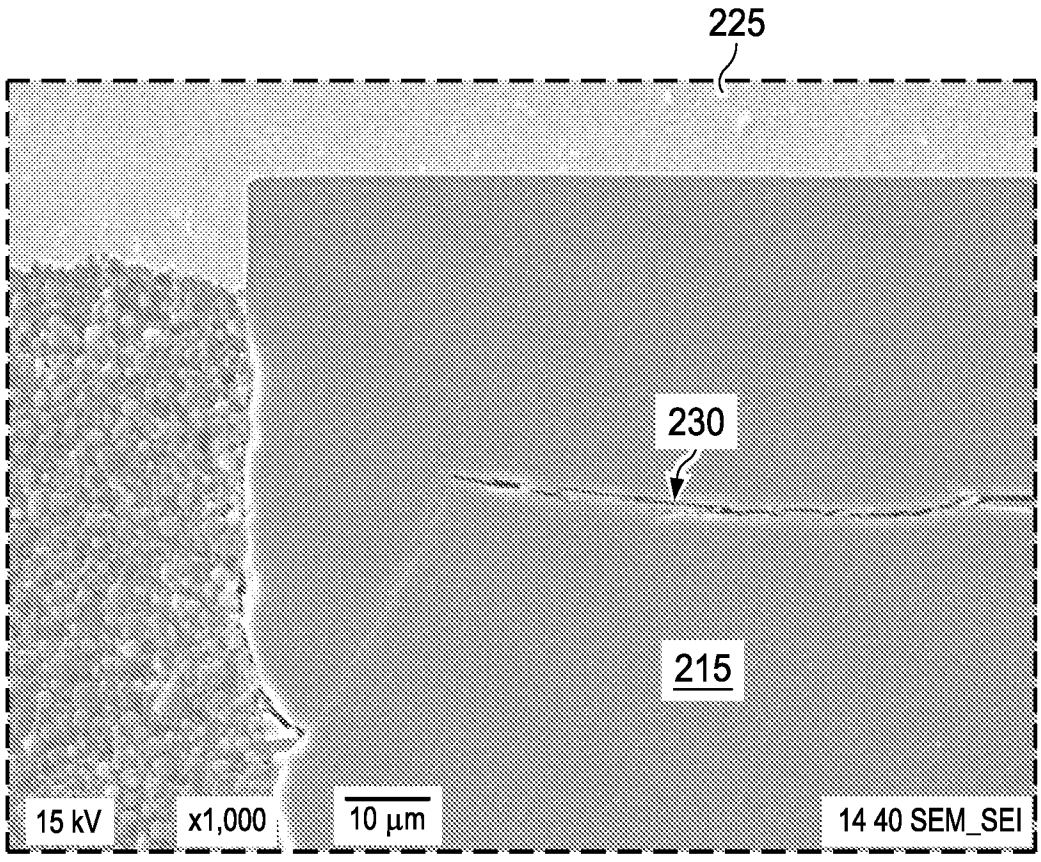


FIG. 2A
(PRIOR ART)

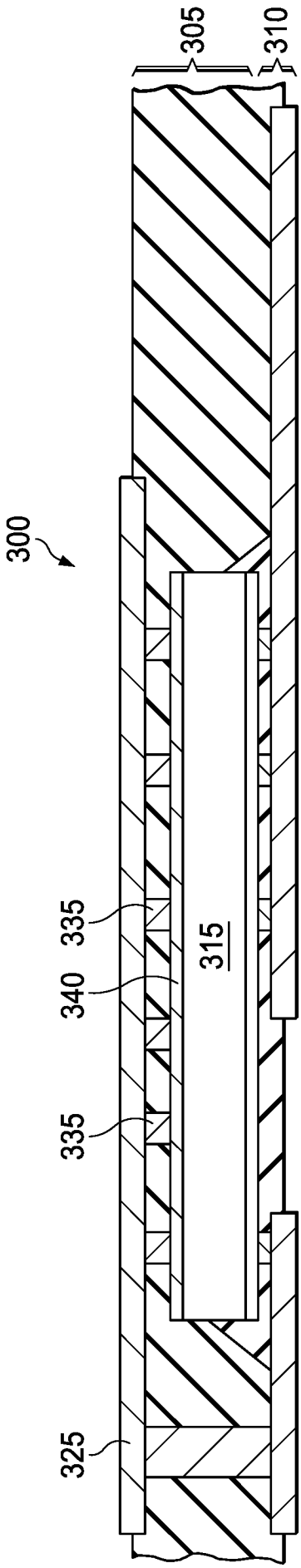


FIG. 3
(PRIOR ART)

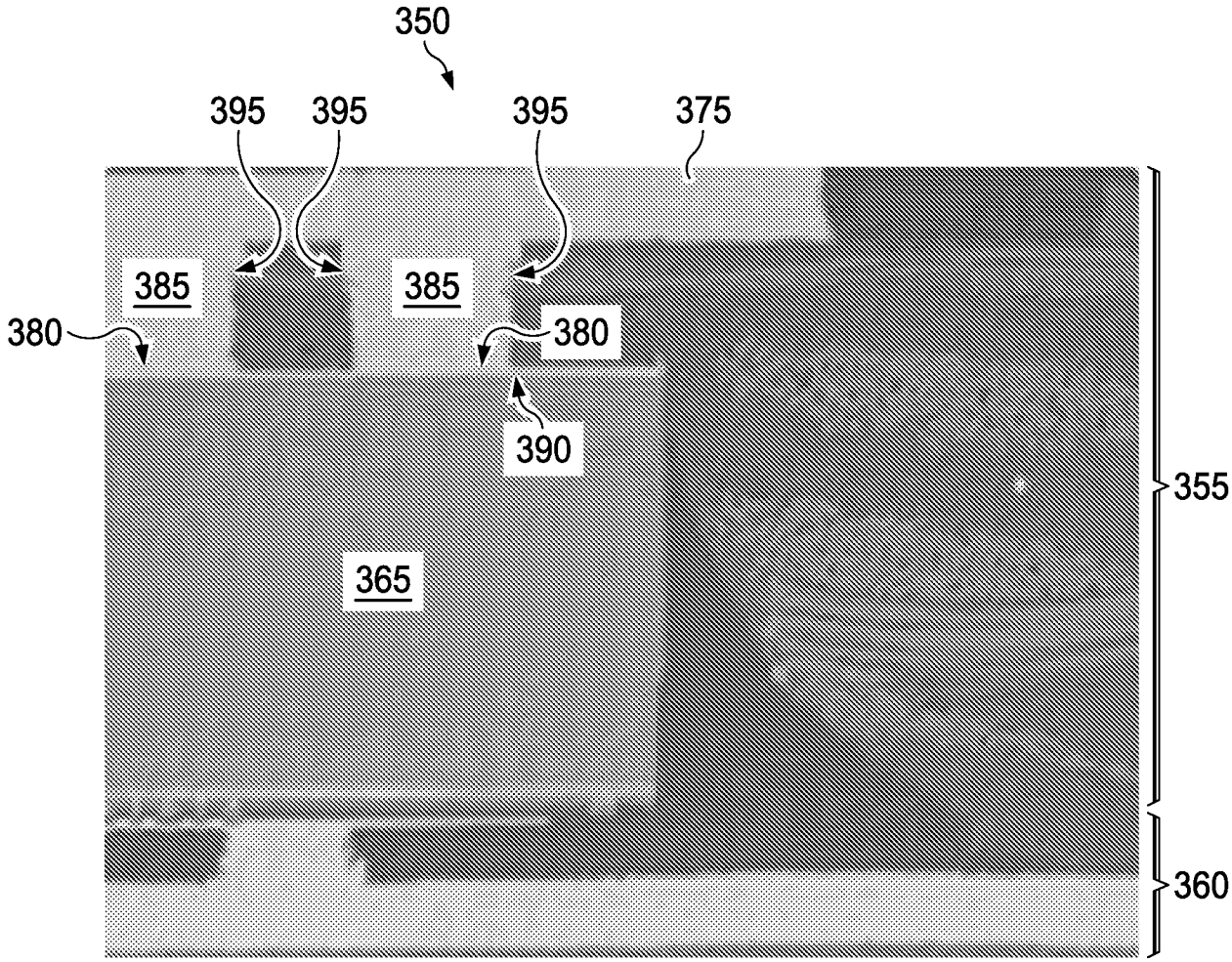


FIG. 3A
(PRIOR ART)

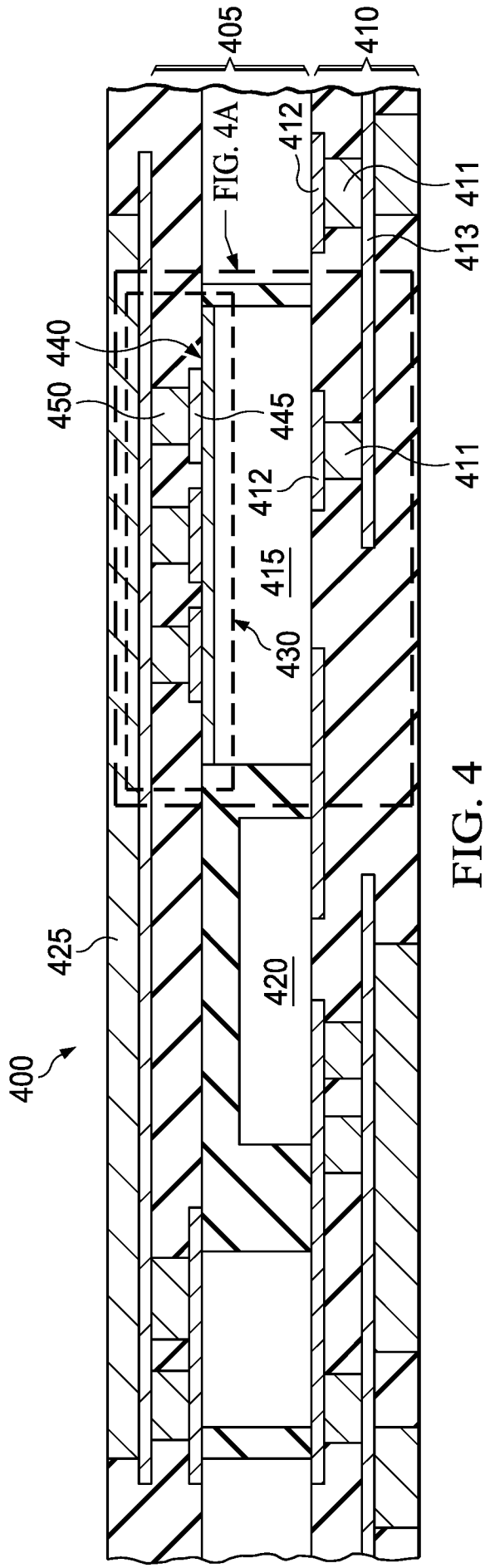

405
410
FIG. 4A
412
411
413
440
450
445
412
411
415
430
425
420
400

FIG. 4

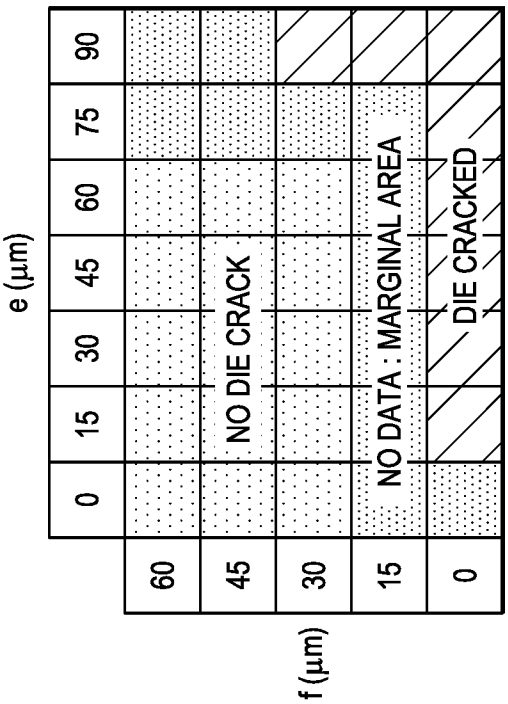

e (µm)
0
15
30
45
60
75
90
NO DIE CRACK
NO DATA : MARGINAL AREA
DIE CRACKED
60
45
30
15
0
f (µm)

FIG. 4B

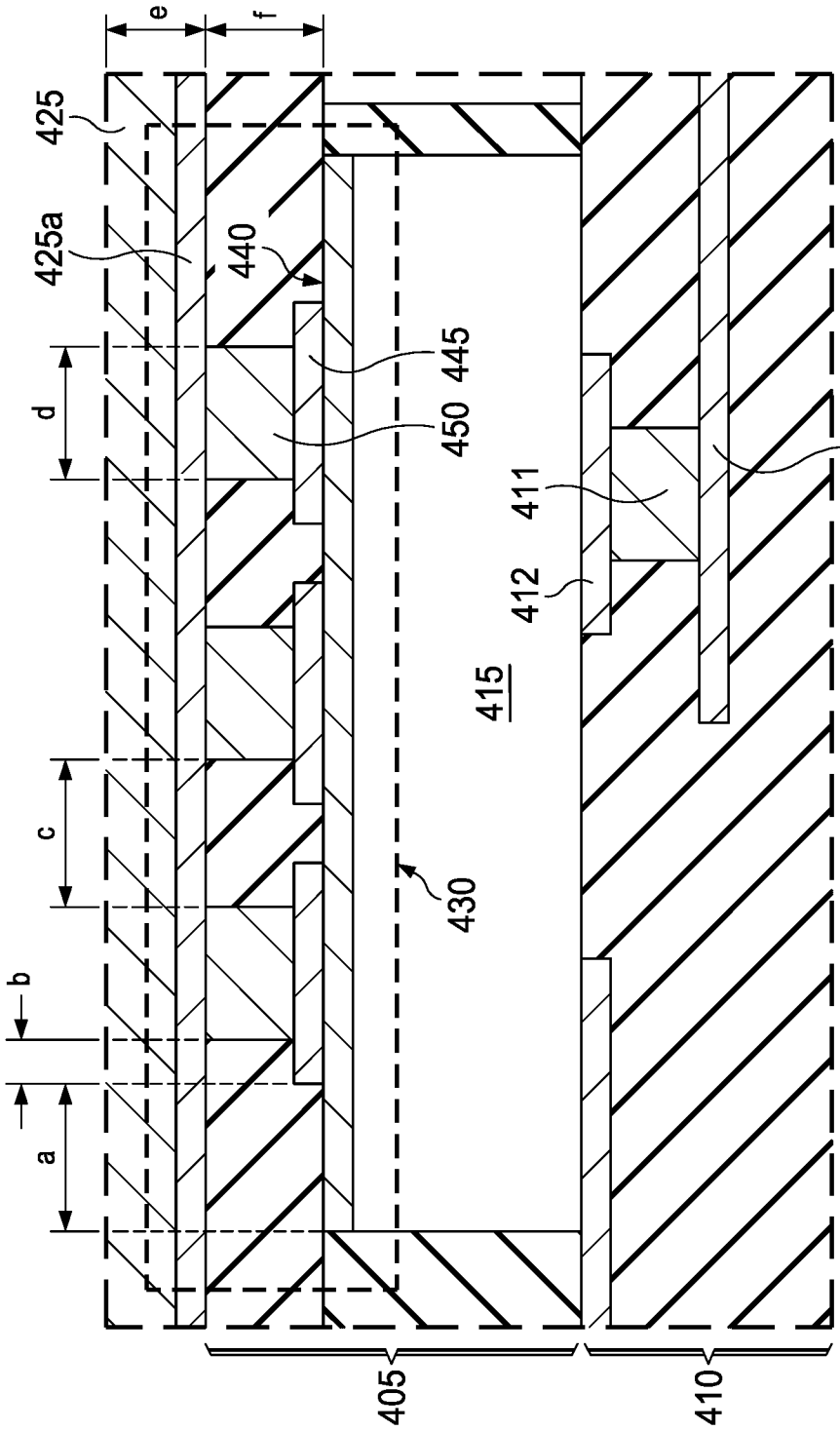


FIG. 4A

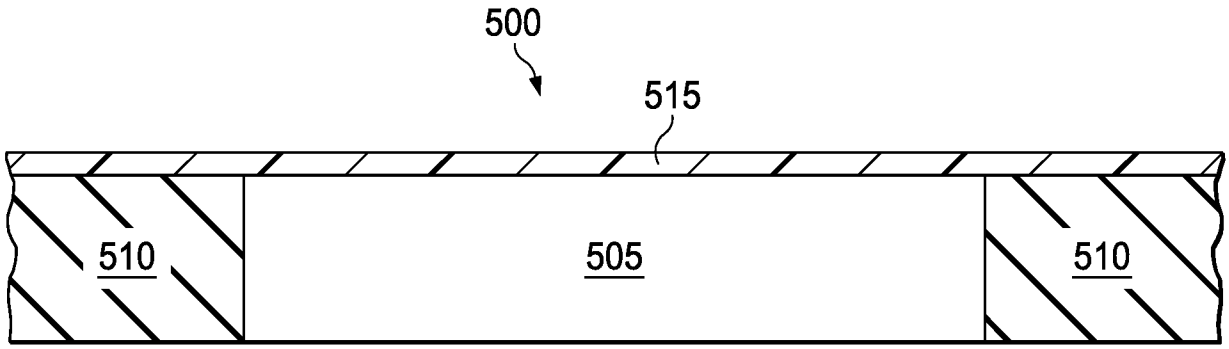


FIG. 5A

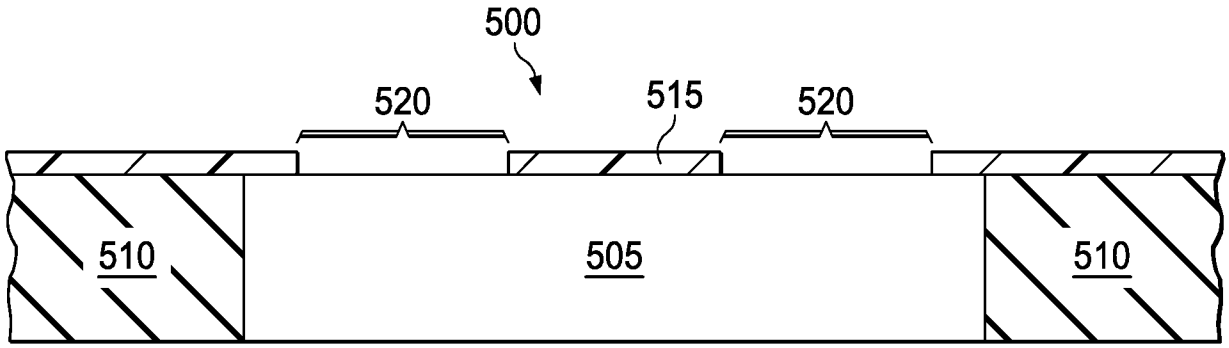


FIG. 5B

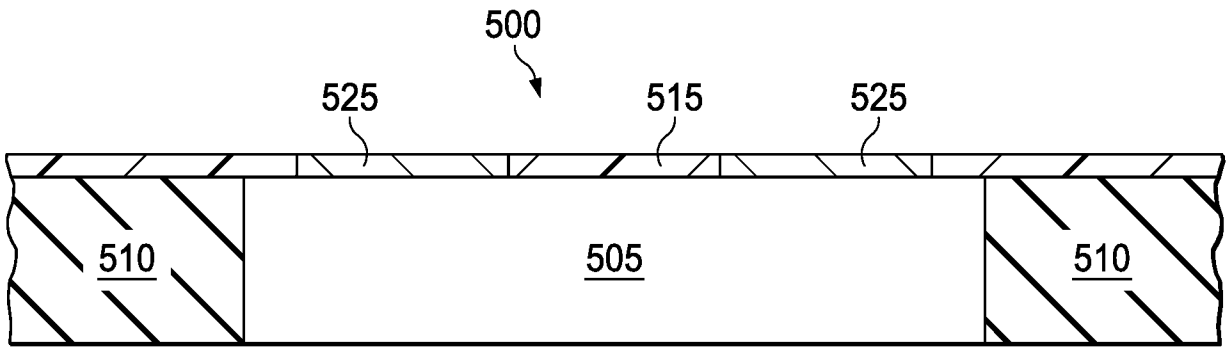


FIG. 5C

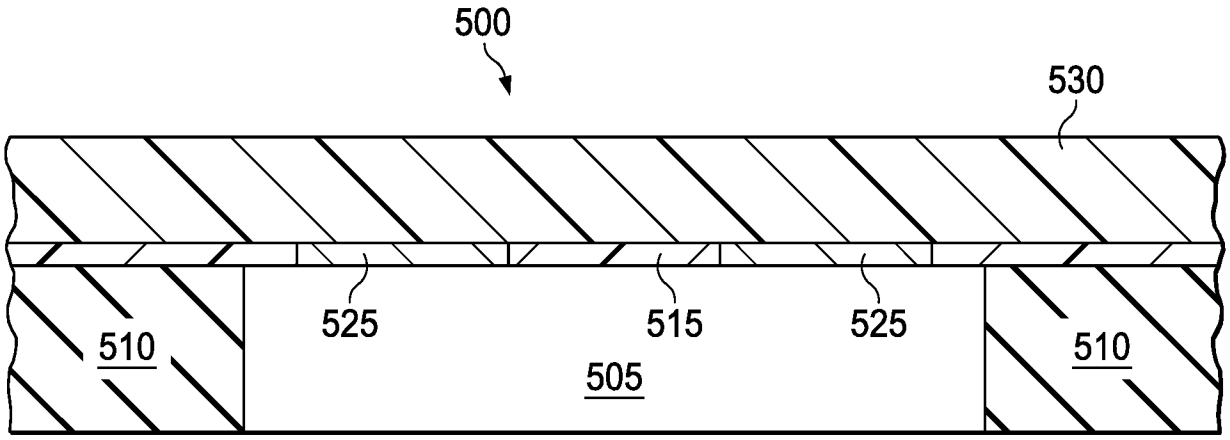


FIG. 5D

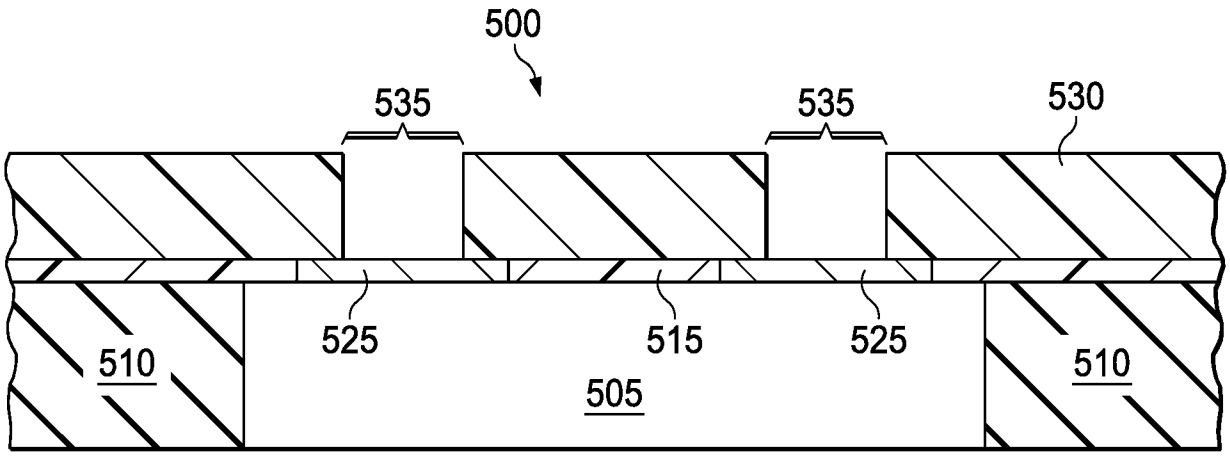


FIG. 5E

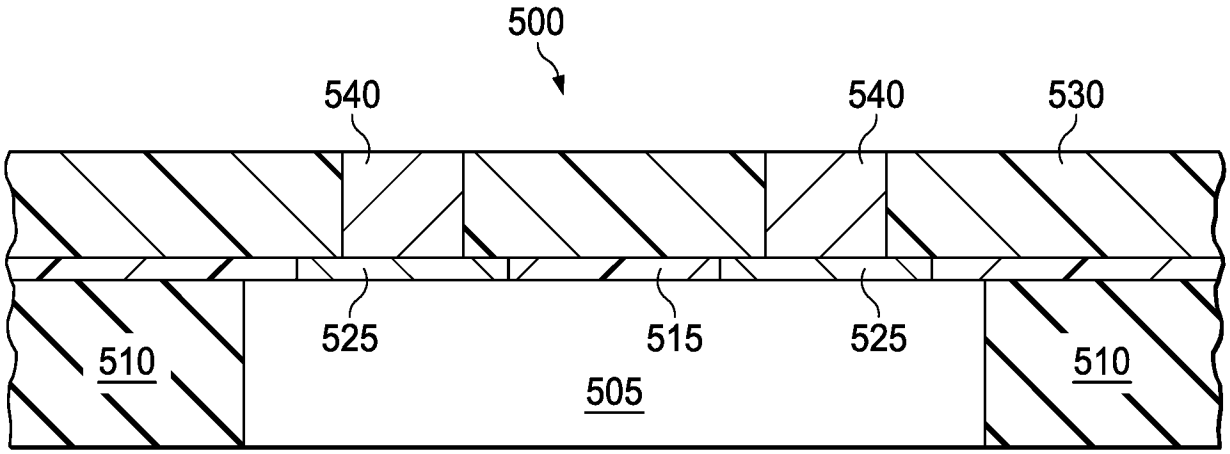


FIG. 5F

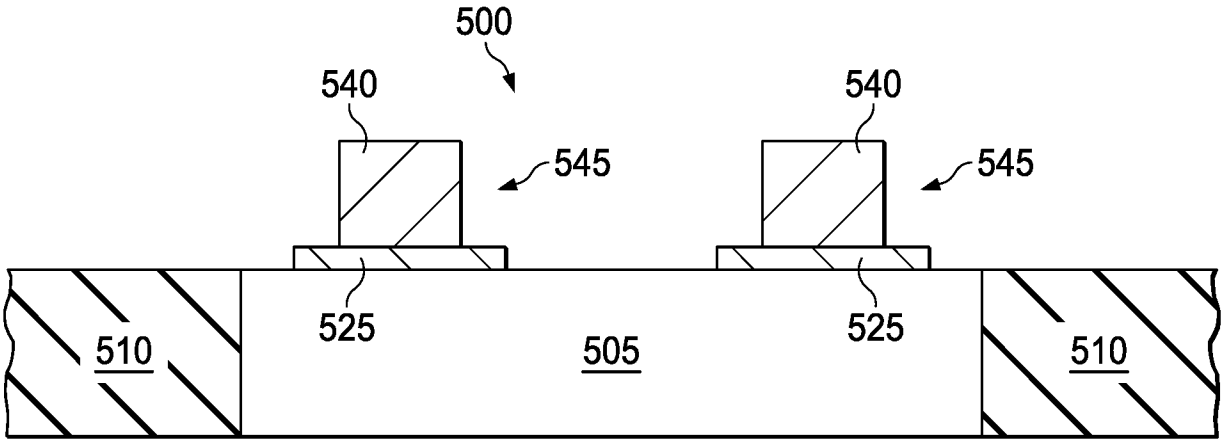


FIG. 5G

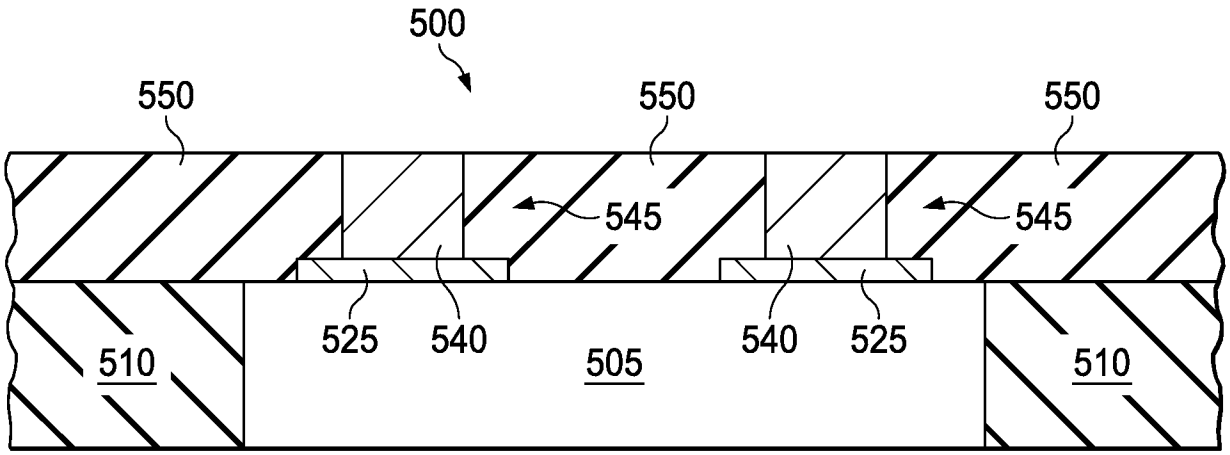


FIG. 5H

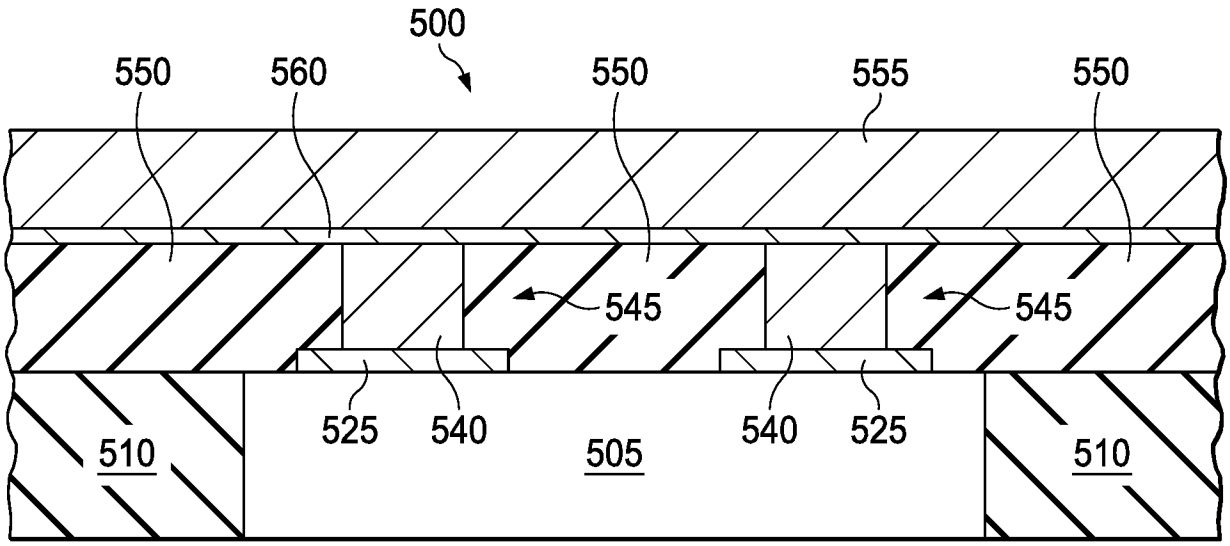


FIG. 5I

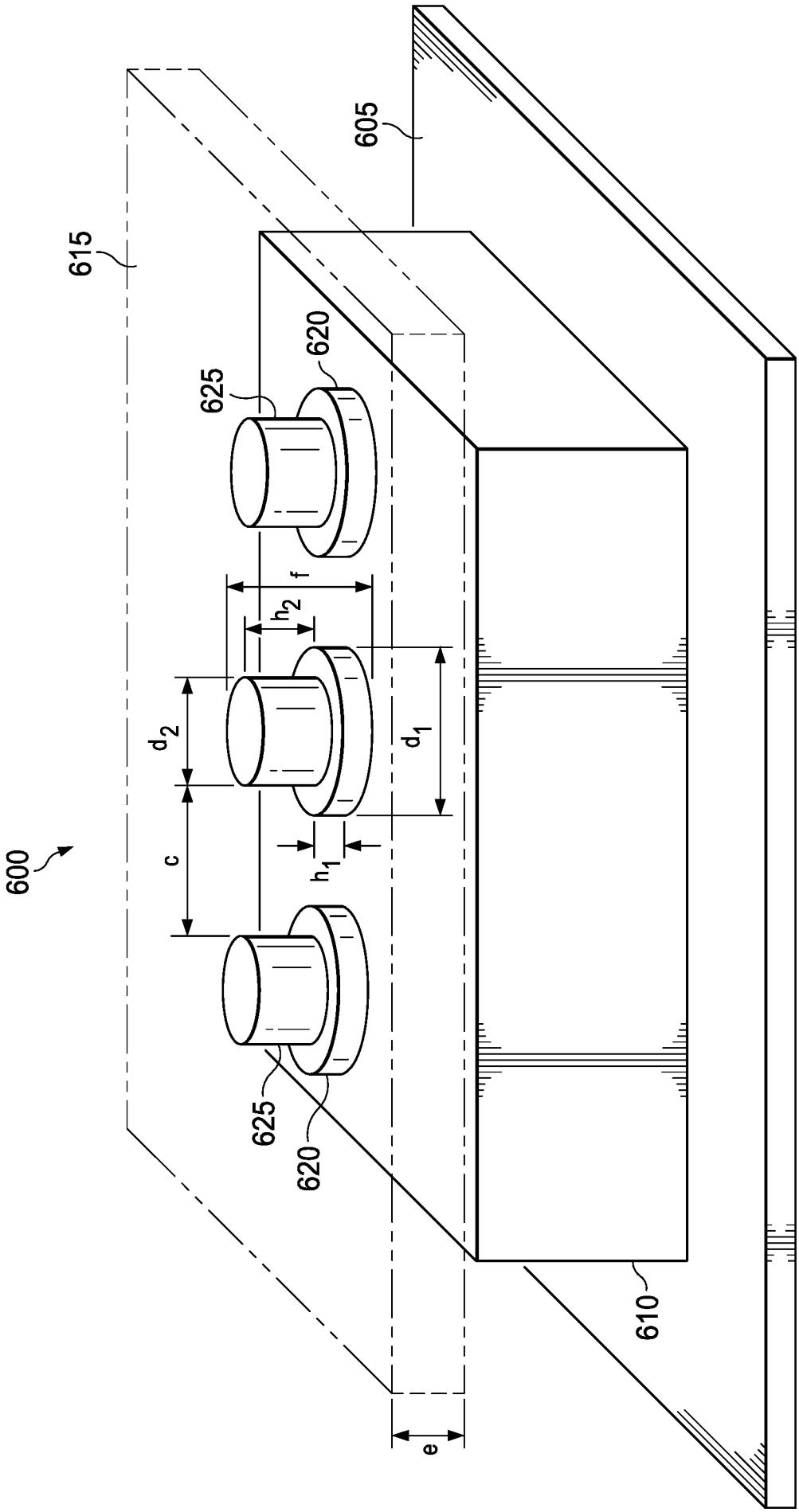


FIG. 6

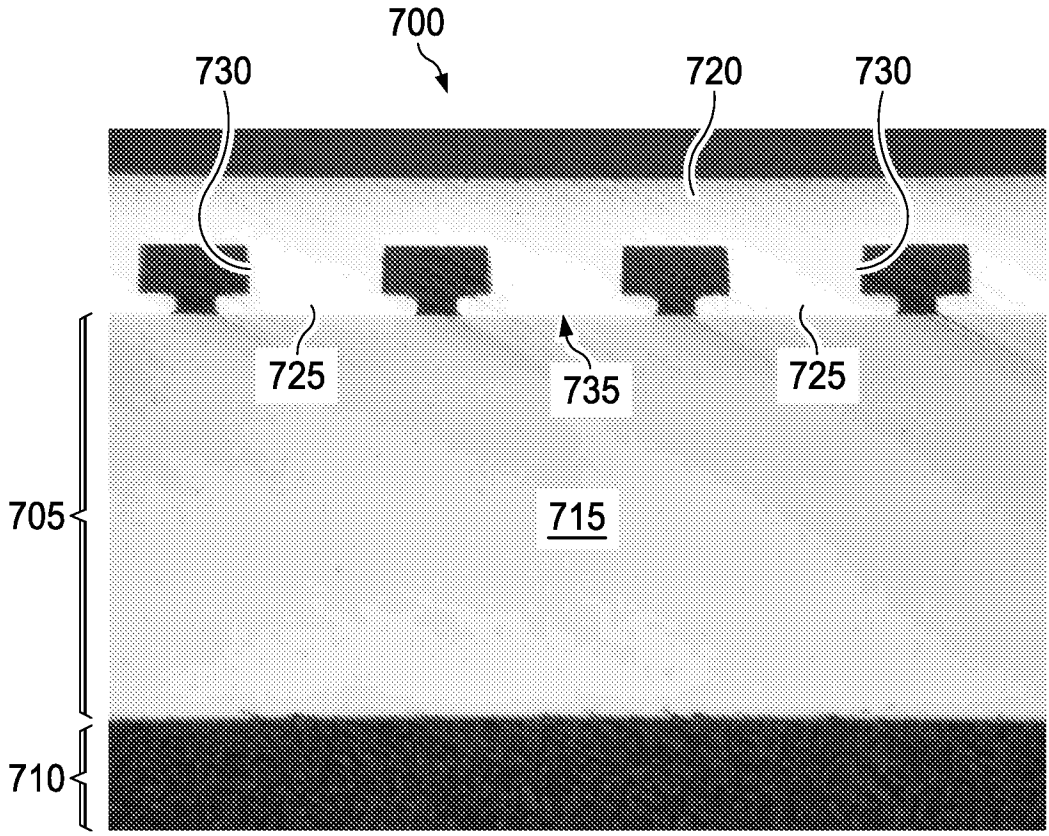


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/037149

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/50 *(2006.01)*
H01L 23/528 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/50, 21/56, 21/60, 21/78, 23/00, 23/04, 23/12, 23/29, 23/31, 23/48, 23/498, 23/50, 23/52, 23/522, 23/528

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/0224992 A1 (PAUL ALAN MCCONNELEE et al.) 09.09.2010	1-20
A	US 2017/0352612 A1 (SK HYNIX INC.) 07.12.2017	1-20
A	US 2016/0190096 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 30.06.2016	1-20
A	WO 2018/063321 A1 (INTEL CORPORATION) 05.04.2018	1-20
A	US 2011/0256664 A1 (REZA ARGENTY PAGAILA et al.) 20.10.2011	1-20

[X] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 October 2019 (10.10.2019)	17 October 2019 (17.10.2019)

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/037149

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6597070 B2 (NEC ELECTRONICS CORPORATION) 22.07.2003	1-20