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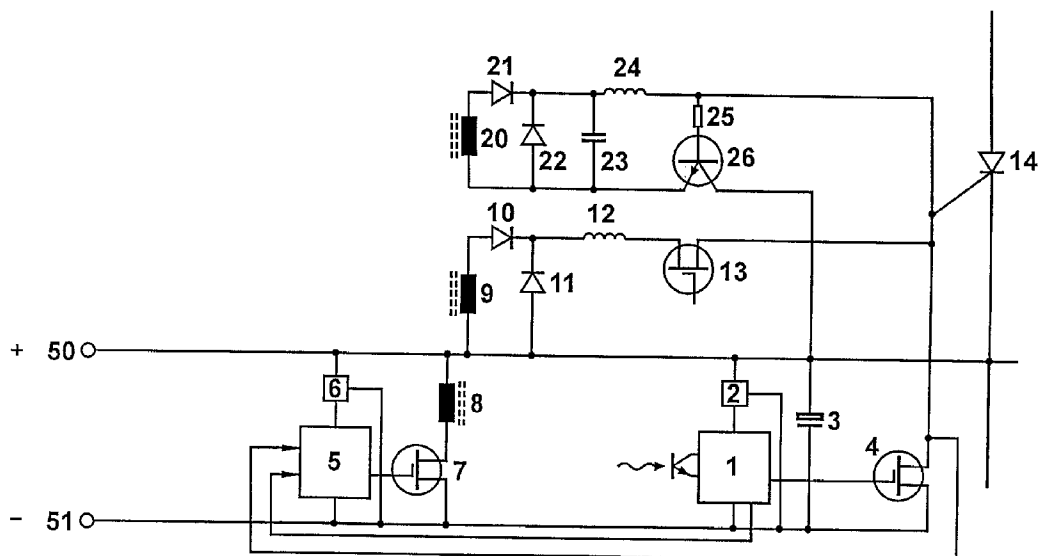
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(54) **DISPOSITIF SERVANT A LIMITER LE COURANT DE
MAINTIEN D'UN THYRISTOR COMMANDE PAR LA
GACHETTE**

(54) **APPARATUS FOR LIMITING THE HOLDING CURRENT OF A
GATE TURN-OFF THYRISTOR**



(57) L'invention est un dispositif servant à limiter le courant de maintien d'un thyristor commandé par la gâchette. Ce dispositif fait partie d'un circuit d'attaque servant à activer et à désactiver le thyristor; un transistor est placé sur le trajet du courant entre le circuit d'activation du circuit d'attaque et la gâchette ou la cathode du thyristor, l'électrode de commande de ce transistor étant connectée à la cathode ou à la gâchette du thyristor. Dans la concrétisation privilégiée de l'invention, on utilise un transistor pnp dans le premier cas et un transistor npn dans le second cas.

(57) An apparatus for limiting the holding current of a GTO is specified. The apparatus is part of a drive circuit for turning the GTO on and off and is defined in that a transistor is connected into the current path between the turn-on circuit of the drive circuit and either the gate or the cathode of the gate turn-off thyristor, the control electrode of the transistor being connected to the cathode or to the gate of the gate turn-off thyristor. A pnp transistor is preferably involved in the first case and an npn transistor in the second case.

ABSTRACT OF THE DISCLOSURE

An apparatus for limiting the holding current of a GTO is specified. The apparatus is part of a drive circuit for turning the GTO on and off and is defined in that a transistor is connected into the current path between the turn-on circuit of the drive circuit and either the gate or the cathode of the gate turn-off thyristor, the control electrode of the transistor being connected to the cathode or to the gate of the gate turn-off thyristor. A pnp transistor is preferably involved in the first case and an npn transistor in the second case. (Figure 2)

TITLE OF THE INVENTION

Apparatus for limiting the holding current of a gate turn-off thyristor

5 BACKGROUND OF THE INVENTIONField of the Invention

The invention is concerned with the field of power electronics. It is based on an apparatus for limiting a holding current of a gate turn-off thyristor
10 according to the preamble of the independent claim.

Discussion of Background

Gate turn-off thyristors or GTOs require a not inconsiderable holding current at the gate in order to
15 maintain the on state. In the case of very high power GTOs, such as, for example, a 3kA/4.5kV type, a holding current of between 4A and 8A, for example, is required in the on state in order that the latching conditions are reliably reestablished even after dips in the anode
20 current and after commutation operations between the GTO and the reverse-connected parallel diode. For the purpose of recombination, moreover, it is often necessary to provide an increased current surge. In the prior art, it is often the case that a turn-on pulse is
25 applied again for this purpose. The power demand, the physical volume and also the cooling requirement of the drive circuits are thereby increased considerably.

However, it would be desirable precisely for what are referred to as hard-driven GTOs to have
30 available a drive circuit which is as compact as possible, in order that said drive circuit can be arranged in the immediate vicinity of the GTO. A drive circuit for hard-driven GTOs is described in the same inventor's European Patent Application EP 0 489 945 A1.
35 In contrast to conventional driving, hard driving of a gate turn-off thyristor means that a higher and very much steeper current is applied to the gate for the purpose of turning the GTO off. Means for generating a

turn-on current are additionally provided. These means generate a current for turning the GTO on and a holding current for maintaining the on state. The means in each case comprise capacitors in which the necessary energy
5 is stored and is drawn as required with the aid of switches.

Furthermore, the German Patent Application having the application number 197 08 873.2, which is likewise the work of the same inventor and was not
10 published before the priority date, discloses a spatial arrangement for a drive unit. For it is arrangements having a structure of very low inductance that are demanded in order to realize the hard driving. For this purpose, the patent application that was not published
15 before the priority date proposes arranging the component in the immediate vicinity of the GTO. Moreover, large structures complicate the overall power converter with regard to stability and overall physical volume as a result of being closely linked with the
20 GTO. Therefore, particularly in the case of hard-driven GTOs, it is necessary to construct the drive circuits such that they are small, reliable and provided with high efficiency.

In particular cases, when the current in the on
25 state has commutated to the reverse-connected parallel diode, a voltage present at the anode of the GTO is negative with respect to the cathode. This voltage is transferred to the gate by the inner structure. On account of the negative voltage of the gate with
30 respect to the cathode, the holding current flowing into the gate would rise unimpeded if there were no suitable measures.

SUMMARY OF THE INVENTION

35 Accordingly, one object of the invention is to provide a novel apparatus for limiting the holding current which has a simple structure yet functions reliably nevertheless. In addition, the intention is to

construct a drive circuit with which the apparatus is associated such that it is compact, reliable and provided with a high efficiency. This object is achieved by means of the features of the independent
5 claim.

The apparatus according to the invention is defined in that a transistor is connected into the current path between the turn-on circuit of the drive circuit and either the gate or the cathode of the gate
10 turn-off thyristor, the control electrode of the transistor being connected to the cathode or to the gate of the gate turn-off thyristor. A pnp transistor is preferably involved in the first case and an npn transistor in the second case.

The drive circuit comprises a turn-on circuit and a turn-off circuit. The turn-on current and the holding current are generated from voltage pulses which are converted into currents with the aid of an electrical energy store. It is particularly
15 advantageous in terms of circuitry if the required voltage pulses are drawn from the same energy source or the same energy store as the pulse which is required for generating the turn-off current. The holding current is preferably generated by repetition of
20 voltage pulses. The repetition frequency of these voltage pulses can then be increased or decreased, depending on the requirement. In particular, if the gate-cathode voltage becomes negative, the frequency is reduced in order to be increased again when the voltage
25 is positive once again. A drive circuit according to the invention thus comprises, in the context of the turn-on circuit, at least one electrical energy store which converts the voltage pulses into currents. It is possible to provide a common energy store for the turn-
30 on current and for the holding current or else separate energy stores. The required energy can be transferred from the energy store of the turn-off circuit to the energy store of the turn-on circuit either by means of
35

inductive coupling or by means of capacitive coupling. A particularly preferred drive circuit is one in which the electrical feeding of the required logic circuits and of the other components is based on the
5 abovementioned energy store of the turn-off circuit.

The apparatus according to the invention enables the holding current to be limited reliably and virtually without any losses, in particular even when a voltage present at the gate is negative with respect to
10 the cathode. The structure of the apparatus according to the invention is very simple. The circuitry outlay of a drive circuit constructed in accordance with the invention can thus be kept extremely low. As a result, it is possible to arrange the drive circuit very close
15 to the GTO and to keep the inductance low as desired.

Further advantageous embodiments emerge from the corresponding dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

20 A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying
25 drawings, wherein:

Figure 1 shows a circuit diagram for elucidating the function of a drive unit for a GTO;

Figure 2 shows a circuit diagram of one embodiment of the invention;

30 Figure 3 shows a circuit diagram of a further embodiment of the invention;

Figure 4 shows a circuit diagram of a third embodiment of the invention;

35 Figure 5 shows a schematic illustration of the voltage pulse and of the current generated thereby;

Figure 6 shows a circuit diagram of a fourth embodiment of the invention.

The reference numerals used in the drawings and their meanings are summarized in the List of Designations.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, Figure 1 shows a circuit diagram of a drive circuit for a gate turn-off thyristor 14. 50 and 51 designate the positive and negative terminals of a voltage source having an output voltage of, for example, 20 V. This voltage source feeds an energy store 3 belonging to a turn-off circuit. The energy store 3 may be designed in particular in the form of an electrolytic capacitor bank. The drive circuit comprises not only the turn-off circuit but also a turn-on circuit. The turn-off circuit is essentially formed by a turn-off logic unit 1, by the energy store 3 and a switch 4. The switch 4 is connected to the gate of the GTO 14 and to the energy store 3 and is driven by the turn-off logic unit 1. The turn-off logic unit 1 is preferably fed by an in-phase regulator 2 (a commercially available voltage regulator). The turn-off logic unit 1 receives the required control signals for example via an optical waveguide, indicated by the arrow and the transistor at the left-hand edge of the block of the turn-off logic unit 1. A command, sent via the optical waveguide, to turn the GTO 14 off is amplified in the logic unit 1 and forms a voltage at the switch 4, with the result that the latter starts to conduct. On account of the polarity of the energy store 3, a current is thus drawn from the gate of the GTO 14. The gate of the GTO consequently becomes negative with respect to the cathode, and the GTO turns off. The switch 4 may also comprise, in particular, a parallel circuit of MOSFETs. The same applies analogously to the energy store 3,

which may comprise a plurality of electrolytic capacitors connected in parallel.

A turn-on circuit is additionally provided. This comprises a turn-on logic unit 5, which is fed by
5 the energy store 3 in the same way as the turn-off logic unit 1. The corresponding in-phase regulator is designated by 6. The two logic units 1 and 5 are connected to one another in terms of signals. If the turn-off logic unit 1 receives a command for turning
10 the GTO 14 off, then activation of the turn-on logic unit 5 is prevented in this way. However, if the logic unit 1 receives a turn-on command, then the turn-on logic unit 5 compels the switch 7 that it drives to effect cyclic pulsing. The switch 7 is likewise
15 arranged between the terminals 50 and 51. The voltage pulses generated in this way are transferred to a rectifier diode 10 with the aid of the transformer 8, 9, which is connected in series with the switch 7, which rectifier diode feeds an electrical energy store,
20 preferably an inductance 12. The inductance of the transformer 8,9 should be smaller than the inductance 12 in order to keep the inductance of the entire arrangement low as desired. Structurally, this can be achieved for example by integrating the coils 8 and 9
25 on the circuit board and coupling them magnetically to a core. Depending on the required size of the inductance 12, it can also be integrated in the form of a conductor loop on the circuit board. The inductance 12 is connected to the gate of the GTO 14 via a further
30 switch 13. The switch 13 disconnects the turn-on circuit from the gate of the GTO during the turn-off operation and in the off state.

Figure 5 shows a voltage pulse V_T of the kind which is transferred via the transformer 8,9. On the
35 secondary side, the voltage pulse is rectified by the diode 10 and converted into a current in the inductance 12. The current can oscillate via the freewheeling diode 11 arranged between positive terminal 50 and

cathode. To a first approximation, the current through the inductance 12 has a triangular waveform, as illustrated in Figure 5. For a 3kA, 4.5kV GTO, approximately 200 A to 400 A are required for the turn-on operation and should be maintained for approximately 5 to 15 μ s. This yields exemplary values for the inductance 12 in the region of 100 nH. After the turn-on operation, however, the GTO 14 still requires a holding current in order to maintain the on state. The simplest way to effect this is for the turn-on pulse described to be repeated at a specific frequency f1.

The current demand for triggering, on the one hand, and for maintaining the triggered state, on the other hand, differs greatly. For triggering, approximately 200 A are necessary for very high power GTOs, as mentioned, whereas the holding current need only be approximately 2 A. For this reason, it would be advantageous if the holding current could be generated with less power than by repetition of the turn-on pulse. Figure 2 shows an exemplary embodiment which meets this requirement. A second inductance 24 is provided which is likewise fed by means of the transformer via a second secondary winding 20. The rectifier diode bears the reference numeral 21 and the freewheeling diode bears the reference numeral 22. A capacitance 23 is preferably connected in parallel with the freewheeling diode 22. The capacitance 23 enables slower drawing of energy, with the result that the repetition frequency can be kept lower and the holding current is nevertheless sufficiently uniform. Consequently, the inductance 24 can be chosen to be larger than the inductance 12, for example in the range from 10 to 50 μ H. Instead of a second secondary winding 22, it is also possible to provide a dedicated transformer and a dedicated logic unit. In the case of this generation of the holding current which is separate from the generation of the turn-on pulse, the switch 13 is opened after the GTO 14 has been

triggered, with the result that the inductance 12 is disconnected from the gate.

In the case of the separate generation of the holding current, active current rise limiting means 25, 26 are connected between the gate and the cathode of the GTO 14. An inventive apparatus for limiting the holding current in any operating state comprises a transistor 26, which is connected into the current path between turn-on circuit and cathode in the case of Figure 2. An emitter follower with a bipolar transistor 26 and a base series resistor 25 is preferred. This apparatus reliably prevents the holding current from being able to rise unimpeded in the event of a negative gate-cathode voltage. Specifically, the diode 22 is switched on in the event of a negative voltage, and the current could thus rise unimpeded. This is effectively prevented by the apparatus according to the invention.

The voltage pulse required for generating the holding current can also be tapped off directly from the rectified voltage after the diode 10 without a second secondary winding. Figure 3 shows a corresponding exemplary embodiment. The common node of the rectifier diode 10 and of the freewheeling diode 11 is connected to the second inductance 24. The current rise limiting means bear the reference numerals 27 for the bipolar transistor and 28 for the series resistor. In this exemplary embodiment, a transistor of opposite polarity is used, and the transistor 27 is connected into the gate current path. The functioning of this embodiment is essentially the same as that according to Figure 2. It functions as follows: in the event of a positive gate-cathode voltage, the current from the inductance 24 is divided into a base current and a collector current of the transistor 27. The base current activates the transistor. Consequently, the inductance 24 is connected directly to the gate of the GTO 14. In the event of a negative gate-cathode voltage, the transistor starts to regulate: in order

that the transistor can carry a collector current, its emitter must be more positive than the base by the forward voltage, i.e. approximately 0.7 V. The inductance 24, which may be regarded as a current
5 source to a first approximation, continues to operate as reverse voltage, however. The collector voltage becomes negative as soon as the commutation operation, i.e. the GTO 14, compels this. Nevertheless, the current from the inductance 24 largely continues to
10 flow via the emitter-collector path. This current is effectively limited because the transistor prevents this due to the regulating condition $V_{on} = V_{EB} + V_R$. V_{on} designates the voltage across the inductance, V_{EB} the emitter-base voltage and V_R the voltage drop across
15 the base series resistor. The apparatus according to Figure 2 with the npn transistor 26 instead of the pnp transistor 27 that has been explained functions in an analogous manner.

Instead of inductive coupling with the aid of a
20 transistor, capacitive coupling with capacitors is also possible. Figure 4 shows a corresponding exemplary embodiment. A turn-on logic unit 5a drives two transistors 31 and 30 arranged between the terminals 50 and 51. The transistor 31 generates a positive voltage
25 pulse, and the transistor 30 resets again. The voltage pulse generated is forwarded to the rectifier diode 10 via a coupling capacitor 32. A charge reversal diode 33 is additionally provided which is arranged between the cathode of the GTO or the positive terminal 50 of the
30 voltage source and the rectifier diode 10. The circuit according to Figure 4 otherwise functions like those which have already been described above.

Figure 6 shows an embodiment of the invention in which the turn-off circuit is used to generate the
35 triggering current. The logic units 1 and 5 are not illustrated here, for the sake of clarity. The circuit functions as follows: a charging transistor 36 connects a connectable triggering inductance 35 to the positive

terminal 50 before the turn-off transistor 4 is switched off. Consequently, a current builds up in the inductance 35, which current commutates directly to the gate after the switching off of the switch 4 and thus forms the required triggering pulse. The inductance 35 can be chosen such that the current decays in approximately 5 to 10 μ s. Afterwards, the charging diode 37 connected upstream of the inductance 35 blocks and the charging transistor 36 can be switched off again. If the transistor 36 is switched off before the current has decayed, then the residual energy can be returned to the energy store 3 via the freewheeling diode 38. A particularly short yet fully effective triggering pulse is generated in this way. That part of the turn-on circuit which is designed for generating the holding current can be constructed in the manner already described, or the required energy can be transferred to the energy store 24 from the energy store 3 by means of a storage inductance 34 and the rectifier diode 21 by cyclic pulsing of the switch 7. To switch the GTO 14 off, a current is drawn from the gate by actuation of the switch 4.

In the description above, different variants of energy coupling and feeding have been specified which, although they have been explained only with reference to individual figures, can, of course, be combined with one another virtually as desired, depending on where a circuitry emphasis is to be formed.

The drive circuit explained enables a reduction in the repetition frequency f_1 of the voltage pulses for the holding current as soon as a negative gate-cathode voltage occurs at the GTO. As a consequence, the loss occurring in the bipolar transistor 26 or 27 of the current rise limiting means is reduced, particularly in very high power GTOs, i.e. those having a high holding current demand ($> 1A$). The repetition frequency can be increased again after a positive voltage has been reestablished between gate and cathode

of the GTO. This means that a higher gate current is achieved again, thereby ensuring continuous recombination of the GTO. A retriggering pulse in the form that has been customary to date consequently becomes superfluous. The risk of the retriggering pulse occurring at the wrong point in time and, in addition, all the other problems associated with exact detection of the correct retriggering instant thus disappear as well. Moreover, the EMC immunity of the arrangement can be increased in this way. Quite generally, the gate current can be set by influencing the repetition frequency of the voltage pulses.

In the text above, it was explained that the voltage pulse required for generating the turn-on current and the holding current is drawn from the same energy store 3 as the pulse required for the turn-off current. The circuit can alternatively be constructed in such a way that the turn-on circuit has a dedicated voltage supply. The transformer 8,9 would be dispensed with in this case, but in return at least one further supply line and a further energy store would be necessary.

Overall, the apparatus according to the invention permits the holding current to be limited reliably. A drive circuit equipped with this apparatus has a compact and extremely efficient structure, with the result that the inductance of the circuit arrangement becomes low. Consequently, the circuit is also especially suitable for hard-driven GTOs.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

CLAIMS:

1. An apparatus for limiting a holding current of a gate turn-off thyristor (14), the apparatus being
5 part of a drive circuit for turning the gate turn-off thyristor (14) on and off, which drive circuit comprises a turn-off circuit and a turn-on circuit and is arranged between the gate terminal and the cathode terminal of the gate turn-off thyristor (14), the turn-
10 on circuit being designed to generate a triggering current and a holding current, which maintains an on state of the gate turn-off thyristor (14), wherein the apparatus comprises a transistor (26, 27), which is connected into the current path between the turn-on
15 circuit and the gate or the cathode of the gate turn-off thyristor and whose control electrode is operatively connected to the cathode or to the gate of the gate turn-off thyristor.
2. The apparatus as claimed in claim 1, wherein
20 the turn-on circuit comprises at least one electrical energy store (12, 23, 24) which converts voltage pulses into the turn-on current and the holding current.
3. The apparatus as claimed in claim 2, wherein
25 the turn-off circuit comprises a capacitive energy store (3), from which energy for generating a turn-off current is drawn by means of a first switch (4), wherein the turn-on circuit comprises a second switch (7) and at least one transformer (8, 9, 20), a coupling capacitance (32) or a storage inductance (34), by means
30 of which voltage pulses are drawn from the energy store (3) for the purpose of generating the turn-on current and the holding current and are fed to the electrical energy store (12, 23, 24) of the turn-on circuit.
4. The apparatus as claimed in claim 3, wherein
35 the electrical energy store (12, 23, 24) of the turn-on circuit comprises a first inductance (12), which is connected to the gate of the gate turn-off thyristor (14) via a third switch (13).

5. The apparatus as claimed in claim 4, wherein the electrical energy store (12, 23, 24) of the turn-on circuit comprises a second inductance (24) and a capacitance (23) with a parallel freewheeling diode (22), which inductance (24) is connected to the gate of the gate turn-off thyristor.

6. The apparatus as claimed in claim 5, wherein the transformer (8, 9, 20) comprises a first secondary winding (9), which feeds the first inductance (12), and a second secondary winding, which feeds the second inductance (24).

7. The apparatus as claimed in claim 2, wherein the turn-off circuit comprises a capacitive energy store (3), from which energy for generating a turn-off current is drawn by means of a first switch (4), wherein the turn-on circuit comprises a second switch (7) and a storage inductance (34), by means of which voltage pulses are drawn from the energy store (3) for the purpose of generating the holding current and are fed to the electrical energy store (12, 24) of the turn-on circuit, and wherein the turn-on circuit comprises a connectable triggering inductance (35) for the purpose of generating the triggering current.

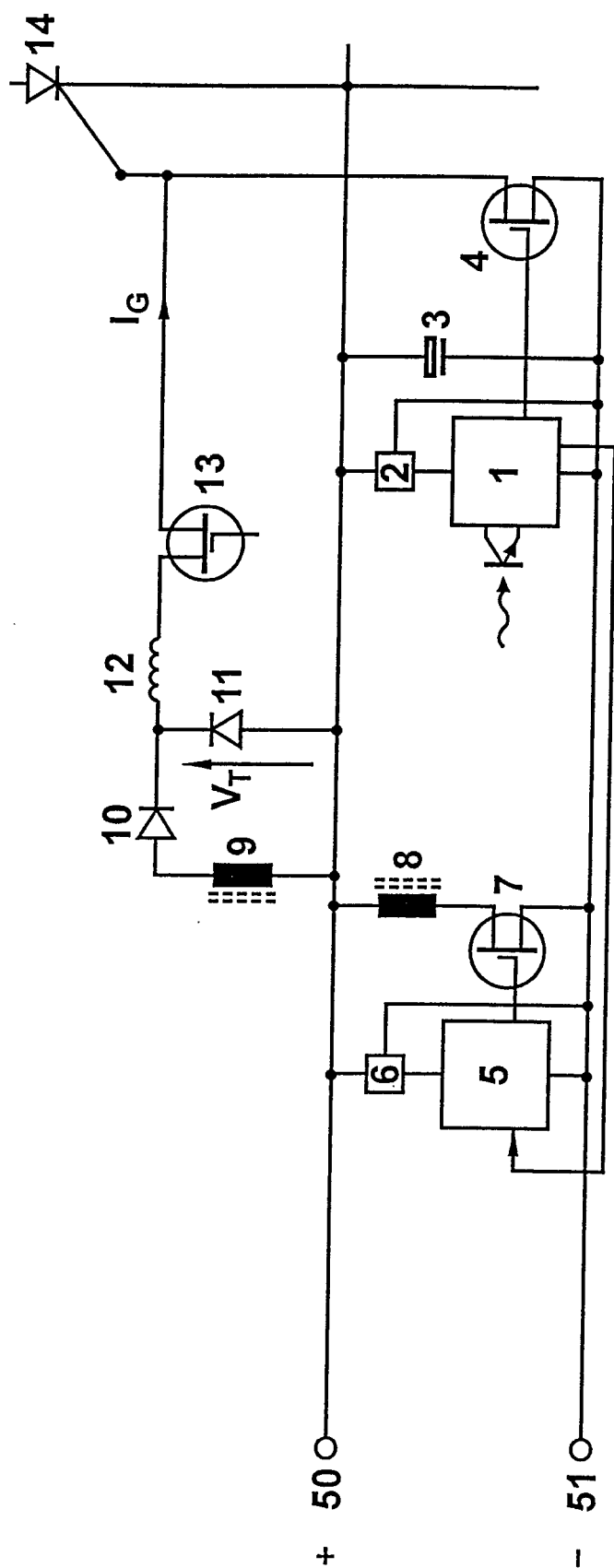
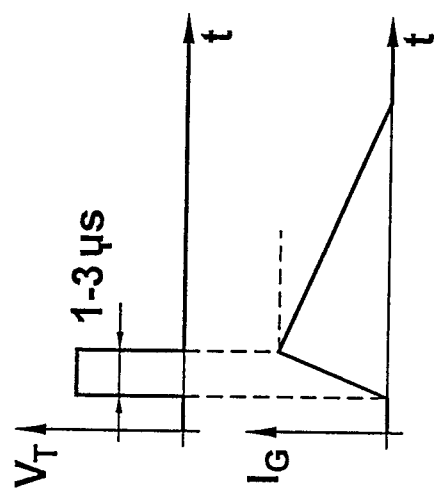
**FIG. 1**

FIG. 5

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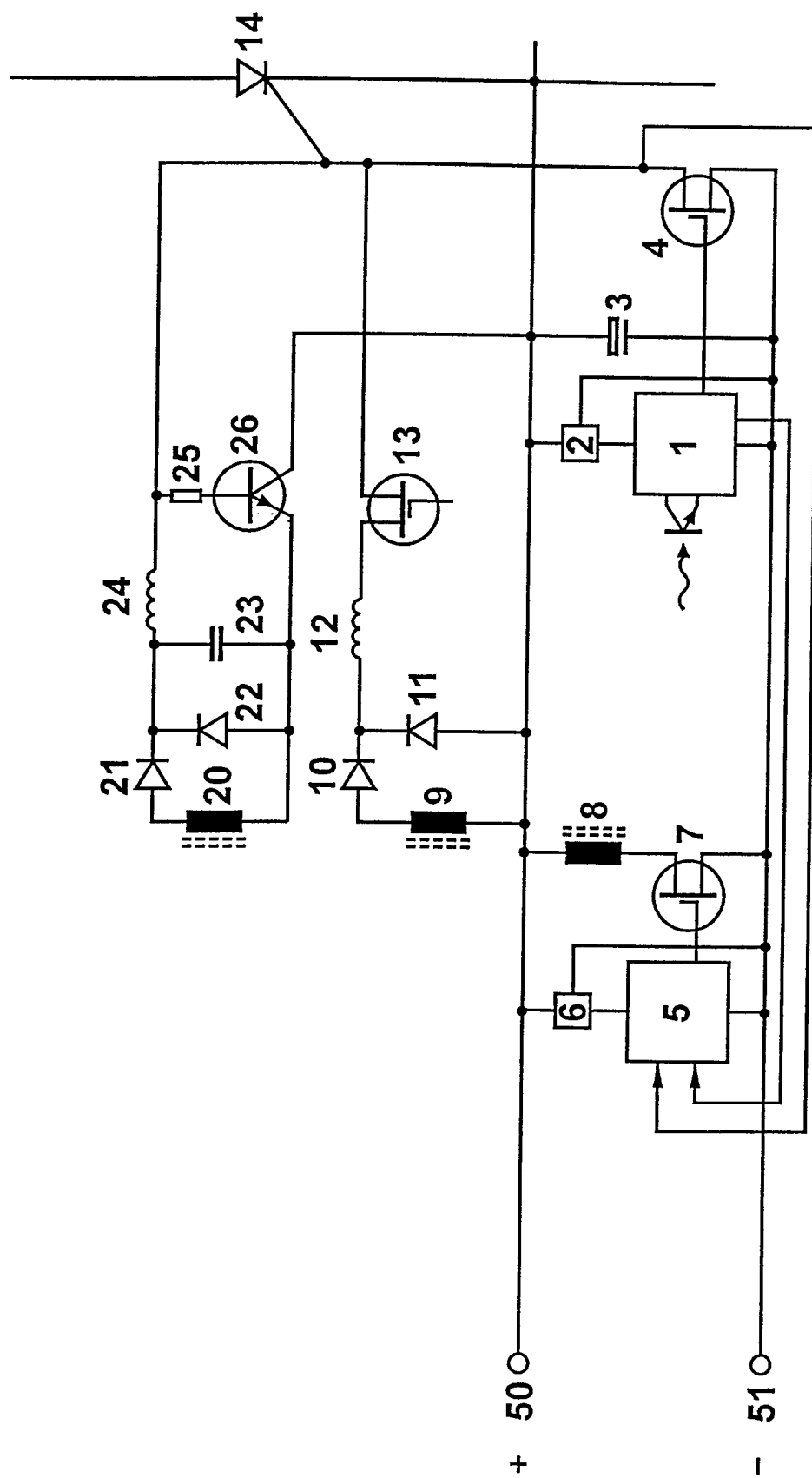


FIG. 2

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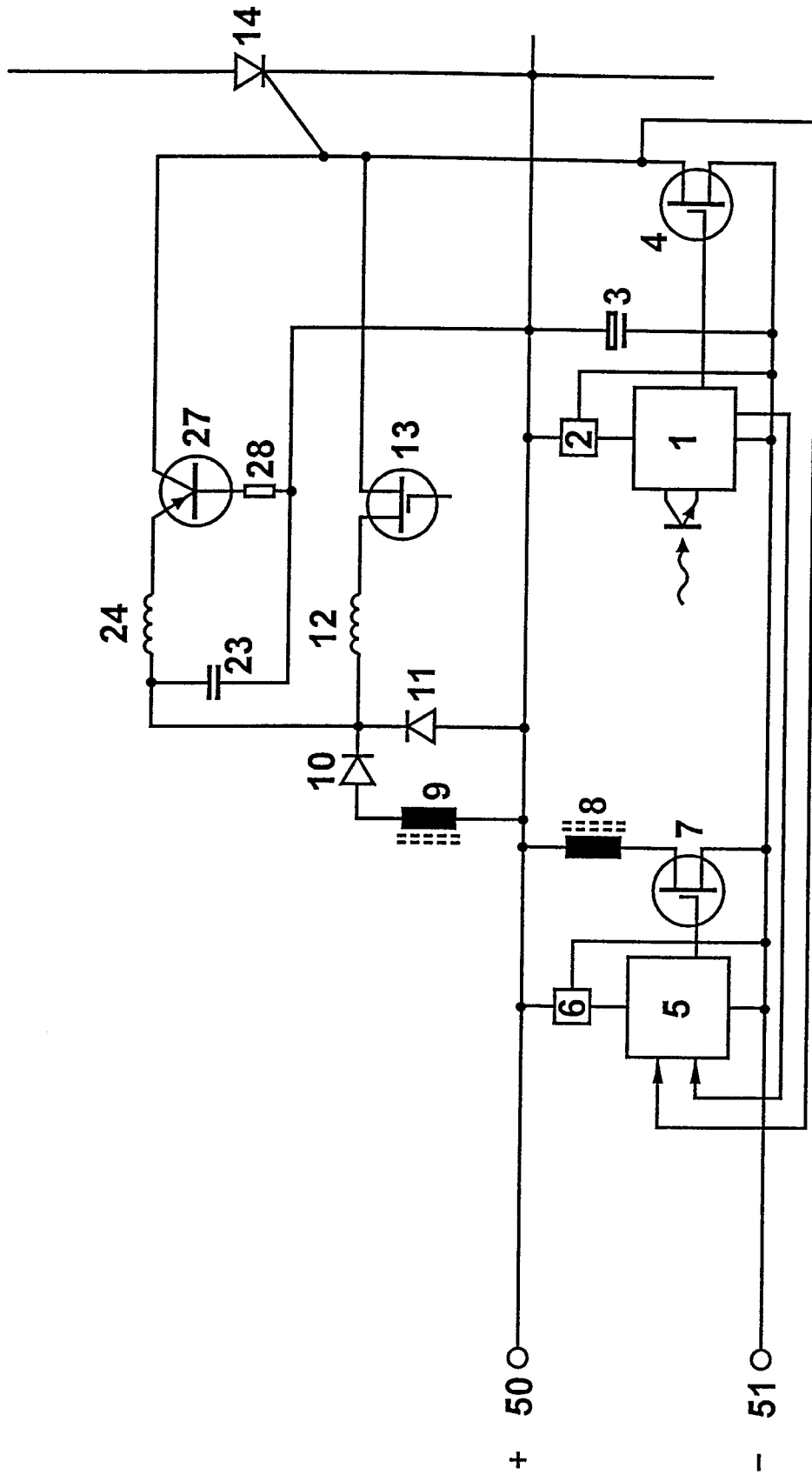


FIG. 3

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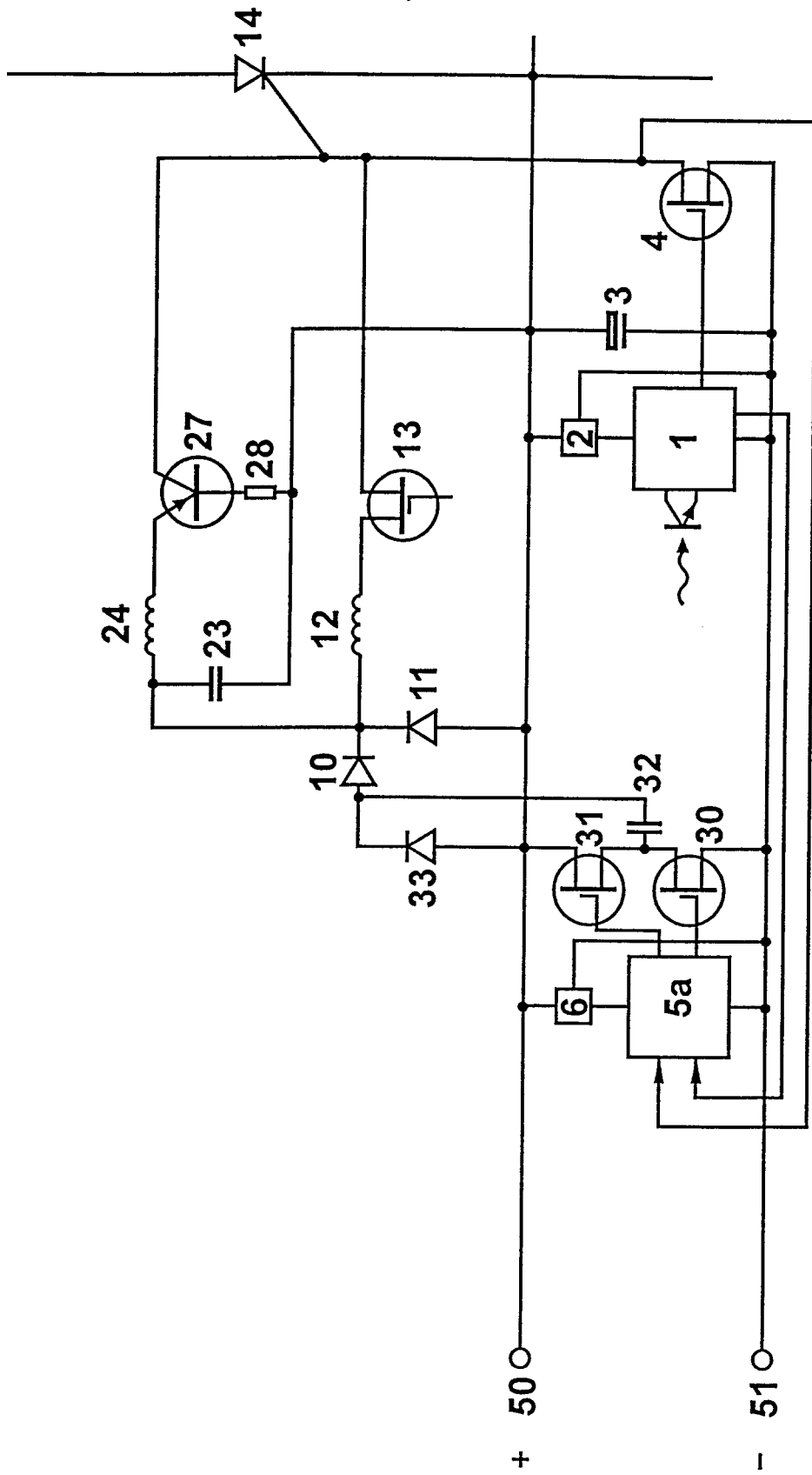


FIG. 4

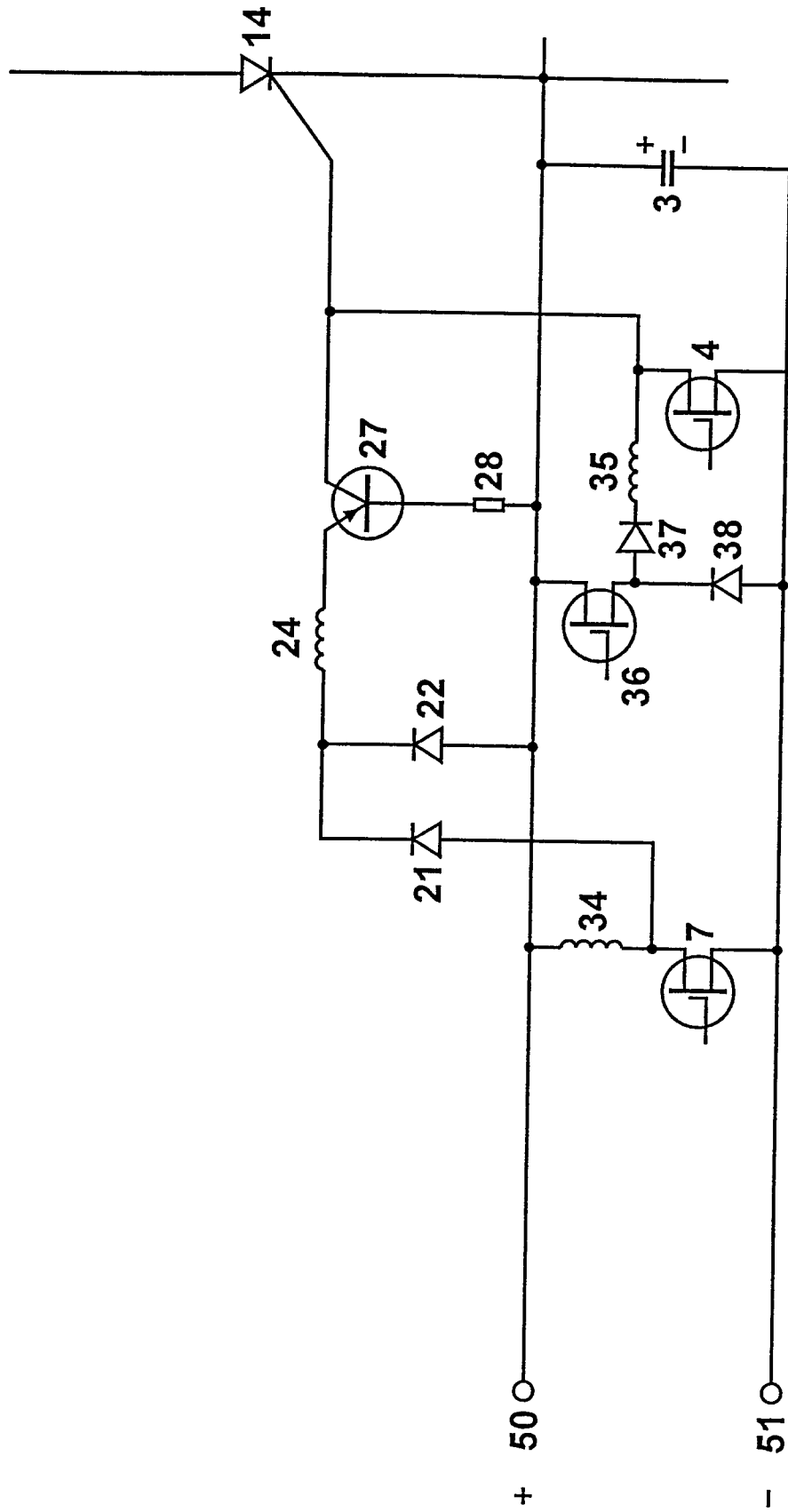


FIG. 6

