Dec. 2, 1969 J. E. STINE 3,482,238

MULTILEVEL BLANKING CONTROL AND MOMENTARY STROKE INHIBITION FOR VISUAL DISPLAY APPARATUS

Filed May 27, 1966 3 Sheets-Sheet 1

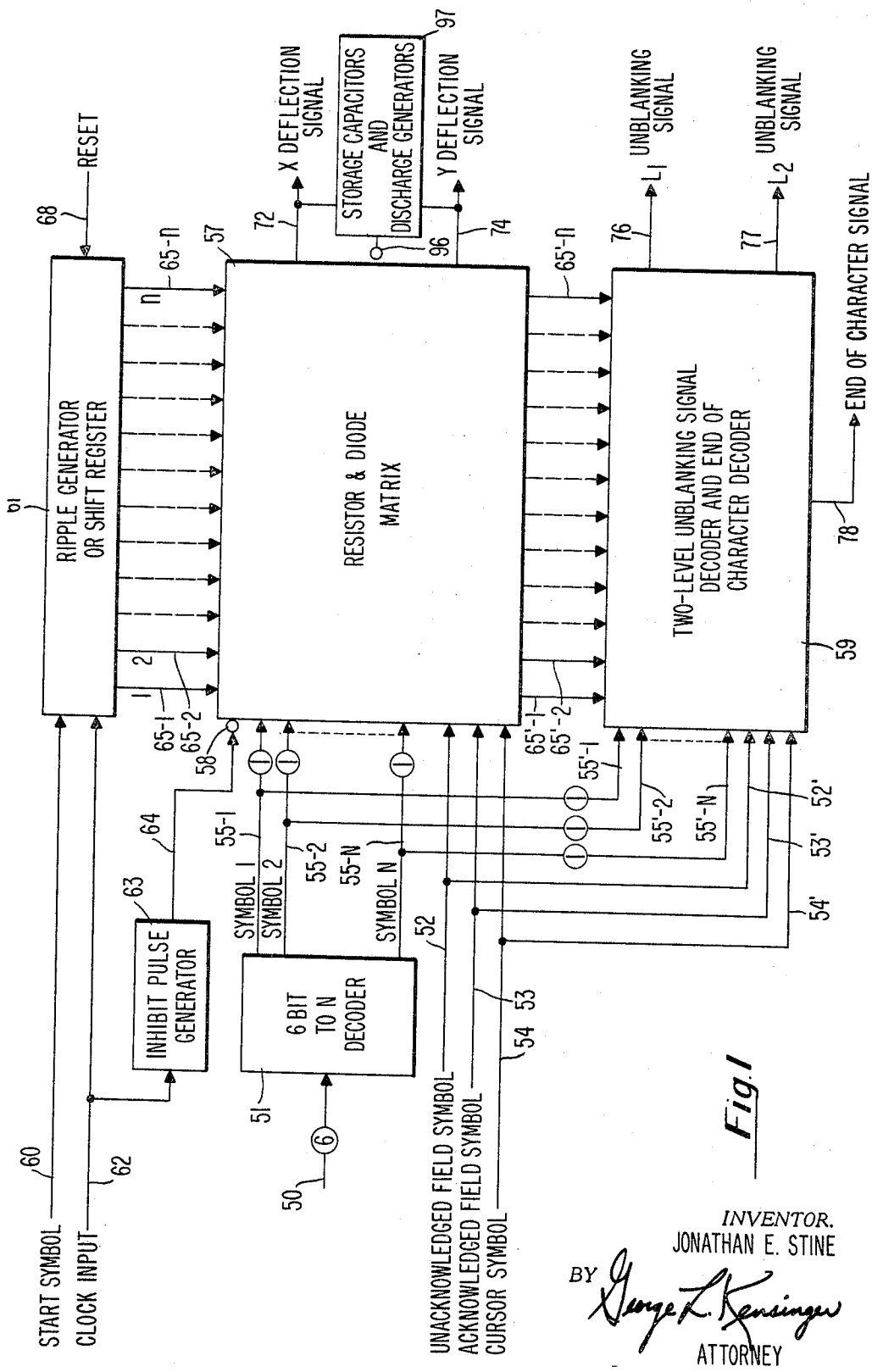



Fig. 1

INVENTOR.
JONATHAN E. STINE

BY George L. Kensinger
ATTORNEY

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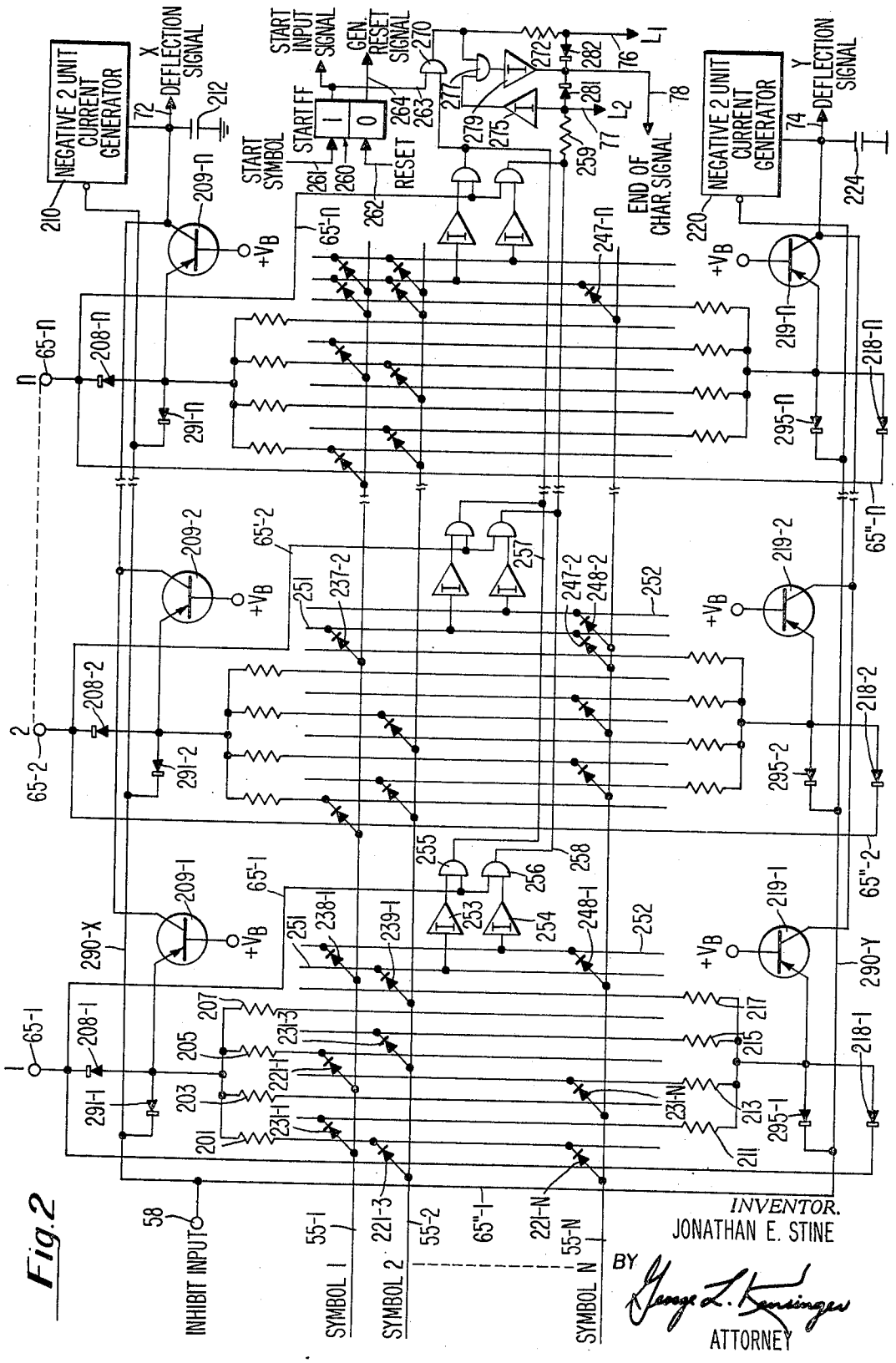



Fig. 2

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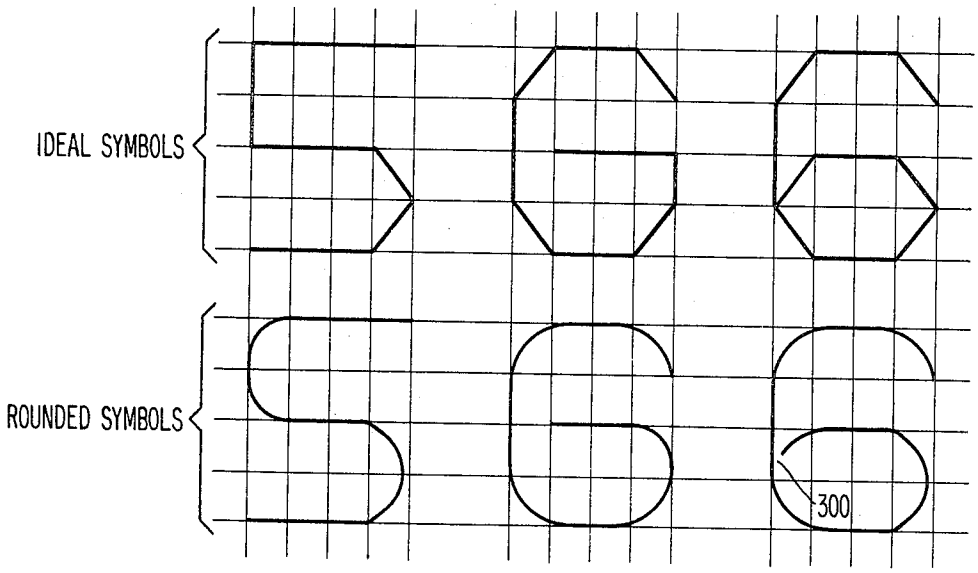



Fig. 3

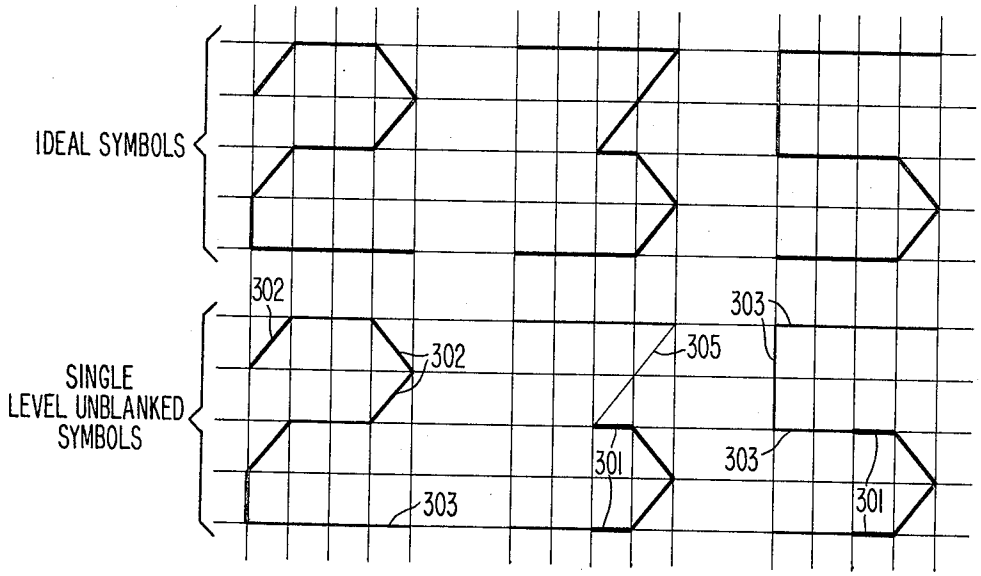



Fig. 4

INVENTOR.
JONATHAN E. STINE
BY George L. Kensinger
ATTORNEY

United States Patent Office 3,482,238 Patented Dec. 2, 1969



3,482,238

# MULTILEVEL BLANKING CONTROL AND MOMENTARY STROKE INHIBITION FOR VISUAL DISPLAY APPARATUS

Jonathan E. Stine, Wayne, Pa., assignor to Burroughs Corporation, Detroit, Mich., a corporation of Michigan

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Int. Cl. G08b 23/00; H01j 29/70
U.S. Cl. 340—324 10 Claims

## ABSTRACT OF THE DISCLOSURE

Multilevel blanking control and momentary stroke inhibition apparatus in resistor matrix symbol generators which include a plurality of sequentially actuated stroke generators each controlled by different groups of resistors. Each stroke generator is combined with decoder means for providing signals representative of a preselected level of unblanking for each character segment and an inhibit pulse generator operates in combination with all of the stroke generators.

This invention relates to the visual display of characters and symbols described by electric stroke signals. More specifically, the subject invention relates to multilevel blanking control and to means for providing improved definition and resolution of character vertices in visual display systems such as cathode ray tube displays and plotting devices incorporating a pointer, stylus or writing instrument and in electromechanical tool positioning control systems of record-controlled machine tools, for example.

Various deficiencies in the fidelity of the form of visually displayed characters or symbols arise in line segment or vector approximation of characters or symbols in visual display systems which are deleterious to symbol distinctiveness. There may be irregular transitions between signals representing successive line segments and there may be a lack of uniformity in the timed intervals provided for the successive segment or stroke signals. Also, the increasingly high operating frequencies required of symbol generators have in many cases exceeded the frequency response capabilities of the relatively limited bandwidth plotter control amplifiers or cathode ray tube deflection amplifiers employed in such display systems. This irregular signal generation and transition between signals and the exceeding of the frequency limitations of display amplifiers causes overlapping in the effect of successive signals in the display apparatus which results in a rounding or deterioration of symbol corners or vertices at the junctions of the line segments forming the symbols.

Another deficiency in display fidelity that occurs in symbol display systems in which equal time intervals are provided for the tracing or writing of line segments of different lengths, is nonuniformity in the brightness of the different length segments. When the line segment-representing signals in such systems are of equal duration, the writing speeds of line segments of different lengths are different, which results in reciprocal differences in the brightness of different line segments. This contributes to deterioration of symbol distinctiveness in both plotting devices and cathode ray tube display systems.

Accordingly, an object of the present invention is to improve the display capability and fidelity of visual display systems for preserving the distinctiveness of displayed symbols and characters.

Another object of the present invention is to make



more uniform the intensity of symbol-forming line segments in visual display apparatus by compensating for differences in writing speeds of different length line segments.

A further object of the subject invention is to preserve the sharpness and distinctiveness of displayed character or symbol vertices by preventing overlapping in the effect of successive line segment-representing electrical signals in visual display systems.

A still further object of the invention is to provide simple, inexpensive logically implemented multilevel blanking control for visual display systems which is applicable to matrix type symbol generators for rendering displayed line segments of different lengths written at different speeds more uniform in intensity or brightness.

In accordance with the above-stated objects, there is provided a blanking control generator matrix, for connection in a multiple stroke matrix character and symbol generator having a first plurality of successively enabled electrical ramp signal generators selectively coupled to a second plurality of character input conductors, comprising a set of conductors associated with each electrical ramp signal generator, asymmetrically conductive means electrically coupling selected conductors of said second plurality of character input conductors to selected ones of said sets of conductors, means electrically connecting the conductors of each of said sets to the associated electrical ramp signal generator for gating electrical signals on said sets of conductors in synchronism with the successive conduction of said ramp signal generators, and decoding means electrically connected to each of the gating means for providing electrical output signals indicative of multiple unblanking control levels and an end of character signal. Also provided is a conduction inhibiting means connected to each of said electrical ramp signal generators for inhibiting conduction of the generators for the duration of an inhibit input pulse for preventing overlapping in the effect of successively generated line segment-representing electrical signals in display systems.

Reference is made to the G. Yanishevsky United States patent application, Ser. No. 553,362, entitled "Resistor Matrix Symbol Generator," filed on May 27, 1966, as an example of the symbol generators with which the present application may be utilized. That Yanishevsky patent application along with the patent applications therein referenced and an article entitled "Improving the Information Flow Rate Between Man and Machine," by Charles Halsted, appearing in the April 1966 issue of Electronics Industries magazine at pages 62–66, are incorporated herein for their disclosure of the manner of interconnecting symbol generators and blanking control generators in cathode ray tube display systems and for an understanding of character display techniques and of the terminology employed herein.

Other objects, features and advantages of the present invention will become clear from a consideration of the following detailed description and claims when read with reference to the accompanying drawings wherein:

FIGURE 1 is a schematic block diagram of symbol generating apparatus incorporating the subject invention;

FIGURE 2 is an electrical schematic circuit diagram of the resistor matrix symbol generator of FIGURE 1 incorporating the blanking control matrix and stroke inhibition means of the present invention;

FIGURE 3 is a pictorial representation of ideal and rounded representative characters and symbols displayed from electrical signals provided by matrix type symbol generation means; and

FIGURE 4 is a pictorial representation of ideal representative numerical symbols formed of segments of uniform intensity and of the same symbols formed of seg-

ments of variable intensity as a result of variable writing speeds in the display thereof.

Referring more particularly to the apparatus of FIGURE 1, a resistor matrix symbol generator having a plurality of stroke generators is shown incorporating resistor and diode matrix **57** having input terminals **55–1** through **55–N** for receiving character input signals and output conductors **72** and **74** on which are provided a series of X deflection signals and Y deflection signals, respectively, upon receiving successive enabling signals on conductors **65–1** through **65–*n*** and a character input signal. A decoder **51** may be utilized for decoding character information codes received on conductors **50** for providing individual character input signals to the resistor and diode matrix. Resistor and diode output conductors **72** and **74** are connected to storage capacitors and discharge generators **97** which maintain potential levels between successive stroke signals and are discharged by a signal on control terminal **96**. Also connected to the resistor and diode matrix are input conductors **52**, **53** and **54** for receiving character input signals indicating an unacknowledged field, an acknowledged field, and a cursor symbol, respectively. Enabling control conductors **65–1** through **65–*n*** are successively actuated by ripple generator or shift register **61** upon receiving a start symbol on conductor **60** and a series of clock pulses on conductor **62**.

Also connected to character and symbol input conductors **55–1** through **55–N** and symbol input conductors **52** through **54** is two level unblanking signal decoder and end of character decoder **59**, through input conductors **55′–1** through **55′–N** and **52′** through **54′**, respectively The unblanking signal decoder provides a series of first, or first and second, unblanking signals on output conductors **76** and **77**, respectively, upon receiving sequential enabling signals on conductors **65′–1** through **65′–*n*** which are electrically connected to conductors **65–1** through **65–*n***. The end of character decoder provides an end of character signal on output conductor **78** at the termination of each character and symbol generation, which may be applied to reset input terminal **68** of ripple generator or shift register **61** and to conductor **262** for resetting start flip-flop **260** and may be provided to the source of character input information for signalling the readiness of the symbol generator to receive new character information.

Resistor and diode matrix **57** also has an inhibit terminal **58** electrically connected through conductor **64** to the output terminal of inhibit pulse generator **63**, which is controlled by clock signals appearing on conductor **62** to which it is connected. Signal generation by the resistor and diode matrix **57** is inhibited or interrupted during an initial portion of each clock pulse period under the control of inhibit pulse generator **63**, which separates the line segment-representing signals provided on output conductors **72** and **74** and thereby enables the distinct formation of displayed character or symbol vertices in a visual display system in which the generator is incorporated.

The resistor matrix symbol generator of FIGURE 1, incorporating the subject invention, is illustrated in more detail in the electrical schematic circuit diagram of FIGURE 2 wherein the resistor and diode matrix comprises X current generating PNP transistors **209–1** through **209–*n*** and Y current generating PNP transistors **219–1** through **219–*n*** and the associated input and control circuitry. Character input signals are received on input conductors **55–1** through **55–N** and are selectively coupled by diodes **221–1** through **221–*n*** and input resistors **201** through **207** of different magnitudes to the emitter of X current generating transistor **209–1** of the first stroke generator. The character input signals are also selectively coupled through unidirectional devices **231–1** through **231–N** and different valued resistors **211** through **217** to the emitter of Y current generating transistor **219–1** of the first stroke generator. The remaining X current generating transistors **209** and Y current generating transistors **219** are likewise selectively coupled to the character input conductors **55–1** through **55–N**. The emitters of the X current generating transistors are also electrically connected to enabling pulse receiving control terminals **65–1** through **65–*n*** by diodes **208–1** through **208–*n*** and the emitters of the Y current generating transistors are electrically connected to enabling control terminals **65–1** through **65–*n*** by diodes **218–1** through **218–*n*** and conductors **65″–1** through **65″–*n***, respectively.

The collectors of the X current generating transistors **209–1** through **209–*n*** are connected to output conductor **72**, to one plate of storage capacitor **212** and to the output terminal of negative 2 unit current generator **210**. The collectors of the Y current generator are connected to output conductor **74**, to one plate of storage capacitor **224** and to the output terminal of negative 2 unit current generator **220**. The base electrodes of all of the current generating transistors are coupled to reference potential +VB, and the other plate of storage capacitors **212** and **224** are grounded. Further details regarding the construction and operation of a symbol generator similar to that shown in FIGURE 2, may be found in the above-identified Yanishevsky United States patent application, Ser. No. 553,362. No discharge generating means is shown in the symbol generator of FIGURE 2 for discharging storage capacitors **212** and **224** between the generation of the series of X and Y signals for successive characters in order to permit a better illustration of the details of the present invention. In practice, discharge generators are electrically connected to storage capacitors **212** and **224** as indicated in FIGURE 1 of the instant patent application and as illustrated in FIGURE 4 of the above-referenced Yanishevsky patent application, for example.

The resistor and diode matrix of the present invention also incorporates an inhibit pulse receiving control terminal **58** which is electrically connected by conductor **290–X** and diodes **291–1** through **291–*n*** to the emitters of X current generating transistors **209–1** through **209–*n*** and to an inhibit control terminal of negative current generator **210**. The inhibit control terminal **58** is also electrically connected by conductor **290–Y** and unidirectional devices **295–1** through **295–*n*** to the emitters of Y current generating transistors **219–1** through **219–*n*** and to an inhibiting control terminal of negative current generator **220**.

Also incorporated in the symbol generator of the present invention are pairs or sets of conductors **251** and **252** associated with each segment or stroke generator of the matrix. Unidirectionally conductive devices **237** through **248** selectively electrically connect the character input conductors **55–1** through **55–N** to the pairs of unblanking decoder conductors **251** and **252** of each of the stroke generators, as shown. The decoder conductor pairs of the stroke generators are also electrically coupled to one of the input terminals of the respective AND gates **255** and **256** through inverters **253** and **254**. The other input terminals of AND gates **255** and **256** are electrically connected to the respective enabling control terminals **65–1** through **65–*n*** via conductors **65′–1** through **65′–*n***. The output terminals of the AND gates **255** and **256** are connected, respectively, to an input terminal of AND gate **270** and to one end of resistor **259**.

The other input terminal of AND gate **270** is electrically connected through conductor **263** to the "one" output of start flip-flop **260** for receiving start input signals. The start flip-flop is set by a start symbol on conductor **261** and is reset by a signal on conductor **262**. The "zero" output of start flip-flop **260** appearing on conductor **264** provides a symbol generator reset signal which may be returned to the source of character input information. The output terminal of AND gate **270** is electrically connected to one end of resistor **272** and to an input terminal of AND gate **277**, the other input terminal of which is electrically coupled to the other end of resistor **259** through inverter **275**.

The other end of resistors **259** and **272** are connected to the anodes of diodes **281** and **282**, respectively, the cathodes of which are electrically coupled through conductor **78** and inverter **279** to the output terminal of AND gate **277**, upon which end of character signals are developed. The second end of resistor **272** is also connected to output conductor **76** for providing a first unblanking signal $L_1$. The second end of resistor **259** is connected to output conductor **277** for providing a second unblanking signal $L_2$.

The development of unblanking control signals $L_1$ and $L_2$, or both, is dependent upon the application of input signals to one or the other of the conductors **251** and **252** of the pairs of decoder conductors associated with the segment or stroke generators. The selective coupling of the character input conductors **55–1** through **55–N** and conductors **51** and **52** by diodes **237** through **248** establishes the level of unblanking to be effected upon the visual indicator in a display system. Four decoded unblanking control signal indications that may be obtained from the use of a pair of unblanking decoder conductors associated with each stroke generator as shown in FIGURE 2 are as follows:

No diode connection between a character input conductor and a pair of decoder conductors **251** and **252**, as at the second stroke generator and the SYMBOL **2** conductor, results in the application of the first unblanking control signal $L_1$ to the display means via conductor **76** at the appropriate stroke time due to inversion performed by AND gate **270** in the $L_1$ circuit.

A diode connection between a character input conductor and a decoder conductor **251**, as effected by diodes **237–2**, **239–1** and **247–*n***, is effective to remove the $L_1$ unblanking signal from output conductor **76** at the appropriate stroke time which signifies that the display beam or visual indicator is to be blanked so as not to be visible.

The connection of a diode between a character input conductor and one of unblanking decoder conductors **252** such as diode **238–1** or **248–1** causes unblanking control signal $L_2$ to be developed on output conductor **77** at the same time as the associated unblanking control signal $L_1$ appears on output conductor **76**.

The diode coupling of a character input conductor to both decoder conductors **251** and **252** of one of the segment or stroke generators, as by diodes **247–2** and **248–2**, opens AND gate **277**, the inverted output of which signals the end of a character and forward biases diodes **281** and **282** which prevents the outputting of either unblanking control signal.

The above-described unblanking control signal decoding arrangement utilizes a minimum of decoding diodes since the most frequently utilized unblanking control signal $L_1$ is supplied to the display means automatically at each stroke time unless a diode is connected between the energized character input conductor and the decoder conductors **251** associated with the stroke generators. Of course, many other decoding schemes and arrangements may be employed for deriving the unblanking control signals in the unblanking control signal matrix and decoder of the invention.

It is noted that any number of additional conductors may be added to the pairs of decoder conductors **251** and **252** associated with the stroke generators of the matrix symbol generator of FIGURE 2 if additional unblanking control signals are desired. It is also noted that any of several well-known digital-to-analog converters may be electrically connected to the output conductors of the unblanking control signal decoder of the subject invention if it is desired to generate different levels of an unblanking control signal rather than different signals indicative of different levels of unblanking for application to a display device.

If it is desired to implement the unblanking control decoder matrix and associated gates of the invention with miniaturized circuit means such as integrated circuits or so-called micrologic circuitry, it may be desirable to connect current-limiting resistors between the unblanking decoder conductors **251** and **252** and inverters **253** and **254**. Also, if current signal AND gates such as certain types of semiconductor AND gates are employed for implementing AND gates **255** and **256**, it may be desirable or necessary to connect the outputs of AND gates **255** to the input terminals of an active OR gate (not shown), connecting the output terminal thereof to an input terminal of the AND gate **270**, and to connect the outputs of AND gates **256** to input terminals of a second active OR gate (not shown), the output terminal thereof being connected to the first end of resistor **259**.

FIGURE 3 presents both ideal and rounded illustrations of line segment-approximated alphanumeric characters and symbols displayed from electrical signals which may be produced by a matrix type symbol generator of the type shown in FIGURE 2. The rounded symbol representations illustrate the deleterious effects upon symbol distinctiveness which results from the inability of deflection amplifiers to cause the associated display indicator to illustrate or display accurately the corners or vertices of characters and symbols written at high frequencies, or from irregular transitions between the timing of the successive line segments, or both. Irregularity in the time intervals provided for the writing or display of different line segments will also make the segments nonuniform in length and may prevent completion of character configurations such as the closing of the character "6" upon itself as illustrated at **300** in FIGURE 3. These rounded and possibly incomplete character and symbol representations result if no compensating measure is taken such as momentary stroke inhibition of each of the segment or stroke signals. If however, inhibit input pulses are applied to the stroke inhibition circuit including input terminal **58**, conductors **290–X** and **290–Y**, and diodes **291–1** through **291–*n*** and diodes **295–1** through **295–*n***, the character and symbol displays developed in a visual display system in which the generator is connected will approach the ideal configurations shown.

This momentary initial inhibition or interruption of the generation of stroke signals provides a period of time for transition between successive line segment signals and allows the deflection amplifier to complete the display of each segment before having applied thereto a successive stroke or segment signal, and, therfore, to more accurately represent the corners or vertices of the characters and symbols. The effects of momentary inhibition of each stroke or segment signal is to permit the charge, and consequently the potential, on storage capacitors **212** and **224** to remain at a level established by the preceding stroke for an initial period of time. This short delay in the application of strokes to the display device allows the display amplifiers utilized to "catch up" to the segment symbol and thus compensate for limitations in the frequency response thereof. This application of momentary stroke inhibit pulses to the symbol generator apparatus may be accomplished by the use of inhibit pulse generator **63** connected to receive clock pulses and to provide the desired inhibit pulse for the initial portion of the clock pulse periods as in FIGURE 1.

In FIGURE 4 are illustrated pictorial representations of ideal numerical symbols formed of segments of uniform intensity and of the same symbols formed of segments of variable intensity resulting from variable writing speeds in the display thereof. This variation in the intensity of the line segments forming the displayed characters or symbols occurs if line segments of different lengths are written in uniform periods of time by matrix symbol generators of the type illustrated in FIGURE 2 if no compensation is provided therefor and the display beam or indicator is uniformly unblanked for each stroke or line segment. There are four different line segment intensities corresponding to different line segment lengths

illustrated in the numerical symbols displayed in FIGURE 4. The longest line segment and hence the least bright is representative line segment **305**, the diagonal of a rectangle having sides of two units each with different aspect ratios for horizontal and vertical components appearing in the **3** symbol and the next shortest and next brightest line segments are representative horizontal and vertical line segments **303** of two units length as illustrated in the **2** and **5** symbols. The lines of four units length appearing in the **2**, **3** and **5** symbols are formed of two, 2-unit line segments. In the character format devised for the resistor matrix symbol generator of FIGURE 2 there is another different line segment length (not shown) of correspondingly different intensity intermediate between representative line segments **305** and **303** which appears in symbols A, B and D as the diagonal of a rectangle having two sides of one unit and two sides of two units as may be seen in FIGURE 5 of the above-identified Yanishevsky patent application, Ser. No. 553,362.

Also illustrated in the representative numerical symbol displays of FIGURE 4 herein are shorter and bright line segments **302** which are the diagonal of a rectangle formed of a 1 unit ordinate and 1 unit abscissa and still shorter and brighter representative line segments **301** which are one unit in length either horizontally or vertically, being the most slowly written line segment of all those illustrated in this figure.

The deleterious effect of this variation in the intensity of line segments upon the distinctiveness of displayed symbols can be reduced by the use of the unblanking control matrix and decoder apparatus shown in FIGURE 2 which effects two levels of unblanking of the display means indicator rather than uniform unblanking of the beam or indicator for each stroke or segment regardless of length. The unblanking control matrix and decoder shown in FIGURE 2 only partially unblanks the beam or indicator for any line segment one unit long or the diagonal of a rectangle having sides of one unit X and Y components, which are of the same order of intensity, by supplying unblanking control signal $L_1$ to the display means. The matrix and decoder more fully unblanks the beam or indicator for line segments of two units length, the one unit by two unit diagonals, and the two unit diagonals, which are of the same order of intensity, by supplying both unblanking control signals $L_1$ and $L_2$ to the display means. The beam indicator furthermore, is blanked for any strokes not to be visible as retracing strokes or beam or indicator positioning strokes in preparation for the generation of a succeeding visible line segment in the formation of a character or symbol.

The fourth decoded combination in the apparatus of FIGURE 2 indicates an end of character or symbol signal which is developed upon the generation of the last line segment signal thereof and which, by rendering diodes **281** and **282** of FIGURE 2 conducting, prevents the subsequent output of either unblanking signal to the display means. The diodes **247–2** and **248–2** of FIGURE 2 illustrate decoding of the end of character symbols. Each succeeding stroke generator may be provided with a diode such as diode **247–*n*** in FIGURE 2 for blanking successive stroke signals, or the enabling ripple generator may be reset thereupon, or blanking diodes such as diode **247–*n*** may be used as well as resetting the ripple generator upon generation of the end of character signal.

Of course, any number of unblanking signals may be generated by the unblanking control matrix and decoder of the subject invention by utilizing additional decoding conductors with each stroke generator. The addition of one more conductor to the pairs of conductors **251** and **252** shown in FIGURE 2 permits four more unblanking signals to be generated which would permit full compensation for each of the different line segment lengths and intensities which arise in the character format illustrated in FIGURE 4 of the present application and FIGURE 5 of the above-identified Yanishevsky patent application, Ser. No. 553,362. It is also clear that other decoding schemes and arrangements can be utilized in the apparatus of FIGURE 2 and that additional decoding means would be required if additional decoding conductors are utilized in the unblanking control decoding matrix.

Of course many variations and modifications of the invention are possible in the light of the above teachings, it is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

I claim:

**1.** Impedance matrix symbol generation apparatus comprising:

a plurality of input conductors;

a plurality of variable electric stroke generators each having a plurality of input terminals;

a plurality of first asymmetrically conductive circuit means of preselected impedance values electrically coupling the input terminals of each of the stroke generators to selected ones of said input conductors;

means for storing energy electrically coupled to the output terminals of said stroke generators responsive to the magnitude of the signals received therefrom;

a plurality of sets of unblanking decoder conductors;

a plurality of second asymmetrically conductive circuit means electrically coupling selected ones of the unblanking decoder conductors to the individual input conductors;

unblanking decoder means electrically coupled to the sets of unblanking decoder conductors; and

timing means coupled to each of said electric stroke generators and to said unblanking decoder means for successively enabling operation thereof.

**2.** The impedance matrix stroke generation apparatus of claim **1** wherein the unblanking decoder means further comprises synchronizing gating means electrically coupled to the sets of unblanking decoder conductors and coupled to said timing means for developing unblanking signals in synchronism with the stroke signals, and decoder gating means coupled to the output of said synchronizing gating means.

**3.** The impedance matrix stroke generation apparatus of claim **1** wherein the plurality of second asymmetrically conductive circuit means incorporate substantially unidirectional semiconductor devices and the unblanking decoder means develops signals indicative of a plurality of levels of unblanking and end of character signals.

**4.** The matrix stroke generation apparatus of claim **1** further comprising inhibit gating means electrically coupled to each of said stroke generators for inhibiting operation thereof while receiving an inhibit control signal.

**5.** The matrix stroke generation apparatus of claim **4** wherein the inhibit gating means incorporate third asymmetrically conductive circuit means coupled to said stroke generators and inhibit pulse forming means electrically coupled between said timing means and said third asymmetrically conductive circuit means.

**6.** In resistor matrix symbol generation apparatus having a plurality of input conductors each for receiving a different selection signal, a plurality of variable electric current stroke generators each having at least one output terminal and a plurality of asymmetrically conductive input circuits electrically coupled to selected ones of said input conductors, constant current generating means having an output terminal, and energy storage means electrically coupled to the output terminals of said stroke generators and of said constant current generating means responsive to the combined currents therefrom, the improvement comprising:

a set of unblanking decoder conductors associated with each stroke generator;

asymmetrically conductive circuit means electrically coupling said character input conductors to selected ones of said unblanking decoder conductors;

unblanking decoder means having a plurality of control

means coupled to the unblanking decoder conductors for producing a plurality of different unblanking control signals; and

timing means coupled to each of said electric current stroke generators and to each of said control means for successively enabling operation of corresponding ones of said stroke generators and said control means.

**7.** In resistor matrix stroke generation apparatus, the improvement of claim **6** wherein the control means further comprises synchronizing gating means coupled to said timing means and electrically coupled to the sets of unblanking decoder conductors for developing control signals in synchronism with the stroke signals and wherein the unblanking decoder means further comprises decoder gating means coupled to the outputs of said synchronizing gating means.

**8.** The combination of claim **6** wherein the plurality of asymmetrically conductive circuit means electrically coupling said character input conductors to selected unblanking decoder conductors incorporate substantially unidirectional semiconductor devices and the unblanking decoder means develops a plurality of different signals indicative of a plurality of levels of unblanking and end of character signals.



**9.** The combination of claim **6** further comprising inhibit gate means electrically coupled to each of said stroke generators for inhibiting operation thereof at the beginning of each stroke period.

**10.** The invention of claim **9** wherein the inhibit gating means incorporates second asymmetrically conductive circuit means coupled to said stroke generators and inhibit pulse forming means coupled to said timing means and electrically coupled to said second asymmetrically conductive circuit means.

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JOHN W. CALDWELL, Primary Examiner

M. M. CURTIS, Assistant Examiner

U.S. Cl. X.R.

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