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[54] **BINARY DIVIDER CIRCUIT FOR ELECTRONIC WATCH**

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[30] **Foreign Application Priority Data**

Feb. 10, 1971 Japan 46/5220

[52] **U.S. Cl.** ..... **58/23 A,** 307/223

[51] **Int. Cl.** **G04b 1/00**

[58] **Field of Search** ..... 307/225, 225 C, 223; 58/23 R, 23 A, 23 AC, 23 D, 57, 59, 85.5

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Primary Examiner—Richard B. Wilkinson
Assistant Examiner—U. Weldon
Attorney—Alex Friedman et al.

[57] **ABSTRACT**

A binary divider circuit for an electronic watch including dual OR-NAND gates and two inverters. The watch includes a time standard oscillator which oscillates at a relatively high frequency, a chain of said binary dividers for dividing said high frequency to a low frequency timing signal, and time display devices for displaying time in response to said low frequency timing signal.

3 Claims, 8 Drawing Figures

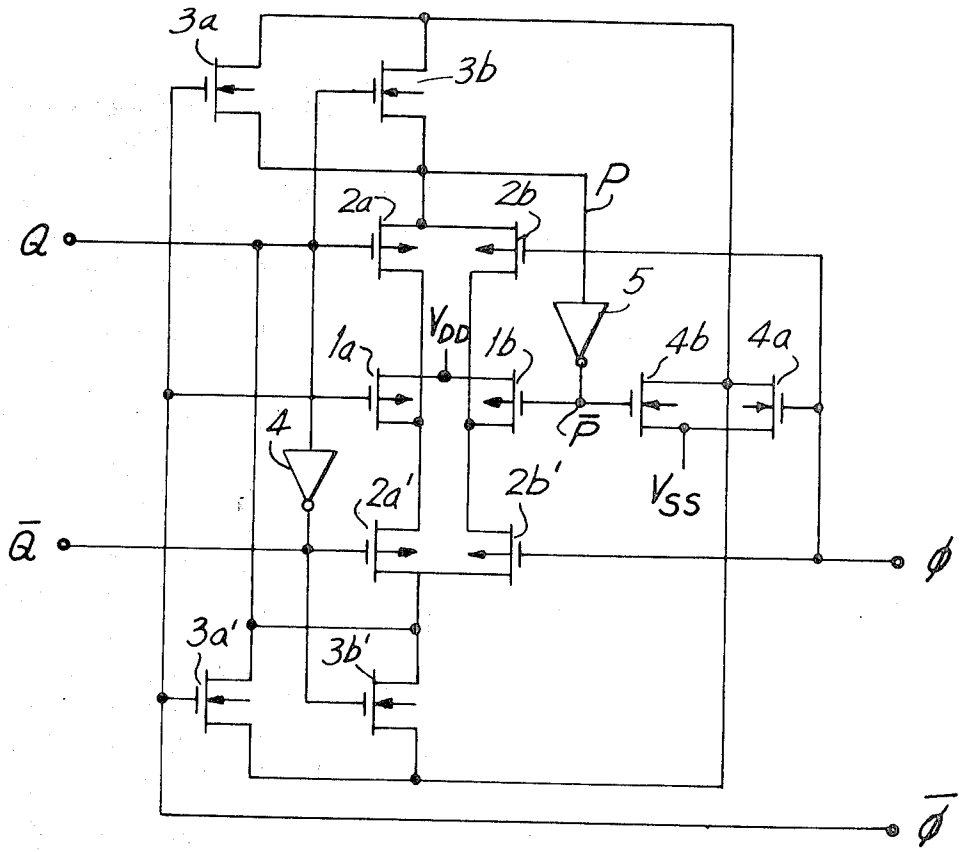


FIG. 1a

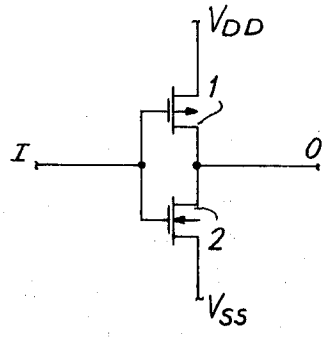


FIG. 1b

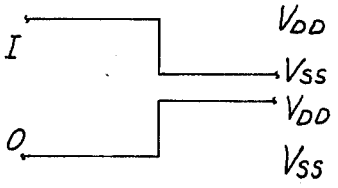


FIG. 1c

CLOCK / LOGIC	ϕ_n	ϕ_{n+1}	ϕ_{n+2}	ϕ_{n+3}	ϕ_{n+4}	ϕ_{n+5}	----
ϕ	0	1	0	1	0	1	----
Q	a	a	$\bar{a}$	$\bar{a}$	a	a	----
P	a	$\bar{a}$	$\bar{a}$	a	a	$\bar{a}$	----

a = 1 OR 0

FIG. 2a

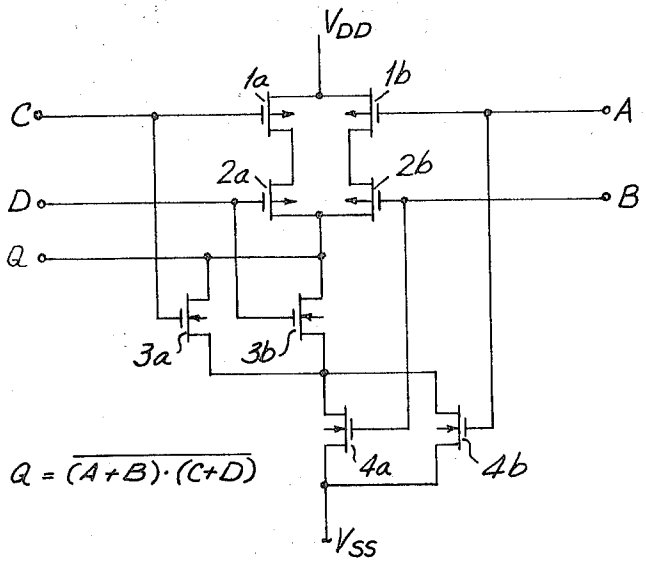


FIG. 2b

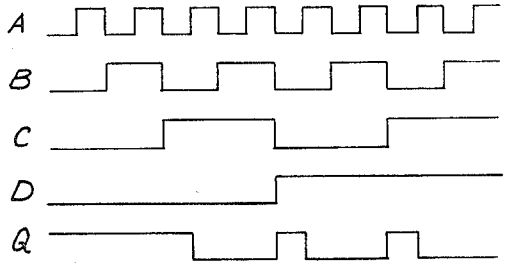


FIG. 3a

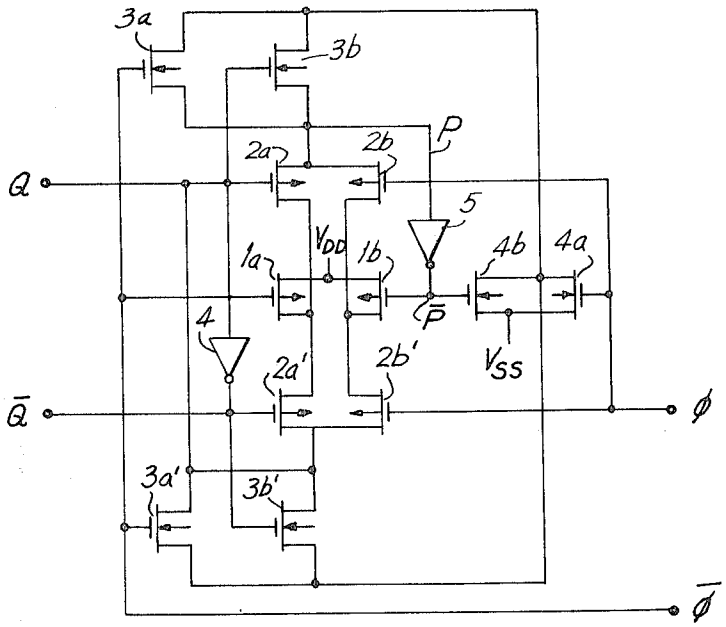
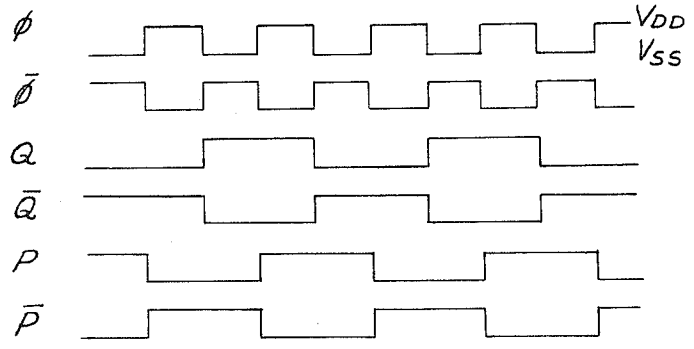

3a
3b
P
2a
2b
Q
5
V_{DD}
1a
1b
4b
4a
$\bar{P}$
4
2a'
2b'
V_{SS}
$\bar{Q}$
ϕ
3a'
3b'
$\bar{\phi}$

FIG. 3b


ϕ
V_{DD}
V_{SS}
$\bar{\phi}$
Q
$\bar{Q}$
P
$\bar{P}$

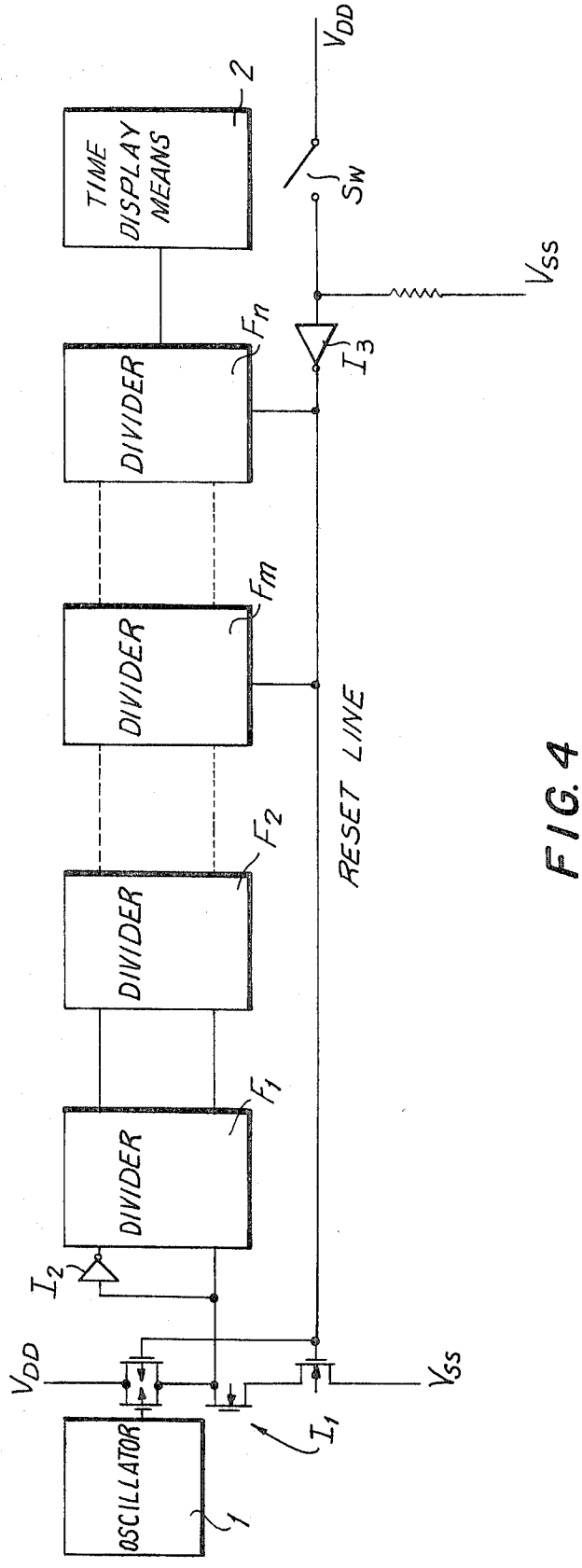

TIME DISPLAY MEANS
2
V_{DD}
SW
V_{SS}
DIVIDER
F_n
I_3
DIVIDER
F_m
DIVIDER
F_2
RESET LINE
DIVIDER
F_1
I_2
V_{DD}
V_{SS}
I_1
OSCILLATOR
1

FIG. 4

BINARY DIVIDER CIRCUIT FOR ELECTRONIC WATCH

BACKGROUND OF THE INVENTION

This invention relates to binary dividers for electronic watches having an oscillator of a relatively high frequency as the time standard. In conventional electronic watches, especially quartz crystal watches, the use of hybrid or bipolar IC precludes the wide distribution of such watches due to high power consumption, large size and high cost. By providing a directly coupled logic binary divider formed of COS/MOS (metal oxide semi-conductors in the complimentary symmetry configuration), the foregoing deficiencies are overcome and it is possible to produce a highly accurate and low-cost wristwatch.

SUMMARY OF THE INVENTION

Generally speaking, in accordance with the invention, an electronic wristwatch is provided having a time standard oscillator for producing a high frequency signal, a plurality of binary divider means connected in a series chain, each of said binary divider means being formed from dual OR-NAND gates and two inverters, said gates and inverters being formed from COS/MOS integrated circuits, and time display means for providing time indication in response to the low frequency signal output of said binary divider chain.

A binary divider may be formed from three pairs of N channel MOS transistors, three pairs of P channel MOS transistors and two COS/MOS inverters.

Accordingly, it is an object of this invention to provide a divider of low power consumption particularly adapted for use in electronic watches.

Still another object of the invention is to provide an electronic wristwatch of small size and low cost by providing a divider formed from a small number of integrated MOS transistors.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

The invention accordingly comprises the features of construction, combinations of elements, and arrangement of parts which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the invention, reference is had to the following description taken in connection with the accompanying drawings, in which:

FIG. 1*a* is a circuit diagram of a COS/MOS inverter;

FIG. 1*b* is a timing chart of the input and output voltage of the circuit of FIG. 1*a*;

FIG. 1*c* is a table illustrating the timing of a binary divider according to the invention;

FIG. 2*a* is a circuit diagram of a COS/MOS OR-NAND gate according to the invention;

FIG. 2*b* is a timing chart of the input and output voltages of the circuit of FIG. 2*a*;

FIG. 3*a* is a binary divider according to the invention;

FIG. 3*b* is a timing chart of the voltages of the circuit of FIG. 3*a*; and

FIG. 4 is a block diagram of an electronic wristwatch according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1*a*, the COS/MOS inverter depicted consists of a P channel MOS transistor 1 and an N channel MOS transistor 2. As more particularly shown in the timing chart of FIG. 1*b*, an input voltage renders the source-drain path of the N channel MOS transistor conductive to turn said transistor on and renders the source-drain path of the P channel MOS transistor non-conductive to turn said transistor off. A no-voltage input condition turns the P channel MOS transistor on and the N channel MOS transistor off.

The inverter of FIG. 1*a* requires little power during normal operation. Where said inverter is applied to a watch, the voltage V_{DD} would be the voltage of the battery in said watch, and the voltage V_{SS} would be the ground voltage. COS/MOS integrated circuits formed from such inverters require little power.

In a binary divider, the change of logic may be expressed in the following equations:

$$Q_n = \overline{(\overline{P}_{n-1} + \phi_n) \cdot (\overline{Q}_{n-1} + \overline{\phi}_n)} \quad (1)$$

$$P_n = \overline{(\overline{P}_{n-1} + \phi_n) \cdot (Q_{n-1} + \overline{\phi}_n)} \quad (2)$$

where, ϕ_n, $\overline{\phi}_n$ are clock signals at the time $t = n$, and Q_n and P_n are output logic at time $t = n$. If P_{n-1} is a where a may equal 1 or 0, the change in ϕ, Q and P at various points in the clock signal is shown in the table of FIG. 1*c*. From a consideration of said table, it is clear that the clock signal ϕ is divided in half by the divider to provide an output signal Q of a frequency equal to one-half the frequency of the input clock signal ϕ.

Referring now to FIG. 2*a*, one example of an OR-NAND gate formed from COS/MOS transistors is depicted, a timing chart of the input voltages A, B, C and D and the output voltage Q being depicted in FIG. 2b. The OR-NAND gate of FIG. 2a consists of a first pair of P channel MOS transistors 1a and 1b having their respective source electrodes connected to the positive terminal of a battery (V_{DD}) and having their gate electrodes connected to input voltages C and A respectively. A second pair of P channel MOS transistors 2*a* and 2*b* are connected with their respective source electrodes connected respectively to the drain electrodes of P channel MOS transistors 1*a* and 1*b*. The gates of P channel MOS transistors 2*a* and 2*b* are respectively connected to receive input voltages D and B. The drain electrodes of P channel MOS transistors 2*a* and 2*b* are connected in common. A first pair of N channel MOS transistors 3*a* and 3*b* are provided having their respective drain electrodes connected to the commonly connected drains of second P channel MOS transistors 2*a* and 2*b*. The source electrodes of said first pair of N channel MOS transistors are connected in common.

A second pair of N channel MOS transistors 4*a* and 4*b* are provided with their drain electrodes connected in common to the common connection of the source electrodes of first N channel MOS transistors 3*a* and 3*b*. The source electrodes of second N channel MOS transistors 4*a* and 4*b* are connected in common to ground (V_{SS}). The gate electrodes of first N channel MOS transistors 3*a* and 3*b* are respectively connected to inputs C and D while the gate electrodes of second

N channel MOS transistors 4*a* and 4*b* are respectively connected to inputs B and A.

Referring now to FIG. 3a, the binary divider circuit according to the invention is depicted. The divider is formed from a pair of OR-NAND gates such as the OR-NAND gate depicted in FIG. 2*a*. In said divider circuit, ϕ and ϕ are input terminals, Q and Q are output terminals. The output signals on said output terminals define the clock signals utilized to drive the next divider stage. A timing chart of the voltages of the binary divider of FIG. 3*a* is depicted in FIG. 3*b*. The divider is formed from a minimum number of MOS transistors. The divider is particularly effective in quartz crystal watches which require a minimum of size and power consumption.

In order to permit a better understanding of the circuit of FIG. 3*a*, reference numerals corresponding to the reference numerals assigned to the components of the OR-NAND gate of FIG. 2*a* have been assigned to the components of the divider of FIG. 3*a*. Said divider incorporates all of the components of two OR-NAND gates except that first P channel MOS transistors 1*a* and 1*b* and second N channel MOS transistors 4*a* and 4*b* are utilized for both OR-NAND gates. In other words, only one set of said first P channel and said second N channel MOS transistors is provided. The input ϕ is applied to the gate electrodes of the two second P channel MOS transistors 2*b*, 2*b'* and second N channel MOS transistor 4*a*. The input ϕ is applied to the gate electrodes of the two first N channel MOS transistors 3*a*, 3*a'* and the first P channel MOS transistor 1*a*. The output Q is taken between the drain electrodes of one of the second P channel MOS transistors 2*a'* of one of the OR-NAND gates and the drain electrode of the associated first N channel MOS transistor 3*a'*. Said output is applied as an input directly to the gate electrodes of first N channel MOS transistor 3*b* and second P channel MOS transistor 2*a* of the other OR-NAND gate, and indirectly through inverter 4 as an input to the gate electrodes of second P channel MOS transistor 2*a'* and first N channel MOS transistor 3*b'* of the OR-NAND gate from which said output was obtained. The output Q is obtained from the output of inverter 4. The output of said other OR-NAND gate is taken at point P between the drain electrodes of first N channel MOS transistor 3*b* and second P channal MOS transistor 2*a* thereof. The output at point P is applied to inverter 5 as the input at point P, to the gate electrodes of first P channel MOS transistor 1*b* and second N channel MOS transistor 4*b*.

Referring now to FIG. 4, a block diagram of a quartz crystal watch according to the invention is depicted. Said watch includes a binary divider chain F_1, F_2 . . . , F_m, . . . F_n, each component of which is formed substantially in accordance with FIG. 3*a*. A quartz crystal oscillator 1 produces an output signal with a high frequency in the range of several kHz — several tens kHz. The clock signals of the first binary divider F_1 are shaped by NAND gate I_1 and inverter I_2, the output of oscillator 1 being applied as the input to said NAND gate. When the binary divider chain is reset by a signal along the reset line, NAND gate I_1 is turned off to reduce the power consumption of the arrangement. Inverter I_3 is connected in the reset line to apply a reset signal to the divider circuits F_m, . . . F_n, when the switch SW is closed. The output of the divider chain is applied to a time display means 2 which includes a pulse motor, a gear train and a dial.

The circuit according to the invention permits the production of an electronic watch, such as a wristwatch, incorporating a relatively high frequency oscillator but requiring only a minimum of power due to the use of COS/MOS binary counters formed from a minmum number of MOS transistors.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above constructions without departing from the spirit and scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting manner.

It is also to be understood that the follwing claims are intended to cover all of the generic and specific features of the invention which, as a matter of language, might be said to fall therebetween.

What is claimed is:

1. An electronic watch comprising time standard oscillator means for producing a high frequency signal; a binary divider chain means connected to said oscillator means for receiving said high frequency signal and for dividing said high frequency signal into low frequency timing signals, said divider chain means including at least one binary divider formed from dual OR-NAND gates and first and second inverter means formed from COS/MOS integrated circuits, each said OR-NAND gate including a source of voltage; a ground; a pair of first P channel MOS transistors (1*a*, 1*b*) having their respective source electrodes connected in common to said source of voltage; a pair of second P channel MOS transistors (2*a*, 2*b*) having their respective source electrodes connected respectively to the drain electrodes of said pair of first P channel MOS transistors (1*a*, 1*b*); a pair of first N channel MOS transistors (3*a*, 3*b*) having their respective drain electrodes connected together and connected to a common connection of the respective drain electrodes of said pair of second P channel MOS transistors (2*a*, 2*b*); and a pair of second N channel MOS transistors (4*a*, 4*b*) having their respective drain electrodes connected together and to the common connection of the source electrodes of said pair of first N channel MOS transistors (3*a*, 3*b*), the respective source electrodes of said pair of second N channel MOS transistors being connected together to said ground, the gate electrodes of one of said second P channel MOS transistors (2*a*) and one of said first N channel MOS transistors (3*b*) being connected together to define a first input, the gate electrodes of one of said first P channel MOS transistors (1*a*) and the other of said first N channel MOS transistors (3*a*) being connected together to define a second input, the gate electrodes of the other of said first P channel MOS transistors (1*b*) and one of said second N channel MOS transistors (4*b*) being connected together to define a third input, the gate electrodes of the other of said second P channel MOS transistors (2*b*) and the other of said second N channel MOS transistors (4*a*) being connected together to define a fourth input, the common connection between the respective drain electrodes of the pair of first N channel MOS transistors (3*a*, 3*b*) and the pair of second P channel MOS transistors (2*a*, 2*b*) defining an output terminal, said dual OR-NAND gates

including two of said OR-NAND gates, a single pair of said first P channel MOS transistors (1*a*, 1*b*) and a single pair of said second N channel MOS transistors (4*a*, 4*b*) being incorporated in both of said OR-NAND gates, a first divider input being defined by the common connection of the fourth inputs of both of said OR-NAND gates, a second divider input being defined by the common connection of both of said second inputs of said OR-NAND gates, the output terminal of one of said OR-NAND gates being connected through said first inverter means to the common connection defining the third inputs of both of said OR-NAND gates, the output terminal of the other of said OR-NAND gates defining a divider output terminal and being connected directly to the first input of said one of said OR-NAND gates and being connected through said second inverter means to the first input of said other of said OR-NAND gates.

2. An electronic watch as recited in claim **1** wherein said oscillator means is a quartz crystal oscillator.

3. An electronic watch as recited in claim **2**, including an input inverter means connected intermediate said oscillator means and said divider chain means; and reset means connected to at least a portion of the divider means of said divider chain means for resetting same, and connected to said input inverter means, said input inverter means being disposed in an off state when said portion of said divider means coupled to said reset means is reset.

* * * * *