(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 November 2016 (10.11.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/179598 A1

(51) **International Patent Classification**:
H01L 29/78 (2006.01)

(21) **International Application Number**:
PCT/US2016/031517

(22) **International Filing Date**:
9 May 2016 (09.05.2016)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
14/706,927 7 May 2015 (07.05.2015) US

(63) **Related by continuation (CON) or continuation-in-part (CIP) to earlier application**:
US 14/706,927 (CON)
Filed on 7 May 2015 (07.05.2015)

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) **Title**: MULTIPLE SHIELDING TRENCH GATE FET

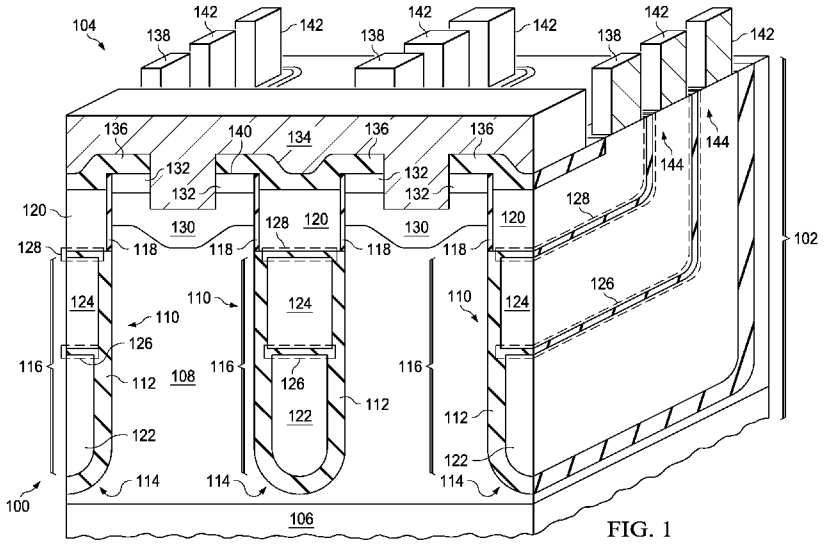

FIG. 1

(57) **Abstract**: In described examples, a semiconductor device (100) contains a vertical MOS transistor (104) having a trench gate (120) in trenches (110) extending through a vertical drift region (108) to a drain region (106). The trenches (110) have field plates (116) under the gate (120). The field plates (116) are adjacent to the drift region (108) and have multiple segments (122) and (124). A dielectric liner (112) in the trenches (110) separating the field plates (116) from the drift region (108) has a thickness greater than a gate dielectric layer (118) between the gate (120) and the body (130). The dielectric liner (112) is thicker on a lower segment (122) of the field plate (116), at a bottom (114) of the trenches (110), than an upper segment (124), immediately under the gate (120).

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

MULTIPLE SHIELDING TRENCH GATE FET

[0001] This relates generally to semiconductor devices, and more particularly to vertical MOS transistors in semiconductor devices.

BACKGROUND

[0002] A vertical metal oxide semiconductor (MOS) transistor with a trench gate in trenches has the gate dielectric layer and gate extending down the trenches past the body, abutting a vertical drift region under the body. The trenches have to be deeper than desired to support a desired operating voltage, because the gate dielectric layer cannot support a high electric field in the drift region. If the thickness of the gate dielectric layer is increased, it undesirably increases the resistance of the channel region in the on state.

SUMMARY

[0003] In described examples, a semiconductor device contains a vertical MOS transistor having a trench gate in trenches. The trenches extend into a substrate of the semiconductor device past a body of the vertical MOS transistor, abutting a drift region of the vertical MOS transistor under the body. The trenches have field plates under the gate. The field plates are adjacent to the drift region and have multiple segments. A dielectric liner in the trenches separating the field plates from the drift region has a thickness greater than a gate dielectric layer between the gate and the body. The dielectric liner is thicker on a lower segment of the field plate, at a bottom of the trenches, than an upper segment, immediately under the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example semiconductor device containing a vertical n-channel MOS transistor.

[0005] FIG. 2A through FIG. 2K are cross sections of the semiconductor device of FIG. 1, depicted in successive stages of fabrication.

[0006] FIG. 3 is a cross section of another example semiconductor device containing a vertical n-channel MOS transistor.

[0007] FIG. 4A through FIG. 4E are cross sections of the semiconductor device of FIG. 3, depicted in successive stages of fabrication.

[0008] FIG. 5 is a cross section of an example semiconductor device containing a vertical p-channel MOS transistor.

[0009] FIG. 6A through FIG. 6H are cross sections of the semiconductor device of FIG. 5, depicted in successive stages of fabrication.

[0010] FIG. 7 is a cross section of another example semiconductor device containing a vertical n-channel MOS transistor.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] The figures are not drawn to scale. Some acts may occur in different orders and/or concurrently with other acts or events. Not all illustrated acts or events are required to implement a methodology in accordance with example embodiments.

[0012] A semiconductor device contains a vertical MOS transistor having trenches that extend into a substrate of the semiconductor device. A drain region of the vertical MOS transistor is disposed in the substrate at, or below, bottoms of the trenches. A drift region is disposed in the substrate above the drain region and between the trenches. A body of the vertical MOS transistor is disposed in the substrate, above the drift region and abutting the trenches. A source of the vertical MOS transistor is disposed above the body. A gate of the vertical MOS transistor is disposed in the trenches adjacent to the body, separated from the body by a gate dielectric layer. A field plate with multiple segments is disposed in the trenches below the gate, separated from the drift region by a dielectric liner on sidewalls of the trenches. The dielectric liner is thicker on a lower segment of the field plate, at a bottom of the trenches, than an upper segment, immediately under the gate. The field plate segments may be connected to each other or may be electrically isolated from each other. The upper field plate segment may be connected to the gate or may be electrically isolated from the gate. The vertical MOS transistor may be an n-channel MOS transistor or a p-channel MOS transistor.

[0013] For the purposes of this description, the term "RESURF" refers to a material that reduces an electric field in an adjacent semiconductor region. For example, a RESURF region may be a semiconductor region with an opposite conductivity type from the adjacent semiconductor region. RESURF structures are described in Appels, et al., "Thin Layer High Voltage Devices" Philips J, Res. 35 1-13, 1980.

[0014] FIG. 1 is a cross section of an example semiconductor device containing a vertical n-channel MOS transistor. The semiconductor device 100 is formed on a substrate 102, which

includes a semiconductor material. The n-channel vertical MOS transistor 104, referred to herein as the transistor 104, may be the only active component of the semiconductor device 100 or may be one of multiple active devices in the semiconductor device 100. The transistor 104 includes an n-type drain region 106 disposed in the substrate 102 below an n-type vertical drift region 108.

[0015] The semiconductor device 100 includes trenches 110, which extend vertically through the vertical drift region 108 proximate to the drain region 106 as depicted in FIG. 1, or possibly into the drain region 106. The trenches 110 contain a dielectric liner 112 on sidewalls of the trenches 110 extending to bottoms 114 of the trenches 110 and abutting the substrate 102, and multiple field plate segments 116 on the dielectric liner 112. The trenches 110 further contain a gate dielectric layer 118 above the dielectric liner 112 abutting the substrate 102, and a trench gate 120 of the transistor 104 contacting the gate dielectric layer 118. In this example, the field plate segments 116 include respective lower field plate segments 122 on the respective dielectric liners 112 at the bottoms 114 of the trenches 110, and respective upper field plate segments 124 disposed above the respective lower field plate segments 122. The field plate segments 116 and the trench gate 120 may include primarily polycrystalline silicon, referred to as polysilicon. The dielectric liner 112 may include primarily silicon dioxide. The dielectric liner 112 separates the lower field plate segment 122 and the upper field plate segment 124 from the substrate 102. The dielectric liner 112 disposed on the sidewalls of the trenches 110 between the lower field plate segment 122 and the substrate 102 is thicker than the dielectric liner 112 disposed on the sidewalls of the trenches 110 between the upper field plate segment 124 and the substrate 102. The dielectric liner 112 disposed on the sidewalls of the trenches 110 between the upper field plate segment 124 and the substrate 102 is thicker than the gate dielectric layer 118 disposed on the sidewalls of the trenches 110 between the trench gate 120 and the substrate 102. For example, in a version of this example in which the transistor 104 is designed to operate up to 250 volts, the dielectric liner 112 disposed on the sidewalls of the trenches 110 between the lower field plate segment 122 and the substrate 102 may be 900 nanometers to 1000 nanometers thick, and the dielectric liner 112 disposed on the sidewalls of the trenches 110 between the upper field plate segment 124 and the substrate 102 may be 300 nanometers to 400 nanometers thick.

[0016] In this example, the lower field plate segment 122 is electrically isolated from the upper field plate segment 124 by a first isolation layer 126, disposed between the lower field plate

segment 122 and the upper field plate segment 124. Also in this example, the upper field plate segment 124 is electrically isolated from the trench gate 120 by a second isolation layer 128, disposed between the upper field plate segment 124 and the trench gate 120. The first isolation layer 126 and the second isolation layer 128 include dielectric material such as silicon dioxide, and may have a similar composition as the dielectric liner 112.

[0017] The transistor 104 includes a p-type body 130 in the substrate 102 above the vertical drift region 108, abutting the gate dielectric layer 118. The transistor 104 further includes an n-type source 132 above the body 130 and abutting the gate dielectric layer 118. The trench gate 120 is partially coextensive with the vertical drift region 108 and the source 132. A source electrode 134 is disposed over the substrate 102 making electrical contact to the source 132 and the body 130. The source electrode 134 is electrically isolated from the trench gate 120 by a dielectric cap layer 136 over the trench gate 120.

[0018] In a version of this example, in which the transistor 104 is designed to operate up to 250 volts, the trenches 110 may be 13 microns to 17 microns deep and 2.5 microns to 2.8 microns wide. The vertical drift region 108 may be 0.5 microns to 3 microns wide, that is, between adjacent trenches 110, and have an average doping density of 1.4×10^{16} cm^{-3} to 1.6×10^{16} cm^{-3}.

[0019] Electrical connection to the trench gate 120 may be made through gate contacts 138 on exposed areas of the gate at a top surface 140 of the substrate 102. Electrical connections to the field plate segments 116 may be made through field plate contacts 142 on field plate risers 144, which extend from the field plate segments 116 up to the top surface 140 of the substrate 102. Other structures for making electrical connections to the field plate segments 116 are within the scope of this example.

[0020] During operation of the semiconductor device 100, the trench gate 120 being disposed in the trenches 110 advantageously provides a higher on-state current in the area of the top surface 140 occupied by the transistor 104 compared to a similar vertical MOS transistor with a planar gate. A combination of the upper field plate segment 124 and the lower field plate segment 122 provide a RESURF configuration to maintain an electric field in the vertical drift region 108 at a desired value with a higher doping density in the vertical drift region 108 compared to a similar vertical MOS transistor with a single field plate. Accordingly, by forming the vertical MOS transistor 104 with the combination of the upper field plate segment 124 and

the lower field plate segment 122, the transistor 104 is enabled to have shallower trenches 110 than the similar vertical MOS transistor with a single field plate, advantageously reducing a fabrication cost of the semiconductor device 100. Forming the lower field plate segment 122, the upper field plate segment 124 and the trench gate 120 to be electrically isolated from each other may advantageously enable biasing the lower field plate segment 122 and the upper field plate segment 124 independently to increase current density in the transistor 104.

[0021] FIG. 2A through FIG. 2K are cross sections of the semiconductor device of FIG. 1, depicted in successive stages of fabrication. Referring to FIG. 2A, the semiconductor device 100 is formed on the substrate 102, such as a bulk silicon wafer or a silicon wafer with an epitaxial layer extending to the top surface 140. Other semiconductor materials in the substrate 102 are within the scope of this example. The drain region 106 is formed in the substrate 102 to have a doping density greater than 1×10^{20} cm^{-3}. For example, the drain region 106 may be formed by implanting n-type dopants such as antimony and possibly arsenic into the substrate 102, followed by an anneal and epitaxial growth of n-type semiconductor material over the implanted n-type dopants, so that the epitaxial layer provides the vertical drift region 108. N-type dopants such as phosphorus in the vertical drift region 108 may be incorporated during epitaxial growth or may be implanted later, followed by a thermal drive to diffuse and activate the implanted dopants.

[0022] A hard mask 146 is formed over the substrate 102, which exposes areas for the trenches 110. The hard mask 146 may be several hundred nanometers of silicon dioxide, and may be patterned by etching through a photoresist mask. The trenches 110 are formed by removing material from the substrate 102 in the areas exposed by the hard mask 146. The material may be removed from the substrate 102 by a timed reactive ion etch (RIE) process to attain a desired depth of the trenches 110.

[0023] Referring to FIG. 2B, the dielectric liner 112 abutting the lower field plate segment 122 of FIG. 1 may be formed as a combined layer of a thermal oxide layer 148 and a first deposited silicon dioxide layer 150. The thermal oxide layer 148 is formed at sidewalls and bottoms 114 of the trenches 110. The thermal oxide layer 148 may be 50 nanometers to 200 nanometers thick. The first deposited silicon dioxide layer 150 is formed on the thermal oxide layer 148. The first deposited silicon dioxide layer 150 may be 200 nanometers to 400 nanometers thick, and may be formed by a sub-atmospheric chemical vapor deposition (SACVD) process using dichlorosilane and oxygen. Alternatively, the first deposited silicon dioxide layer 150 may be formed by a

plasma enhanced chemical vapor deposition (PECVD) process using tetraethyl orthosilicate, also known as tetraethoxysilane or TEOS. The first deposited silicon dioxide layer 150 may be subsequently densified in an anneal step. Other layer structures and other processes for the dielectric liner 112 are within the scope of this example.

[0024] A first polysilicon layer 152 is formed on the dielectric liner 112 and extending over the top surface 140 of the substrate 102. For example, the first polysilicon layer 152 may be 500 nanometers to 700 nanometers thick over the top surface 140. Also, for example, the first polysilicon layer 152 may be doped with phosphorus, during formation to have an average doping density of 1×10^{18} cm^{-3} to 5×10^{18} cm^{-3}. Alternatively, the first polysilicon layer 152 may be doped by ion implanting dopants, such as phosphorus, at a dose of 1×10^{14} cm^{-2} to 5×10^{15} cm^{-2}, and subsequent annealed at 900 °C to 1000 °C for 10 to 60 minutes.

[0025] Referring to FIG. 2C, a blanket etchback process removes polysilicon from the first polysilicon layer 152 of FIG. 2B over the top surface 140 and in the trenches 110, leaving polysilicon in the lower portions of the trenches 110 to form the lower field plate segment 122. For example, the blanket etchback may be performed using a timed plasma etch including fluorine radicals and/or a timed wet etch using choline, ammonium hydroxide or tetramethyl ammonium hydroxide. The blanket etchback may be performed in one or more etch steps. In one version of this example, the blanket etchback does not remove a significant amount of the dielectric liner 112.

[0026] Referring to FIG. 2D, a first blanket oxide etchback process removes at least portion, and possibly all, of the first deposited silicon dioxide layer 150 from over the top surface 140 of the substrate 102 and from the trenches 110 above the lower field plate segment 122. The lower field plate segment 122 prevents removal of the first deposited silicon dioxide layer 150 from the trenches 110 below a top of the lower field plate segment 122. A majority, and possibly all, of the thermal oxide layer 148 remains on sidewalls of the trenches 110 after the first blanket oxide etchback process is completed. For example, the first blanket oxide etchback process may include a timed wet etch using a buffered hydrofluoric acid solution. An example buffered hydrofluoric acid solution is 10 parts of 40 percent ammonium fluoride in deionized water and 1 part of 49 percent hydrofluoric acid in deionized water; this buffered hydrofluoric acid exhibits an etch rate of densified SACVD silicon dioxide that is more than twice an etch rate of thermal oxide.

[0027] Referring to FIG. 2E, a second deposited silicon dioxide layer 154 is formed over the thermal oxide layer 148 in the trenches 110 and over the lower field plate segment 122. For example, the second deposited silicon dioxide layer 154 may be 160 nanometers to 280 nanometers thick, and may be formed by an SACVD process or a PECVD process. The second deposited silicon dioxide layer 154 may be subsequently densified in an anneal step. The second deposited silicon dioxide layer 154 combined with the thermal oxide layer 148 provide the dielectric liner 112 abutting the upper field plate segment 124 of FIG. 1. A portion of the second deposited silicon dioxide layer 154 on the lower field plate segment 122 provides the first isolation layer 126.

[0028] Referring to FIG. 2F, a second polysilicon layer is formed on the dielectric liner 112 in the trenches 110 and over the top surface 140 of the substrate 102, such as described in reference to FIG. 2B. A subsequent etchback process removes the polysilicon from over the top surface 140 and from a top portion of the trenches 110, leaving polysilicon on the second deposited silicon dioxide layer 154 to form the upper field plate segment 124. The etchback process may be a timed plasma etch and/or a timed wet etch, such as described in reference to FIG. 2C. In this example, the upper field plate segment 124 is electrically isolated from the lower field plate segment 122 by the second deposited silicon dioxide layer 154.

[0029] Referring to FIG. 2G, a second blanket oxide etchback process removes the second deposited silicon dioxide layer 154 and the thermal oxide layer 148 from over the top surface 140 of the substrate 102 and from the trenches 110 above the upper field plate segment 124. The upper field plate segment 124 prevents removal of the second deposited silicon dioxide layer 154 from the trenches 110 below a top of the upper field plate segment 124. A portion of the hard mask 146 may be removed by the second blanket oxide etchback process, as depicted in FIG. 2G. The second blanket oxide etchback process may be performed so that substantially no semiconductor material is removed from the substrate 102.

[0030] Referring to FIG. 2H, the gate dielectric layer 118 is formed on sidewalls of the trenches 110 above the upper field plate segment 124, and the second isolation layer 128 are concurrently formed on the upper field plate segment 124. The gate dielectric layer 118 and the second isolation layer 128 may be formed by thermal oxidation, or a combination of thermal oxidation and deposition of dielectric material. Removing the thermal oxide layer 148 to expose the sidewalls of the trenches 110 advantageously improves process control of a thickness of the

gate dielectric layer 118.

[0031] Referring to FIG. 2I, a third layer pf polysilicon 156 is formed contacting the gate dielectric layer 118 and over the top surface 140 of the substrate 102. The third layer of polysilicon 156 may be doped with n-type dopants during formation, or may be subsequently implanted with n-type dopants, followed by an anneal.

[0032] Referring to FIG. 2J, a blanket etchback process removes polysilicon from the third layer pf polysilicon 156 of FIG. 2I from over the top surface 140 of the substrate 102 to leave polysilicon contacting the gate dielectric layer 118 to form the trench gate 120 of the transistor 104. In this example, the trench gate 120 is electrically isolated from the upper field plate segment 124 by the second isolation layer 128.

[0033] Referring to FIG. 2K, the body 130 is formed by implanting p-type dopants such as boron into the substrate 102 above the vertical drift region 108. The trench gate 120 may optionally be covered by an implant mask while the p-type dopants are implanted, to prevent counterdoping the trench gate 120. The source 132 is formed by implanting n-type dopants such as phosphorus and arsenic into the substrate 102 above the body 130. The substrate 102 is subsequently annealed to activate the implanted dopants. The body 130 and source 132 extend across the substrate 102 between adjacent trenches 110. After the body 130 and the source 132 are formed, the cap layer 136 is formed by deposition of silicon dioxide and optionally a sub-layer of silicon nitride. The cap layer 136 may be formed by a PECVD process using TEOS. After the cap layer 136 is formed, source contact opening are formed through the cap layer 136 and through the source 132 into the body 130. Additional p-type dopants may be implanted into the body 130 where exposed by the source contact openings, which provides the downward bulge in the body depicted in FIG. 1. The source electrode 134 of FIG. 1 is subsequently formed, and further fabrication provides the structure of FIG. 1.

[0034] FIG. 3 is a cross section of another example semiconductor device containing a vertical n-channel MOS transistor. The semiconductor device 300 is formed on a substrate 302, which includes a semiconductor material. The n-channel vertical MOS transistor 304, referred to herein as the transistor 304, includes an n-type drain region 306 disposed in the substrate 302 below an n-type vertical drift region 308.

[0035] The semiconductor device 300 includes trenches 310, which extend vertically through the vertical drift region 308 proximate to the drain region 306, or possibly into the drain region

306. The trenches 310 contain a dielectric liner 312 extending to bottoms 314 of the trenches 310 and abutting the substrate 302, and multiple field plate segments 316 on the dielectric liner 312. The trenches 310 further contain a gate dielectric layer 318 above the dielectric liner 312 abutting the substrate 302, and a trench gate 320 of the transistor 304 contacting the gate dielectric layer 318. In this example, the field plate segments 316 include respective lower field plate segments 322 on the respective dielectric liners 312 at the bottoms 314 of the trenches 310, and respective upper field plate segments 324 disposed above the respective lower field plate segments 322. The field plate segments 316 and the trench gate 320 may include primarily n-type polysilicon. The dielectric liner 312 may include primarily silicon dioxide. The dielectric liner 312 separates the lower field plate segment 322 and the upper field plate segment 324 from the substrate 302. The dielectric liner 312 separating the lower field plate segment 322 from the substrate 302 is thicker than the dielectric liner 312 separating the upper field plate segment 324 from the substrate 302. The dielectric liner 312 disposed on the sidewalls of the trenches 310 between the upper field plate segment 324 and the substrate 302 is thicker than the gate dielectric layer 318 disposed on the sidewalls of the trenches 310 between the trench gate 320 and the substrate 302. For example, in a version of this example in which the transistor 304 is designed to operate up to 40 volts, the dielectric liner 312 disposed on the sidewalls of the trenches 310 between the lower field plate segment 322 and the substrate 302 may be 100 nanometers to 150 nanometers thick, and the dielectric liner 312 disposed on the sidewalls of the trenches 310 between the upper field plate segment 324 and the substrate 302 may be 50 nanometers to 80 nanometers thick.

[0036] In this example, the lower field plate segment 322 is contacting the upper field plate segment 324 in the trenches 310. The upper field plate segment 324 is contacting the trench gate 320 in the trenches 310. A bias voltage applied to the trench gate 320 in this example also biases the upper field plate segment 324 and the lower field plate segment 322 to the same bias voltage.

[0037] The transistor 304 include a p-type body 330 in the substrate 302 above the vertical drift region 308, abutting the gate dielectric layer 318. The transistor 304 further includes an n-type source 332 above the body 330 and abutting the gate dielectric layer 318. The trench gate 320 is partially coextensive with the vertical drift region 308 and the source 332. A source electrode 334 is disposed over the substrate 302 making electrical contact to the source 332 and the body 330. The source electrode 334 is electrically isolated from the trench gate 320 by a

dielectric cap layer 336 over the trench gate 320. Other configurations for the source electrode 334 with respect to the source 332 and body 330 are within the scope of this example.

[0038] In one version of this example, in which the transistor 304 is designed to operate up to 40 volts, the trenches 310 may be 2.2 microns to 2.8 microns deep and 600 nanometers to 700 nanometers wide. The vertical drift region 308 may be 500 nanometers to 1.5 microns wide, that is, between adjacent trenches 310, and have an average doping density of 1.8×10^{16} cm^{-3} to 2.0×10^{16} cm^{-3}.

[0039] Electrical connection to the trench gate 320 may be made through gate contacts 338 on exposed areas of the gate at a top surface 340 of the substrate 302. Other structures for making electrical connections to the trench gate 320 are within the scope of this example. Forming the upper field plate segment 324 to contact the trench gate 320 in the trenches 310, and forming the lower field plate segment 322 to contact the upper field plate segment 324 in the trenches 310, so that electrical connections to the upper field plate segment 324 and the lower field plate segment 322 may be made through the gate contacts 338 may advantageously reduce complexity and fabrication cost of the semiconductor device 300.

[0040] During operation of the semiconductor device 300, the trench gate 320 advantageously provides higher current density as explained in reference to FIG. 1. The field plate segments 316 provide a RESURF configuration to maintain an electric field in the vertical drift region 308 at a desired value, as explained in reference to FIG. 1. Accordingly, by forming the vertical MOS transistor 304 with the combination of the upper field plate segment 324 and the lower field plate segment 322, the transistor 304 is enabled to have shallower trenches 310 than the similar vertical MOS transistor with a single field plate, advantageously reducing a fabrication cost of the semiconductor device 300.

[0041] FIG. 4A through FIG. 4E are cross sections of the semiconductor device of FIG. 3, depicted in successive stages of fabrication. Referring to FIG. 4A, the semiconductor device 300 is formed on the substrate 302. The drain region 306 is formed in the substrate 302 to have a doping density greater than 1×10^{20} cm^{-3}. N-type dopants such as phosphorus in the vertical drift region 308 may be incorporated during epitaxial growth or may be implanted later. A hard mask 346 is formed over the substrate 302, which exposes areas for the trenches 310. The trenches 310 are formed by removing material from the substrate 302 in the areas exposed by the hard mask 346. The drain region 306, hard mask 346 and trenches 310 may be formed as described in

reference to FIG. 2A.

[0042] A thermal oxide layer 348 is formed at sidewalls and bottoms 314 of the trenches 310. In this example, the thermal oxide layer 348 is sufficiently thick to provide the complete dielectric liner 312 disposed on the sidewalls of the trenches 310 between the upper field plate segment 324 of FIG. 3 and the substrate 302, such as 70 nanometers to 80 nanometers thick for an operating voltage of 40 volts. A deposited silicon dioxide layer 350 is formed on the thermal oxide layer 348. The deposited silicon dioxide layer 350 may be 130 nanometers to 170 nanometers thick, formed by an SACVD process or a PECVD process.

[0043] A lower field plate segment 322 is formed in the trenches 310 on the deposited silicon dioxide layer 350, such as described in reference to FIG. 2B and FIG. 2C. The thermal oxide layer 348 combined with the deposited silicon dioxide layer 350 provide the dielectric liner 312 separating the lower field plate segment 322 from the substrate 302.

[0044] A first blanket oxide etchback process removes at least portion, and possibly all, of the deposited silicon dioxide layer 350 from the trenches 310 above the lower field plate segment 322. The lower field plate segment 322 prevents removal of the deposited silicon dioxide layer 350 from the trenches 310 below a top of the lower field plate segment 322. In this example, substantially all of the thermal oxide layer 348 remains on sidewalls of the trenches 310 after the first blanket oxide etchback process is completed. The first blanket oxide etchback process exposes a top of the lower field plate segment 322.

[0045] Referring to FIG. 4B, an upper field plate segment 324 is formed on the thermal oxide layer 348 and on the lower field plate segment 322 in the trenches 310, such as described in reference to FIG. 2F. In this example, the thermal oxide layer 348 provides the dielectric liner 312 separating the upper field plate segment 324 from the substrate 302, which may advantageously reduce fabrication complexity and cost of the semiconductor device 300.

[0046] Referring to FIG. 4C, a second blanket oxide etchback process removes the thermal oxide layer 348 from the trenches 310 above the upper field plate segment 324. The upper field plate segment 324 prevents removal of the thermal oxide layer 348 from the trenches 310 below a top of the upper field plate segment 324. The second blanket oxide etchback process may be performed so that substantially no semiconductor material is removed from the substrate 302.

[0047] The gate dielectric layer 318 is formed on sidewalls of the trenches 310 above the upper field plate segment 324, and dielectric material 358 is concurrently formed on the upper field

plate segment 324. The gate dielectric layer 318 may be formed by thermal oxidation, or a combination of thermal oxidation and deposition of dielectric material. Removing the thermal oxide layer 348 to expose the sidewalls of the trenches 310 advantageously improves process control of a thickness of the gate dielectric layer 318. The dielectric material 358 on the upper field plate segment 324 may be thicker than the gate dielectric layer 318 due to a higher thermal oxide growth rate on polysilicon compared to crystalline silicon.

[0048] Referring to FIG. 4D, an anisotropic etch process such as an RIE process removes the dielectric material 358 of FIG. 4C from the top of the upper field plate segment 324 without significantly degrading the gate dielectric layer 318. In one version of this example, the gate dielectric layer 318 may be protected by a sacrificial layer of polysilicon or silicon nitride, while the dielectric material 358 is removed, after which the sacrificial layer is removed without significantly degrading the gate dielectric layer 318.

[0049] Referring to FIG. 4E, the trench gate 320 is formed contacting the gate dielectric layer 318 and the upper field plate segment 324. The trench gate 320 may be formed as described in reference to FIG. 2I and FIG. 2J. In this example, removing the dielectric material 358 of FIG. 4C from the top of the upper field plate segment 324 enables the trench gate 320 to make electrical contact with the upper field plate segment 324. Further fabrication provides the structure of FIG. 3.

[0050] FIG. 5 is a cross section of an example semiconductor device containing a vertical p-channel MOS transistor. The semiconductor device 500 is formed on a substrate 502, which includes a semiconductor material. The p-channel vertical MOS transistor 504, referred to herein as the transistor 504, includes a p-type drain region 506 disposed in the substrate 502 below a p-type vertical drift region 508.

[0051] The semiconductor device 500 includes trenches 510, which extend vertically through the vertical drift region 508 proximate to the drain region 506, or possibly into the drain region 506. The trenches 510 contain a dielectric liner 512 extending to bottoms 514 of the trenches 510 and abutting the substrate 502, and multiple field plate segments 516 on the dielectric liner 512. The trenches 510 further contain a gate dielectric layer 518 above the dielectric liner 512 abutting the substrate 502, and a trench gate 520 of the transistor 504 contacting the gate dielectric layer 518. In this example, the field plate segments 516 include respective lower field plate segments 522 on the respective dielectric liners 512 at the bottoms 514 of the trenches 510,

and respective upper field plate segments 524 disposed above the respective lower field plate segments 522. The field plate segments 516 and the trench gate 520 may include primarily p-type polysilicon. The dielectric liner 512 may include primarily silicon dioxide. The dielectric liner 512 separates the lower field plate segment 522 and the upper field plate segment 524 from the substrate 502. The dielectric liner 512 separating the lower field plate segment 522 from the substrate 502 is thicker than the dielectric liner 512 separating the upper field plate segment 524 from the substrate 502. The dielectric liner 512 disposed on the sidewalls of the trenches 510 between the upper field plate segment 524 and the substrate 502 is thicker than the gate dielectric layer 518 disposed on the sidewalls of the trenches 510 between the trench gate 520 and the substrate 502. For example, in a version of this example in which the transistor 504 is designed to operate up to 100 volts, the dielectric liner 512 disposed on the sidewalls of the trenches 510 between the lower field plate segment 522 and the substrate 502 may be 400 nanometers to 500 nanometers thick, and the dielectric liner 512 disposed on the sidewalls of the trenches 510 between the upper field plate segment 524 and the substrate 502 may be 150 nanometers to 200 nanometers thick.

[0052] In this example, the lower field plate segment 522 is contacting the upper field plate segment 524 in the trenches 510. The upper field plate segment 524 is isolated from the trench gate 520 by an isolation layer 528, disposed between the upper field plate segment 524 and the trench gate 520. A bias voltage applied to the upper field plate segment 524 in this example also biases the lower field plate segment 522 to the same bias voltage.

[0053] The transistor 504 includes an n-type body 530 in the substrate 502 above the vertical drift region 508, abutting the gate dielectric layer 518. The transistor 504 further includes a p-type source 532 above the body 530 and abutting the gate dielectric layer 518. The trench gate 520 is partially coextensive with the vertical drift region 508 and the source 532. A source electrode 534 is disposed over the substrate 502 making electrical contact to the source 532 and the body 530. The source electrode 534 is electrically isolated from the trench gate 520 by a dielectric cap layer 536 over the trench gate 520. Other configurations for the source electrode 534 with respect to the source 532 and body 530 are within the scope of this example.

[0054] In one version of this example, in which the transistor 504 is designed to operate up to 100 volts, the trenches 510 may be 6 microns to 7 microns deep and 1.2 microns to 1.4 microns wide. The vertical drift region 508 may be 0.5 microns to 2.0 microns wide, that is, between

adjacent trenches 510, and have an average doping density of 1.8×10^{16} cm^{-3} to 2.0×10^{16} cm^{-3}.

[0055] Electrical connection to the trench gate 520 may be made through gate contacts 538 on exposed areas of the gate at a top surface 540 of the substrate 502. Electrical connections to the field plate segments 516 may be made through combined field plate contacts 542 on field plate risers 544, which extend from the field plate segments 516 up to the top surface 540 of the substrate 502. Other structures for making electrical connections to the trench gate 520 and the field plate segments 516 are within the scope of this example. Forming the upper field plate segment 524 to be isolated from the trench gate 520 may advantageously enable biasing the field plate segments 516 independently to increase current density in the transistor 504, while forming the lower field plate segment 522 to contact the upper field plate segment 524 in the trenches 510, so that electrical connections to the upper field plate segment 524 and the lower field plate segment 522 may be made through the combined field plate contacts 542 may advantageously reduce complexity and fabrication cost of the semiconductor device 500.

[0056] During operation of the semiconductor device 500, the trench gate 520 advantageously provides higher current density as explained in reference to FIG. 1. The field plate segments 516 provide a RESURF configuration to maintain an electric field in the vertical drift region 508 at a desired value, as explained in reference to FIG. 1. Accordingly, by forming the vertical MOS transistor 504 with the combination of the upper field plate segment 524 and the lower field plate segment 522, the transistor 504 is enabled to have shallower trenches 510 than the similar vertical MOS transistor with a single field plate, advantageously reducing a fabrication cost of the semiconductor device 500.

[0057] FIG. 6A through FIG. 6H are cross sections of the semiconductor device of FIG. 5, depicted in successive stages of fabrication. Referring to FIG. 6A, the semiconductor device 500 is formed on the substrate 502. The drain region 506 is formed in the substrate 502 to have a doping density greater than 1×10^{20} cm^{-3}. P-type dopants such as boron in the vertical drift region 508 may be incorporated during epitaxial growth or may be implanted later. A hard mask 546 is formed over the substrate 502, which exposes areas for the trenches 510. The trenches 510 are formed by removing material from the substrate 502 in the areas exposed by the hard mask 546. The drain region 506, hard mask 546 and trenches 510 may be formed as described in reference to FIG. 2A.

[0058] A first thermal oxide layer 548 is formed at sidewalls and bottoms 514 of the trenches

510. A deposited silicon dioxide layer 550 is formed on the first thermal oxide layer 548, by an SACVD process or a PECVD process. A lower field plate segment 522 is formed in the trenches 510 on the deposited silicon dioxide layer 550, such as described in reference to FIG. 2B and FIG. 2C. In this example, the lower field plate segment 522 may be p-type polysilicon to provide an effective charge balance in the RESURF structure of the vertical drift region 508. The first thermal oxide layer 548 combined with the deposited silicon dioxide layer 550 provide the dielectric liner 512 separating the lower field plate segment 522 from the substrate 502. For example, in this example, the first thermal oxide layer 548 may be 70 nanometers to 80 nanometers thick, and the deposited silicon dioxide layer 550 may be 330 nanometers to 420 nanometers thick, for an operating voltage of 100 volts.

[0059] Referring to FIG. 6B, a first blanket oxide etchback process removes substantially all of the dielectric liner 512, both the first thermal oxide layer 548 and the deposited silicon dioxide layer 550, from the trenches 510 above the lower field plate segment 522. The lower field plate segment 522 prevent removal of the dielectric liner 512 from the trenches 510 below tops of the lower field plate segment 522. For example, the first blanket oxide etchback process may include a timed wet etch using a buffered hydrofluoric acid solution.

[0060] Referring to FIG. 6C, a second thermal oxide layer 560 is formed at sidewalls of the trenches 510 above the lower field plate segment 522, and on a top surface of the lower field plate segment 522. In this example, the second thermal oxide layer 560 provides the dielectric liner 512 between the upper field plate segment 524 of FIG. 5 and the substrate 502. The second thermal oxide layer 560 may be 150 nanometers to 200 nanometers thick to provide 100 volt operation for the transistor 504.

[0061] Referring to FIG. 6D, an anisotropic etch process such as an RIE process removes the second thermal oxide layer 560 from the top surface of the lower field plate segment 522, to expose the top surface of the lower field plate segment 522. The anisotropic etch process is performed to avoid significantly degrading the second thermal oxide layer 560 on the sidewalls of the trenches 510. The anisotropic etch process may form a protective polymer on the second thermal oxide layer 560 on the sidewalls of the trenches 510, which is subsequently removed after the top surface of the lower field plate segment 522 is exposed.

[0062] Referring to FIG. 6E, an upper field plate segment 524 is formed on the second thermal oxide layer 560 and on the lower field plate segment 522 in the trenches 510, such as described

in reference to FIG. 2F. In this example, the upper field plate segment 524 may be p-type polysilicon, as explained in reference to FIG. 6E. In this example, the second thermal oxide layer 560 provides the dielectric liner 512 separating the upper field plate segment 524 from the substrate 502, which may advantageously reduce fabrication complexity and cost of the semiconductor device 500 be eliminating need to form a second dielectric layer in the dielectric liner 512 separating the upper field plate segment 524 from the substrate 502.

[0063] Referring to FIG. 6F, a second blanket oxide etchback process removes the second thermal oxide layer 560 from the trenches 510 above the upper field plate segment 524. The upper field plate segment 524 prevents removal of the second thermal oxide layer 560 from the trenches 510 below a top of the upper field plate segment 524. The second blanket oxide etchback process may be performed so that substantially no semiconductor material is removed from the substrate 502. The hard mask 546 of FIG. 6E may be removed by the second blanket etchback to expose the top surface 540 of the substrate 502, as depicted in FIG. 6F.

[0064] Referring to FIG. 6G, the gate dielectric layer 518 is formed on sidewalls of the trenches 510 and the isolation layer 528 is formed on a top surface of the upper field plate segment 524, concurrently. In this example, if the top surface 540 of the substrate 502 is exposed by the second blanket etchback discussed in reference to FIG. 6F, the gate dielectric layer 518 may also be formed on the top surface 540 as depicted in FIG. 6G. The gate dielectric layer 518 and the isolation layer 528 may be formed by thermal oxidation, or a combination of thermal oxidation and deposition of dielectric material. Thermal oxide in the isolation layer 528 may be thicker than thermal oxide in the gate dielectric layer 518, due to a higher thermal oxide growth rate on polysilicon compared to crystalline silicon.

[0065] Referring to FIG. 6H, the trench gate 520 is formed contacting the gate dielectric layer 518 and the isolation layer 528. The trench gate 520 may be formed as described in reference to FIG. 2I and FIG. 2J. In this example, the isolation layer 528 on the top of the upper field plate segment 524 electrically isolates the field plate segments 516 from the trench gate 520, enabling an independent bias of the field plate segments 516 with respect to the trench gate 520. Further fabrication provides the structure of FIG. 5.

[0066] FIG. 7 is a cross section of another example semiconductor device containing a vertical n-channel MOS transistor. The semiconductor device 700 is formed on a substrate 702, which includes a semiconductor material. The n-channel vertical MOS transistor 704, referred to

herein as the transistor 704, includes an n-type drain region 706 disposed in the substrate 702 below an n-type vertical drift region 708.

[0067] The semiconductor device 700 includes trenches 710, which extend vertically through the vertical drift region 708 proximate to the drain region 706, or possibly into the drain region 706. The trenches 710 contain a dielectric liner 712 extending to bottoms 714 of the trenches 710 and abutting the substrate 702, and multiple field plate segments 716 on the dielectric liner 712. The trenches 710 further contain a gate dielectric layer 718 above the dielectric liner 712 abutting the substrate 702, and a trench gate 720 of the transistor 704 contacting the gate dielectric layer 718. In this example, the field plate segments 716 include respective lower field plate segments 722 on the respective dielectric liners 712 at the bottoms 714 of the trenches 710, respective middle field plate segments 762 disposed above the respective lower field plate segments 722, and respective upper field plate segments 724 disposed above the respective middle field plate segments 762 and below the respective trench gates 720. The field plate segments 716 and the trench gate 720 may include primarily n-type polysilicon. The dielectric liner 712 may include primarily silicon dioxide. The dielectric liner 712 separates the lower field plate segment 722, the middle field plate segment 762 and the upper field plate segment 724 from the substrate 702. The dielectric liner 712 separating the lower field plate segment 722 from the substrate 702 is thicker than the dielectric liner 712 separating the middle field plate segment 762 from the substrate 702, which is in turn thicker than the dielectric liner 712 separating the upper field plate segment 724 from the substrate 702. The dielectric liner 712 disposed on the sidewalls of the trenches 710 between the upper field plate segment 724 and the substrate 702 is thicker than the gate dielectric layer 718 disposed on the sidewalls of the trenches 710 between the trench gate 720 and the substrate 702.

[0068] In this example, the lower field plate segment 722 is contacting the middle field plate segment 762 in the trenches 710, and the upper field plate segment 724 is contacting the trench gate 720 in the trenches 710, while the middle field plate segment 762 is separated from the upper field plate segment 724 by an isolation layer 726, disposed between the upper field plate segment 724 and the trench gate 720. A bias voltage applied to the trench gate 720 is also thus applied to the upper field plate segment 724 in this example, while an independent bias voltage applied to the middle field plate segment 762 also biases the lower field plate segment 722 to the same independent bias voltage.

[0069] The transistor 704 includes a p-type body 730 in the substrate 702 above the vertical drift region 708, abutting the gate dielectric layer 718. The transistor 704 further includes an n-type source 732 above the body 730 and abutting the gate dielectric layer 718. The trench gate 720 is partially coextensive with the vertical drift region 708 and the source 732. A source electrode 734 is disposed over the substrate 702 making electrical contact to the source 732 and the body 730. The source electrode 734 is electrically isolated from the trench gate 720 by a dielectric cap layer 736 over the trench gate 720. Other configurations for the source electrode 734 with respect to the source 732 and body 730 are within the scope of this example.

[0070] Electrical connection to the trench gate 720 and the upper field plate segment 724 may be made through gate contacts 738 on exposed areas of the gate at a top surface 740 of the substrate 702. Electrical connections to the middle field plate segment 762 and the lower filed plate segment 722 may be made through combined field plate contacts 742 on field plate risers 744, which extend from the middle field plate segment 762 up to the top surface 740 of the substrate 702. Other structures for making electrical connections to the trench gate 720 and the middle field plate segment 762 are within the scope of this example. Forming the trench gate 720 and the upper field plate segment 724 to be isolated from the middle field plate segment 762 and the lower field plate segment 722 may advantageously enable a balance of the advantages of independent biases for the trench gate 720 and the field plate segments 716 as discussed in reference to FIG. 1, and the advantages of the combined field plate contacts 742 as discussed in reference to FIG. 3.

[0071] During operation of the semiconductor device 700, the trench gate 720 advantageously provides higher current density as explained in reference to FIG. 1. The field plate segments 716 provide a RESURF configuration to maintain an electric field in the vertical drift region 708 at a desired value, as explained in reference to FIG. 1. Accordingly, by forming the vertical MOS transistor 704 with the combination of the upper field plate segment 724 and the lower field plate segment 722, the transistor 704 is enabled to have shallower trenches 710 than the similar vertical MOS transistor with a single field plate, advantageously reducing a fabrication cost of the semiconductor device 700.

[0072] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate including a semiconductor material;

a drain region of a vertical metal oxide semiconductor (MOS) transistor disposed in the semiconductor material of the substrate;

a vertical drift region of the vertical MOS transistor disposed in the semiconductor material above the drain region;

trenches disposed in the substrate in the vertical drift region;

a dielectric liner disposed in the trenches;

a gate dielectric layer of the vertical MOS transistor disposed in the trenches above the dielectric liner;

a trench gate of the vertical MOS transistor disposed in the trenches contacting the gate dielectric layer;

a body of the vertical MOS transistor disposed in the substrate above the vertical drift region; and

a plurality of field plate segments disposed in the trenches, separated from the substrate by the dielectric liner, including: a lower field plate segment at bottoms of the trenches; and an upper field plate segment disposed above the lower field plate segment and below the trench gate;

wherein the dielectric liner disposed on sidewalls of the trenches between the lower field plate segment and the substrate is thicker than the dielectric liner disposed on the sidewalls of the trenches between the upper field plate segment and the substrate, and the dielectric liner disposed on the sidewalls of the trenches between the upper field plate segment and the substrate is thicker than the gate dielectric layer disposed on the sidewalls of the trenches between the trench gate and the substrate.

2. The semiconductor device of claim 1, wherein the upper field plate segment is electrically isolated from the trench gate in the trenches by a dielectric isolation layer disposed between the trench gate and the upper field plate segment.

3. The semiconductor device of claim 1, wherein the upper field plate segment is connected to the trench gate in the trenches.

4. The semiconductor device of claim 1, wherein the upper field plate segment is electrically isolated from the lower field plate segment.

5. The semiconductor device of claim 1, wherein the upper field plate segment is connected to the lower field plate segment.

6. The semiconductor device of claim 1, wherein the plurality of field plate segments includes a middle field plate segment disposed between the upper field plate segment and the lower field plate segment, and wherein the dielectric liner separating the lower field plate segment from the substrate is thicker than the dielectric liner separating the middle field plate segment from the substrate, and the dielectric liner separating the middle field plate segment from the substrate is thicker than the dielectric liner separating the upper field plate segment from the substrate.

7. A method of forming a semiconductor device, comprising:

providing a substrate including a semiconductor material;

forming a drain region of a vertical MOS transistor in the substrate;

forming a vertical drift region of the vertical MOS transistor in the semiconductor material above the drain region;

forming trenches in the vertical drift region;

forming a dielectric liner in the trenches abutting the substrate;

forming a lower field plate segment in the trenches on the dielectric liner;

removing at least a portion of the dielectric liner above the lower field plate segment;

forming an upper field plate segment in the trenches above the lower field plate segment, wherein dielectric material between the upper field plate segment and the substrate provides the dielectric liner between the upper field plate segment and the substrate, and the dielectric liner disposed on sidewalls of the trenches between the lower field plate segment and the substrate is thicker than the dielectric liner disposed on the sidewalls of the trenches between the upper field plate segment and the substrate;

removing the dielectric liner from the trenches above the upper field plate segment;

forming a gate dielectric layer of the vertical MOS transistor abutting the substrate in the trenches above the upper field plate segment, thinner than the dielectric liner between the upper field plate segment and the substrate;

forming a trench gate of the vertical MOS transistor in the trenches contacting the gate

dielectric layer; and

forming a body of the vertical MOS transistor in the substrate abutting the gate dielectric layer above the vertical drift region.

8. The method of claim 7, wherein forming the dielectric liner in the trenches includes forming a thermal oxide layer in the trenches abutting the substrate and forming a first deposited silicon dioxide layer in the trenches on the thermal oxide layer, so that the lower field plate segment is on the first deposited silicon.

9. The method of claim 8, wherein:

removing at least a portion of the dielectric liner above the lower field plate segment includes removing at least a portion of the first deposited silicon dioxide layer above the lower field plate segment, leaving a majority of the thermal oxide layer in place above the lower field plate segment; and

the remaining thermal oxide layer between the upper field plate segment and the substrate provides at least a portion of the dielectric liner on the sidewalls of the trenches between the upper field plate segment and the substrate.

10. The method of claim 9, comprising forming a second deposited silicon dioxide layer on the remaining thermal oxide layer above the lower field plate segment, after removing the first deposited silicon dioxide layer and before forming the upper field plate segment, so that the dielectric liner on the sidewalls of the trenches separating the upper field plate segment from the substrate includes the second deposited silicon dioxide layer.

11. The method of claim 10, comprising removing the second deposited silicon dioxide layer on the lower field plate segment, before forming the upper field plate segment, so that the upper field plate segment contacts the lower field plate segment.

12. The method of claim 10, wherein the upper field plate segment is formed on a portion of the second deposited silicon dioxide layer on the lower field plate segment so that the upper field plate segment is electrically isolated from the lower field plate segment.

13. The method of claim 9, wherein the upper field plate segment is formed on the remaining thermal oxide layer above the lower field plate segment, so that the remaining thermal oxide layer above the lower field plate segment provides the dielectric liner on the sidewalls of the trenches separating the upper field plate segment from the substrate.

14. The method of claim 7, wherein removing at least a portion of the dielectric liner above the lower field plate segment includes removing substantially all of the dielectric liner above the lower field plate segment, and comprising:

forming a thermal oxide layer in the trenches abutting the substrate above the lower field plate segment after forming the lower field plate segment, so that the thermal oxide layer provides at least a portion of the dielectric liner on the sidewalls of the trenches between the upper field plate segment and the substrate.

15. The method of claim 7, comprising removing dielectric material on the lower field plate segment, before forming the upper field plate segment, so that the upper field plate segment contacts the lower field plate segment.

16. The method of claim 7, wherein the upper field plate segment is formed over dielectric material on the lower field plate segment so that the upper field plate segment is electrically isolated from the lower field plate segment.

17. The method of claim 7, comprising removing the gate dielectric layer on the upper field plate segment, before forming the trench gate, so that the trench gate contacts the upper field plate segment.

18. The method of claim 7, wherein the trench gate is formed on a portion of the gate dielectric layer on the upper field plate segment so that the trench gate is electrically isolated from the upper field plate segment.

19. The method of claim 7, wherein forming the lower field plate segment includes forming a layer of polysilicon in the trenches and over a top surface of the substrate, and removing the layer of polysilicon from over the top surface of the substrate and from a portion of the trenches, leaving a portion of the layer of polysilicon in the trenches to provide the lower field plate segment.

20. A method of forming a semiconductor device, comprising:

providing a substrate including a semiconductor material;

forming a drain region of a vertical MOS transistor in the substrate;

forming a vertical drift region of the vertical MOS transistor in the semiconductor material above the drain region;

forming trenches in the vertical drift region;

forming a thermal oxide layer in the trenches abutting the substrate;

forming a first deposited silicon dioxide layer in the trenches on the thermal oxide layer;

forming a lower field plate segment in the trenches on the first deposited silicon, wherein a combination of the thermal oxide layer and the first deposited silicon dioxide layer provide a dielectric liner on sidewalls of the trenches separating the lower field plate segment from the substrate;

removing at least a portion of the first deposited silicon dioxide layer above the lower field plate segment, leaving a majority of the thermal oxide layer in place above the lower field plate segment;

forming an upper field plate segment in the trenches above the lower field plate segment, wherein the remaining thermal oxide layer between the upper field plate segment and the substrate provides at least a portion of the dielectric liner on the sidewalls of the trenches between the upper field plate segment and the substrate, and the dielectric liner disposed on the sidewalls of the trenches between the lower field plate segment and the substrate is thicker than the dielectric liner disposed on the sidewalls of the trenches between the upper field plate segment and the substrate;

removing the thermal oxide layer from the trenches above the upper field plate segment;

forming a gate dielectric layer of the vertical MOS transistor abutting the substrate in the trenches above the upper field plate segment, thinner than the dielectric liner on the sidewalls of the trenches between the upper field plate segment and the substrate;

forming a trench gate of the vertical MOS transistor in the trenches contacting the gate dielectric layer; and

forming a body of the vertical MOS transistor in the substrate abutting the gate dielectric layer above the vertical drift region.

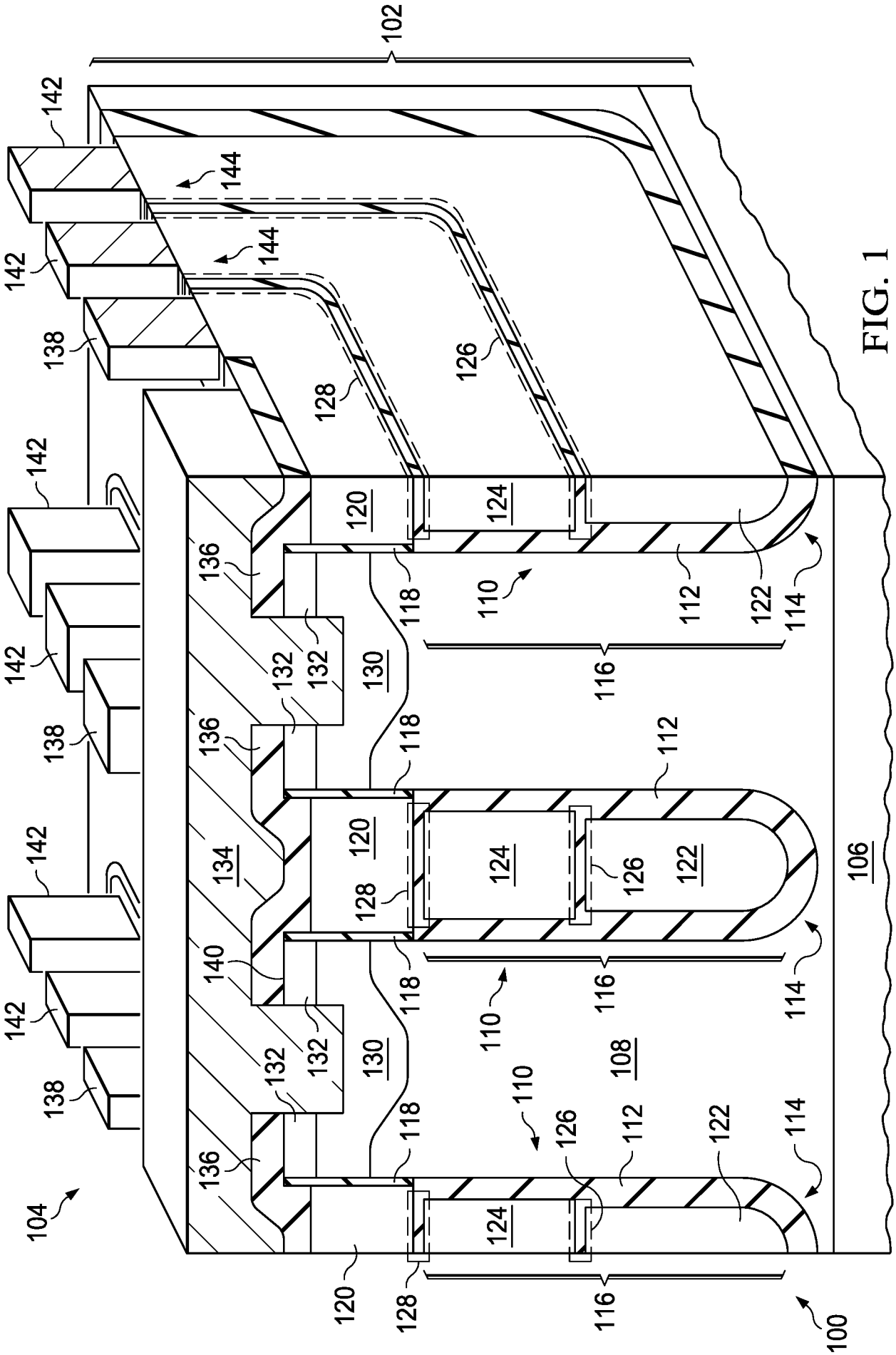
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FIG. 1

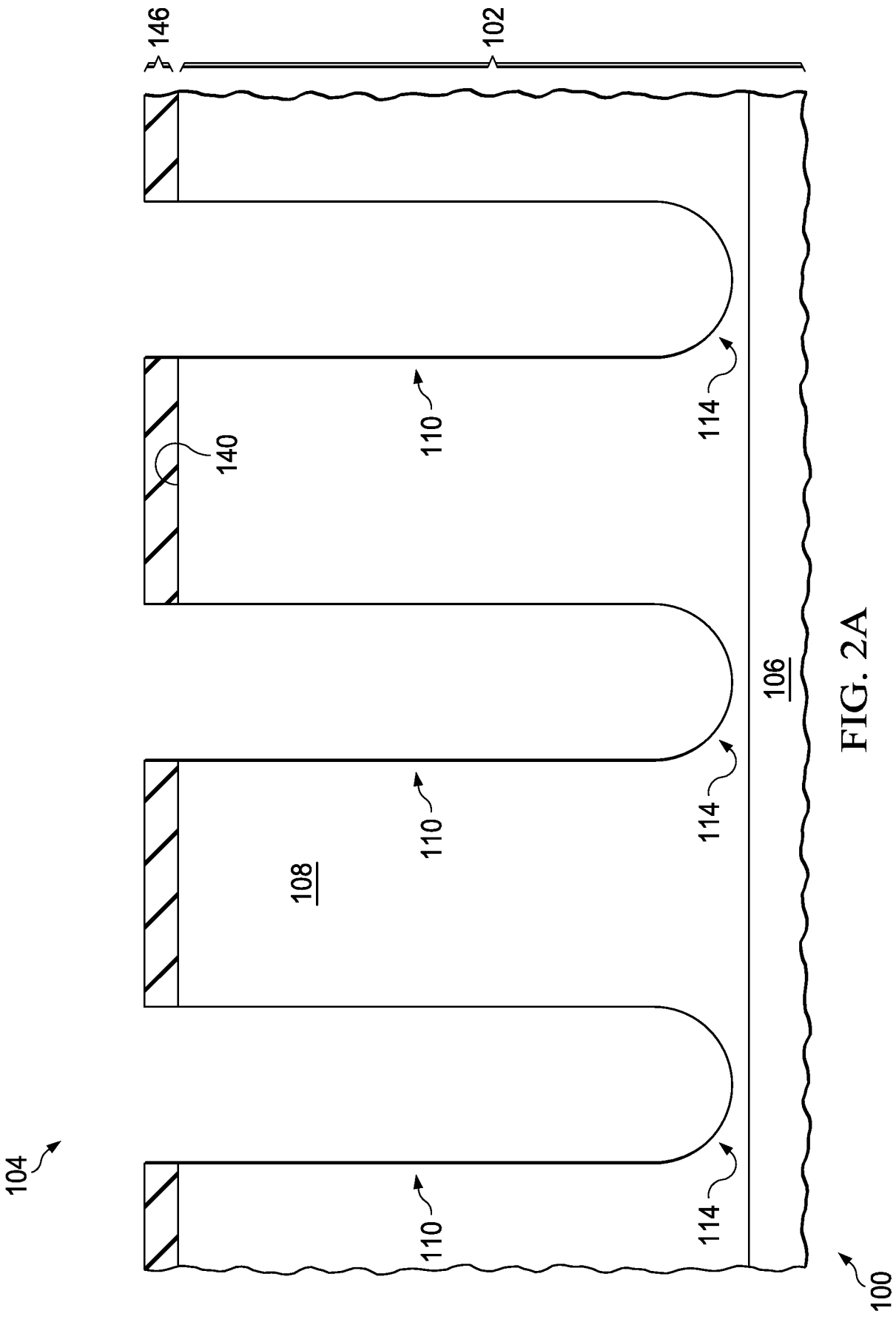

FIG. 2A

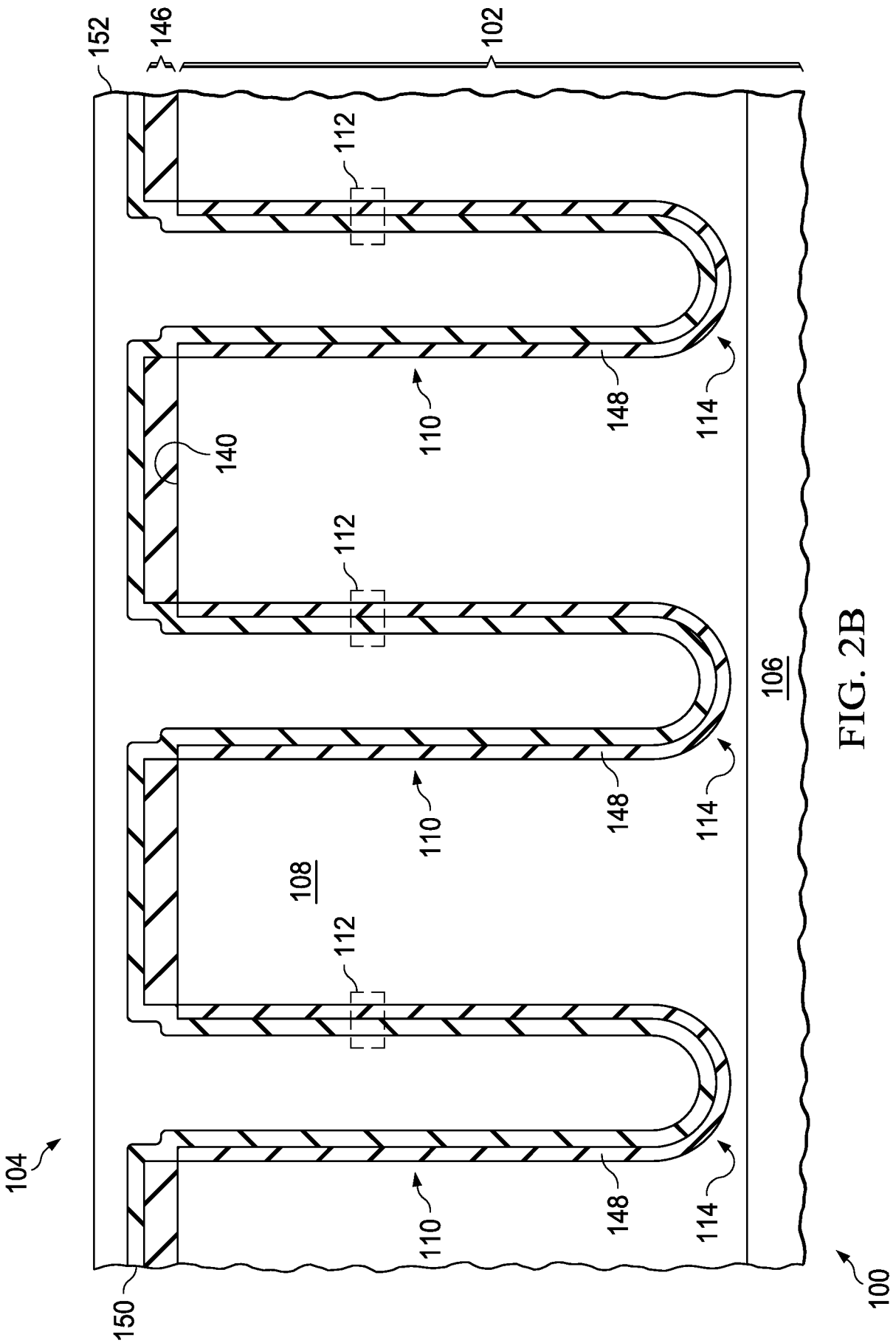
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FIG. 2B

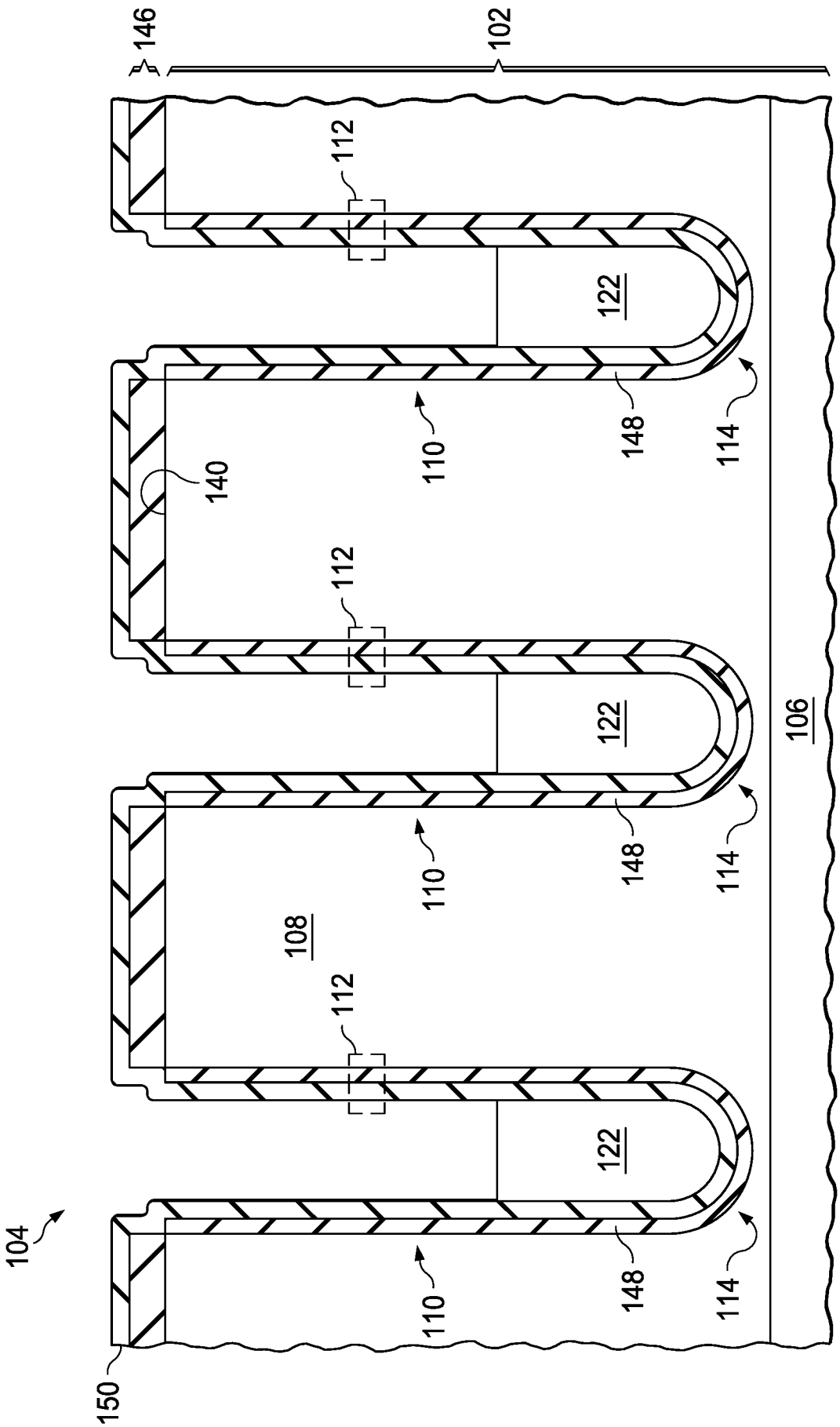

FIG. 2C

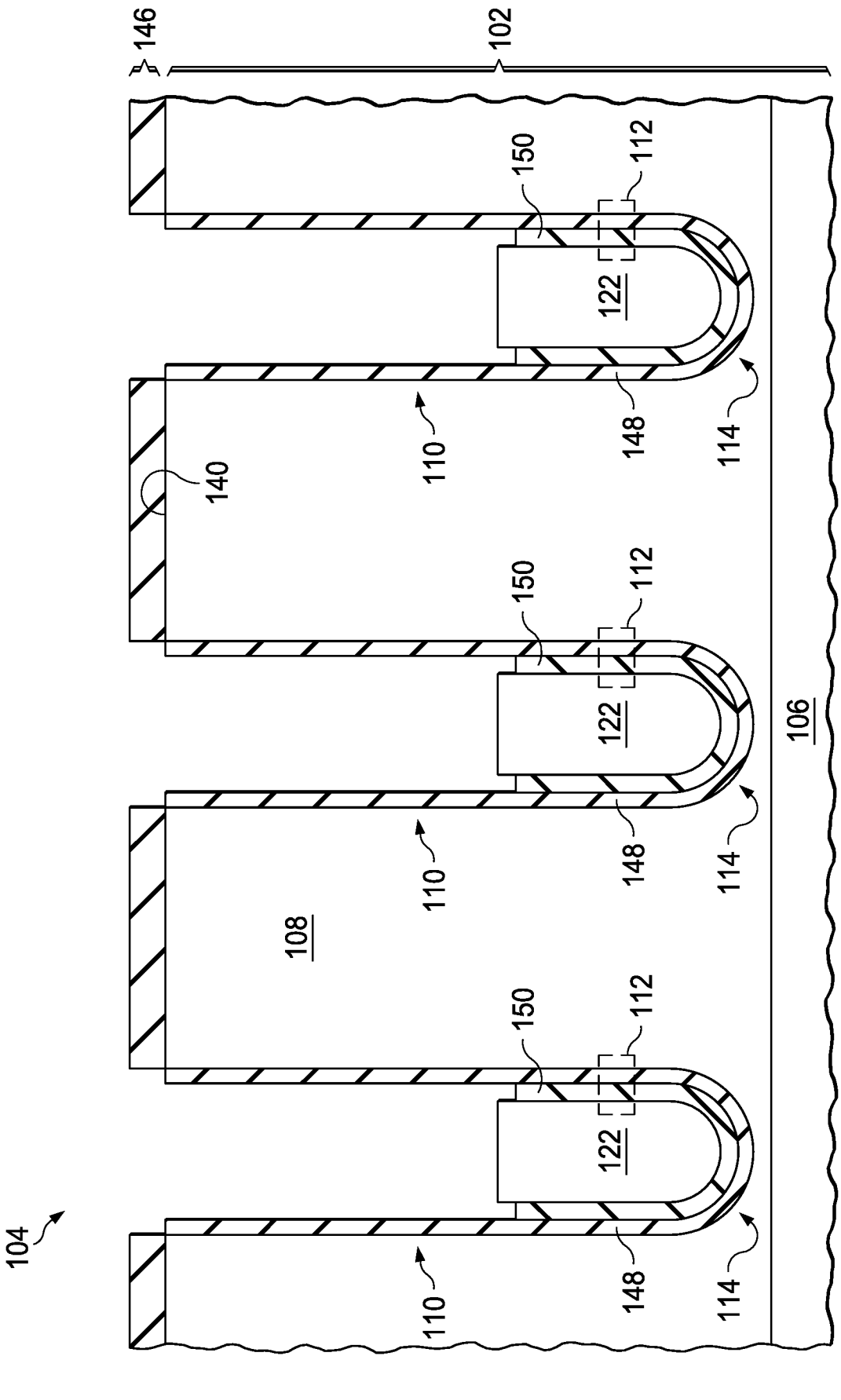

FIG. 2D

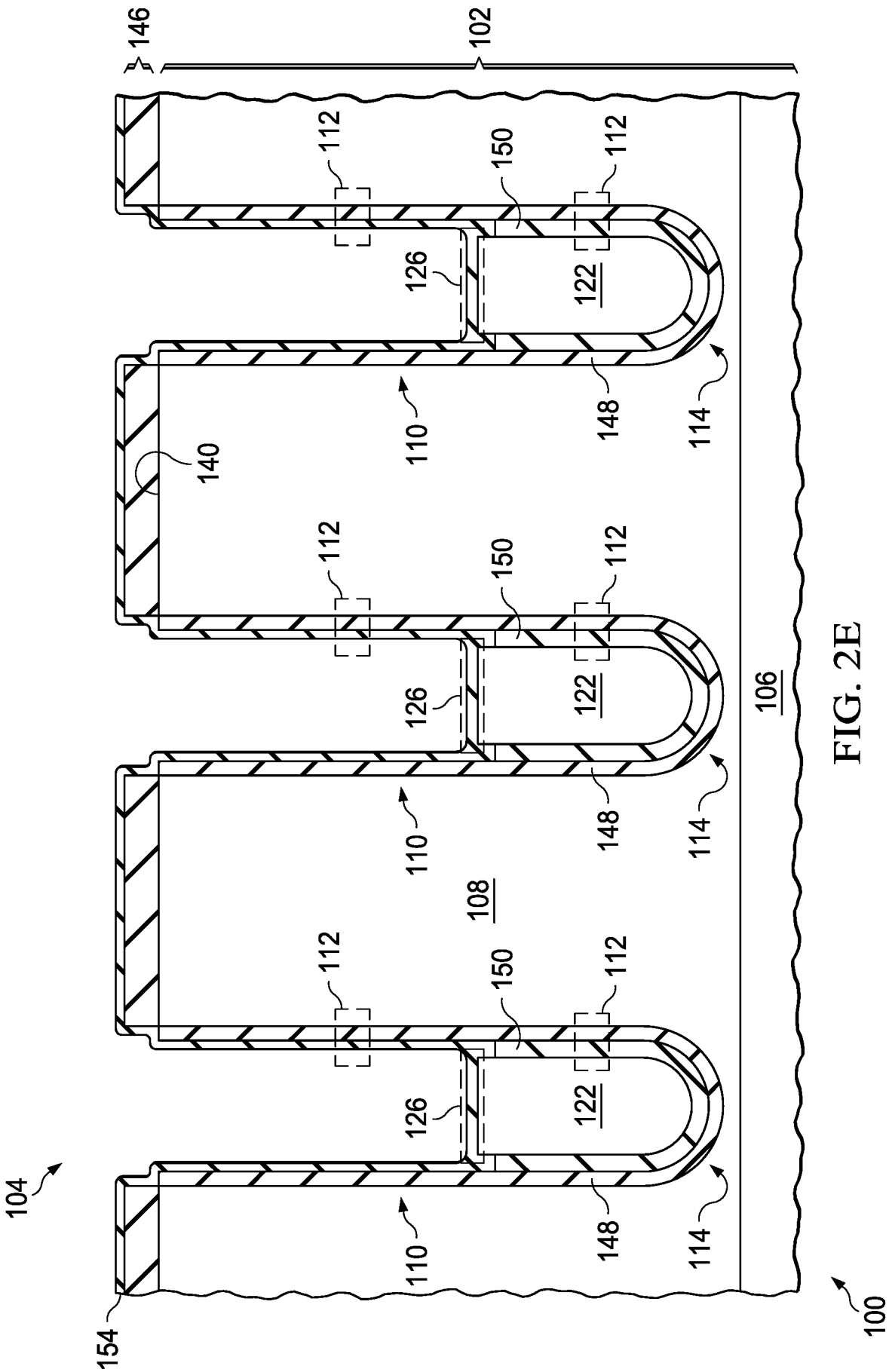
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FIG. 2E

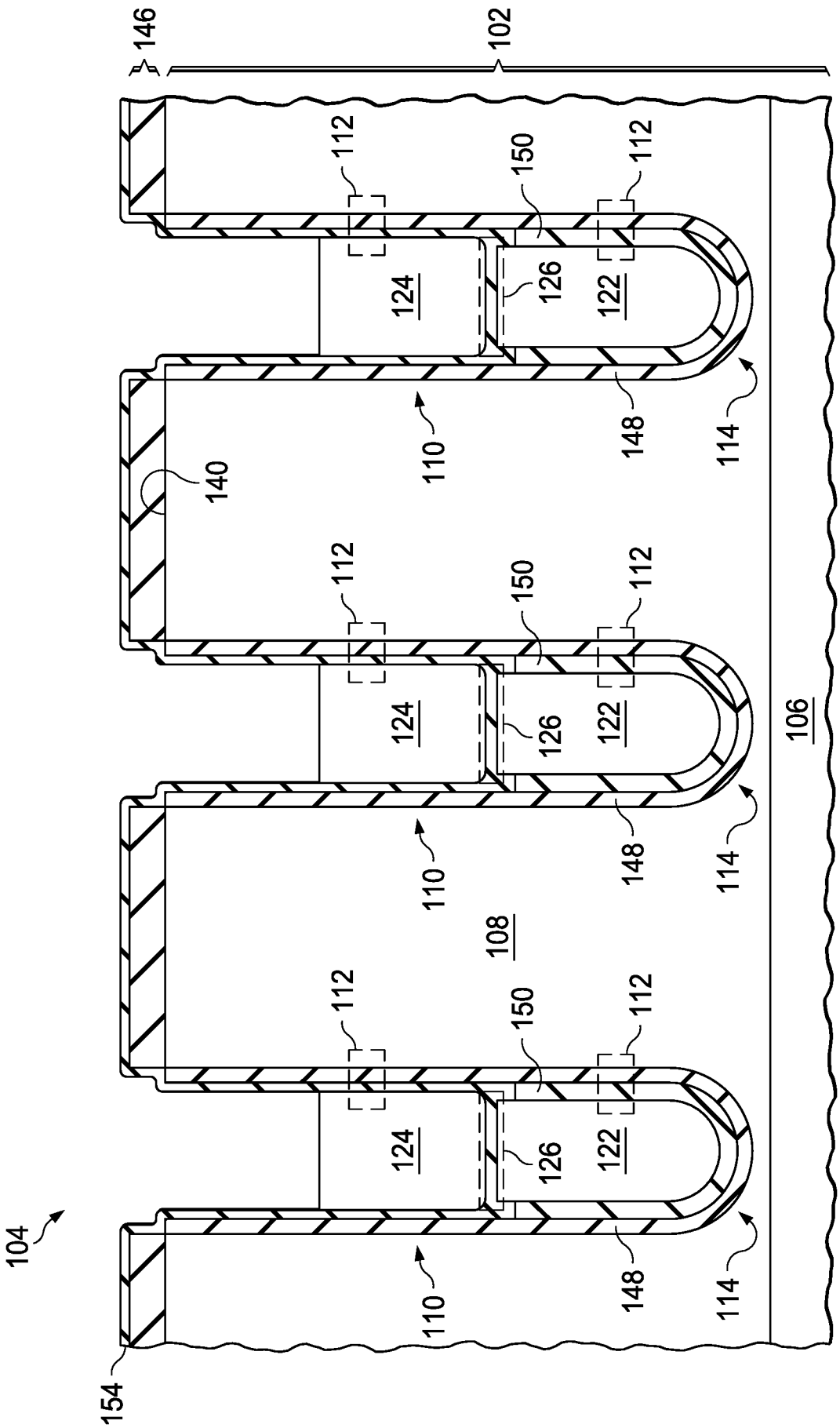
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FIG. 2F

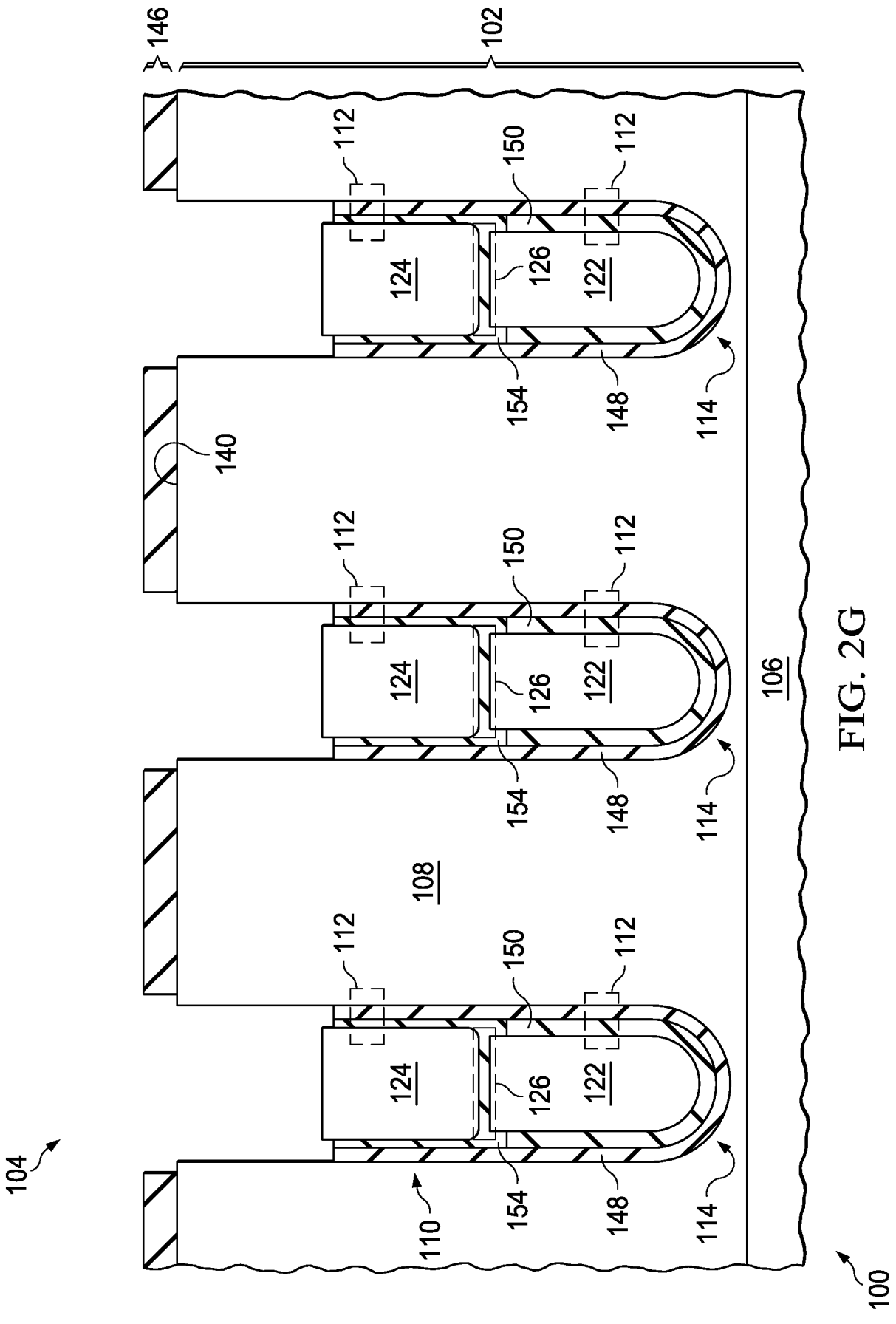
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FIG. 2G

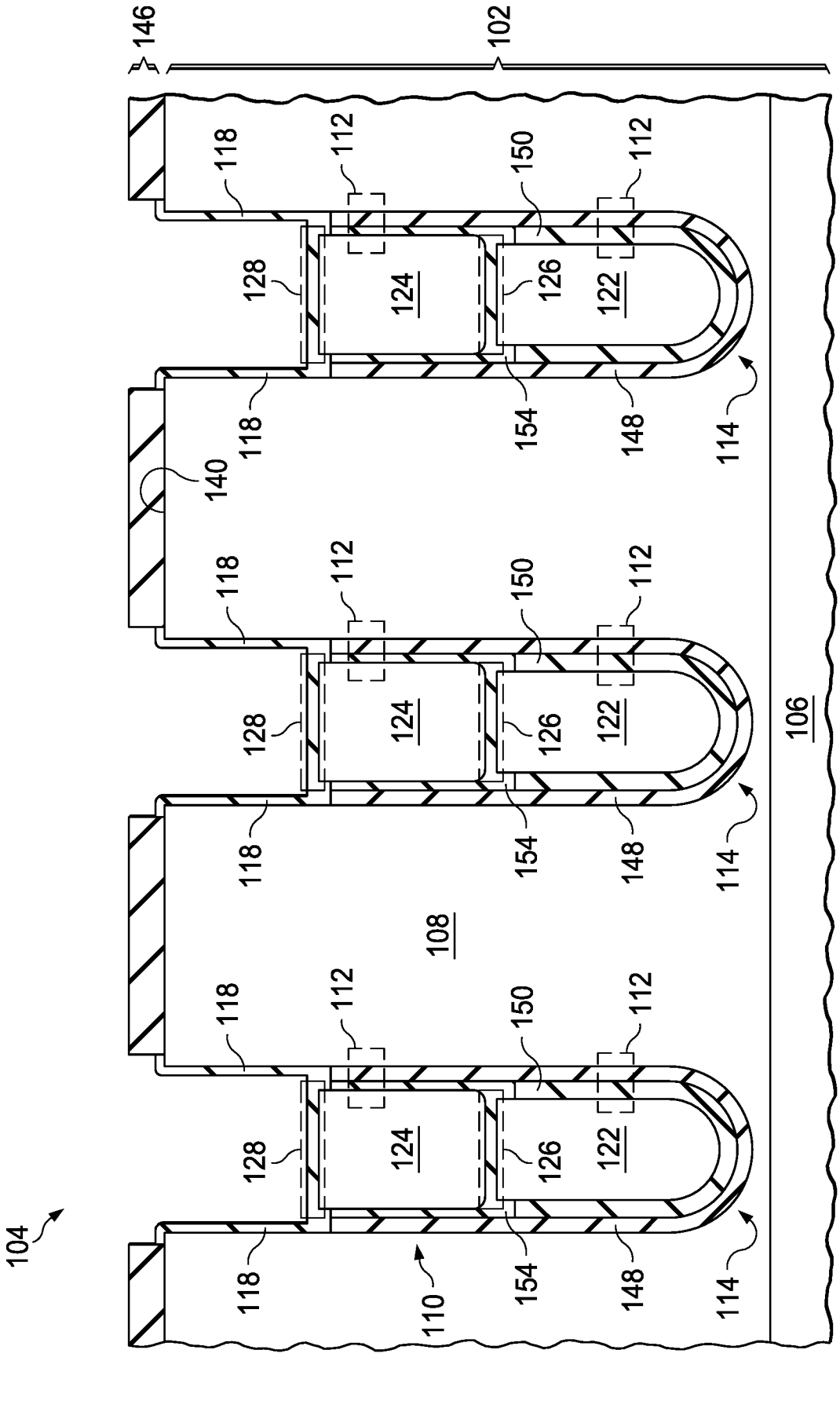
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FIG. 2H

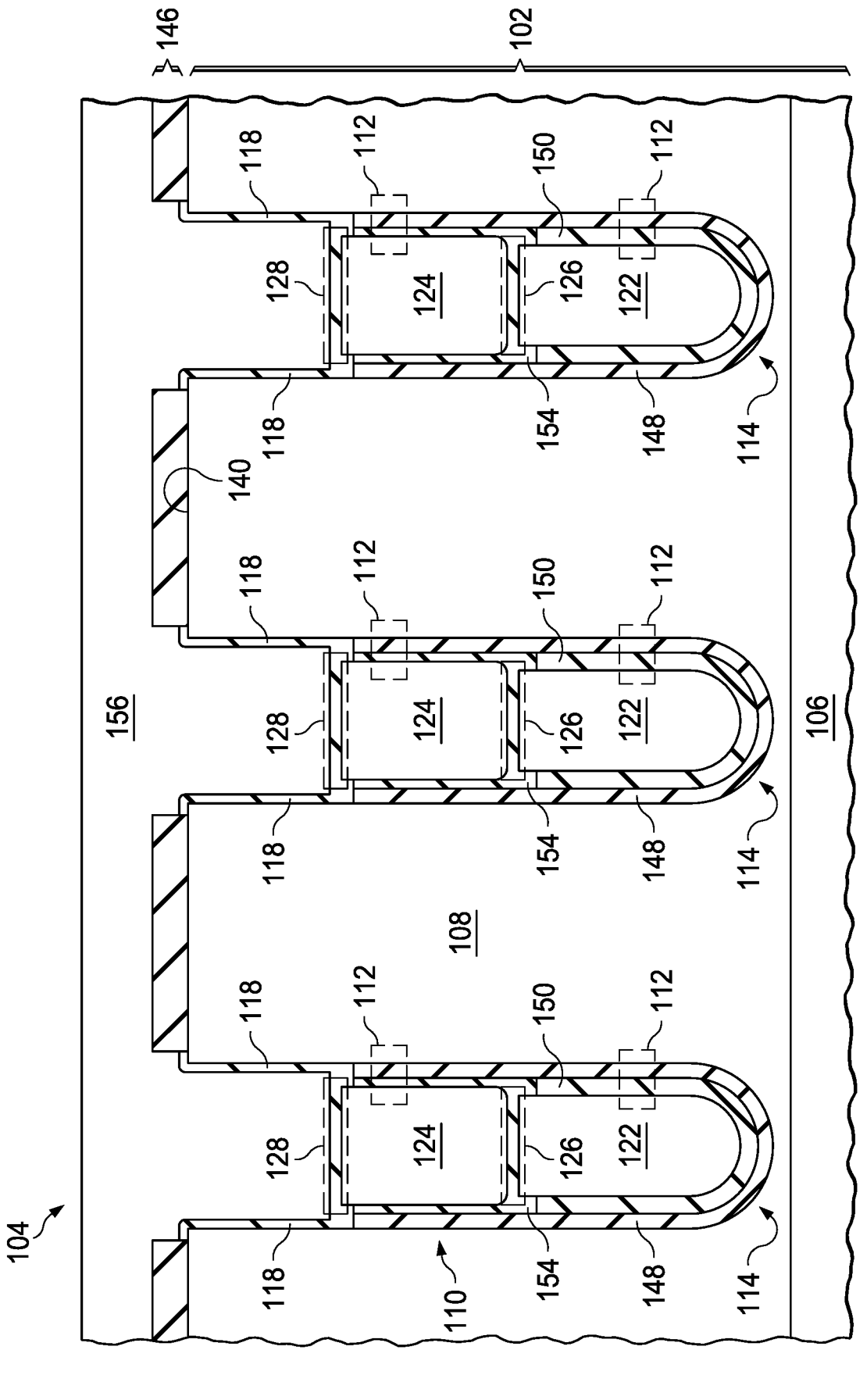
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FIG. 2I

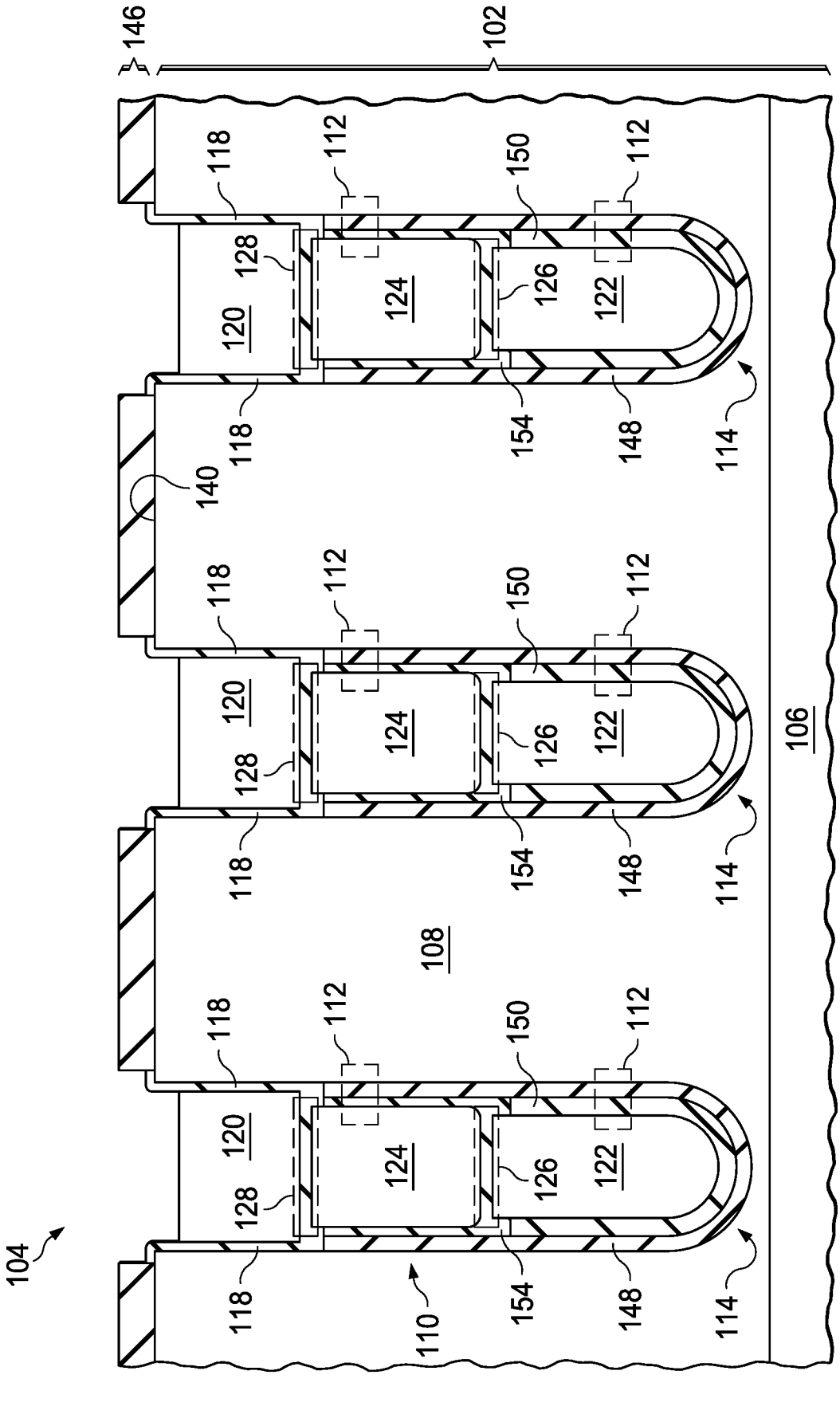
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FIG. 2J

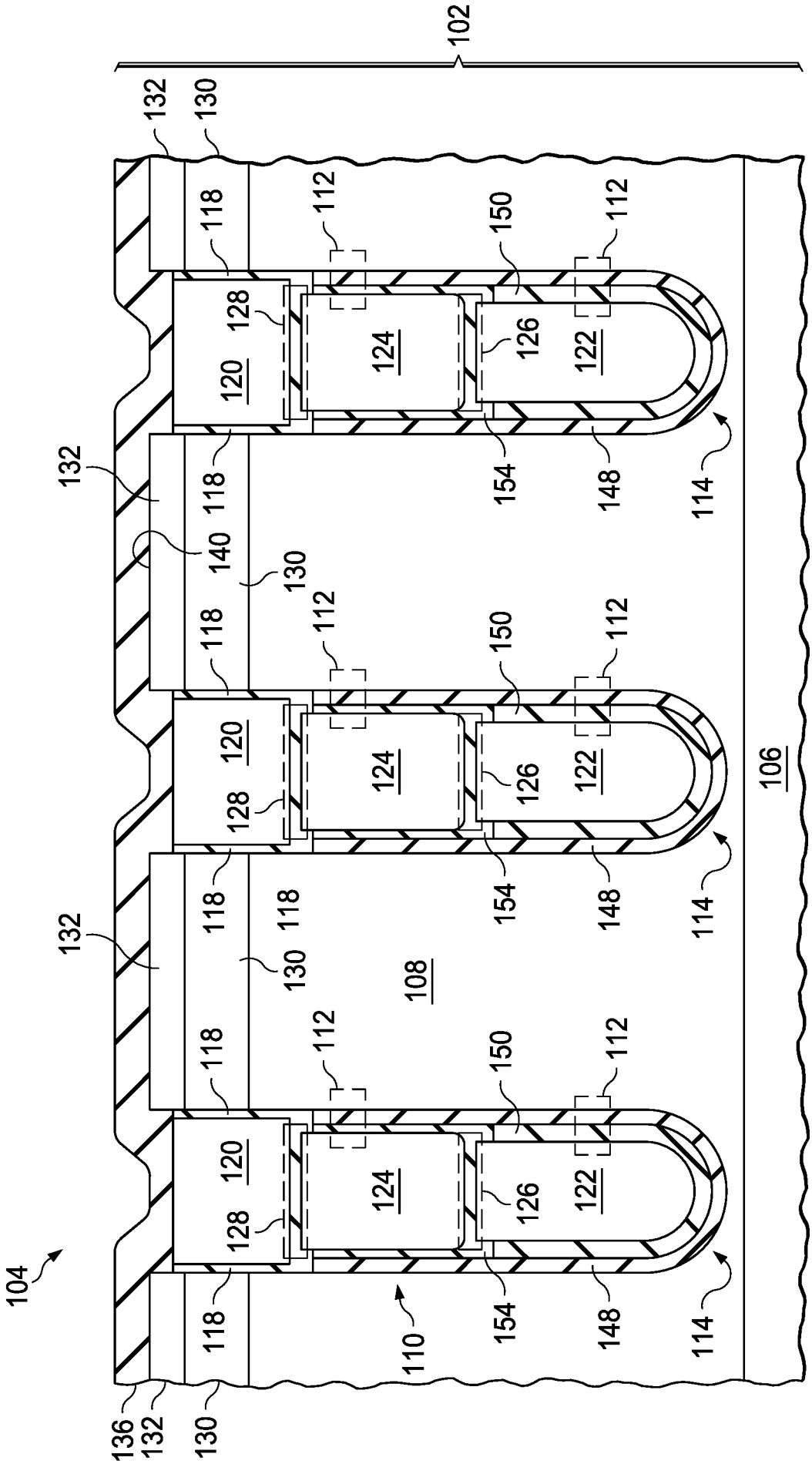
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FIG. 2K

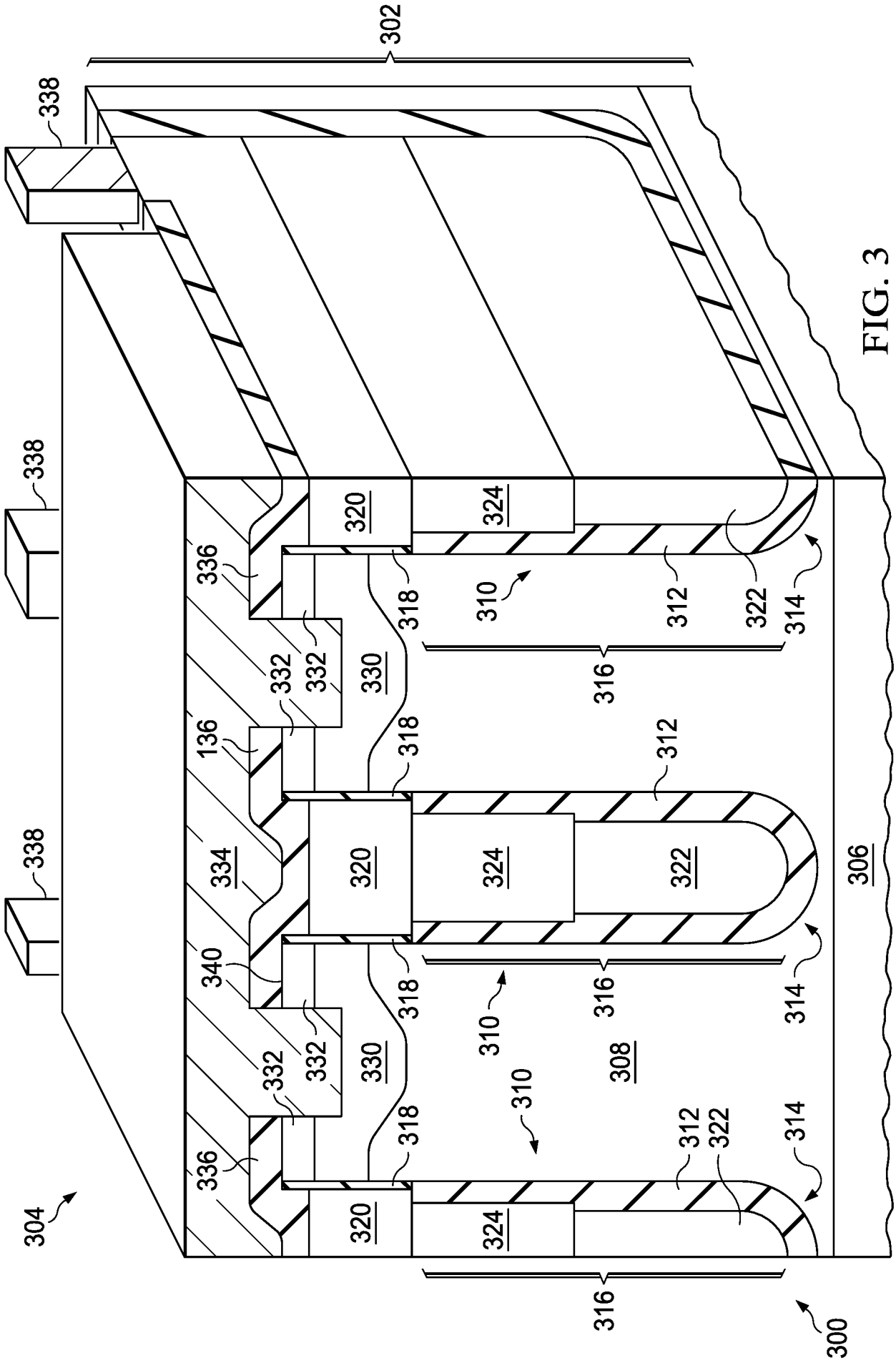
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FIG. 3

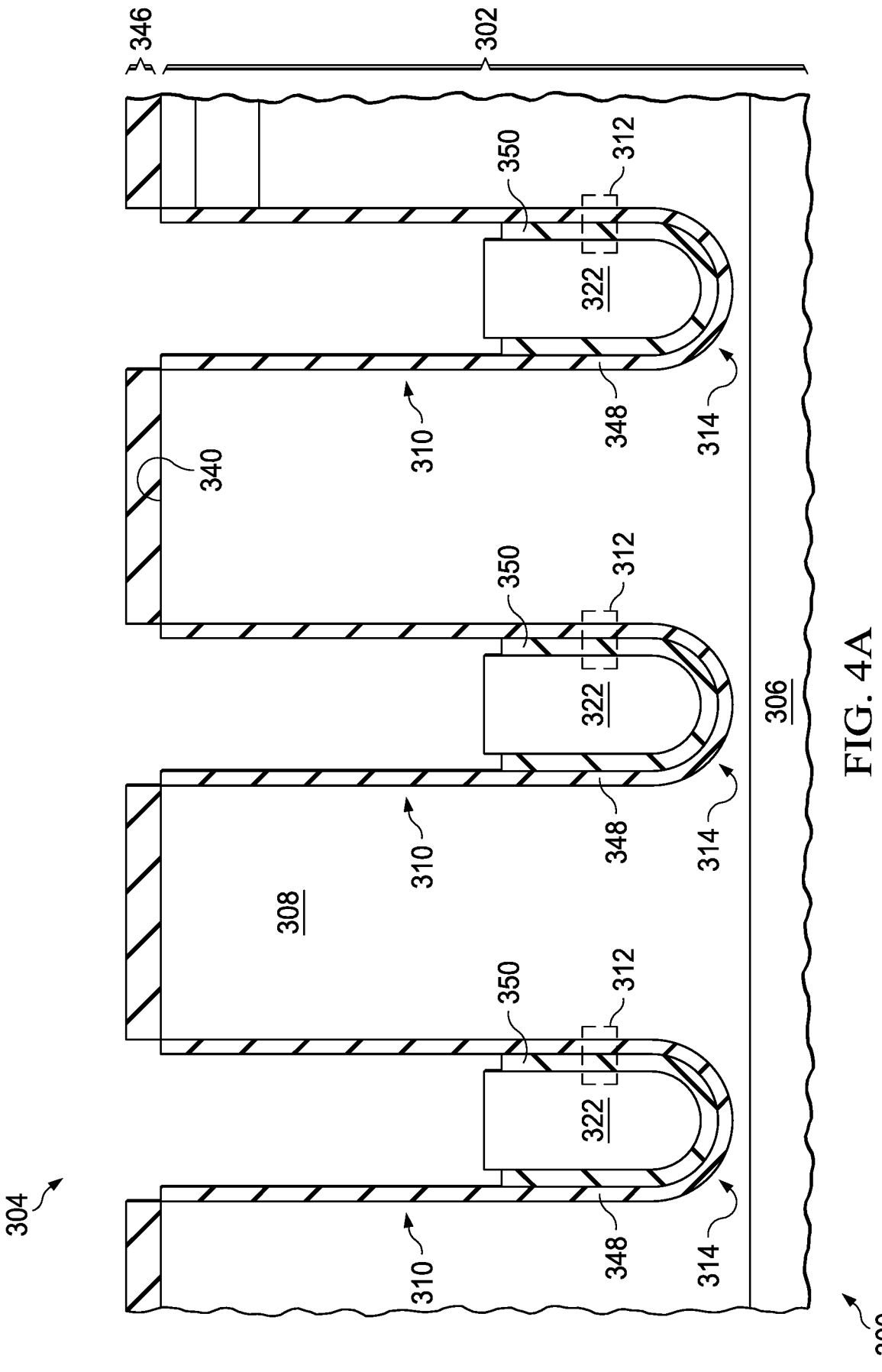

FIG. 4A

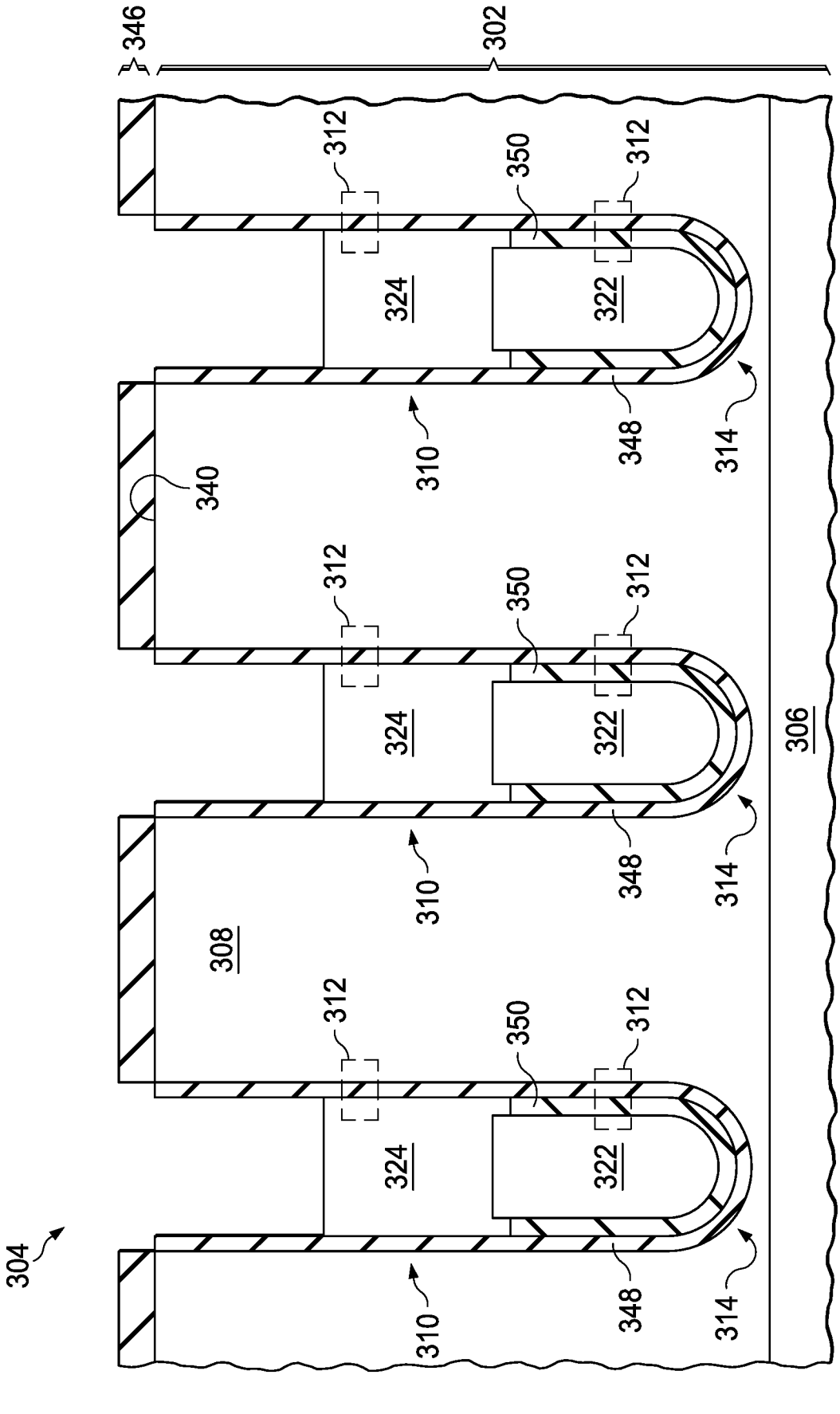
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FIG. 4B

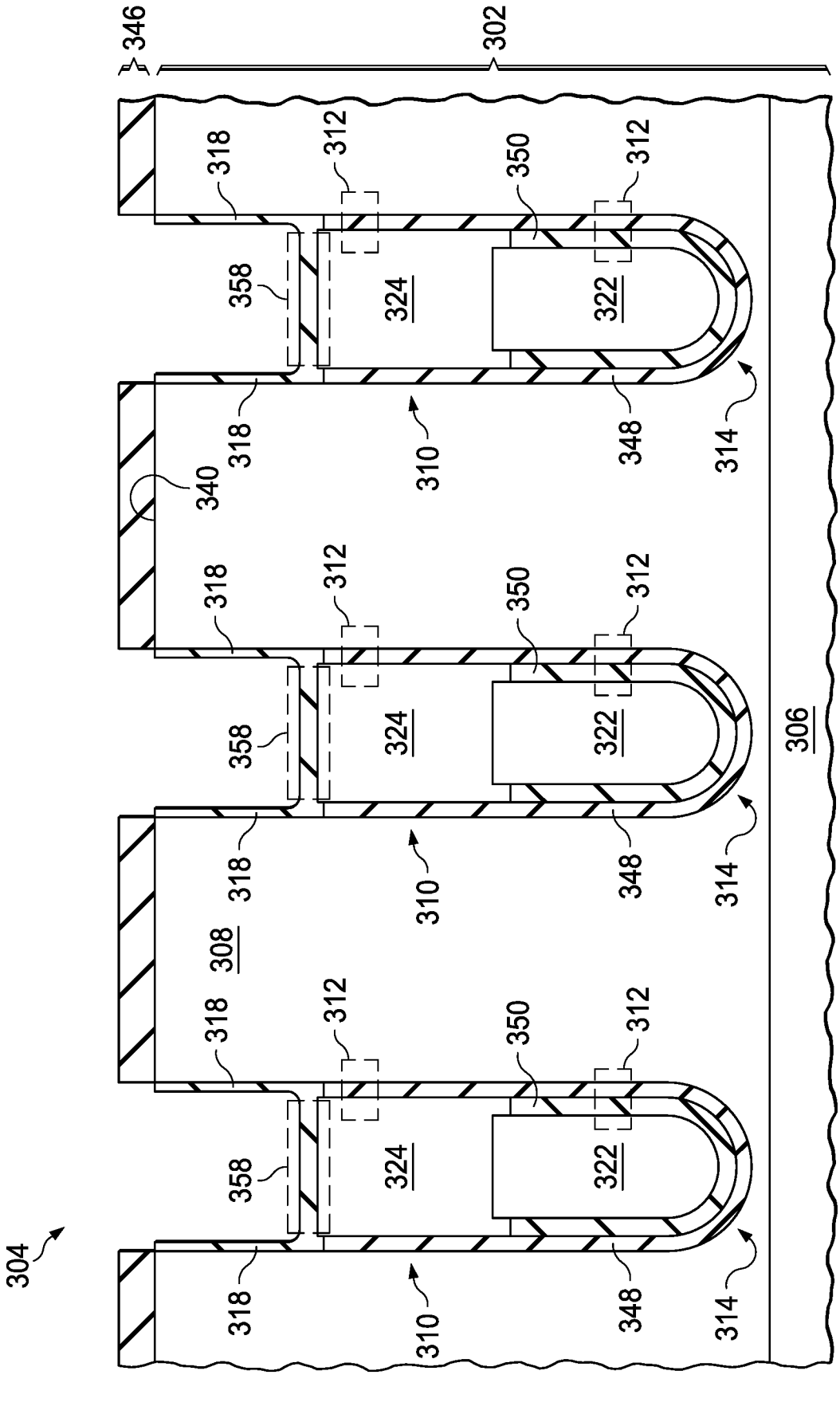
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FIG. 4C

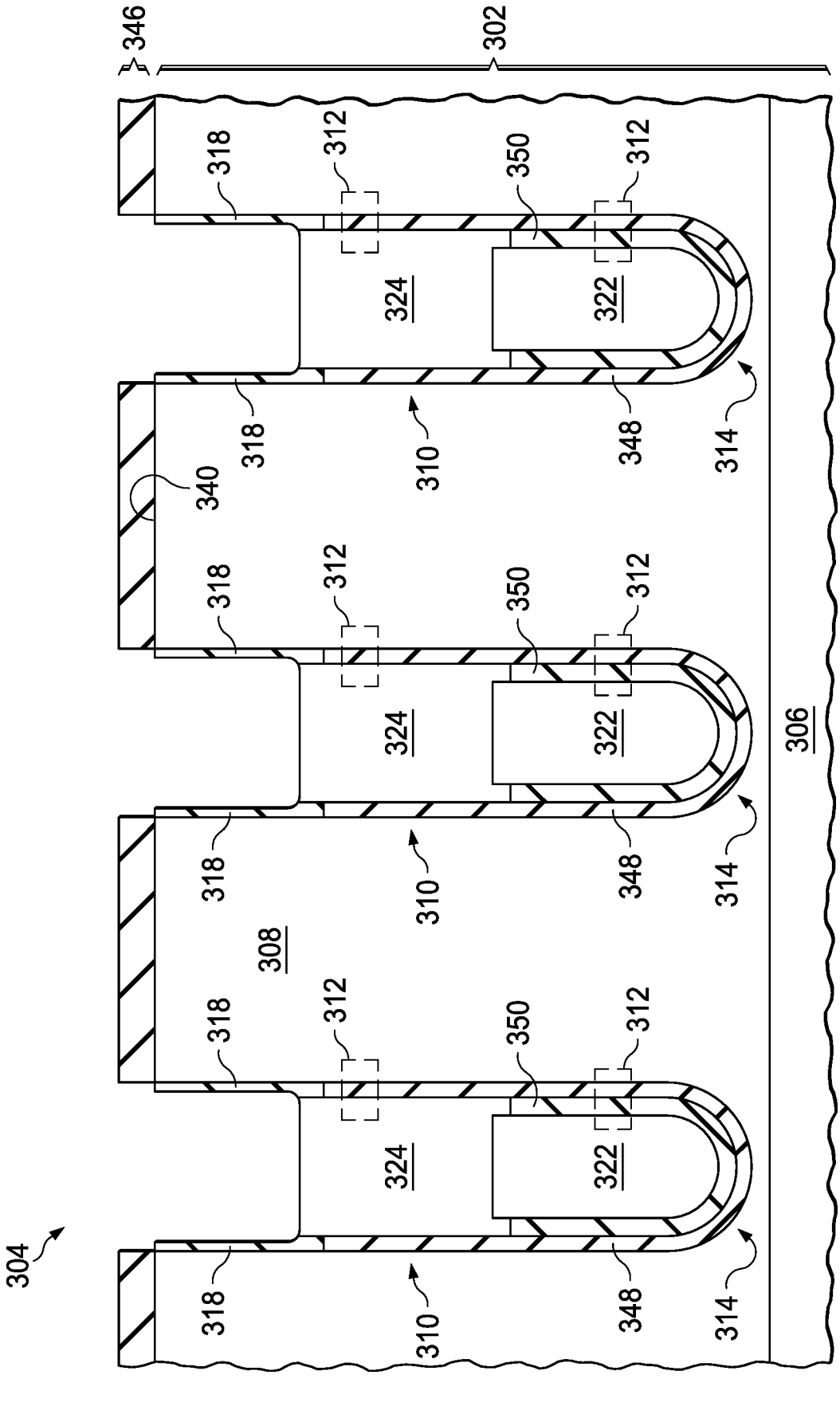
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FIG. 4D

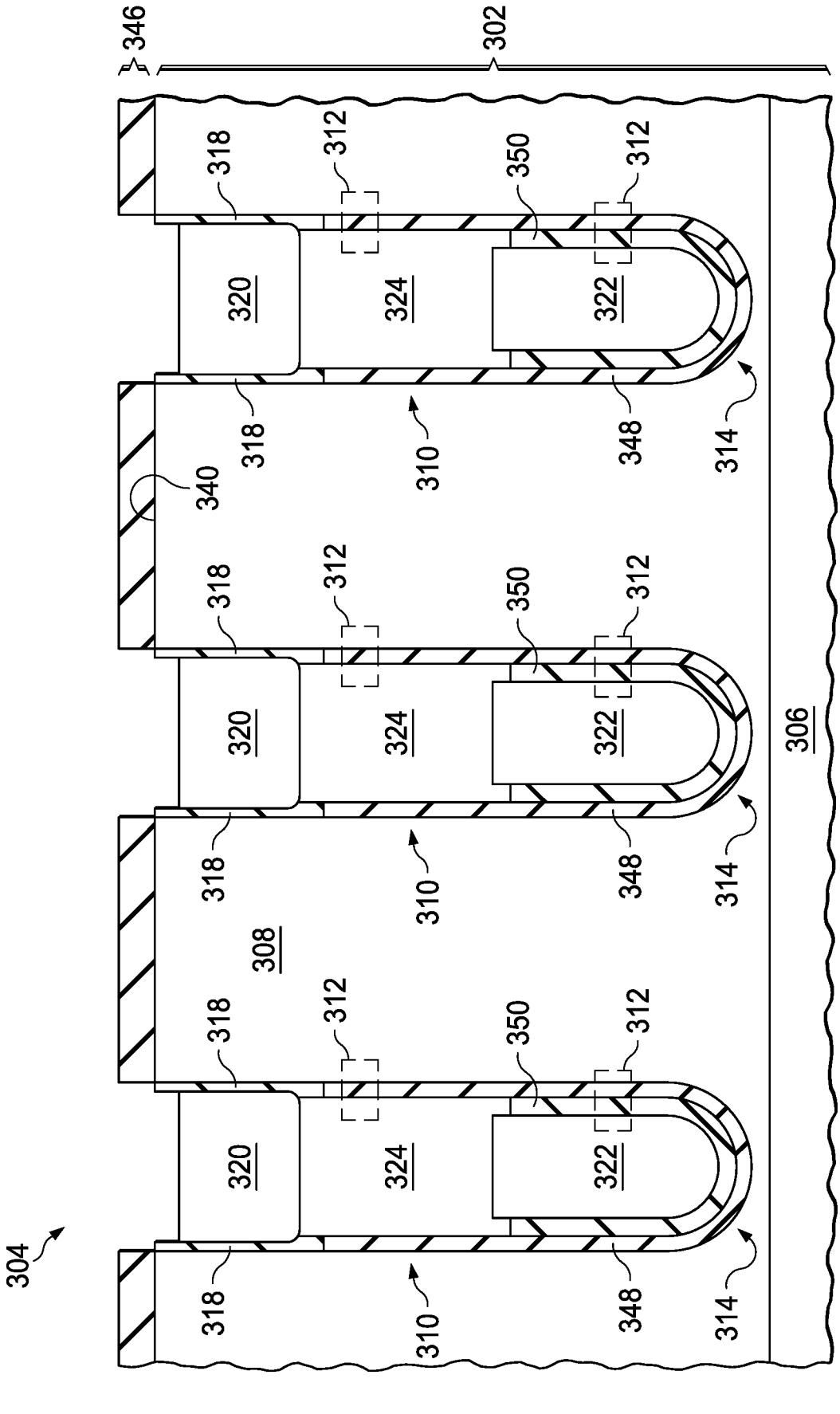
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FIG. 4E

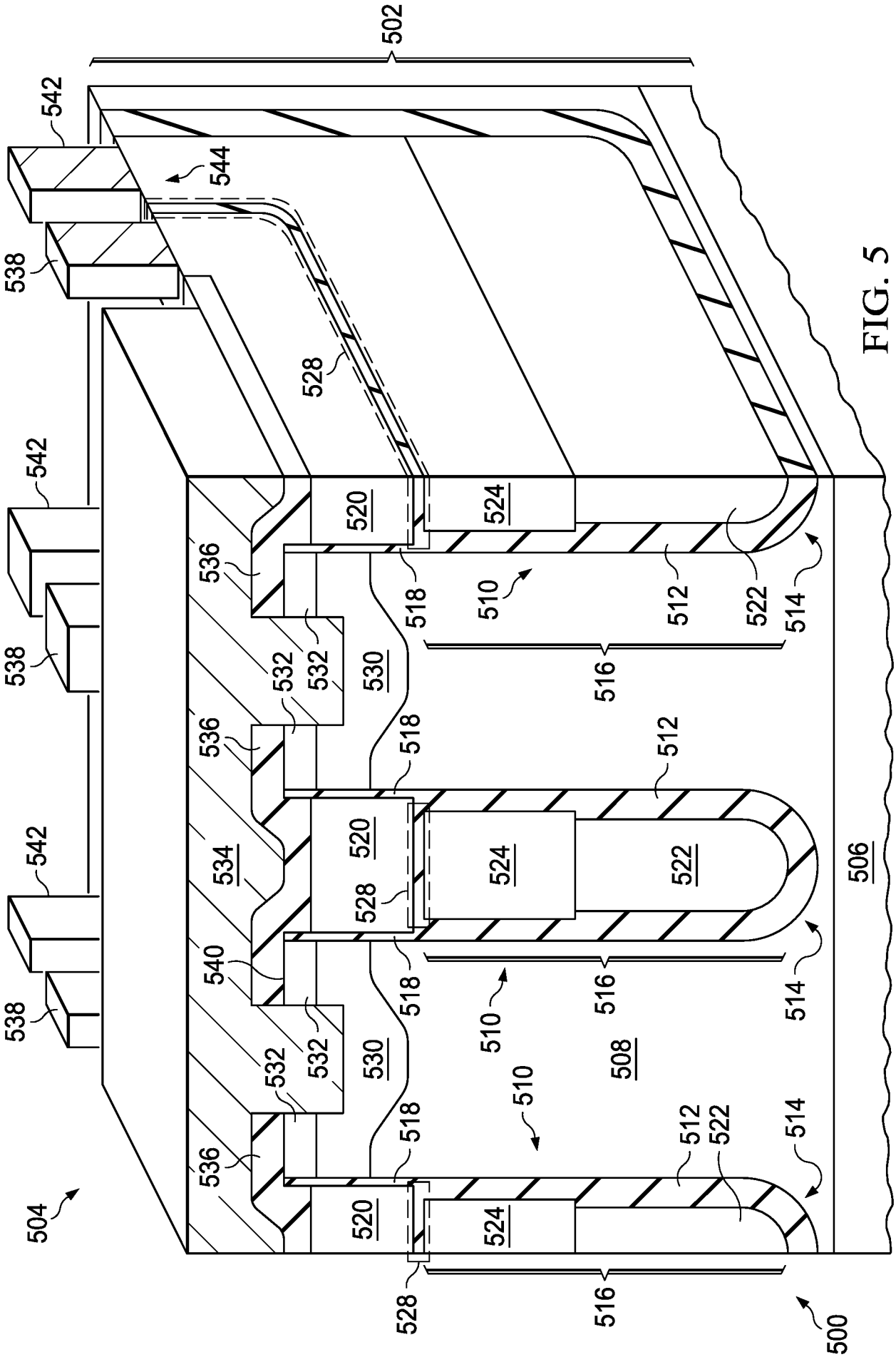
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FIG. 5

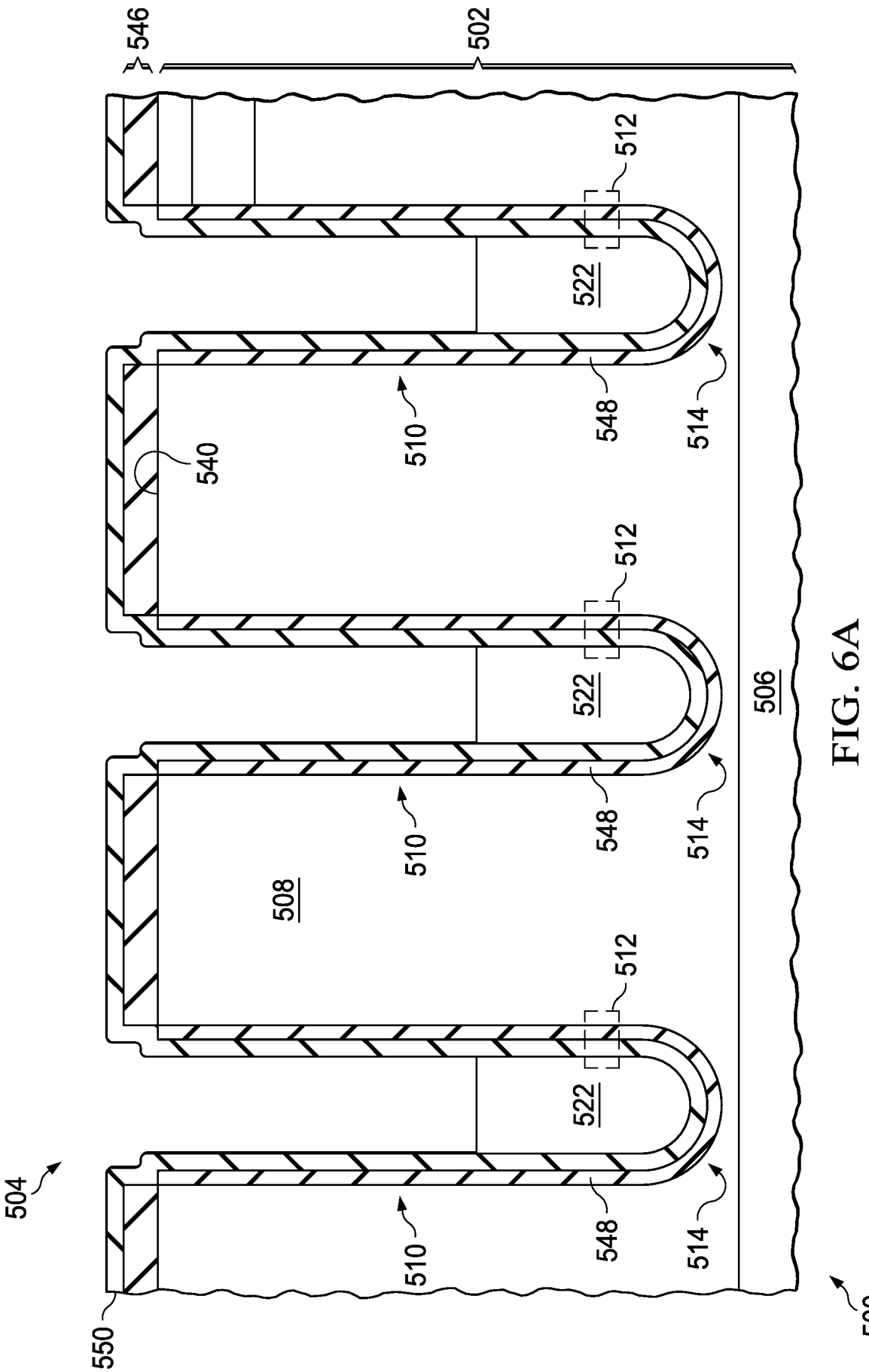

FIG. 6A

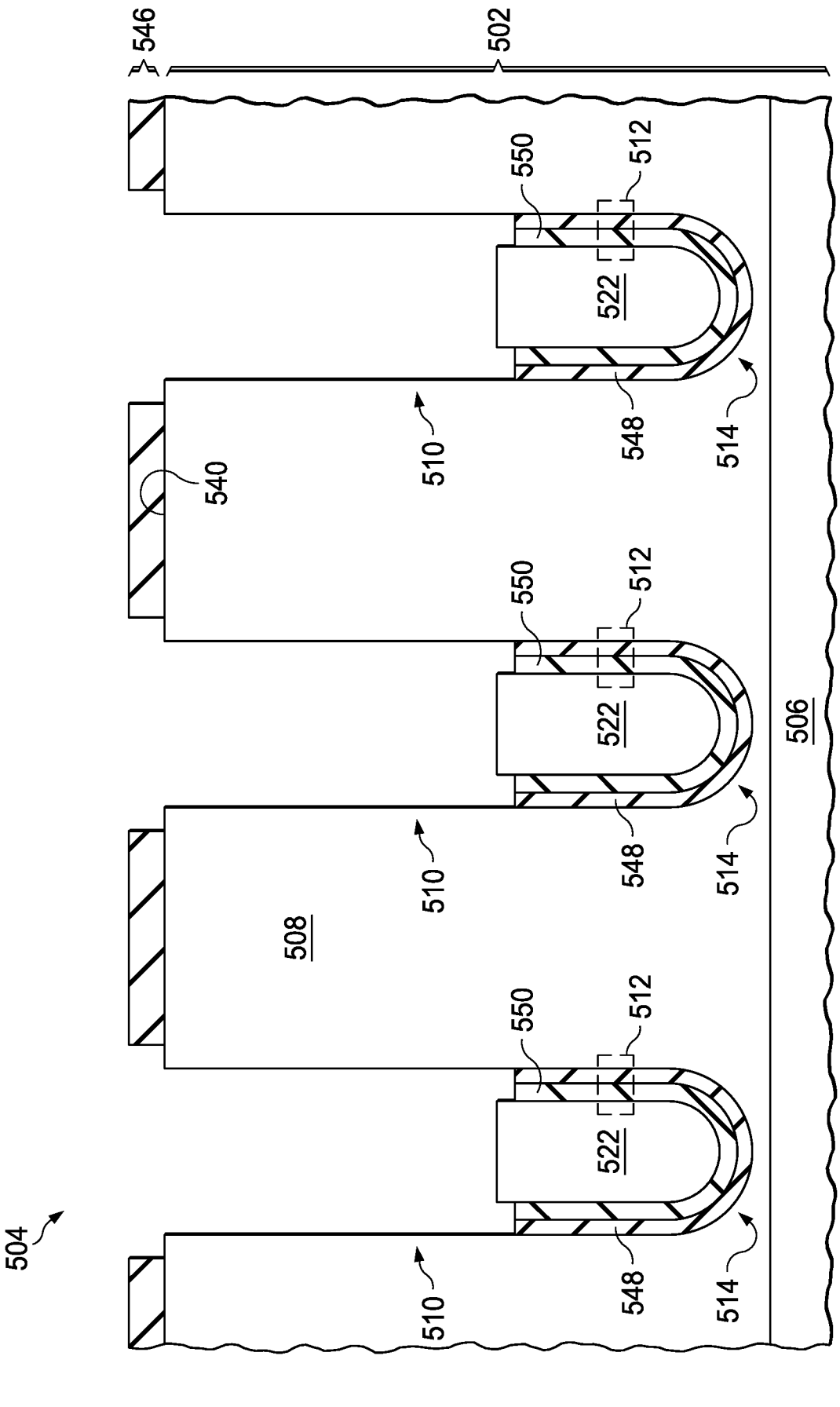

FIG. 6B

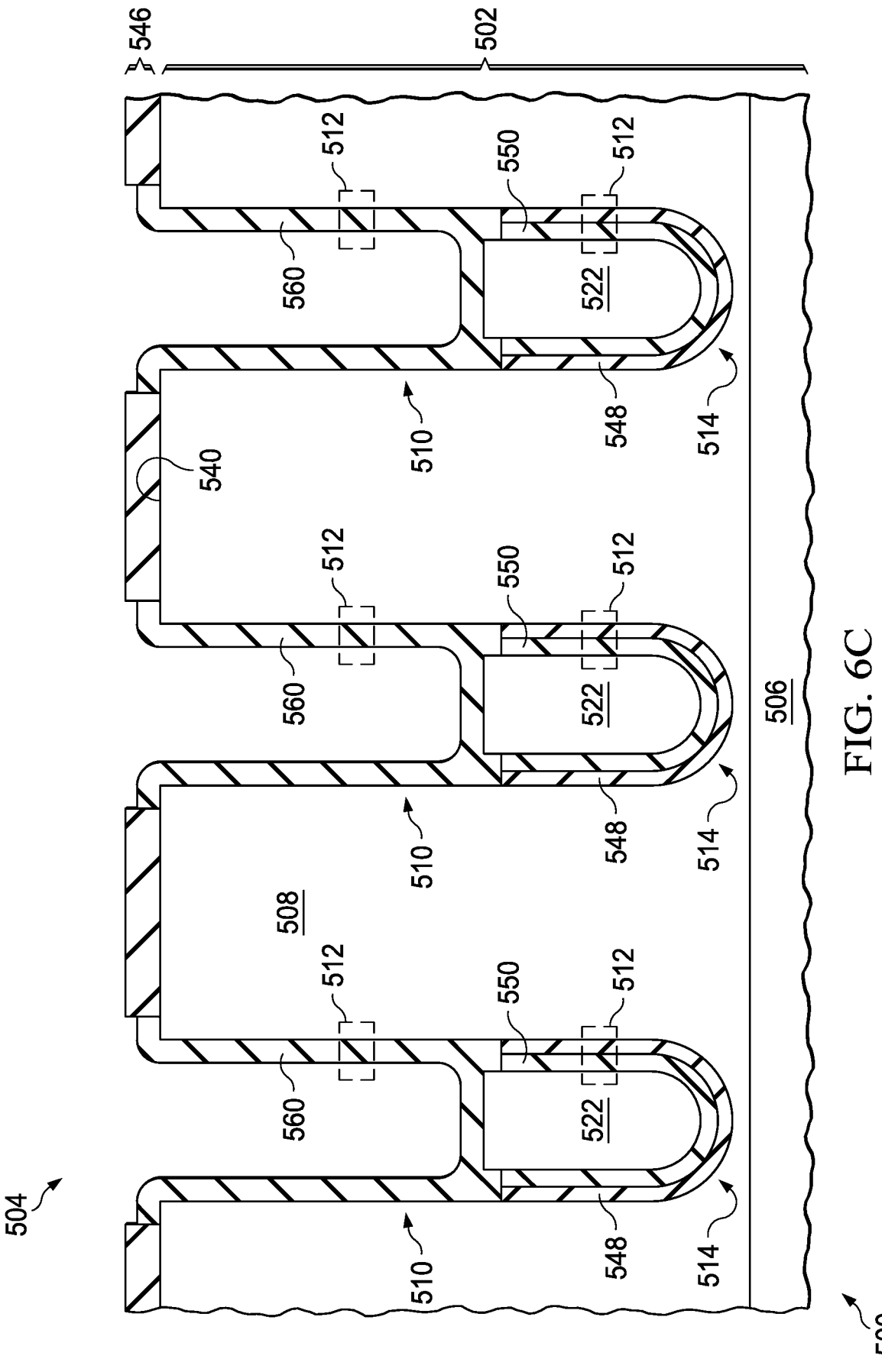

FIG. 6C

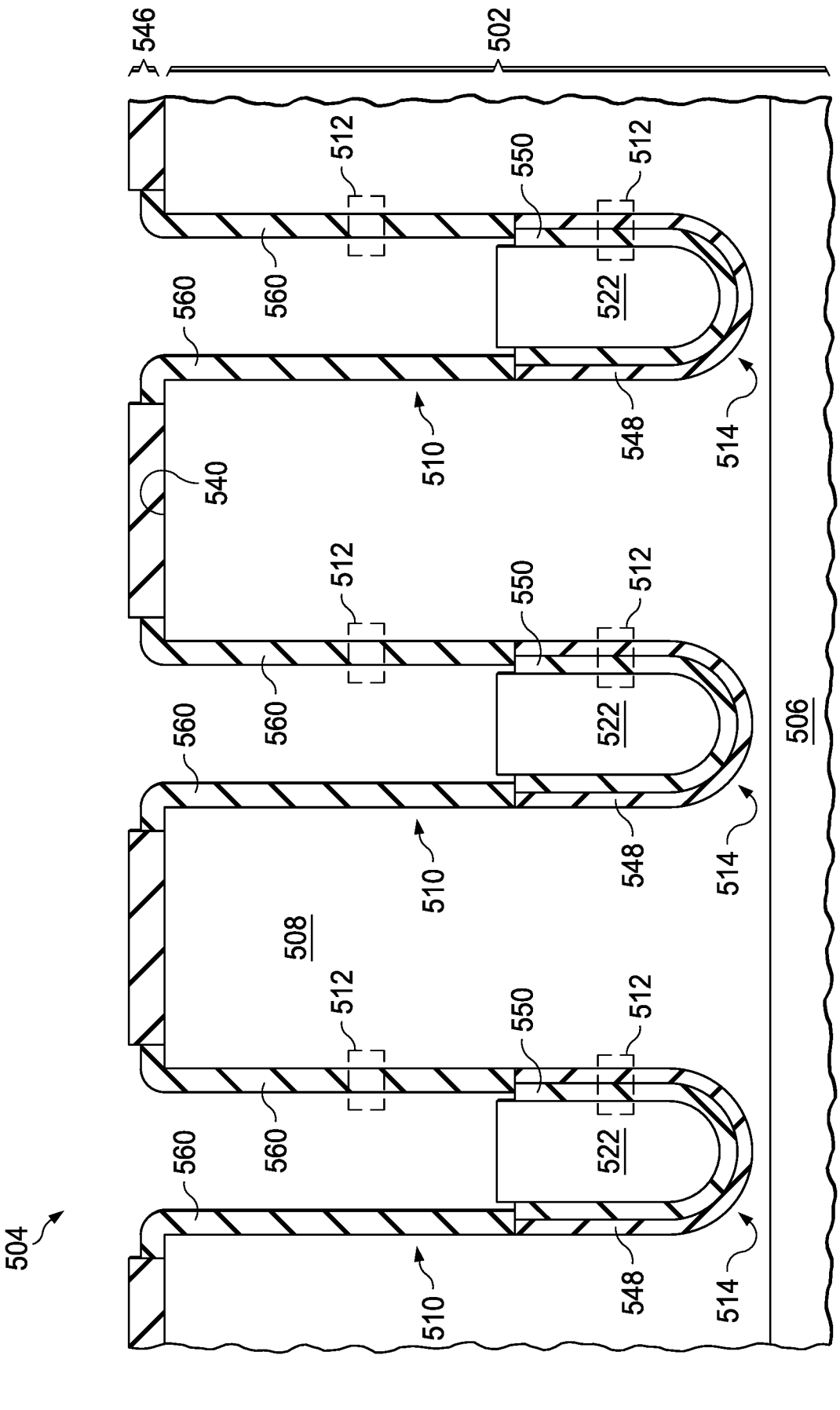
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FIG. 6D

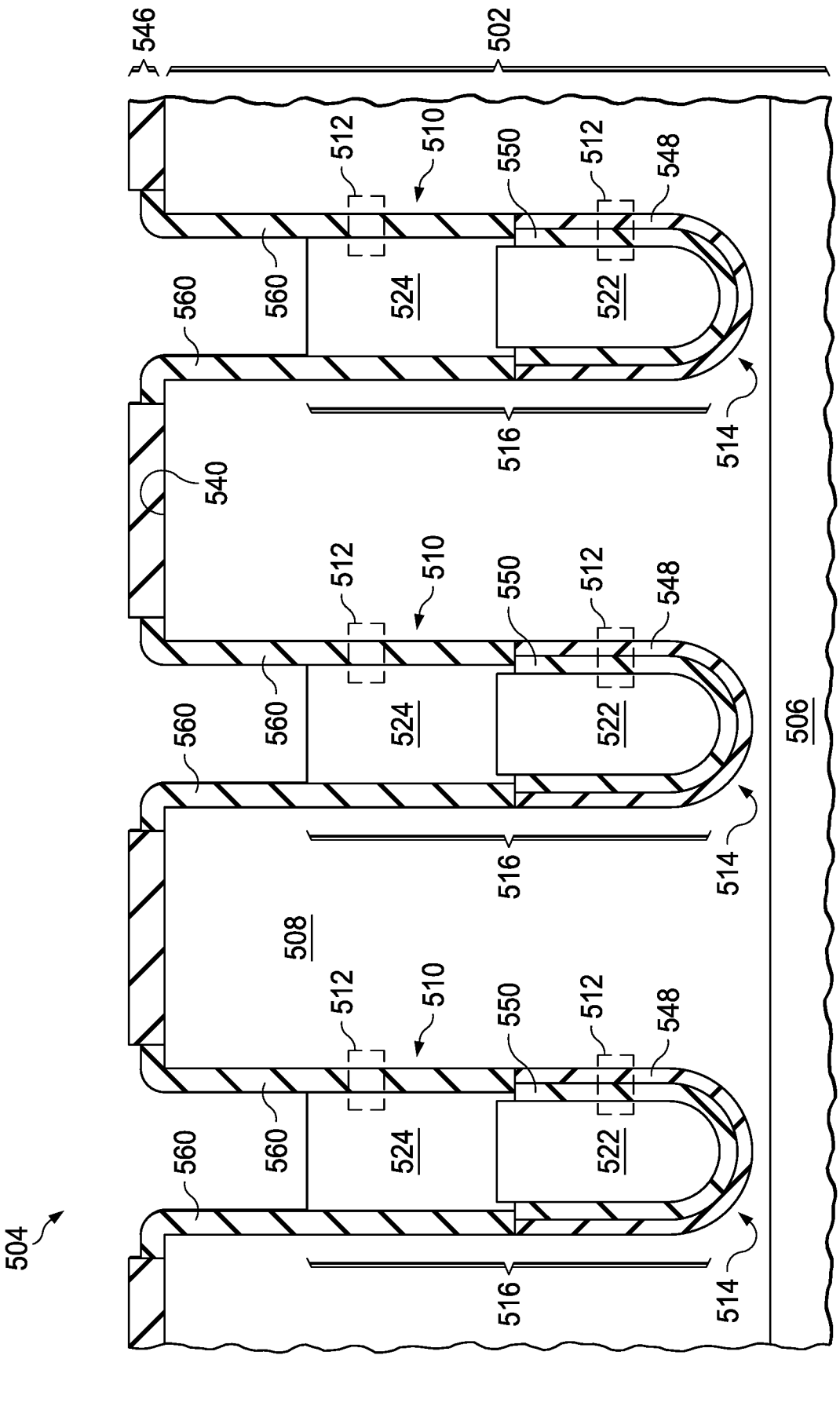
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FIG. 6E

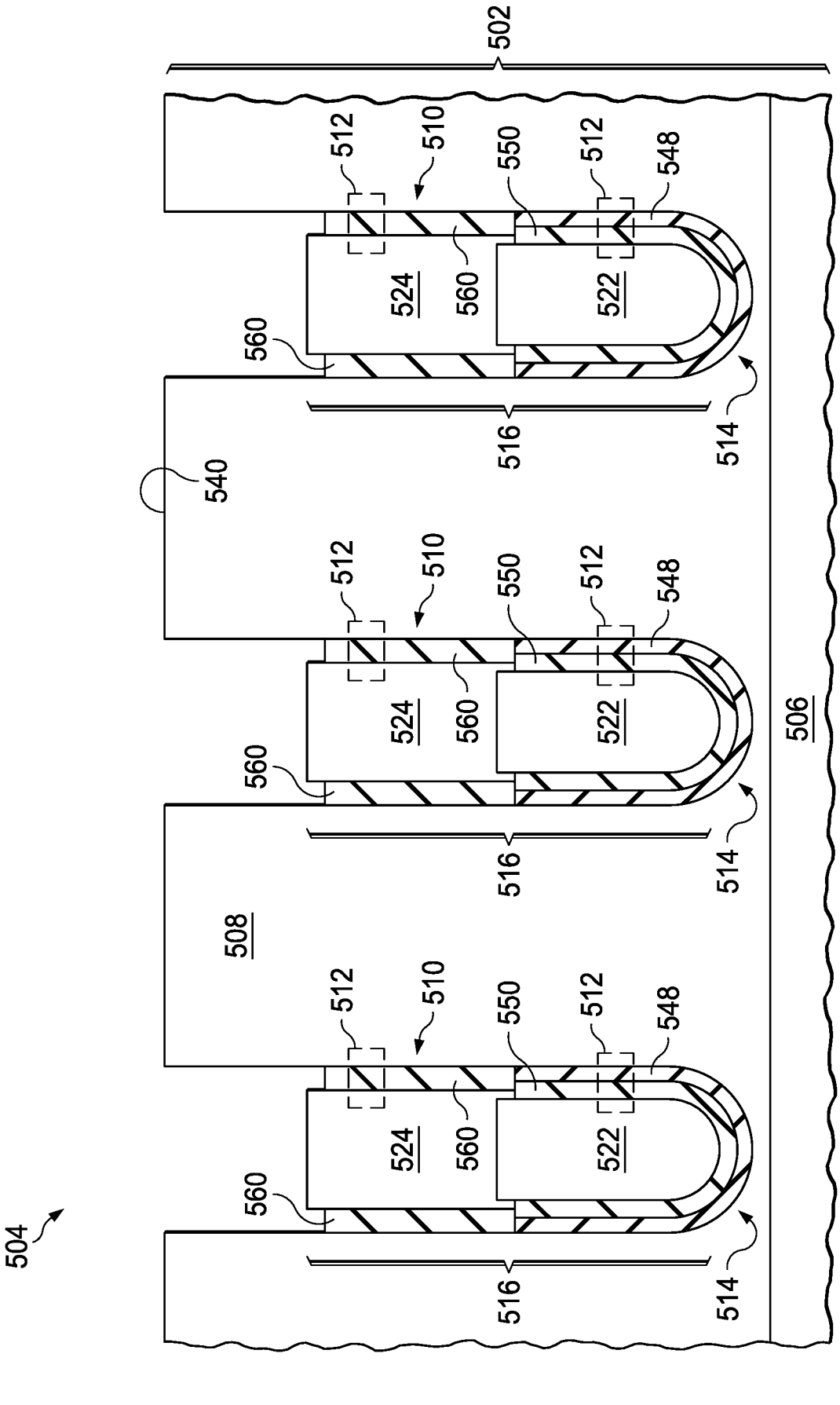
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FIG. 6F

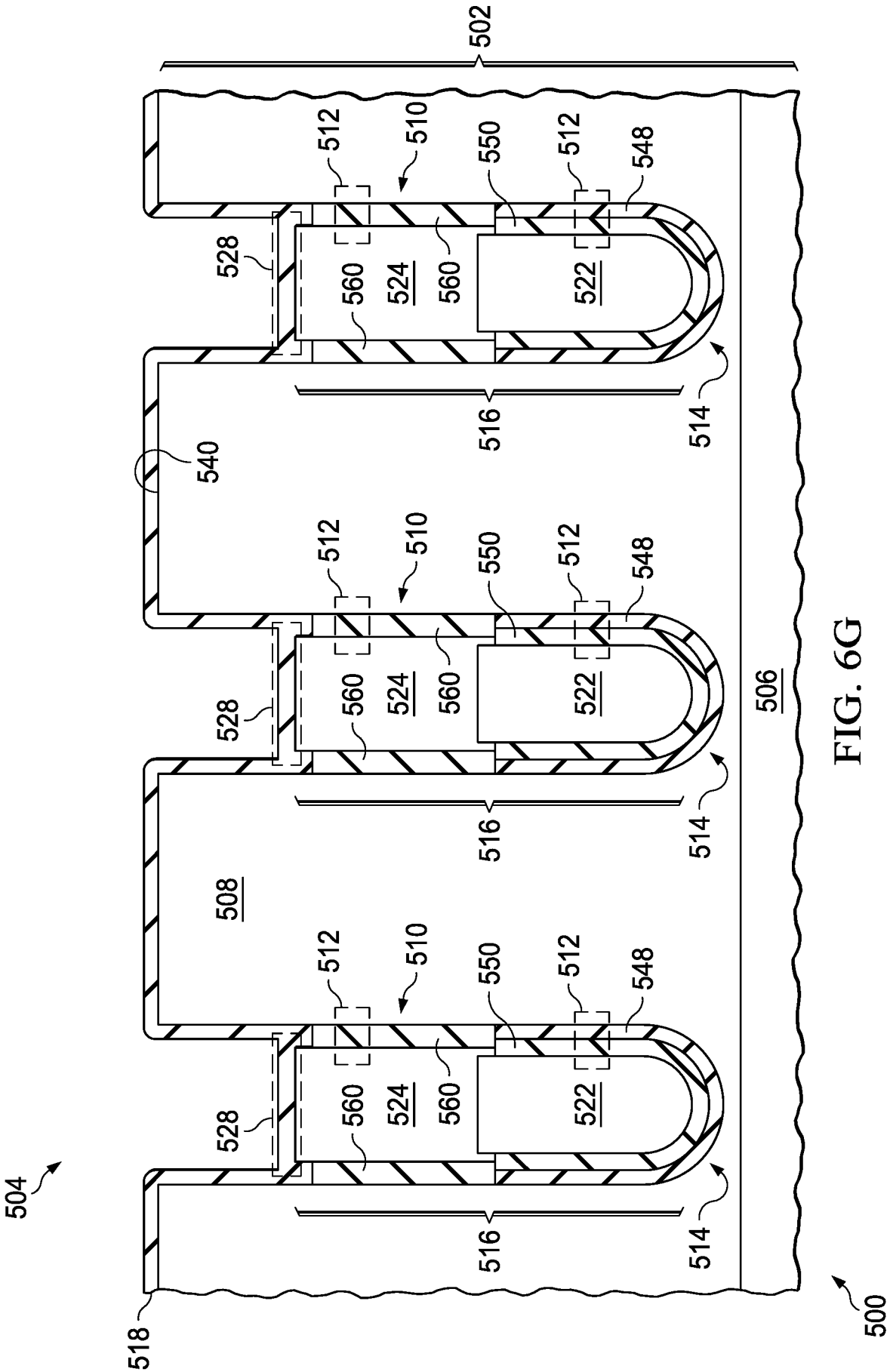
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FIG. 6G

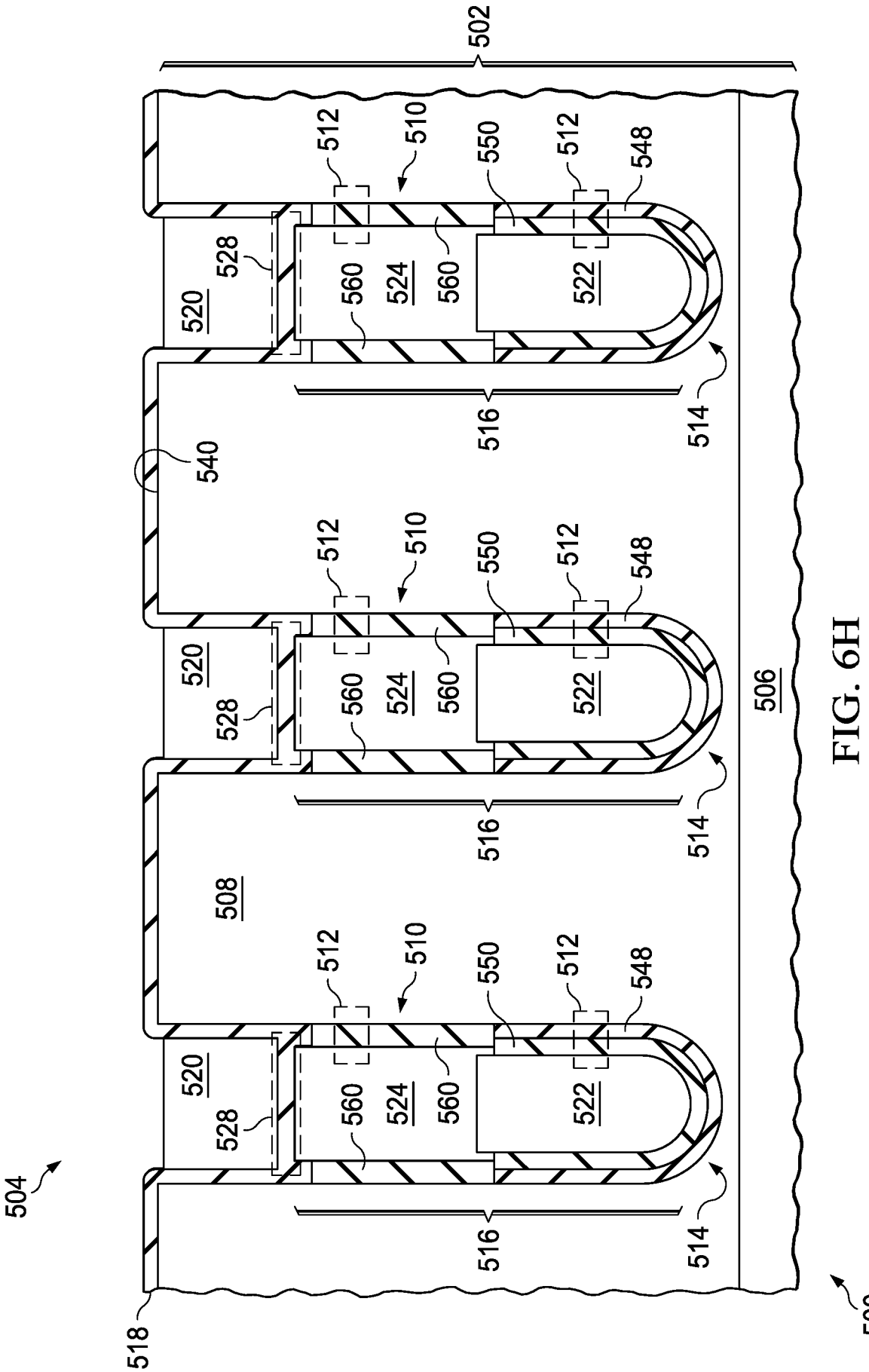
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FIG. 6H

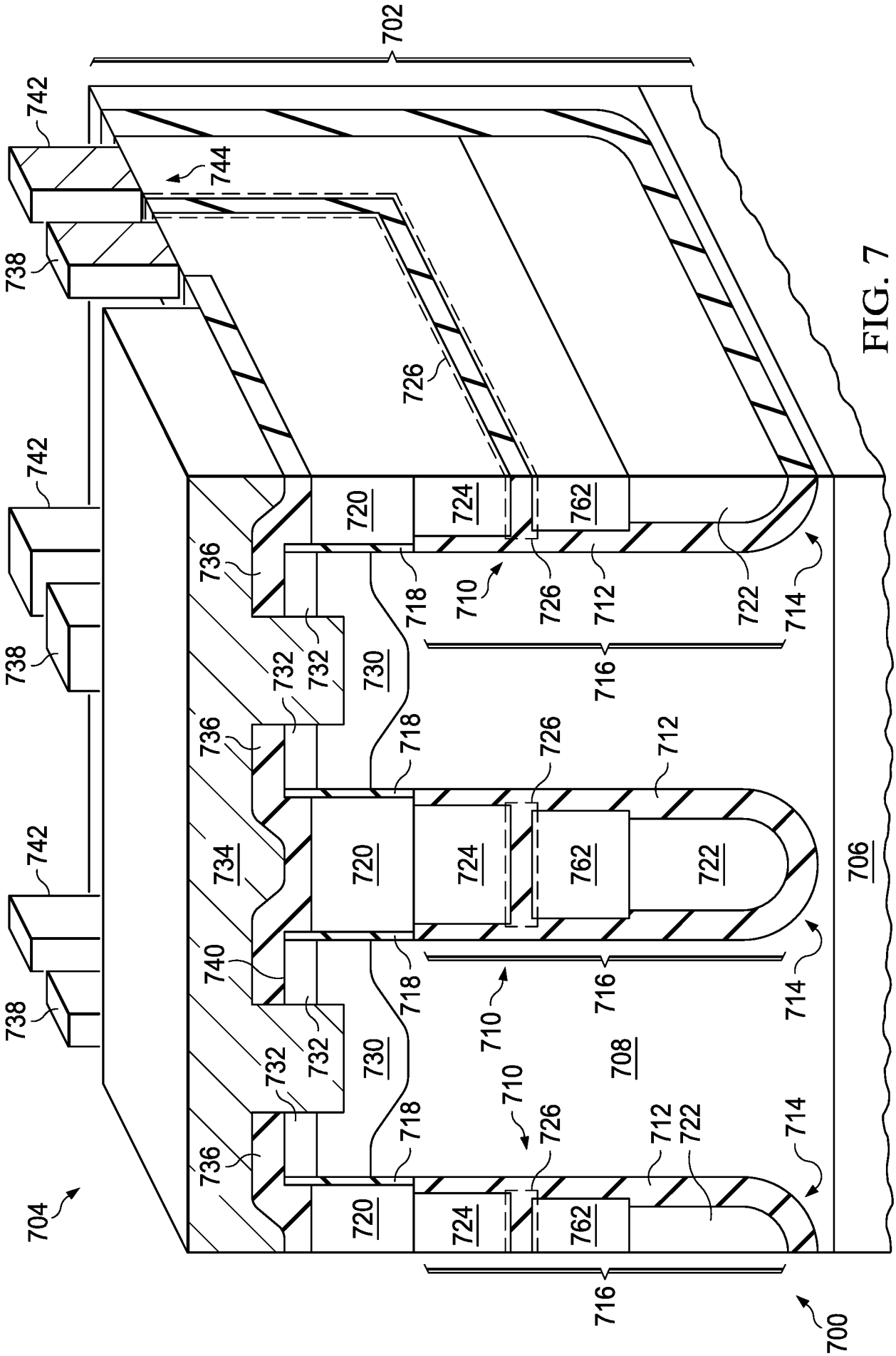
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FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2016/031517

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/28, 29/40-29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2014/138453 A1 (TEXAS INSTRUMENTS INCORPORATED et al.) 12.09.2014	1-20
A	US 2006/0267084 A1 (INFINEON TECHNOLOGIES AG) 30.11.2006	1-20
A	US 2009/0026531 A1 (INFINEON TECHNOLOGIES AUSTRIA AG) 29.01.2009	1-20
A	US 2008/0164516 A1 (MAXPOWER SEMICONDUCTOR, INC.) 10.07.2008	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 July 2016 (12.07.2016)	18 August 2016 (18.08.2016)

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