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(54) **INTEGRITY TESTS FOR MIXED ANALOG DIGITAL SYSTEMS**

INTEGRITÄTSTESTS FÜR GEMISCHTE ANALOGE DIGITALE SYSTEME

TESTS D'INTÉGRITÉ POUR SYSTÈMES ANALOGIQUES NUMÉRIQUES MIXTES

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Description

BACKGROUND

[0001] Some vehicle systems (e.g., a warning system, infotainment system, a user interface device) generate information for output to acoustical components. Digitized audio information is propagated over digital transmissions within these systems for eventual output as analog signals or sounds. These digital transmissions can encounter faults or introduce transient errors, which can propagate at intermittent or unpredictable times. Errors may be caused by many issues, and when present in an audio output, they can be unpleasant and impact driving safety if they cause distractions or mask other simultaneous warnings (e.g., chimes or announcement). Integrity checks can be performed to check whether a purely digital transmission path is inducing errors in an output. However, these techniques may not be suitable for checking mixed systems having digital and analog transmission paths, or they may be too expensive or time consuming for many validation tasks. Several days of computer simulation, and months or years of real-world road driving are not acceptable ways to verify integrity of an output from a mixed digital and analog system.

[0002] US2019/139399A1 discloses methods, systems and apparatus for functional safety systems. Specifically, the disclosure relates to validating functional safety warnings that may be communicated to an operator. Such warnings may include safety warning chimes.

[0003] US2011/299581A1 discloses a method of generating at least one test sequence for testing a data connection, the method involving selectively combining by a logic function the output sequences of a plurality of pseudo-random bit sequence (PRBS) generators, each generator having a specific number of states that is different from those of the other generators.

SUMMARY

[0004] This summary introduces simplified concepts related to integrity tests for mixed analog digital systems, as further described in the Detailed Description and conveyed by the Drawings. According to one aspect of the present invention, there is provided a device as defined in claim 1 hereinafter. In one example, at least one processor of the device is configured to check integrity of a digital transmission for an analog output of a system and output an indication of whether any errors are introduced by a digital path of the digital transmission, as opposed to an analog path of the analog output. To check the integrity, a test signal produced from a first test signal generator (TSG), for example, a pseudo random number generator (PRNG), of the system or device being tested is estimated. The test signal is injected into the digital transmission that is output on an analog path of the analog output. Then, all without direct access to the digital transmission, to estimate the test signal, a second TSG

that relies on a same test signal generation function as the first TSG is used. The second TSG is compensated, however, for a linear transfer function of the digital path of the digital transmission and the analog path of the analog output combined. Whether the estimated test signal is identifiable from the analog path of the analog output enables the at least one processor to determine if the digital path of the digital transmission is free from errors. An indication of whether any errors, including transient or static (e.g., faults), are introduced by the digital path of the digital transmission may be output. This indication can be used downstream by a warning system, infotainment system, vehicle controller, or other actor of a vehicle that may execute operations to account for, or act, based on digital transmissions that may have been corrupted.

[0005] This summary is not intended to identify essential features of the claimed subject matter, nor is it intended for use in determining the scope of the claimed subject matter. Although primarily described in the context of integrity tests for mixed analog digital systems in vehicles, the techniques for integrity tests for mixed analog digital systems, as described herein, can be applied to other applications where signal integrity and reliability are as important as processing speed, such as, computer technology, information technology, communications and mobility technology, industrial technology, manufacturing technology, power production technology, other vehicles including airplanes and marine craft, and other systems.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The details of one or more aspects of integrity tests for mixed analog digital systems are described in this document with reference to the Drawings, in which same numbers are used throughout the figures to indicate like components, and which are briefly described as follows:

FIG. 1 illustrates a conceptual diagram of an environment for a vehicle system configured to perform integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure;

FIG. 2 illustrates a conceptual diagram of a vehicle system configured to perform integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure;

FIG. 3 illustrates a flow chart of processes for performing integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure; and

FIG. 4 illustrates a conceptual diagrams of an example data flow for using integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure.

FIG. 5 illustrates a conceptual diagrams of an example data flow for using integrity tests for mixed analog digital systems, in accordance with techniques of this

disclosure.

DETAILED DESCRIPTION

INTRODUCTION

[0007] Vehicle systems are equipped with complex computer systems to make driving easier and more enjoyable; ensuring reliability of their functionality is important. Digitized audio information may be propagated within these systems from analog outputs as analog signals or sounds. Driving alerts, chimes, announcements, phone calls, entertainment content, and the like, are examples of information that is digitally transmitted before conversion and output on analog paths. These digital transmissions can introduce transient errors in the information, which can propagate at intermittent or unpredictable times. Transient errors are observable in an audio signal as audio skips, or popping/cracking sounds, may be caused by errors in a digitized sequence of information received at an analog output, or may occur because of unexplained glitches or duplicate reads from a buffer. Errors in an audio output can be unpleasant to a driver of a car, additionally, errors can impact driving safety if they cause loud sounds or are able to corrupt other simultaneous warnings (e.g., chimes or announcement). This can be especially important in self-driving vehicles that are configured to instruct an operator when the driver is to resume manual control. Failure to heed to an audible instruction causes a self-driving vehicle to pull over as a safety precaution, for instance.

[0008] Expensive and time consuming checks can be performed by conducting physical tests to evaluate long term performance. Several days of computer simulation, and several months or years of real-world on-vehicle testing may be required to finish checking and verifying operation with sufficient confidence to release it into a product. Some existing techniques for checking quality of audio outputs in a test or engineering development cycle of a vehicle typically involve checking the big six parameters, including level, frequency response, total harmonic distortion (THD), phase, cross talk, and signal to noise ratio (SNR). Each of these checks bears a risk that transient errors are not found and therefore, not debugged during development and test. Even if some of these existing checks are passed, the vehicle system remains prone to never-before-observed transient errors corrupting audio for an end user of the vehicle.

[0009] Other ways to test continuous, error free propagation of a digital transmission is known from telecommunication, in which a test signal is transmitted and compared on reception. Often used is a pseudo random bit sequence (PRBS) produced by a PRNG as the test signal. Conducting such tests in an end to end digital system can identify transient errors. However, these techniques are not applicable to a large distributed system where access to a digital transmission path is not available. Such test would find this described transient errors, but

they are not practically suited because other than in some specialized systems there is typically no easy access to the digital transmissions, unlike in telecommunications. As such, in a mixed digital and analog system distributed at different parts of a vehicle, existing techniques are not suitable for checking whether transient errors are caused in a digital transmission or due to an analog path of an analog output. Existing integrity checks for digital systems are not useful for mixed digital and analog systems and may not be suitable for replacing long term on-vehicle reliability tests. Furthermore, the described techniques enable the identification of transient errors that appear intermediately over time in the analog output, and static errors or faults that consistently reappear over time in the analog output.

EXAMPLE ENVIRONMENT

[0010] FIG. 1 illustrates a conceptual diagram of an environment 100 for a vehicle system configured to perform integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure. In the environment 100, a vehicle 102 is shown integrated with a vehicle system 104. The vehicle 102 can be any other application for a mixed digital and analog system. Non-vehicles (e.g., computers, servers, media players, sound equipment) can also include a mixed digital and analog system, such as the vehicle system 104, but for other purposes than for vehicle use. Therefore, the techniques of this disclosure may apply to other computer systems in other contexts.

[0011] The vehicle system 104 represents any mixed digital and analog system in which transient errors can propagate through digital transmissions and into an analog output. The vehicle system 104 may be implemented on a single computer card, as a single processing unit, as a system on chip, or in any other suitable architecture. Commonly referred to herein as audio systems, other types of systems can benefit from the described techniques. Any application in which a propagation path includes digital and analog forms can be checked using these techniques. The vehicle system 104 includes a device under test 106 and a test device 120.

[0012] The device under test 106 can be any component or element of the vehicle system 104 that transmits digital data for output using an analog device. The device under test 106 has an analog output 110 that is configured to receive a digital transmission 112 and produce an analog response 114 via an analog path 118. The device under test 106 may include a source of the digital transmission (e.g., an audio decoder, an audio encoder decoder) that decompresses digital audio data and then transmits the uncompressed digital data as the digital transmission 112 to the analog output 110 (e.g., a speaker device, a microphone), from which it is converted into an analog signal (e.g., sound).

[0013] Although shown as part of the same vehicle system 104 as the device under test 106, the test device 120

may exist on different hardware, or outside the vehicle 102. The test device 120 is configured to check integrity of digital transmissions from the device under test 106 without any invasive probing or procedures to the digital transmission 112 itself. The test device 120 is configured to check integrity of the digital transmission 112 from information obtained via the analog output 110 of the vehicle system 104 itself. The test device 120 may have an interface inside the vehicle 102 (e.g., a sound card input connected to the analog output 110 or other speaker of the vehicle system 104, a microphone) and may execute the integrity check from a remote workstation that executes the functionality of the test device 120 from outside the vehicle 102.

[0014] In some examples, the test device 120 is configured to check the integrity of the digital transmission 112 while the vehicle system 104 is operational and in use. This is due in part because no direct probe of the digital transmission 112 is performed. For instance, an onboard controller of the vehicle can initiate an integrity check via a software routine by calling on the test device 120 embedded in the vehicle 102. Still in some examples, the test device 120 is additionally, or alternatively, configured to check the integrity while the vehicle system is non-operational, under maintenance, or parked. Development and engineering is made easier because the digital transmission 112 can be checked in an automated fashion that does not require an expensive test bench or road test to check the performance of the vehicle system 104 under a seemingly endless possible set of environmental conditions. Further, a mechanic workstation, a charging station, a filling pump, or other off-vehicle device can instead initiate a similar integrity check with a remote terminal connection to the test device 120.

[0015] To enable the integrity check with the test device 120, the device under test 106 includes a test signal generator (TSG) 108-1. The TSG 108-1 can be a PRNG or other test sequence generator that can reliably produce a same, consistent test signal, and in the case of a PRBS, with a seemingly noisy or random pattern. During the digital transmission 112, the TSG 108-1 injects a test signal (e.g., a PRBS) into the digital transmission 112 for output by the analog output 110. The source of the digital transmission 112 may include the TSG 108-1, or the TSG 108-1 may have an input to the digital path of the digital transmission 112 to inject a test signal within the digital transmission 112 without requiring any modification to an audio decoder or other source.

[0016] The test device 120 includes or has access to a corresponding TSG 108-2 that uses a same test signal generation function as the TSG 108-1. For example, if the TSG 108-1 is a PRNG, the TSG 108-2 is also a PRNG with a same polynomial or randomization algorithm as the PRNG 108-1. This enables the TSG 108-2 to reproduce the same test signal that the TSG 108-1 produces, when given the same input parameters. The TSG 108-1 and the TSG 108-2 are matched to enable non-intrusively testing of the digital transmission 112 from analyzing only

the analog output 110.

[0017] Rather than perform exhaustive physical test or achieve unusable results from applying purely digital testing techniques, a test module 122 of the test device 120 checks the analog output 110 for errors 116 (e.g., transient errors, static errors) that are attributed to the digital transmission 112, or any other digital transmissions that can occur anywhere within the device under test 106. The test module 122 estimates the test signal generated by the TSG 108-1, using an output from the TSG 108-2 as the initial test signal estimate. However, the test module 122 further compensates the test signal estimate using a linear transfer function of a digital path of the digital transmission 112 and an analog path of the analog output 110. In this way, the test module 122 compensates the test signal estimated for the linear transfer function between the digital transmission 112 and the analog path 118. The estimated test signal can be compared against the analog response 114 to determine whether the digital transmission 112 was free from transient errors based on whether the test signal estimated with the TSG 108-2 is identifiable from the analog response 114 (an analog signal, an audio signal based on the digital transmission 112) on the analog path 118 of the analog output 110.

[0018] Based on whether a measured signal corresponds to the compensated estimated test signal (e.g., within some acceptable degree of tolerance), the test module 122 can determine whether the digital transmission 112 propagated errors or performed as expected. To this end, if unable to identify the estimated test signal, the result of this check is that it can pinpoint when errors are appearing due to the digital transmission 112. This may aid in debugging and engineering design to obtain confidence that errors are not appearing because of the analog output 110.

[0019] An indication of whether any errors are introduced by the digital transmission can be reported as an indication 124, for instance, graphically, audibly, or via a log (e.g., as indication 124-1, indication 124-1, ... indication 124-n). The test module 122 may output an indication 124-2 in case an error is observed. Else, if no errors are detected, the test module 122 may output an indication 124-1 through 124-n to indicate that the vehicle system 104 is operating as expected.

[0020] In this way, debugging an installation of the vehicle system 104 becomes easier, and therefore takes less time and is less expensive. Also, achieving reliability of a mixed analog and digital transmission system becomes less of a challenge and when obtained, it can be verified with greater confidence.

EXAMPLE ARCHITECTURE OF TEST DEVICE

[0021] FIG. 2 illustrates a conceptual diagram of a vehicle system 200 configured to perform integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure. The vehicle system 200 is an example of the vehicle system 104. Included is a device

under test 106-1, and a test device 120-1.

[0022] The device under test 106-1 includes a source 212 for the digital transmission 112. The source 212 generates the digital information that is received by the analog output 110 to elicit the analog response 114, or sound. The source 212 may include a decoder 214 configured convert compressed digital information into uncompressed audio information that is suitable for playback from the analog output 110. The decoder 214 may include the TSG 108-1, which is shown as a PRNG 108-1, and may be a separate component of the source 212. The PRNG 108-1 is configured to inject a test signal in the digital transmission 112 output by the decoder 214. That is, the PRNG 108-1 and the decoder 214 is further configured to inject the test signal into the digital transmission along with the uncompressed audio information.

[0023] The test device 120-1 includes a processor 202 and a computer-readable storage media (CRM) 204 that stores instructions, which when executed by the processor 202, implement the functions associated with the test module 122, the TSG 108-2, which is shown as a PRNG 108-2, a test interface 206, a transfer function estimator 208, and a folding block 210. The processor 202 can be any processing device, processing unit, controller, or other computer. The CRM 204 can be any type of computer storage suitable for maintaining instructions that can be executed by the processor 202 to implement the functions of the test device 120-1.

[0024] The test interface 206 receives the analog response 114 from the analog path 118 (e.g., a signal in air). The test interface 206 can be a sound card input to the test device 120, which can receive an output from the analog output 110 (or other speaker of the vehicle system 104), or in some cases, rely on a microphone input to the test interface 106. In this way, the test device 120-1 does not impact the digital transmission 112 by not having to directly probe the device under test 106; this indirect check improves confidence that the digital transmission 112 and not something else is the focus of the integrity check.

[0025] The PRNG 108-2 is tied to the transfer function estimator 208 and the folding block 210. These three logical blocks or units, use the PRNG 108-2 to measure the linear transfer function of the digital path of the digital transmission 112 and the analog path 118 of the analog output 110.

[0026] The transfer function estimator 208 obtains a test signal estimated by the PRNG 108-2. The transfer function estimator 208 then determines the linear transfer function of the digital transmission 112 and the analog path 118, combined. This linear transfer function is computed by the transfer function estimator 208 from estimating, using a cross correlation function, a phase correlation between a source of the digital transmission 112 (e.g., the decoder 214) and the first PRNG 108-1. The cross correlation can be set based on predetermined measurements of the device under test 106-1.

[0027] The folding block 210 configures the processor

202 to estimate the test signal by compensating the PRNG 108-2 for the linear transfer function of the digital path and the analog path combined, by folding the impulse response with the second PRNG. The folding block 210 also obtains the test signal estimated by the PRNG 108-2, as well as the phase correlation computed by the transfer function estimator 208. From these inputs, the folding block 210 derives an impulse response 114 of the analog output 110 associated with the test signal estimated by the transfer function estimator 208 and the PRNG 108-2.

[0028] From this, the test module 122 can deduce a realistic position in a time sequence of the digital transmission 112 at which to obtain a measurement of the analog response 114 of the analog output 110 from the analog path 118. The test module 122 obtains a measured analog response and compares it with the test signal estimated by the folding block 210 to determine whether errors are appearing in the digital transmission 112 itself.

[0029] For examples, the test module 122, when loaded from the CRM 204 and executed by the processor 202, can determine whether the test signal estimated is identifiable from the analog path compare the measured response of the analog output obtained from the test interface 206, with the test signal estimated by the folding block 210. The test module 122 determines the digital path of the digital transmission 112 to be free of errors, including transient errors or static errors, when the test signal estimated is approximately identifiable from the measured response.

[0030] In practice, the test signal injected by the PRNG 108-1 satisfies a signal tolerance level such that the test signal estimated is identifiable in the digital transmission 112 that also appears in the measured response. The signal tolerance level need to vary (e.g., increase or decrease), to adjust for variations in the vehicle system 104, the unit under test 106, and components used to implement the test device 120 as less precise modeling may fail to account for additional crosstalk that impacts the analog response 114.

[0031] The test module 122 determines the digital path of the digital transmission 112 to have errors when the test signal estimated is not identifiable from the measured response. Any significant failure in the digital transmission 112, like bit errors in a higher value bit or dropped frames or dropped buffers cause such significant deformation in the analog response that these, in addition to transient errors, can be detected

[0032] In this way, an unintrusive way to check integrity of a mixed analog digital transmission system is provided by the test device 120. The vehicle 102 may include the test device 120 within the vehicle system 104, or may interface with the test device 120, which can execute outside the vehicle 102 (e.g., during engineering or test, on a workstation in a garage).

EXAMPLE PROCESS

[0033] FIG. 3 illustrates a flow chart of processes 300 for performing integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure. The process 300 may be performed by the test device 120, the unit under test 106, or a combination of the two. The steps of the process 300 may be repeated, rearranged, omitted, or otherwise modified depending on application. For ease of description, the process 300 is performed in the context of elements of FIG. 1.

[0034] At 302, integrity of a digital transmission for an analog output of a vehicle system is checked. For example, the test module 122 of the test device 120 obtains the analog response 114 from the analog path 118 out of the analog output 110 to check integrity of the digital transmission 112 occurring within the device under test 106.

[0035] At 304, a test signal produced from a first TSG is injected into the digital transmission to the analog output. For example, the PRNG 108-1 inputs a test signal in the digital transmission 112 that is sent to the analog output 110.

[0036] At 306, a test signal generated by the first TSG is estimated using a second TSG that relies on a same test signal generation function as the first TSG. For example, the PRNG 108-2 is a mirror component to the PRNG 108-1 and able to reproduce the same test signal that the PRNG 108-1 injects in the digital transmission 112 from executing the same polynomial as the PRNG 108-1.

[0037] At 308, the test signal estimated by the second TSG is compensated using a linear transfer function computed for a digital path of the digital transmission and an analog path of the analog output. For example, the test module 122 determines the linear transfer function by estimating, using a cross correlation function, a phase correlation between a source of the digital transmission 112 (e.g., an audio decoder of the device under test 106) and the first TSG. Based on the phase correlation, the test module 122 can derive an impulse response of the analog output 110 associated with the test signal estimated. In other words, the test module 122 can determine more accurately how the test signal is likely to appear if it is free from error when measured from the analog response 114, given known relationships (linear transfer function) of the source and the analog output 110.

[0038] At 310, whether the test signal estimated is identifiable from the analog output is determined. For example, the test module 122 can cross correlate, the test signal estimated, with the analog output 110, to determine a realistic position in a time sequence of the digital transmission 112 at which to obtain a measured response of the analog output 110 from the analog path 118. Then, from comparing the measured response of the analog output 110 with the test signal estimated, the test module 122 may determine the digital path of the digital transmission to be free of errors when the test

signal estimated is approximately identifiable from the measured response (see Yes branch out of 310) and may determine the digital path of the digital transmission 112 to have errors when the test signal estimated is not identifiable from the measured response (see No branch out of 310).

[0039] If no errors are identified, at 316, an indication that the digital path is not introducing errors is output. For example, the test module 122 may cause the test device 120 to output a graphical user interface that provides confidence in the digital transmission 112.

[0040] Otherwise, if errors are identified, at 312, it is determined that the digital path is introducing errors. At 314, an indication that the digital path is introducing errors is output. For example, the test module 122 may cause the test device 120 to output a graphical user interface that provides an indication of which digital path of the vehicle system 104 includes errors or is introducing errors in the digital transmission 112.

EXAMPLE APPLICATION FOR TEST DEVICE

[0041] FIG. 4 illustrates a conceptual diagram 400 of an example data flow for using integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure. FIG. 4 shows an application for the test device 120, which can easily connect to a device under test 106-2 to verify absence of sporadic digital faults in the digital transmission 112.

[0042] A Media player or dedicated test pattern player plays a test signal (e.g., PRNG pattern of a given polynomial). A digital transportation mechanism conducts this data in real time thru the device under test 106-2 and to a processing stage executed by a sound processor.

[0043] In the processing stage (e.g., an equalizer) the sound processor sets the audio data to a neutral tuning during the test. Another transportation system delivers the audio data to a digital to analog converter and amplifier, in real time

[0044] The digital to analog converter changes the digital transmission 112 and embedded test signal to an analog signal or analog response 114. According to principal theory of digital to analog conversion theory, the analog response 114 is modified by a linear time invariant transfer function, that is not specified, or known to the test device 120.

[0045] The test system receives the analog response 114 via an analog to digital converter (e.g., a soundcard input of the test system 120) to digitalize the audio signal 114 for evaluation for errors. At the test module 122, a signal modification of the test signal estimated with the linear transfer function happens. The test module 122 has a way to characterize and compensate for the linear transfer function without direct access to the test signal injected by the device under test 106.

FURTHER APPLICATION FOR TEST DEVICE

[0046] FIG. 5 illustrates a conceptual diagram 500 of an example data flow for using integrity tests for mixed analog digital systems, in accordance with techniques of this disclosure. FIG. 5 shows an application for the test device 120, which can connect to a device under test 106-3 to verify absence of transient errors or other sporadic digital faults in the digital transmission 112. In general, as the nature of the test signal is a neutral noise sound, a subset of the bits, e.g., the four topmost bits of the PRNG can be utilized to replace the real four least significant bits of a music channel, and an analog sampled feedback of the outgoing channel can test this PRNG fraction for existence.

[0047] A Media player plays the entertainment audio content, like music. A warning chime player plays a warning message, but the lower significant bits are replaced by a PRNG of a particular polynomial. As the PRNG will acoustically sound like white noise and only the lower bits are used, it can be injected as an almost inaudible noise floor to the chime.

[0048] From the playing music, the least significant bits are removed to make room for the test pattern. Both, the music, and the chime can be added to one audio signal, and the unchanged PRNG sequence can be in the lower significant bits.

[0049] A transportation mechanism conducts this data in real time thru the computer system to a processing stage. Another transportation system delivers the audio data to an audio coder decoder, in real time

[0050] At that point the signal can be tapped at the path 118 and given to the test module 122 to confirm fault free playback of the chime. This is done by the test module 122 removing all upper bits, carrying the mix of music and chime, and extracting only the test pattern (PRNG) and used it in the test module 122 evaluation of whether the digital transmission 112 is error free. The linear transfer function compensation is performed to compensate for filters and volume settings of the processing stage (e.g., the equalizer).

[0051] Think of an example where a strong rattling sound is added when the lane departure warning of the vehicle recognized that the vehicle drifts over the lane boundary. Such sound shall suggest to the driver, the wheel are on uneven ground as it would be real if one gets to some gravel aside to the road. It is a nice way of alerting the driver without interrupting all other music. Such a warning needs to be well supervised, so in case it fails to play a safe state can be triggered, e.g., a simple warning sound generator on an independent speaker may engage. The suggested techniques are similar to injecting a watermark into the wanted sound, that has the acoustical characteristics of white noise and that can be tested for presence in an easy way to check for errors that are too seldom to be apparent from test.

[0052] While various embodiments of the disclosure are described in the foregoing description and shown in

the drawings, it is to be understood that this disclosure is not limited thereto but may be variously embodied to practice within the scope of the following claims. From the foregoing description, it will be apparent that various changes may be made without departing from the scope of the claims. Problems associated with digital transfers of information can occur in other systems besides automobile, truck, and vehicle systems. Therefore, although described as a way to improve safety and reliability of a vehicle system, the techniques of the foregoing description can be applied to other systems that would benefit from a fast integrity check of a digital transfer of information.

[0053] The use of "or" and grammatically related terms indicates non-exclusive alternatives without limitation unless the context clearly dictates otherwise. As used herein, a phrase referring to "at least one of" a list of items refers to any combination of those items, including single members. As an example, "at least one of: a, b, or c" is intended to cover a, b, c, a-b, a-c, b-c, and a-b-c, as well as any combination with multiples of the same element (e.g., a-a, a-a-a, a-a-b, a-a-c, a-b-b, a-c-c, b-b, b-b-b, b-b-c, c-c, and c-c-c or any other ordering of a, b, and c).

Claims

1. A device (120) for checking the integrity of a digital transmission (112) of a system (104), where an analog output (110) of the system (104) is configured to receive the digital transmission (112) and produce an analog output signal (114) transmitting it via an analog path (118), and where the system (104) includes a first test signal generator, TSG, (108-1) for producing a test signal using a test generation function and for injecting the test signal into the digital transmission (112) for output by the analog output (110), the device (120) comprising:

a second TSG (108-2) using same test generation function as the first TSG (108-1); and at least one processor (202) configured to check the integrity of the digital transmission (112) and output an indication (124) of whether any errors are introduced due to a digital path of the digital transmission (112) by:

estimating the test signal using the second TSG (108-2) and compensating the test signal estimated for a linear transfer function of the digital path and the analog path (118) of the analog output (110) combined, and determining whether the compensated test signal estimated corresponds to the analog output signal (114) transmitted by the analog output (110) to determine whether the digital path of the digital transmission (112) is free from errors.

2. The device (120) according to claim 1, wherein the at least one processor (202) is configured to determine whether the test signal estimated is identifiable from the analog path (118) by:

cross correlating the test signal estimated with the analog output (110) to determine a realistic position in a time sequence of the digital transmission (112) at which to obtain a measured response of the analog output (110) from the analog path (118);
 comparing the measured response of the analog output (110) with the test signal estimated;
 determining the digital path of the digital transmission (112) to be free of errors when the test signal estimated is approximately identifiable from the measured response; and
 determining the digital path of the digital transmission (112) to have errors when the test signal estimated is not identifiable from the measured response.

3. The device (120) according to claim 2, wherein the first TSG (108-1) comprises a first pseudo random bit generator, PRNG, and the test signal comprises a first PRNG that is injected by the first PRNG at least above a signal tolerance level such that the test signal estimated is identifiable in the measured response, and the second TSG (108-2) comprises a second PRNG that relies on a same polynomial function as the first PRNG.

4. The device (120) according to any preceding claim, wherein the at least one processor (202) is further configured to:
 determine the linear transfer function of the digital path and the analog path (118) combined by:

estimating, using a cross correlation function, a phase correlation between a source (212) of the digital transmission (112) and the first TSG (108-1); and
 deriving, based on the phase correlation, an impulse response of the analog output (110) associated with the test signal estimated.

5. The device (120) according to claim 4, wherein the at least one processor (202) is further configured to estimate the test signal by compensating the second TSG (108-2) for the linear transfer function of the digital path and the analog path (118) combined by folding the impulse response with the second TSG (108-2).

6. The device (120) according to any of claims 4 or 5, wherein the test signal is injected into the digital path of the digital transmission (112) by the source (212) or the first TSG (108-1).

7. The device (120) according to claim any of claims 4-6, wherein the source (212) is separate from the first TSG (108-1).

8. The device (120) according to any of claims 4-6, wherein the source (212) comprises the first TSG (108-1).

9. The device (120) according to any of claims 4-6, wherein the source (212) comprises an audio decoder configured to output uncompressed audio information into the digital transmission (112).

10. The device (120) according to claim 9, wherein the source (212) further comprises the first TSG (108-1) and the audio decoder is further configured to inject the test signal into the digital transmission (112) along with the uncompressed audio information.

11. The device (120) according to any preceding claim, wherein the errors include at least one of (i) transient errors that appear intermediately over time in the analog output (110) and (ii) faults that consistently reappear over time in the analog output (110).

12. The device (120) according to any preceding claim, wherein the analog output (110) comprises a microphone or speaker device and the analog path (118) comprises an audio signal based on the digital transmission (112).

13. The device (120) according to any preceding claim, wherein the system (104) comprises a vehicle system installed on a vehicle, the device is separate from the vehicle, and the at least one processor is configured to check the integrity while the vehicle system is operational and in use.

14. The device (120) according to any of claims 1-12, wherein the system comprises a vehicle system (104) installed on a vehicle (102), the device (120) is separate from the vehicle (102), and the at least one processor (202) is configured to remotely check the integrity while the vehicle system (104) is non-operational, under maintenance, or parked.

15. The device (120) according to any of claims 1-12, wherein the device (120) comprises the system (104).

16. A computer-readable media comprising instructions that, when executed, cause computer hardware components of a vehicle system (104) to:

check the integrity of a digital transmission (112) of the vehicle system (104), where an analog output (110) of the system (104) is configured to receive the digital transmission (112) and pro-

duce an analog output signal (114) transmitted by an analog path (118); and
 output an indication (124) of whether any errors are introduced due to a digital path of the digital transmission (112),
 wherein the instructions, when executed, cause the computer hardware components to check the integrity of the digital transmission (112) by:

estimating a test signal, produced from a first test signal generator, TSG, (108-1) of the system (104) using a test generation function and injected into the digital transmission for output by the analog output (110), using a second TSG (108-2) that uses the same test signal generation function as the first TSG (108-1) and compensating the test signal estimated for a linear transfer function of the digital path and an analog path (118) of the analog output (110) combined; and
 determining whether the compensated test signal estimated corresponds to the analog output signal (114) transmitted by the analog output (110) to determine whether the digital path of the digital transmission (112) is free from errors.

17. The computer-readable media according to claim 16, wherein the vehicle system (104) comprises the computer hardware components, the vehicle system (104) and the computer hardware components are part of the vehicle (102), and the computer hardware components are configured check the integrity while the vehicle system (104) is operational and in use.

18. The computer-readable media according to claim 16, wherein the vehicle system (104) is part of the vehicle (102), the computer hardware components are separate from the vehicle (102) and the vehicle system (104), and the computer hardware components are configured check the integrity while the vehicle (102) is non-operational, in a maintenance mode, unoccupied, or parked.

19. A method for checking integrity of a digital transmission of a system (104), where an analog output (110) of the system (104) is configured to receive the digital transmission (112) and produce an analog output signal (114) transmitted by an analog path (118), the method comprising:

estimating a test signal, produced from a first test signal generator, TSG, (108-1) of the system (104) using a test generation function and injected into the digital transmission (112) for output by the analog output (110), using a second TSG (108-2) that uses the same test signal

generation function as the first TSG (108-1) and compensating the test signal estimated for a linear transfer function of the digital path and an analog path (118) of the analog output (110) combined;
 determining whether the compensated test signal estimated corresponds to the analog output signal (114) transmitted by the analog output (110) to determine whether the digital path of the digital transmission (112) is free from errors; and
 outputting an indication (124) of whether any errors are introduced due to a digital path of the digital transmission (112).

20. A system (104) comprising:
 a device under test (106) comprising:

an analog output (110) configured to receive a digital transmission (112) and produce an analog output signal (114) transmitted by an analog path (118);
 a digital path to the analog output (110);
 a source (212) configured to produce a digital transmission (112) on the digital path for the analog output (110);
 a first test signal generator, TSG, (108-1) for producing a test signal using a test generation function and for injecting the test signal into the digital path; and
 a test device (120) comprising:

a second TSG (108-2) that relies on a same test generation function as the first TSG (108-1); and
 at least one processor (212) configured to check integrity of the digital path of the device under test (106) by:

estimating, using the second TSG (108-2), the test signal produced from the first TSG (108-1);
 compensating the test signal estimated for a linear transfer function of the digital path and an analog path (118) of the analog output (110) combined;
 determining whether the compensated test signal estimated corresponds to the analog output signal (114) transmitted by the analog output (110) to determine whether the digital path of the digital transmission (112) is free from errors; and
 outputting an indication (124) of whether any errors are introduced due to a digital path of the digital transmission (112).

Patentansprüche

1. Gerät (120) zum Prüfen der Vollständigkeit einer digitalen Übertragung (112) eines Systems (104), wobei ein analoger Ausgang (110) des Systems (104) konfiguriert ist, die digitale Übertragung (112) zu empfangen und ein analoges Ausgangssignal (114) zu erzeugen und es über einen analogen Pfad (118) zu übertragen, und wobei das System (104) einen ersten Prüfsignalgenerator, PSG, (108-1) beinhaltet, um ein Prüfsignal anhand einer Testgenerierungsfunktion zu erzeugen, und um das Prüfsignal in die digitale Übertragung (112) für die Ausgabe über den analogen Ausgang (110) zu injizieren, das Gerät (120) umfassend:

Einen zweiten PSG (108-2) mit derselben Testgenerierungsfunktion wie bei dem ersten PSG (108-1); und mindestens einen Prozessor (202), der konfiguriert ist, die Vollständigkeit der digitalen Übertragung (112) zu prüfen und eine Anzeige (124) dazu auszugeben, ob Fehler über einen digitalen Pfad der digitalen Übertragung (112) durch Folgendes eingeführt wurden:

Schätzen des Prüfsignals unter Verwendung des zweiten PSG (108-2) und Ausgleichen des geschätzten Prüfsignals für eine lineare Übertragungsfunktion des digitalen Pfads und des analogen Pfads (118) des analogen Ausgangs (110) zusammen, und

Bestimmen, ob das geschätzte ausgeglichene Prüfsignal dem analogen Ausgangssignal (114) entspricht, das über den analogen Ausgang (110) übertragen wurde, um zu bestimmen, ob der digitale Pfad der digitalen Übertragung (112) frei von Fehlern ist.

2. Gerät (120) nach Anspruch 1, wobei der mindestens eine Prozessor (202) konfiguriert ist, zu bestimmen, ob das geschätzte Prüfsignal von dem analogen Pfad (118) durch Folgendes identifiziert werden kann:

Kreuzkorrelieren des geschätzten Prüfsignals mit dem analogen Ausgang (110), um eine realistische Position in einer Zeitsequenz der digitalen Übertragung (112) zu bestimmen, an der eine gemessene Antwort des analogen Ausgangs (110) von dem analogen Pfad (118) erlangt wird;

Vergleichen der gemessenen Antwort des analogen Ausgangs (110) mit dem geschätzten Prüfsignal;

Bestimmen, dass der digitale Pfad der digitalen Übertragung (112) frei von Fehlern ist, wenn das geschätzte Prüfsignal von der gemessenen Antwort annähernd identifizierbar ist; und

Bestimmen, dass der digitale Pfad der digitalen

Übertragung (112) Fehler aufweist, wenn das geschätzte Prüfsignal von der gemessenen Antwort nicht identifizierbar ist.

3. Gerät (120) nach Anspruch 2, wobei der erste PSG (108-1) einen ersten Pseudozufallszahlengenerator, PRNG, umfasst und das Prüfsignal einen ersten PRNG umfasst, der durch den ersten mindestens oberhalb eines Signaltoleranz-Levels liegenden PRNG injiziert wird, so dass das geschätzte Prüfsignal in der gemessenen Antwort identifizierbar ist und der zweite PSG (108-2) einen zweiten PRNG umfasst, der sich auf eine selbe polynomielle Funktion stützt wie der erste PRNG.

4. Gerät (120) nach einem der vorhergehenden Ansprüche, wobei der mindestens eine Prozessor (202) ferner für Folgendes konfiguriert ist: Bestimmen der linearen Übertragungsfunktion des digitalen Pfads und des analogen Pfads (118), kombiniert durch:

Schätzen, unter Verwendung einer Kreuzkorrelations-Funktion, einer Phasenkorrelation zwischen einer Quelle (212) der digitalen Übertragung (112) und dem ersten PSG (108-1); und Ableiten, basierend auf der Phasenkorrelation, einer Impulsantwort des analogen Ausgangs (110), der mit dem geschätzten Prüfsignal verbunden ist.

5. Gerät (120) nach Anspruch 4, wobei der mindestens eine Prozessor (202) ferner konfiguriert ist, das Prüfsignal durch Ausgleichen des zweiten PSG (108-2) für die lineare Übertragungsfunktion des digitalen Pfads und des analogen Pfads (118) zusammen zu schätzen, indem die Impulsantwort mit dem zweiten PSG (108-2) zusammengelegt wird.

6. Gerät (120) nach einem der Ansprüche 4 oder 5, wobei das Prüfsignal in den digitalen Pfad der digitalen Übertragung (112) durch die Quelle (212) oder den ersten PSG (108-1) injiziert wird.

7. Gerät (120) nach einem der Ansprüche 4-6, wobei die Quelle (212) separat von dem ersten PSG (108-1) ist.

8. Gerät (120) nach einem der Ansprüche 4-6, wobei die Quelle (212) den ersten PSG (108-1) umfasst.

9. Gerät (120) nach einem der Ansprüche 4-6, wobei die Quelle (212) einen Audio-Decoder umfasst, der konfiguriert ist, unkomprimierte Audioinformationen in die digitale Übertragung (112) auszugeben.

10. Gerät (120) nach Anspruch 9, wobei die Quelle (212) ferner den ersten PSG (108-1) umfasst und der Au-

dio-Decoder ferner konfiguriert ist, das Prüfsignal in die digitale Übertragung (112) zusammen mit der unkomprimierten Audioinformation zu injizieren.

11. Gerät (120) nach einem der vorhergehenden Ansprüche, wobei die Fehler mindestens entweder (i) transiente Fehler beinhalten, die zwischendurch über die Zeit an dem analogen Ausgang (110) erscheinen und (ii) Fehler, die konstant über die Zeit immer wieder an dem analogen Ausgang (110) auftreten. 5
12. Gerät (120) nach einem der vorhergehenden Ansprüche, wobei der analoge Ausgang (110) ein Mikrofon oder ein Lautsprechergerät umfasst und der analoge Pfad (118) ein Audiosignal basierend auf der digitalen Übertragung (112) umfasst. 10
13. Gerät (120) nach einem der vorhergehenden Ansprüche, wobei das System (104) ein in ein Fahrzeug installiertes Fahrzeugsystem umfasst, das Gerät separat von dem Fahrzeug ist und der mindestens eine Prozessor konfiguriert ist, die Vollständigkeit zu prüfen, während das Fahrzeugsystem funktionsbereit und in Betrieb ist. 20
14. Gerät (120) nach einem der Ansprüche 1-12, wobei das System ein in ein Fahrzeug (102) installiertes Fahrzeugsystem (104) umfasst, das Gerät (120) separat von dem Fahrzeug (102) ist und der mindestens eine Prozessor (202) konfiguriert ist, per Fernabfrage die Vollständigkeit zu prüfen, während das Fahrzeugsystem (104) nicht in Betrieb, in Wartung oder geparkt ist. 30
15. Gerät (120) nach einem der Ansprüche 1-12, wobei das Gerät (120) das System (104) umfasst. 35
16. Computerlesbares Medium, das Anweisungen umfasst, die, wenn sie ausgeführt werden, die Computer-Hardwarekomponenten eines Fahrzeugsystems (104) zu Folgendem veranlassen: 40

Prüfen der Vollständigkeit einer digitalen Übertragung (112) des Fahrzeugsystems (104), wobei ein analoger Ausgang (110) des Systems (104) konfiguriert ist, die digitale Übertragung (112) zu empfangen und ein analoges Ausgangssignal (114) zu erzeugen, das von einem analogen Pfad (118) übertragen wird; und 45

Ausgeben einer Anzeige (124) dazu, ob Fehler über einen digitalen Pfad der digitalen Übertragung (112) eingeführt werden, wobei die Anweisungen, wenn sie ausgeführt werden, die Computer-Hardwarekomponenten veranlassen, die Vollständigkeit der digitalen Übertragung (112) durch Folgendes zu prüfen: 50

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Schätzen eines Prüfsignals, das von einem ersten Prüfsignalgenerator, PSG, (108-1) des Systems (104) unter Verwendung einer Testgenerierungsfunktion erzeugt und in die digitale Übertragung für die Ausgabe über den analogen Ausgang (110), unter Verwendung eines zweiten PSG (108-2), injiziert wird, der dieselbe Prüfsignalgenerator-Funktion nutzt wie der erste PSG (108-1) und das geschätzte Prüfsignal für eine lineare Übertragungsfunktion des digitalen Pfads und eines analogen Pfads (118) des analogen Ausgangs (110) zusammen ausgleicht; und

Bestimmen, ob das geschätzte ausgeglichene Prüfsignal dem analogen Ausgangssignal (114) entspricht, das über den analogen Ausgang (110) übertragen wird, um zu bestimmen, ob der digitale Pfad der digitalen Übertragung (112) frei von Fehlern ist.

17. Computerlesbares Medium nach Anspruch 16, wobei das Fahrzeugsystem (104) die Computer-Hardwarekomponenten umfasst, das Fahrzeugsystem (104) und die Computer-Hardwarekomponenten Teil des Fahrzeugs (102) sind und die Computer-Hardwarekomponenten konfiguriert sind, die Vollständigkeit zu prüfen, während das Fahrzeugsystem (104) funktionsbereit und in Betrieb ist.
18. Computerlesbares Medium nach Anspruch 16, wobei das Fahrzeugsystem (104) Teil des Fahrzeugs (102) ist, die Computer-Hardwarekomponenten separat von dem Fahrzeug (102) und dem Fahrzeugsystem (104) sind und die Computer-Hardwarekomponenten konfiguriert sind, die Vollständigkeit zu prüfen, während das Fahrzeug (102) nicht in Betrieb, im Wartungsmodus, nicht belegt ist oder geparkt ist.
19. Verfahren zum Prüfen der Vollständigkeit einer digitalen Übertragung eines Systems (104), wobei ein analoger Ausgang (110) des Systems (104) konfiguriert ist, die digitale Übertragung (112) zu empfangen und ein analoges Ausgangssignal (114) zu erzeugen, das von einem analogen Pfad (118) übertragen wird; das Verfahren umfassend:

Schätzen eines Prüfsignals, das von einem ersten Prüfsignalgenerator, PSG, (108-1) des Systems (104) unter Verwendung einer Testgenerierungsfunktion erzeugt und in die digitale Übertragung (112) für die Ausgabe über den analogen Ausgang (110), unter Verwendung eines zweiten PSG (108-2), injiziert wird, der dieselbe Prüfsignalgenerator-Funktion nutzt wie der erste PSG (108-1) und das geschätzte Prüfsignal für eine lineare Übertragungsfunktion des

digitalen Pfads und eines analogen Pfads (118) des analogen Ausgangs (110) zusammen ausgleicht; und
Bestimmen, ob das geschätzte ausgeglichene Prüfsignal dem analogen Ausgangssignal (114) entspricht, das von dem analogen Ausgang (110) übertragen wird, um zu bestimmen, ob der digitale Pfad der digitalen Übertragung (112) frei von Fehlern ist; und
Ausgeben einer Anzeige (124) dazu, ob Fehler über einen digitalen Pfad der digitalen Übertragung (112) eingeführt werden.

20. System (104) umfassend:

Device under Test (106), umfassend:

Einen analogen Ausgang (110), der konfiguriert ist, eine digitale Übertragung (112) zu empfangen und ein analoges Ausgangssignal (114) zu erzeugen, das über einen analogen Pfad (118) übertragen wird;
einen digitalen Pfad zu dem analogen Ausgang (110);
eine Quelle (212), die konfiguriert ist, eine digitale Übertragung (112) auf dem digitalen Pfad für den analogen Ausgang (110) zu erzeugen;
einen ersten Prüfsignalgenerator, PSG, (108-1), um ein Prüfsignal unter Verwendung einer Testgenerierungsfunktion zu erzeugen und das Prüfsignal in den digitalen Pfad zu injizieren;
und ein Prüfgerät (120), umfassend:

Einen zweiten PSG (108-2), der sich auf dieselbe Testgenerierungsfunktion stützt wie der erste PSG (108-1); und
mindestens ein Prozessor (212), der konfiguriert ist, die Vollständigkeit des digitalen Pfads des Device under Test (106) durch Folgendes zu prüfen:
Schätzen, unter Verwendung des zweiten PSG (108-2), des von dem ersten PSG (108-1) erzeugten Prüfsignals;

Ausgleichen des geschätzten Prüfsignals für eine lineare Übertragungsfunktion des digitalen Pfads und des analogen Pfads (118) des analogen Ausgangs (110) zusammen;
Bestimmen, ob das geschätzte ausgeglichene Prüfsignal dem analogen Ausgangssignal (114) entspricht, das über den analogen Ausgang (110) übertragen wurde, um zu bestimmen, ob der digitale Pfad der digitalen Übertragung (112) frei von Fehlern ist; und
Ausgeben einer Anzeige (124) dazu, ob Fehler über einen digitalen Pfad der digitalen Übertragung (112) eingeführt werden.

Revendications

1. Dispositif (120) destiné à vérifier l'intégrité d'une transmission numérique (112) d'un système (104), où une sortie analogique (110) du système (104) est configurée pour recevoir la transmission numérique (112) et produire un signal de sortie analogique (114) le transmettant par l'intermédiaire d'une voie analogique (118), et où le système (104) comporte un premier générateur de signal de test, TSG (108-1) destiné à produire un signal de test à l'aide d'une fonction de génération de test et pour injecter le signal de test dans la transmission numérique (112) pour émettre par la sortie analogique (110), le dispositif (120) comprenant :
un second TSG (108-2) à l'aide de la même fonction de génération de test que le premier TSG (108-1) ;
et au moins un processeur (202) configuré pour vérifier l'intégrité de la transmission numérique (112) et émettre une indication (124) si oui ou non de quelques erreurs sont introduites en raison de la voie numérique de la transmission numérique (112) par :
l'estimation du signal de test à l'aide du second TSG (108-2) et la compensation du signal de test estimé pour une fonction de transfert linéaire de la voie numérique et de la voie analogique (118) de la sortie analogique (110) combinée, et la détermination si le signal de test estimé compensé correspond au signal de sortie analogique (114) transmis par la sortie analogique (110) pour déterminer si la voie numérique de la transmission numérique (112) est exempte d'erreurs.
2. Dispositif (120) selon la revendication 1, dans lequel ledit au moins un processeur (202) est configuré pour déterminer si le signal de test estimé est identifiable à partir de la voie analogique (118) par :
la corrélation croisée du signal de test estimé avec la sortie analogique (110) pour déterminer une position réaliste dans une séquence temporelle de la transmission numérique (112) à laquelle obtenir une réponse mesurée de la sortie analogique (110) à partir de la voie analogique (118) ;
la comparaison de la réponse mesurée de la sortie analogique (110) avec le signal de test estimé ;
la détermination que la voie numérique de la transmission numérique (112) est exempte d'erreurs lorsque le signal de test estimé est approximativement identifiable à partir de la réponse mesurée ; et
la détermination que la voie numérique de la transmission numérique (112) présente des erreurs lorsque le signal de test estimé n'est pas identifiable à partir de la réponse mesurée.

3. Dispositif (120) selon la revendication 2, dans lequel le premier TSG (108-1) comprend un premier générateur de bits pseudo-aléatoires, PRNG, et le signal de test comprend un premier PRNG qui est injecté par le premier PRNG au moins au-dessus d'un niveau de tolérance du signal de sorte que le signal de test estimé est identifiable dans la réponse mesurée, et le second TSG (108-2) comprend un second PRNG qui repose sur une même fonction polynomiale que le premier PRNG.
4. Dispositif (120) selon une quelconque revendication précédente, dans lequel ledit au moins un processeur (202) est configuré en outre pour :
déterminer la fonction de transfert linéaire de la voie numérique et de la voie analogique (118) combinées par :
l'estimation, à l'aide d'une fonction de corrélation croisée, d'une corrélation de phase entre une source (212) de la transmission numérique (112) et le premier TSG (108-1) ; et
la dérivation, en fonction de la corrélation de phase, une réponse impulsionnelle de la sortie analogique (110) associée au signal de test estimé.
5. Dispositif (120) selon la revendication 4, dans lequel ledit au moins un processeur (202) est configuré en outre pour estimer le signal de test par la compensation du second TSG (108-2) pour la fonction de transfert linéaire de la voie numérique et de la voie analogique (118) combinée en pliant la réponse d'impulsion avec le second TSG (108-2).
6. Dispositif (120) selon une quelconque des revendications 4 ou 5, dans lequel le signal de test est injecté dans la voie numérique de la transmission numérique (112) par la source (212) ou le premier TSG (108-1).
7. Dispositif (120) selon l'une des revendications 4 à 6, dans lequel la source (212) est séparée du premier TSG (108-1).
8. Dispositif (120) selon l'une des revendications 4 à 6, dans lequel la source (212) comprend le premier TSG (108-1).
9. Dispositif (120) selon l'une des revendications 4 à 6, dans lequel la source (212) comprend un décodeur audio configuré pour émettre des informations audio non compressées dans la transmission numérique (112).
10. Dispositif (120) selon la revendication 9, dans lequel la source (212) comprend en outre le premier TSG (108-1) et le décodeur audio est configuré en outre pour injecter le signal de test dans la transmission numérique (112) ainsi qu'avec les informations audio non compressées.
11. Dispositif (120) selon une quelconque revendication précédente, dans lequel les erreurs comprennent au moins l'une des deux catégories suivantes parmi (i) les erreurs transitoires qui apparaissent de façon intermittente au fil du temps dans la sortie analogique (110) et (ii) les défauts qui réapparaissent de façon constante dans la sortie analogique (110) au fil du temps.
12. Dispositif (120) selon une quelconque revendication précédente, dans lequel la sortie analogique (110) comprend un dispositif de microphone ou de haut-parleur et la voie analogique (118) comprend un signal audio basé sur la transmission numérique (112).
13. Dispositif (120) selon une quelconque revendication précédente, dans lequel le système (104) comprend un système de véhicule installé sur un véhicule, le dispositif est séparé du véhicule, et ledit au moins un processeur est configuré pour vérifier l'intégrité pendant que le système de véhicule est fonctionnel et lors de l'utilisation.
14. Dispositif (120) selon l'une quelconque des revendications 1 à 12, dans lequel le système comprend un système de véhicule (104) installé sur un véhicule (102), le dispositif (120) est séparé du véhicule (102), et ledit au moins un processeur (202) est configuré pour vérifier l'intégrité à distance pendant que le système de véhicule (104) n'est pas fonctionnel, est en cours de maintenance ou stationné.
15. Dispositif (120) selon l'une quelconque des revendications 1 à 12, dans lequel le dispositif (120) comprend le système (104).
16. Support lisible par ordinateur comprenant des instructions qui, lorsqu'elles sont exécutées, amènent les composants de matériel informatique d'un système de véhicule (104) à :
vérifier l'intégrité d'une transmission numérique (112) du système du véhicule (104), où une sortie analogique (110) du système (104) est configurée pour recevoir la transmission numérique (112) et produire un signal de sortie analogique (114) transmis par une voie analogique (118) ; et émettre une indication (124) si oui ou non de quelconques erreurs sont introduites en raison d'une voie numérique de la transmission numérique (112),
dans lequel les instructions, lorsqu'elles sont exécutées, amènent les composants de maté-

riel informatique à vérifier l'intégrité de la transmission numérique (112) par :

l'estimation d'un signal de test, produit par un premier générateur de signal de test, TSG (108-1) du système (104) à l'aide d'une fonction de génération de test et injecté dans la transmission numérique destinée à émettre par la sortie analogique (110), à l'aide d'un second TSG (108-2) qui utilise la même fonction de génération de signal de test que le premier TSG (108-1) et la compensation du signal de test estimé destiné à une fonction de transfert linéaire de la voie numérique et d'une voie analogique (118) de la sortie analogique (110) combinées ; et la détermination si le signal de test estimé compensé correspond au signal de sortie analogique (114) transmis par la sortie analogique (110) pour déterminer si la voie numérique de la transmission numérique (112) est exempte d'erreurs.

17. support lisible par ordinateur selon la revendication 16, dans lequel le système de véhicule (104) comprend les composants de matériel informatique, le système de véhicule (104) et les composants de matériel informatique font partie du véhicule (102), et les composants de matériel informatique sont configurés pour vérifier l'intégrité pendant que le système de véhicule (104) est fonctionnel et lors de l'utilisation.

18. Support lisible par ordinateur selon la revendication 16, dans lequel le système de véhicule (104) fait partie du véhicule (102), les composants de matériel informatique sont séparés du véhicule (102) et du système de véhicule (104) et les composants de matériel informatique sont configurés pour vérifier l'intégrité pendant que le véhicule (102) n'est pas fonctionnel, en mode de maintenance, inoccupé ou stationné.

19. Procédé destiné à vérifier l'intégrité d'une transmission numérique d'un système (104), où une sortie analogique (110) du système (104) est configurée pour recevoir la transmission numérique (112) et produire un signal de sortie analogique (114) transmis par une voie analogique (118). le procédé comprenant :

l'estimation d'un signal de test, produit par un premier générateur de signal de test, TSG, (108-1) du système (104) à l'aide d'une fonction de génération de test et injecté dans la transmission numérique (112) destinée à émettre par la sortie analogique (110), à l'aide d'un second

TSG (108-2) qui utilise la même fonction de génération de signal de test que le premier TSG (108-1) et la compensation du signal de test estimé destiné à une fonction de transfert linéaire de la voie numérique et d'une voie analogique (118) de la sortie analogique (110) combinées ; la détermination si le signal de test estimé compensé correspond au signal de sortie analogique (114) transmis par la sortie analogique (110) pour déterminer si la voie numérique de la transmission numérique (112) est exempte d'erreurs ; et l'émission d'une indication (124) si oui ou non de quelconques erreurs sont introduites en raison d'une voie numérique de la transmission numérique (112).

20. Système (104) comprenant :
un dispositif sous test (106) comprenant :

une sortie analogique (110) configurée pour recevoir une transmission numérique (112) et produire un signal de sortie analogique (114) transmis par une voie analogique (118) ;
une voie numérique vers la sortie analogique (110) ;
une source (212) configurée pour produire une transmission numérique (112) sur la voie numérique pour la sortie analogique (110) ;
un premier générateur de signal de test, TSG (108-1) destiné à produire un signal de test à l'aide d'une fonction de génération de test et pour injecter le signal de test dans la voie numérique ; et
un dispositif de test (120) comprenant :

un second TSG (108-2) qui relie sur la même fonction de génération de test que le premier TSG (108-1) ; et
au moins un processeur (212) configuré pour vérifier l'intégrité de la voie numérique du dispositif sous test (106) par :
l'estimation, à l'aide du second TSG (108-2), du signal de test produit par le premier TSG (108-1) ;

la compensation du signal de test estimé pour une fonction de transfert linéaire de la voie numérique et de la voie analogique (118) de la sortie analogique (110) combinée ;
la détermination si le signal de test estimé compensé correspond au signal de sortie analogique (114) transmis par la sortie analogique (110) pour déterminer si la voie numérique de la transmission numérique (112) est exempte d'erreurs ; et
l'émission d'une indication (124) si oui ou non de quelconques erreurs sont introduites en rai-

son d'une voie numérique de la transmission numérique (112).

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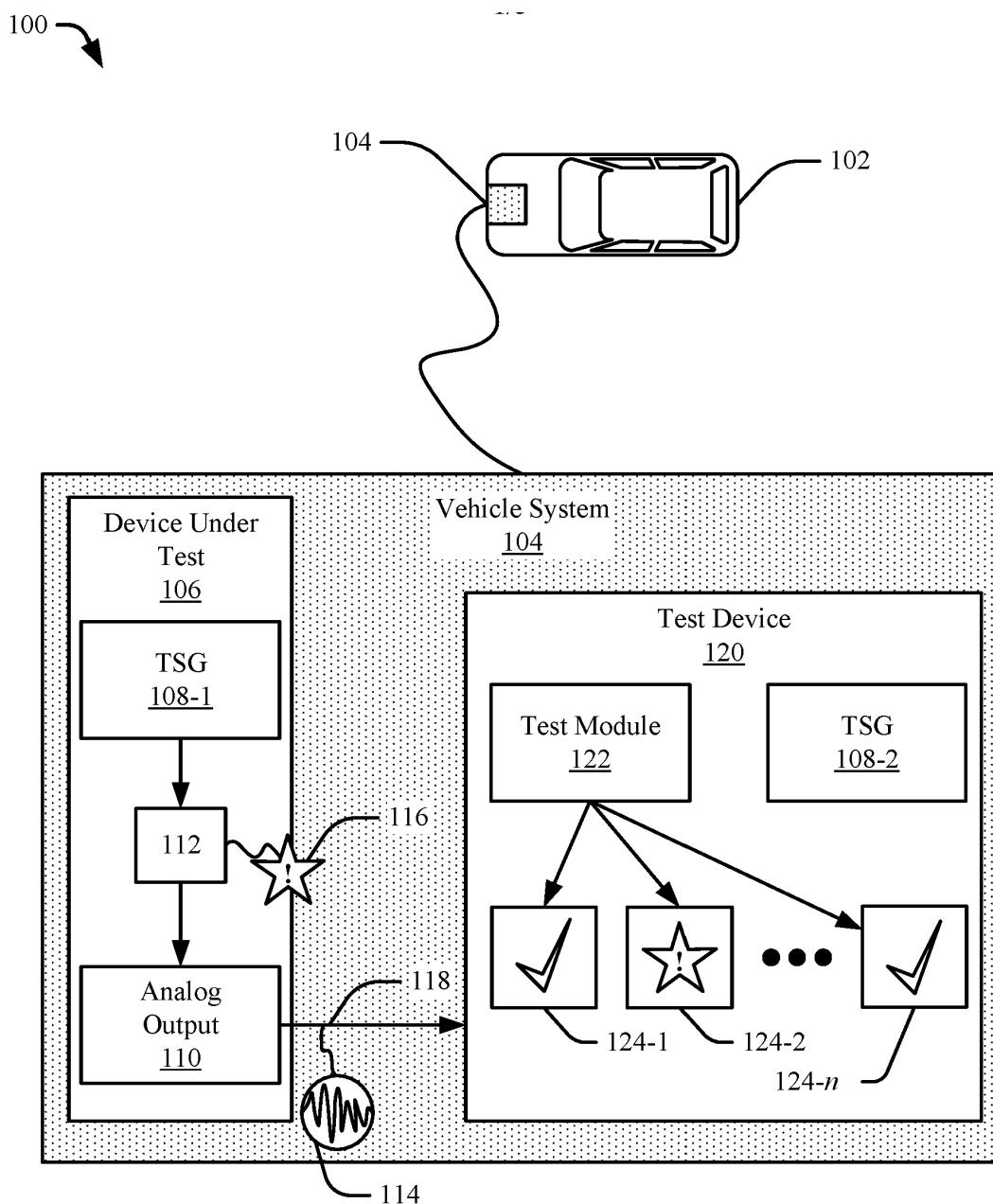


FIG. 1

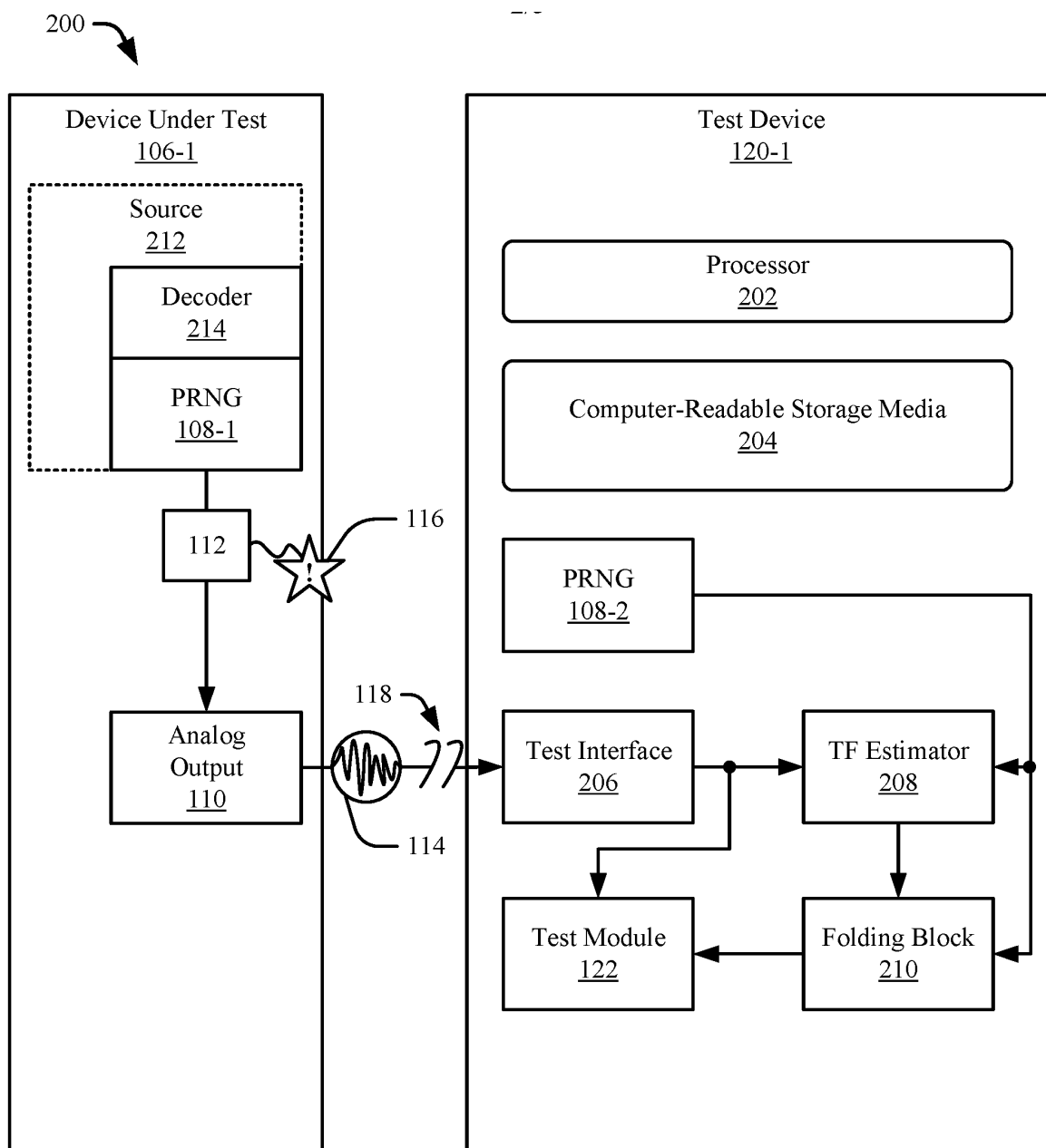


FIG. 2

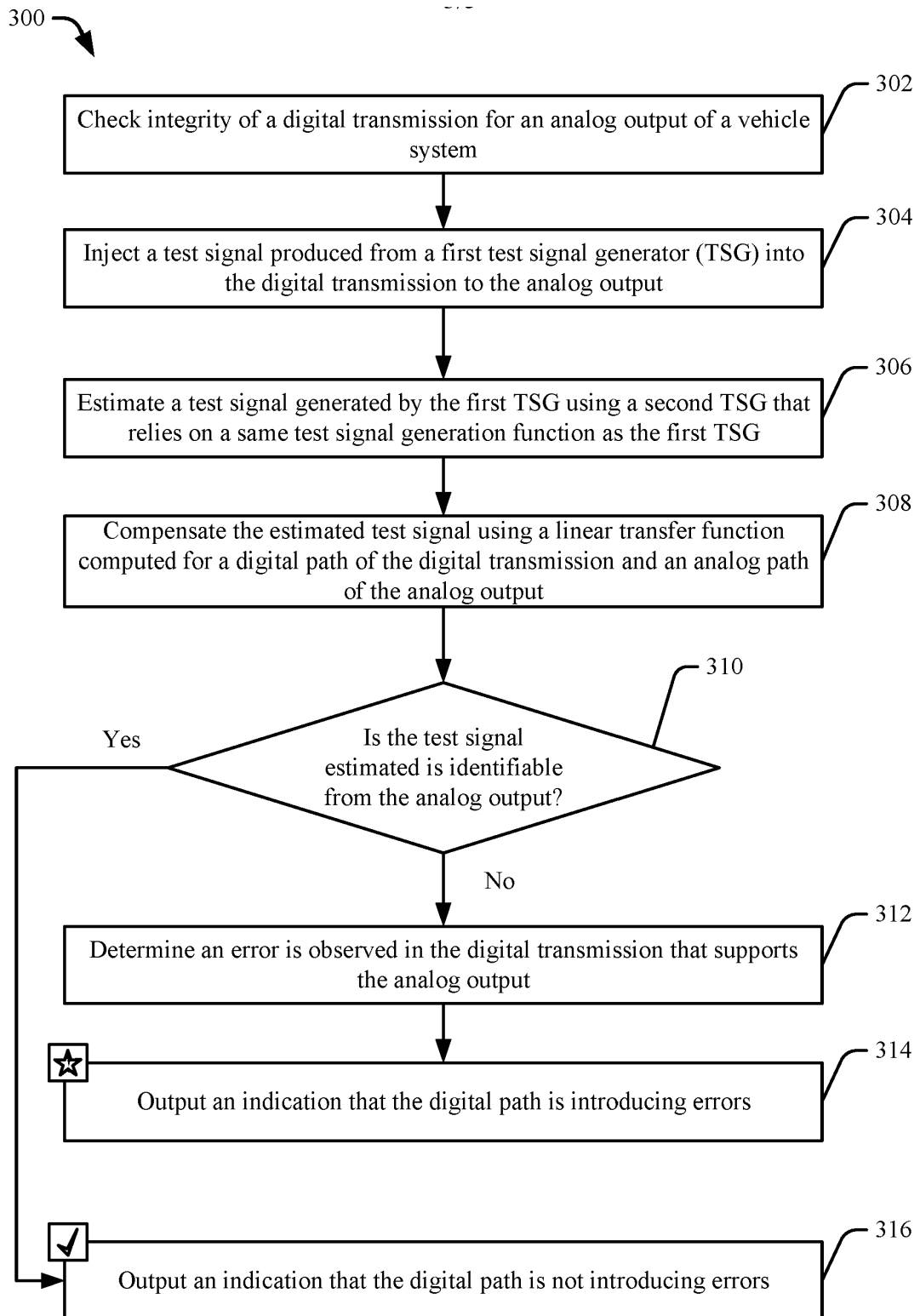


FIG. 3

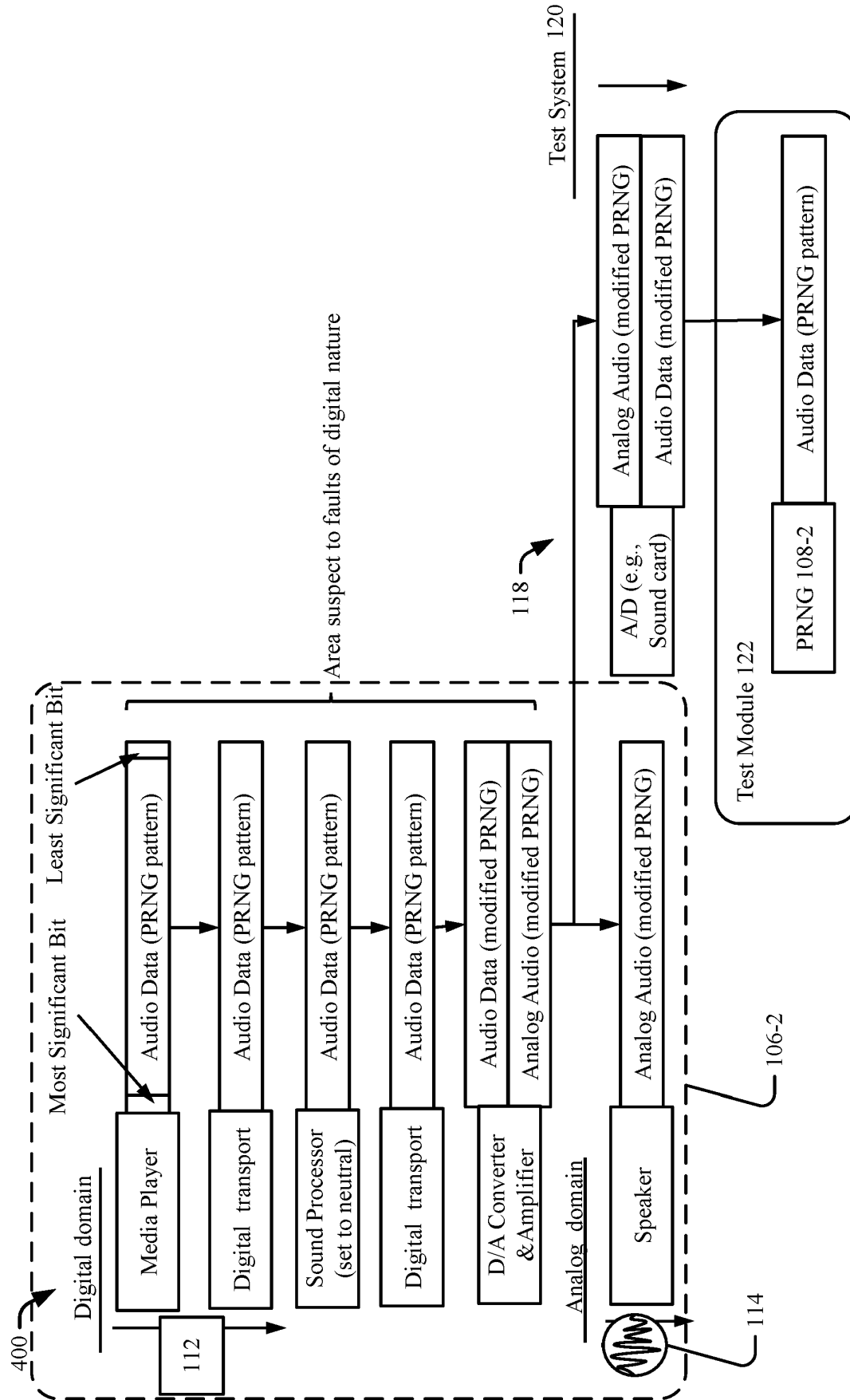


FIG. 4

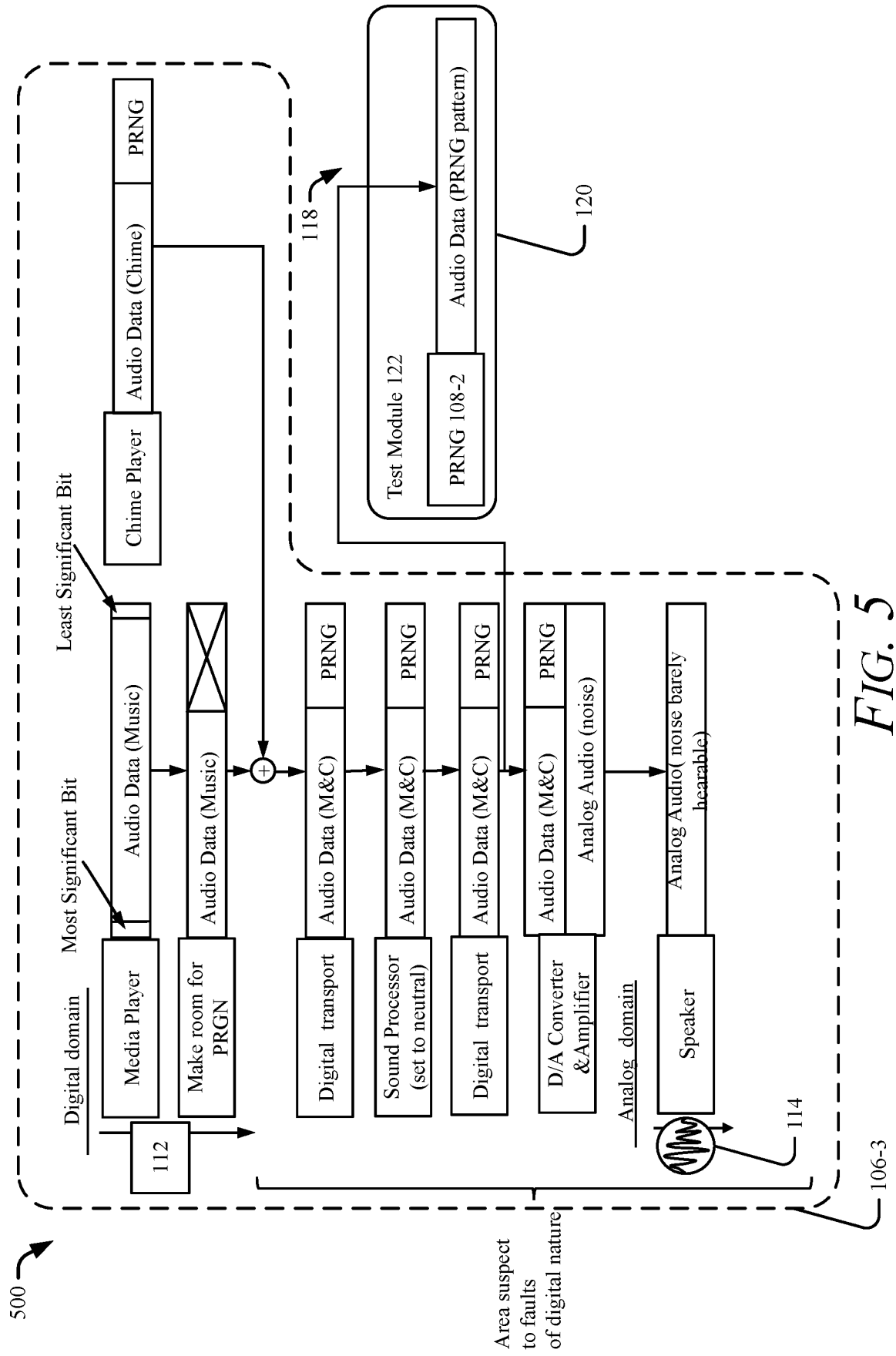


FIG. 5

REFERENCES CITED IN THE DESCRIPTION

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