United States Patent

De Pasquale

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[54] **APPARATUS FOR CONTROLLING PLURAL ELECTRICALLY ACTUATED OPERATING DEVICES**

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[52] **U.S. Cl.** **250/208,** 250/215, 307/311, 328/2, 353/30, 353/94

[51] **Int. Cl.**.....**G01j 5/00,** G03b 21/26, H03k 3/42

[58] **Field of Search** ..250/209, 214, 219 DI, 219 DC, 250/208, 215; 340/339; 353/30, 94; 307/311; 328/2; 35/42.5

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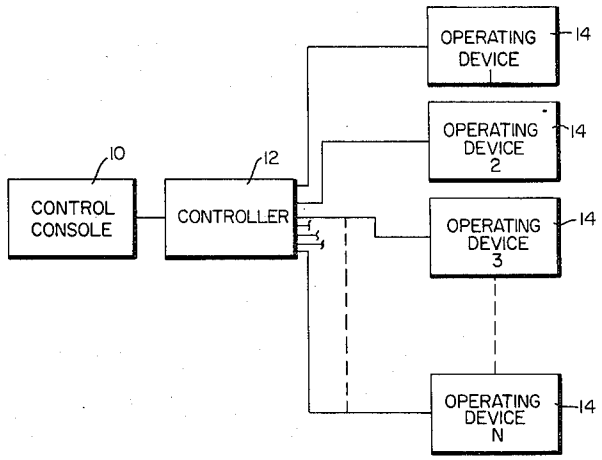
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Assistant Examiner—T. N. Grigsby
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[57] **ABSTRACT**

A control system for remotely controlling a plurality of operation devices, permitting selective individual actuation of those operating devices. A slide projector has its lens system replaced by a plurality of light-sensitive semiconductor devices. Each step of the control "program" comprises a card of a size to fit within the slide holder of the control projector and having openings corresponding to the light-sensitive semiconductor devices associated with those operating devices which are to be actuated at that step. Thus, those operating devices which are to be actuated for a particular program step have their associated light sensitive semiconductors illuminated while the program card for that program step is within the projection position of the control projector. The operating devices, by way of example, might be slide projectors, providing a composite visual display which can have portions of the display changed individually.

7 Claims, 8 Drawing Figures



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4 Sheets-Sheet 1

FIG. 1.

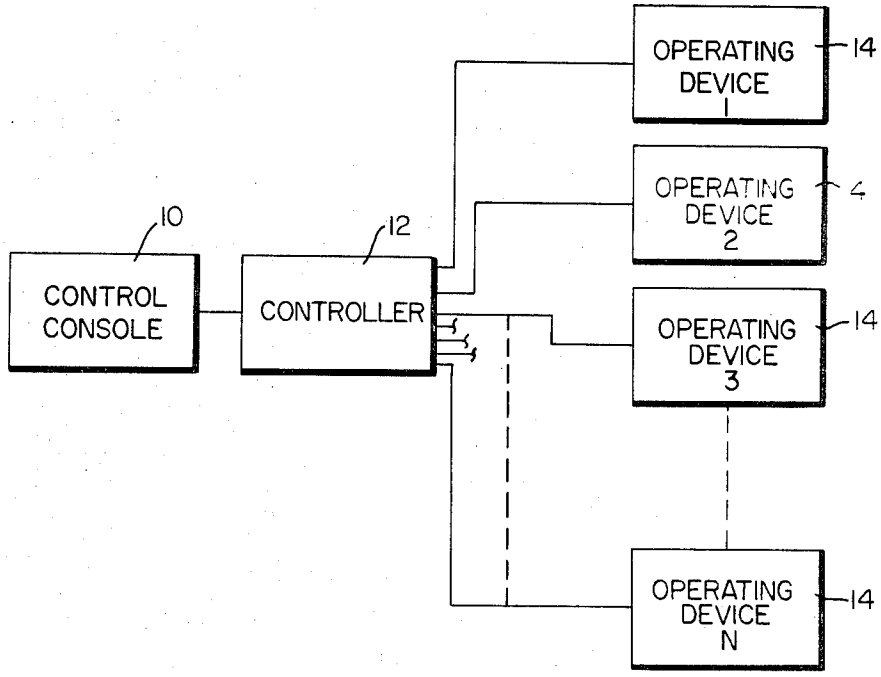


FIG. 2.

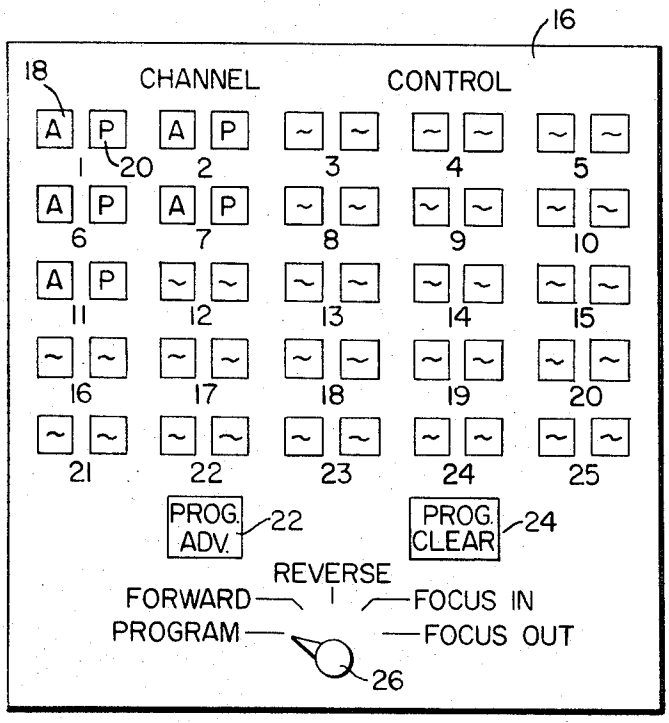
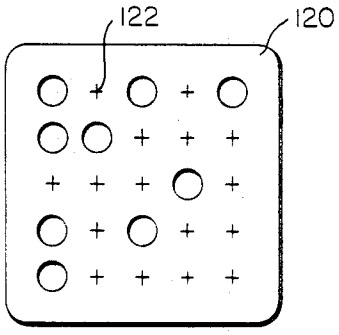


FIG. 3.



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FIG.8.

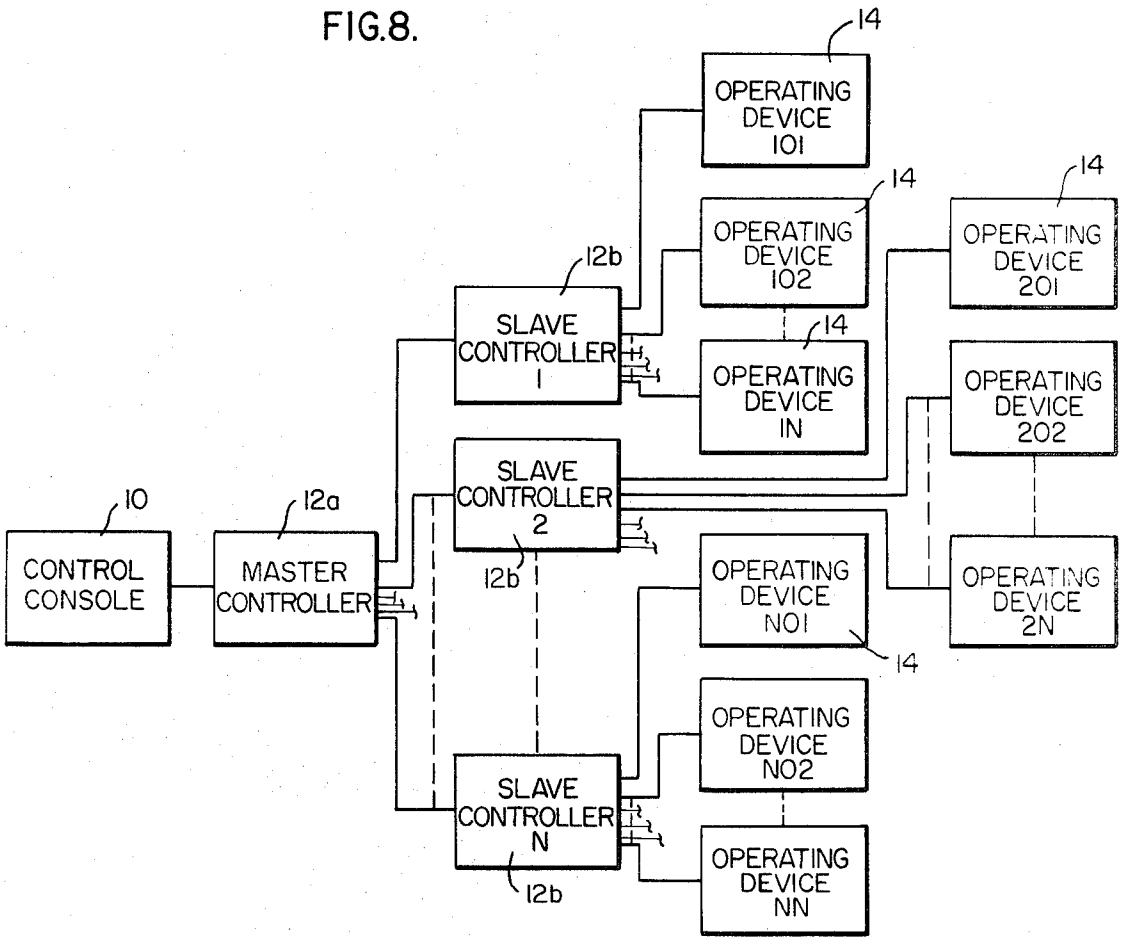
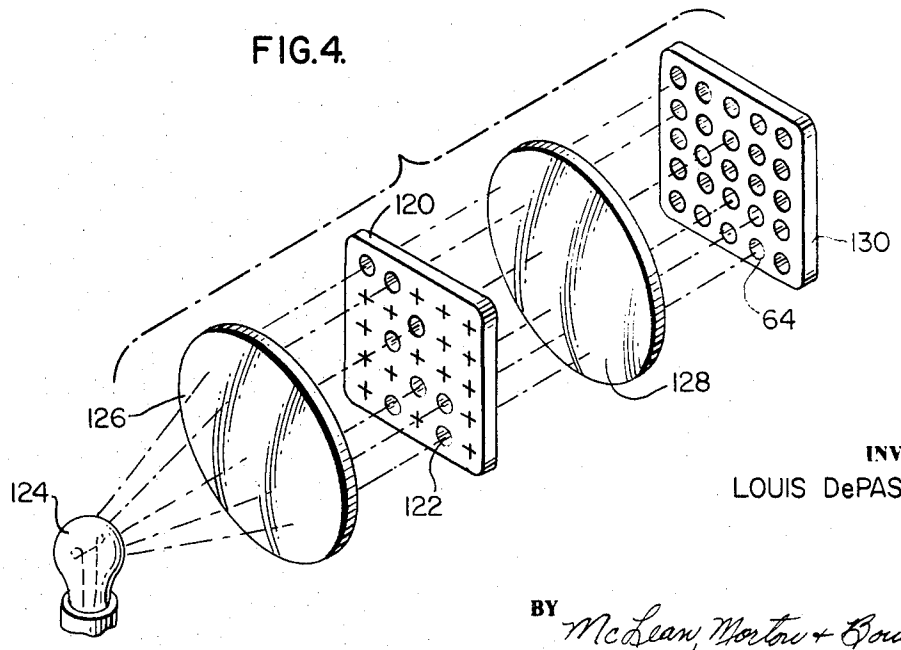


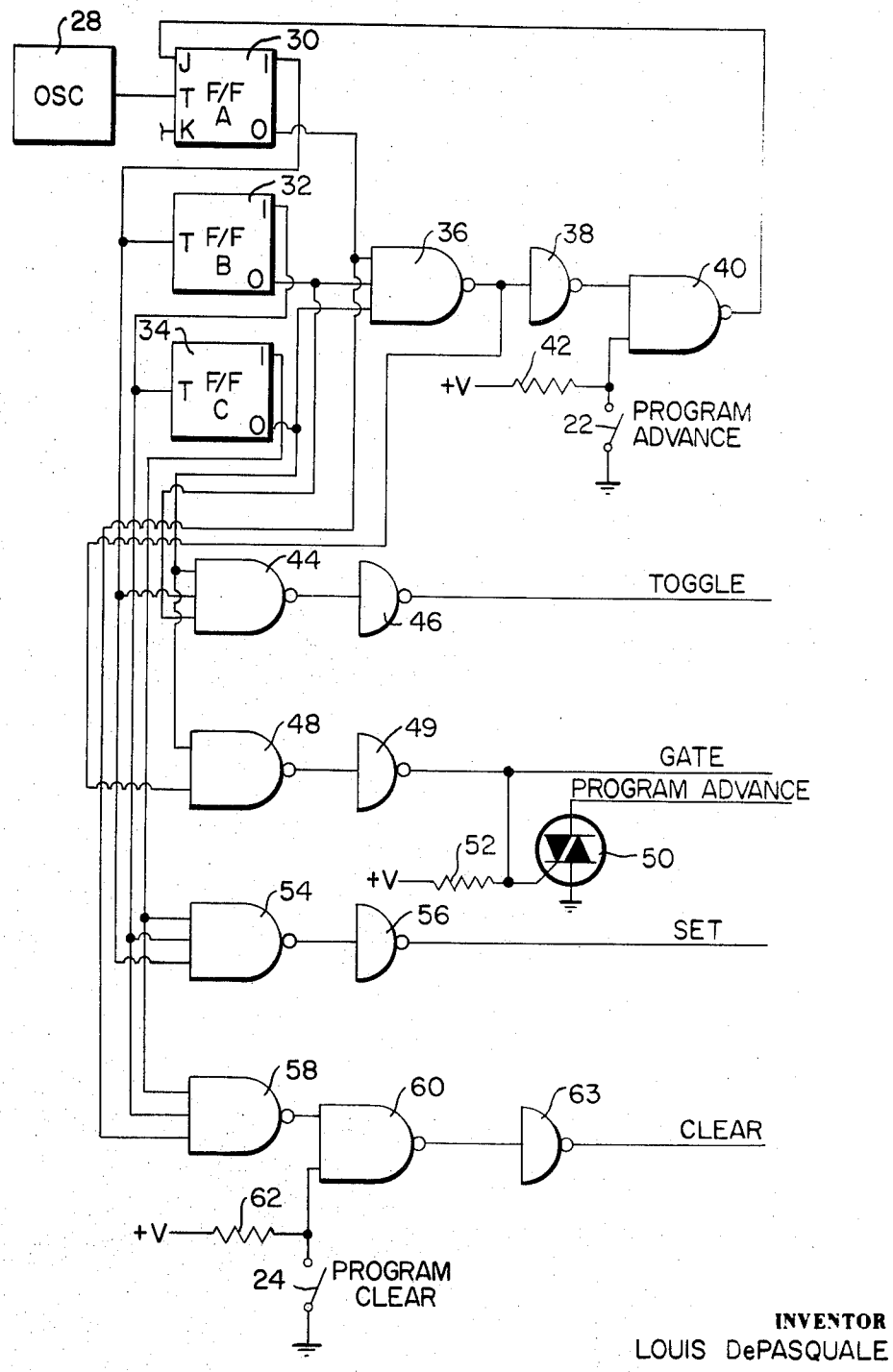
FIG.4.



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FIG. 5.



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FIG.6.

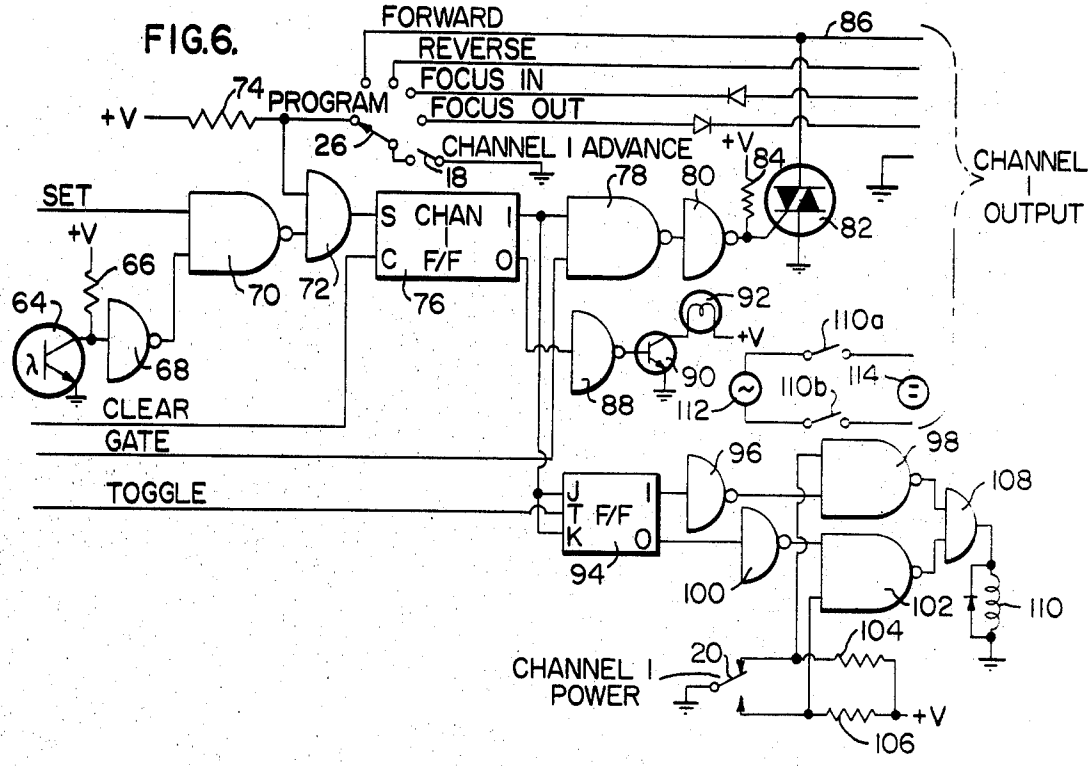
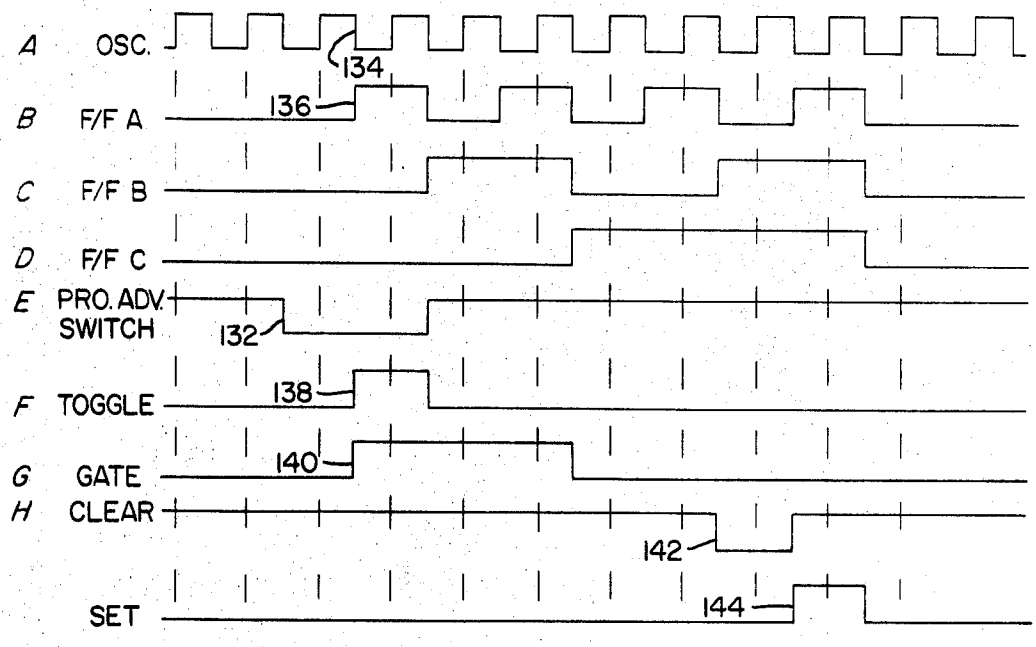


FIG.7.



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APPARATUS FOR CONTROLLING PLURAL ELECTRICALLY ACTUATED OPERATING DEVICES

The present invention pertains to a control system. More particularly, the present invention pertains to a system by means of which a plurality of operating devices can be selectively controlled from a remote location utilizing selectively illuminated light-sensitive electrical components. One application of the present invention is in visual display systems in which a visual display is set up by means of a large number of individually operated slide projectors to produce a composite picture. Portions of the picture can be changed by actuating one or more of the slide projectors to change the portion of the picture originating from them while others of the slide projectors are not actuated and so do not change their portion of the picture. Accordingly, the present invention will be described with reference to the control of a plurality of slide projectors in a visual display system; however, the control system of the present invention is suited for the control of other operating devices.

In many audio-visual systems it is desired to generate composite pictures by means of the simultaneous projection of a large number of slides. These composite pictures can be shown in one plane or on a single curved surface to produce a large panoramic effect. Alternatively, different portions of the picture can be projected on different planes to produce a three dimensional effect. In either instance it is frequently desired to change some but not all of the slides so as to produce a varied picture which, e.g., illustrates varying conditions or progressing activity of the displayed scene. Such audio-visual displays can be utilized in large Worlds Fair type of exhibits. Additionally, they can be utilized in commercial display or teaching situations.

If, for example, a composite picture is made by the simultaneous projection of 25 slides, changes in the picture can be made by changing anywhere from one to 25 of these slides at any given time. Quite obviously, if the 25 slide projectors are to be changed manually, a considerable amount of time would be required, and the likelihood of an error occuring would be great. This would detract considerably from the effect of the presentation. There have been developed apparata for the automatic control of a large number of slide projectors. Thus, for example, a system has been developed by means of which a large number of slide projectors are automatically controlled in accordance with pin-operating holes punched in paper tape. This system, however, has numerous shortcomings. First of all, the number of tracks of possible holes in the paper tape is limited generally to a maximum in the order of eight. Accordingly, only eight slide projectors can be controlled by means of such a system. Additionally, if it is desired to make a change at some point in the middle of the program, it is necessary that the holes punched in the tape corresponding to that portion of the program be changed. Since the paper tape is a continuous strip, this necessitates making a completely new punched paper tape. This is a time consuming and wasteful process.

The present invention is a system by means of which a large number of operating devices such as slide projectors can be automatically controlled to selectively operate so that one or more of the devices is actuated

at any given time. There is theoretically no limit to the number of operating devices which can be controlled, and a single master controlling device can directly control, for example, 25 operating devices. The program which determines which operating devices are to be actuated at any given step is contained on a series of punched cards, and so changes to the program can be readily made simply by removing the one or more cards corresponding to the steps to be changed and replacing them with new cards.

In accordance with the present invention, the lens of a slide projector is replaced by a plurality of light-sensitive electrical components such as light-sensitive semiconductive devices. A card of a size and shape to fit within the slide carrier of the projector is selectively punched to permit light from the projector lamp to illuminate the light-sensitive semiconductive devices corresponding with those operating devices which are to be actuated. In response to this illumination, the illuminated semiconductive devices trigger control circuits corresponding with their respective operating devices to cause actuation of those operating devices. The slide can contain, for example, **25** locations for holes corresponding to 25 light-sensitive semiconductors, thus permitting the control of 4b **25** operating devices. By connecting controllers in tandem so that the first master controller controls 25 slave controllers which in turn each control 25 operating devices, 625 operating devices can be controlled from a single master controller. This tandeming could continue, thereby increasing the number of operating devices controlled from a single master controller.

These and other aspects and advantages of the present invention are apparent in the following detailed description and claims, particularly when considered in conjunction with the accompanying drawings in which like parts bear like reference numerals. In the drawings:

FIG. **1** is a block diagram of a control system in accordance with the present invention;

FIG. **2** depicts a master control panel suitable for use in the present invention;

FIG. **3** illustrates a program slide suitable for use in the present invention;

FIG. **4** schematically illustrates a portion of a controller in accordance with the present invention;

FIG. **5** is a block diagram of a master timing circuit suitable for use in the present invention;

FIG. **6** is a block diagram of a channel control logic suitable for use in the present invention;

FIG. **7** depicts waveforms found within the master timing circuit of the present invention; and

FIG. **8** is a block diagram of a control system in accordance with the present invention and utilizing control devices connected in tandem.

FIG. **1** depicts in block diagram form an overall control system in accordance with the present invention. The control console **10** contains the necessary switches for providing commands to controller **12** which is connected to console **10**. A large number of operating devices **14** are individually connected to controller **12** for operation in accordance with commands sent by controller **12** to the individually operating devices **14**. By way of illustration, each operating device **14** can be a slide projector of the type which includes a storage cartridge or tray containing a large number of slides

which are one at a time sequentially moved to a projection position in which light passes through the slides and through an appropriate lens system to provide an image of the slide upon a large display screen or wall.

FIG. 2 depicts a control panel 16 suitable for use on control console 10. Panel 16 includes two actuator-indicators or switches for each operating device to be controlled. Thus, for the first operating device, referred to as Channel 1, there is an Advance actuator-indicator 18 and a Power actuator-indicator 20. Likewise, for each of the other operating devices or channels 2-25, there is an Advance actuator-indicator or switch 18 and a Power actuator-indicator or switch 20. In addition, control panel 16 includes a Program Advance switch 22, a Program Clear switch 24, and a five-position Function Select switch 26. The positions of switch 26 are designated Program, Forward, Reverse, Focus-in and Focus-out.

FIG. 3 depicts a control card or slide 120 suitable for use within controller 12. Slide 120 is of an opaque, relatively stiff material such as cardboard and is of a size to fit within the slide holder of a commercially available slide projector such as a Kodak Carousel 800 projector. In the illustrative example of FIG. 3, slide 120 has 25 control locations 122 designated thereon, in five rows of five locations each. One control location is associated with each operating device 14. For those sequence steps for which it is desired to cause the actuation of a particular device 14, an opening is punched on the slide 120 corresponding with that sequence step and at the control location 122 of slide 120 corresponding with that particular operating device 14. Thus, the "program" which controls the slide sequence is made up of a series of slides 120 having holes punched in control locations 122 for each associated operating device 14 which is to be actuated at that program step.

Controller 12 preferably is a specially adapted, commercially available slide projector such as a Kodak Carousel 800 slide projector. The projection lens of that slide projector is removed and replaced by a plurality of light-sensitive electrical components such as light-sensitive semiconductor devices 64 which for example might be Texas Instrument Corporation LS 600 phototransistors, for example. As depicted in FIG. 4, light from lamp 124, within the slide projector utilized as controller 12, passes through lens 126 and strikes slide 120. Light passes through those control locations 122 at which openings have been made through slide 120. That light is focused by lens 128 to strike the corresponding light-sensitive semiconductor devices 64 on board 130. The devices 64 are mounted on board 130 in locations corresponding with the control locations 122 of slide 120.

FIG. 5 depicts the master timing circuitry within controller 12. Oscillator 28, which by way of example can be a free running multivibrator having a frequency in the order of 5 cycles per second, has its output connected to the trigger input of JK flip-flop 30. JK flip-flop 30 is of the type which is capable of providing a one output and a zero output and which has a J input, a K input and a trigger input. When the JK flip-flop has its J input tied to ground, the flip-flop is inhibited from assuming its one condition. Similarly, when the K input is tied to ground, the flip-flop is inhibited from assuming its zero condition. In the absence of grounds on the J and K inputs, the flip-flop alternates between its one condition and its zero condition with each negative-going pulse applied to its trigger input.

The one output of flip-flop 30 is tied to the trigger input of flip-flop 32 which can be a JK flip-flop with no connections to its J and K input terminals. The one output of flip-flop 32 is connected to the trigger input of flip-flop 34 which likewise can be a JK flip-flop with no connections to the J and K input terminals.

The zero outputs of flip-flops 30, 32 and 34 are connected as inputs to NAND gate 36 which has its output coupled through inverter 38 to the first input of NAND gate 40. The second input of gate 40 is tied to one terminal of the Program Advance switch 22, the second terminal of which is tied to ground. The second input of gate 40 is also coupled through resistor 42 to a source of positive voltage. The output of gate 40 is tied to the J input of JK flip-flop 30. There is no connection to the K input of flip-flop 30.

Flip-flops 30, 32 and 34 are functionally referred to as flip-flop A, flip-flop B and flip-flop C, respectively. When flip-flop 30 is in its one state, the A1 signal is present on the output line from the one output of flip-flop 30. When flip-flop 30 is in its zero state, the $\overline{A1}$ signal is present on that line. Likewise the B1 and the $\overline{B1}$ signals are provided on the output line from the one output of flip-flop 32 when that flip-flop is in its one state and its zero state, respectively, and the C1 and $\overline{C1}$ signals are provided on the output line from the one output of flip-flop 34 when that flip-flop is in its one state and in its zero state, respectively. Similarly, the AO and $\overline{A0}$ signals, the BO and $\overline{BO}$ signals, and the C0 and $\overline{C0}$ signals are provided by the zero outputs of flip-flops 30, 32 and 34, respectively as those flip-flops are in their zero state and their one state, respectively. The A0, A1, B0, B1, C0 and C1 signals are each the presence of a positive voltage on the respective output lines, while the $\overline{A0}$, $\overline{A1}$, $\overline{B0}$, $\overline{B1}$, $\overline{C0}$ and $\overline{C1}$ signals are each indicated by the grounding of the respective output lines.

NAND gate 44 receives as inputs the one output of flip-flop 30, the zero output of flip-flop 32 and the zero output of flip-flop flip-flop 34. The output of gate 44 is applied to inverter 46, the output of which provides a Toggle signal.

NAND gate 48 receives as inputs the zero output of flip-flop 34 and the output of NAND gate 36. The output of gate 48 is connected to inverter 49 which provides as an output a Gate signal. The output of inverter 49 is also connected to the gate of Triac 50. Triac 50 has its gate coupled through resistor 52 to a source of positive voltage and its terminal T1 tied to ground. The T2 terminal of Triac 50 is connected to a Program Advance output line.

NAND gate 54 receives as inputs the one output of flip-flop 30, to one output of flip-flop 32 and the one output of flip-flop 34. The output of gate 54 is applied to inverter 56, the output of which provides a Set output signal.

NAND gate 58 receives as inputs the zero output of flip-flop 30, the one output of flip-flop 32 and the one output of flip-flop 34. The output of gate 58 is connected to the first input of NAND gate 60. The second input of gate 60 is tied to one terminal of the Program

Clear switch 24, the second terminal of which is tied to ground. The second input of gate 60 is also coupled through resistor 62 to a source of positive voltage. The output of gate 60 is passed through inverter 62 to provide a Clear output signal.

FIG. 6 depicts the control logic circuitry of one of the operating device control channels, designated as Channel 1. Identical channels of logic circuitry are provided for the other operating devices. Light passing through an opening 122 corresponding with that channel impinges upon a light-sensitive semiconductor device such as phototransistor 64. Phototransistor 64 has its emitter tied to ground and its collector coupled through resistor 66 to a positive voltage source. The selector of phototransistor 64 is tied to the input of inverter 68, the output of which is connected to one input of NAND gate 70. The second input of gate 70 receives the Set signal from inverter 56 within the master timing circuitry. The output of gate 70 is connected to one input of AND gate 72. The second input of gate 72 is also connected to the Program terminal of Function Control switch 26. The common terminal of switch 26 is connected to one terminal of the Channel 1 Advance switch 18, the second terminal of which is tied to ground.

The output of AND gate 72 is connected to the set input of flip-flop 76. The clear input of flip-flop 76 is connected to the output of inverter 63 within the master timing unit to receive the Clear signal. The one output of flip-flop 76 is connected to the first input of NAND gate 78. The second input of gate 78 is connected to the output of inverter 49 within the master timing unit to receive the Gate signal. The output of gate 78 is connected to the input of inverter 80 which has its output connected to the gate of Triac 82. Triac 82 has its gate coupled through resistor 84 to a source of positive voltage, its terminal T1 tied to ground, and its terminal T2 tied to output line 86 to provide the channel one Advance output signal. Line 86 is also connected to the Forward position of function control switch 26.

If desired, the zero output of flip-flop 76 can be tied to the input of an inverter 88 which has its output connected to the base of NPN transistor 90. Transistor 90 has its emitter tied to ground and its collector connected to one terminal of light 92, the second terminal of which is tied to a positive voltage source. Light 92 provides the indication for the Channel 1 Advance actuator-indicator 18.

The one output of flip-flop 76 is connected to both the J and the K inputs of JK flip-flop 94. The trigger input of flip-flop 94 is connected to the output of inverter 46 within the master timing unit to receive the Toggle signal. The one output of the flip-flop 94 is tied to the input of inverter 96 which has its output connected to one input of NAND gate 98. The zero output of flip-flop 94 is connected as the input to inverter 100 which has its output tied to one input of NAND gate 102. The second input of gate 98 is tied to the first fixed contact of the Channel 1 Power actuator-indicator 20 and is coupled through resistor 104 to a positive voltage source. The second input of gate 102 is tied to the second fixed contact of that actuator-indicator 20 and is coupled through resistor 106 to that positive voltage source. The moving contact of the that actuator-indicator 20 is tied to ground.

AND gate 108 receives as inputs the output of NAND gate 98 and the output of NAND gate 102. The output of AND gate 108 is connected to one side of relay coil 110, the second side of which is tied to ground. Relay coil 110 controls normally open contact 110*a* and normally open contact 110*b* which are connected to the output lines between power source 112 and female connector 114. Source 112 might be a male connector provided on controller 12 for connection to a locally available source of power.

Output lines are also provided in the control logic circuitry of each channel from that Channel's Reverse, Focus-in, and Focus-out positions of the Program Select switch 26. Additionally, a ground line is provided as an output to ensure a common reference.

In the quiescent condition, flip-flops 30, 32 and 34, are each in their zero state. As a consequence, NAND gate 36 receives a positive voltage at each of its input terminals, and so applies a ground signal to inverter 38. Inverter 38, therefore, applies a positive signal to the first input of NAND gate 40. With the Program Advance switch 22 open, a positive voltage is applied through resistor 42 to the second input of NAND gate 40. Therefore, the output of gates 40 ties the J input of JK flip-flop 30 to ground. This inhibits that flip-flop from responding to the pulses applied to its trigger input by oscillator 28. Thus, the three flip-flops 30, 32 and 34 are locked in their zero states. FIG. 7 depicts the waveforms found in this condition As there illustrated, the oscillator output pulses of FIG. 7A occurs at a rate in the order of five pulses per second. Flip-flops 30, 32 and 34 are providing the $\overline{A1}$, the $\overline{B1}$ and the $\overline{C1}$ signals, respectively, and so the one outputs of flip-flop A, flip-flop B and flip-flop C are each at ground, as depicted in FIGS. 7B, 7C, and 7D, respectively. As shown in FIG. 7E, the output of the Program Advance switch 22 is positive since switch 22 is open.

NAND gate 44 receives as inputs the $\overline{A1}$, B0, and C0 signals. Consequently, gate 44 applies a positive voltage to inverter 46, and so the Toggle output is at ground, as depicted in FIG. 7F. NAND gate 48 receives as inputs the C0 signal and the ground level output of NAND gate 36. Consequently, gate 48 applies a positive signal to inverter 49. Thus, in the quiescent state the Gate signal obtained as the output of inverter 49, is at substantially ground, as shown in FIG. 7G. In addition, Triac 50 is in its nonconducting state, and so the Program Advance output line is isolated from ground.

NAND gate 54 receives as inputs the $\overline{A1}$, $\overline{B1}$ and $\overline{C1}$ signals. Accordingly, gate 54 provides a positive output signal, and so the output of inverter 56, which is the Set output signal, is substantially ground as depicted by FIG. 7I. NAND gate 58 receives as inputs the A0, $\overline{B1}$ and $\overline{C1}$ signals, and so the output of gate 58 applies a positive voltage to NAND gate 60. With the Program Clear switch 24 open, a positive voltage is applied through resistor 62 to the second input of NAND gate 60. Consequently, the output of gate 60 is substantially ground, and inverter 63 applies a positive voltage as the Clear output signal, as depicted in FIG. 7H.

Assume that flip-flop 76, within the Channel 1 control circuitry of FIG. 6, is in its zero state. Then, the first input of NAND gate 78 is at ground, and so gate 78 applies a positive voltage to inverter 80. The output of inverter 80 is accordingly at ground, holding Triac 82 in its nonconductive condition. The ground signal from

the one output of flip-flop 76 is applied to both the J and the K inputs of JK flip-flop 94, preventing that flip-flop from changing state. Assume that flip-flop 94 is in its zero state. The positive level zero output is inverted by inverter 100, and so the first input of NAND gate 102 is tied to ground. With the moving contact of Power actuator-indicator 20 contacting the fixed contact connected to NAND gate 98, as depicted in FIG. 6, gate 98 has one of its inputs tied to ground. Consequently, both NAND gate 98 and NAND gate 102 are applying positive outputs to NAND gate 108 which therefore applies a positive voltage to relay 110 to energize the relay. Thus, contacts 110*a* and 110*b* are closed, connecting power source 112 with output connector 114. The positive level zero output of flip-flop 76 is applied to inverter 88 which ties the base of transistor 90 to ground. Consequently, transistor 90 is cut off, and indicator 92 is de-energized.

When the Program Advance switch 22 is closed, one input of NAND gate 40 is tied to ground, as depicted by pulse 132 in FIG. 7E. Consequently, the output of gate 40 becomes positive, removing the inhibiting signal from the J input of JK flip-flop 30. The next time the output of oscillator 28 goes negative, as depicted by pulse 134 in FIG. 7A, flip-flop 30 assumes its one condition, as indicated by pulse 136 in FIG. 7B. Therefore, the output of NAND gate 36 become positive, and inverter 38 applies ground to one input of NAND gate 40. This maintains the positive output from the gate 40.

The one output from flip-flop 30 is applied to NAND gate 44, which then is receiving the A1, B0 and C0 signals. Therefore, the output of gate 44 becomes negative. Consequently, inverter 46 provides a positive pulse as the Toggle output signal, as depicted by pulse 138 in FIG. 7F. This Toggle pulse is applied to the trigger input of JK flip-flop 94. Since both the J and K inputs of flip-flop 94 are tied to ground by the one output of flip-flop 76, the toggle pulse produces no effect on flip-flop 94. When flip-flop 30 assumes its one condition, NAND gate 48 receives the CO signal and the positive level output from NAND gate 36, and so the output of gate 48 becomes negative, and inverter 49 generates the Gate pulse 140 depicted in FIG. 7G. This signal is applied as an input to NAND gate 78. Since the channel 1 flip-flop 76 is in its zero state, this Gate signal has no effect on gate 78.

As depicted in FIGS. 7A–7D, with each succeeding negative pulse from oscillator 28, the chain of flip-flops 30, 32 and 34 changes state. Since the Toggle signal is only provided when the condition $A1 \cdot B0 \cdot C0$ is present, the Toggle output pulse 138 ends the first time flip-flop 30 returns to its zero state. Similarly, since the Gate output signal is only during the condition $(\overline{A0} + \overline{B0}) \cdot C0$ the Gate pulse 140 ends when flip-flop 34 assumes its one state.

When the output of inverter 49 becomes positive to generate Gate pulse 140, a positive voltage is applied to the gate of Triac 50. As a consequence that Triac assumes its conductive state, providing a ground path of the Program Advance output line. This output line is connected to the actuation circuit of controller 12. Thus, if the controller 12 is a slide projector, this ground path through Triac 50 is connected to the a.c. motor which activates the slide changer to change the slide 120.

If the slide 120 moved into the projection position in controller 12 has an opening at the location 122 corresponding with this control channel, light from lamp 124 reaches the light-sensitive semiconductor device 64 associated with this channel, and so the input of inverter 68 is tied to ground through semiconductor 64. The output of inverter 68, therefore, applies a positive voltage to one input of NAND gate 70, thereby enabling the NAND gate. With Channel 1 Advance switch 18 open, positive voltage is applied through resistor 74 to one input of AND gate 72. In the absence of the Set Signal, NAND gate 70 applies a positive voltage to the second input of AND gate 72, and so gate 72 applies a positive signal to the set input of flip-flop 76. When the output of inverter 49 returns to ground, the gate of Triac 50 no longer has a positive voltage on it. At the next negative half-cycle of current through the slide changer motor in controller 12, Triac 50 stops conducting, shutting off the slide changer motor. By this time the new slide 120 is in the projection position in controller 12.

When the flip-flop chain reaches the condition AO.B1.C1, the output of NAND gate 58 becomes negative. Therefore, NAND gate 60 provides a positive signal and so the output of inverter 63 becomes negative, providing the Clear pulse 142, shown in FIG. 7H. This pulse is applied to the clear input of channel 1 flip-flop 76. Since the flip-flop is already in its zero state, it has no effect. At the next negative pulse from oscillator 28, flip-flops 30, 32 and 34 are all set to their one state. Since NAND gate 54 is then receiving the A1, B1, and C1 signals, the output of gate 54 becomes negative. Inverter 56, therefore, provides the Set signal as a positive pulse 144 depicted in FIG. 7I. This pulse is applied to the second input of NAND gate 70 which has been enabled by the output of inverter 68. The output of gate 70, therefore, goes to ground causing the output of AND gate 72 to go to ground. This negative pulse is applied to the set input of flip-flop 76, causing that flip-flop to assume its one state.

Flip-flop 76 acts as a memory device storing the fact that the channel 1 operating device is to be actuated when the program next is advanced. The one output from flip-flop 76 enables gate 78 and removes the inhibiting signals from the J and K inputs of flip-flop 94. Since the zero output of flip-flop 76 is now at ground, inverter 88 turns on transistor 90, and so indicator 92 is energized to indicate that this channel's operating device will be actuated by the next closure of the Program Advance switch 22.

When the cycle is next repeated by the closing of the Program Advance switch 22, flip-flop 30 assumes its one state, resulting in the generation of the Toggle pulse by inverter 46. This pulse triggers flip-flop 94 to its one state. There is no change in NAND gate 98, since one of its inputs is still connected to ground through the Channel 1 Clear switch 20. As both inputs of NAND gate 102 are now positive, the output of gate 102 is essentially ground, and so the output of AND gate 108 drops to ground. Consequently, relay 110 is de-energized. Accordingly, contacts 110a and 110b open, isolating output connector 114 from voltage source 112.

When flip-flop 30 assumes its one state, the Gate output signal is generated by NAND gate 48 and is applied

to NAND gate 78. Accordingly, the output of gate 78 becomes ground, and the inverter 80 output becomes positive. A positive pulse is thus applied to the gate of Triac 82, causing the Triac to assume its conductive state. This provides a ground path for the Forward output line 86. Line 86 is connected to the a.c. actuating motor within the operating device 12 associated with this channel, and so when Triac 82 becomes conductive, that operating device is actuated. If the operating devices 14 are slide projectors providing a panoramic or three-dimensional picture, conduction of Triac 82 permits actuation of the slide changing motor to change a portion of the picture. When the Gate signal ends, the output of inverter 80 again becomes ground and during the next negative half-cycle of current in the slide-changer motor, Triac 82 cuts off.

At the same time that the Gate signal is generated by NAND gate 48, Triac 50 is triggered to its conductive state. This again advances master controller 12 to cause the next slide 120 to drop into the projection position. If there is an opening in that slide at the position 122 corresponding with this channel, NAND gate 70 is again enabled. In that event the subsequent Set pulse from inverter 56 causes another negative pulse to be applied to the set input of flip-flop 76. However, if there is no opening in the position 122 of that slide 120 corresponding with this channel, then the associated operating device is not be actuated, and so light-sensitive semiconductive device 64 is not illuminated. Consequently, positive voltage is applied through resistor 66 to the input of inverter 68. That inverter output clamps one input of NAND gate 70 to ground, and so the next Set signal does not affect gate 70. The output of AND gate 72 therefore remains positive, and flip-flop 76 is not triggered to its one condition. Accordingly, at the Gate pulse of the next cycle, Triac 84 does not become conductive, and the associated operating device is not actuated.

If there is no opening in slide 120 at the position 122 corresponding with this channel, and it is nevertheless desired to actuate the associated operating device 14 at the next closure of Program Advance switch 22, the Channel 1 Advance actuator-indicator 18 is depressed. This causes the output of AND gate 72 to become ground. Accordingly, a negative pulse is applied to the set input of flip-flop 76, setting that flip-flop to its one condition, just as would have been the case had there been an opening at that position 122. Thus, the program can be selectively altered.

The energized indicators 92 illuminate the Channel Advance actuator-indicators 18 on control panel 16 of those channels, which have their memory flip-flops 76 to set to one condition, thus indicating the operating devices which are to be actuated the next time Program Advance switch 22 is closed. Should it be desired that some of these operating devices 14 not be actuated, the Program Clear switch 24 is depressed. This places ground on one input of NAND gate 60, causing the output of that gate to become positive, and the negative Clear pulse is generated by inverter 63. This returns the flip-flop 76 of each channel to the zero condition, and a new program can then be instituted, either by removing that slide 120 and inserting a different one, or by manually actuating the Program Advance switches 18 associated with those operating devices it is desired to actuate. Alternatively, of course, an individual Channel Program Clear switch could be provided for each channel in the same manner as the Channel Advance switches 18.

If it is desired to actuate one operating device 14 independently of the program on the slides 120, Function Select switch 26 is placed in the Forward position, and the Channel Advance switch 18 is depressed. This provides a ground path for output line 86, causing actuation of the operating device 14. Alternatively, inverter 80 could be replaced by a NAND gate having one input converted to the output of NAND gate 78 and one input connected to the Forward position of Function Select switch 26. Then, with switch 26 in the Forward position, closure of the Channel Advance switch 18 grounds one input of the new NAND gate 80, resulting in a positive pulse on the gate of Triac 82. If it is desired to step on operating device 14 backward in the program independently of the designated program on the slides 120, Function Select switch 26 is placed in the Reverse position, and the Channel Advance switch 18 is closed. This provides a ground path for the Reverse output line for that channel, and that line can be connected to the necessary circuitry within the operating device 14 to step that operating device backward. If desired, a semiconductor ground path for the Reverse line could be provided similar to the alternative path for the Forward position of Function Select switch 26 described above. In addition, switching in the connection between Triac 82 and line 86 could permit selective connection of the Triac to either the Forward output line or the Reverse output line, thereby allowing the program to be run in reverse with each closure of Program Advance switch 22.

Other channel output lines can be provided to permit actuation of other controls on the operating device 14. Thus, for example, if the operating device 14 is a slide projector having a motor-driven focusing lens, Function Select switch 26 can include Focus-in and Focus-out positions which permit actuation of the focusing motor by the placement of Function Selection switch 26 in the desired position and the closing of the Channel Advance switch 18 to provide the necessary ground path for the focusing motor. These output lines can include diodes, as depicted in FIG. 6, polarized to ensure current flow through the motor in the proper direction.

Each time the operating device 14 associated with a particular channel is to be actuated that channel's flip-flop 76 is in its one condition prior to the time Program Advance switch 22 is closed. Accordingly, JK flip-flop 94 is not inhibited when the Toggle signal is applied to its trigger input. Each time flip-flop 94 changes state, relay 10 changes state between its activated condition and its deactivated condition. Accordingly, each time an operating device 14 is activated, the associated channel's connector 114 output toggles between its powered condition, in which contacts 110*a* and 110*b* are closed to connect connector 114 to power source 112, and its isolated condition, in which contacts 110*a* and 110*b* are opened to isolate connector 114 from power source 112. Likewise, each time a channel's Power switch 20 is moved between its two positions, the inputs applied to AND gate 108 change, and so relay 110 changes state, to toggle the condition of that channel's connector 114 output. The channel's Power

output connector 114 thus toggles between its powered condition and its isolated condition with each actuation of that channel's operating device 14. Connector 114 can be utilized for any of a variety of auxiliary features such as coordinating an audio program with the visual display when operating devices 14 are slide projectors.

If it is desired to control more operating devices 14 from a single controller 12 than can be accommodated by a single slide 120, then the controllers can be connected in tandem, as depicted in FIG. 8. As there shown, control console 10 is connected to master controller 12*a* which can be a slide projector utilizing the slides 120 and semiconductor board 130 of FIG. 4. In place of operating devices 14, master controller 12*a* actuates a plurality of slave controllers 12*b* which likewise can be slide projectors with the apparatus of FIG. 4 incorporated therein. Slave controllers 12*b* in turn actuate operating devices 14 which by way of example can be commercially available slide projectors. In this manner the number of operating devices 14 under the control of single master controller 12*a* can be increased considerably. By continued tandem connections, the number of operating devices can be increased without limit.

While controller 12 includes manual Program Advance actuator 22, automatic means could be utilized to actuate that actuator. Thus, a timer to be utilized to close actuator 22 at periodic intervals, or an audio program could be taped to be used in conjunction with the operation of devices 14, and such tape could include signals which activate a device to close actuator 22 at desired times.

What is claimed is:

1. Apparatus for controlling the selective actuation of a plurality of electrically actuated operating devices in combination with a light source and slide card holding means for positioning a slide card in the path of light from said source, which apparatus comprises:

a plurality of light-sensitive electrically responsive devices positioned in relation to said light source and said slide card holding means in alignment such that a plurality of control locations exist on a slide card in said holding means, each such location being uniquely associated in the path of light between said light source and one of said electrically responsive devices;

master program advance actuator means actuatable to control the actuation of said operating devices selectively in response to the impingement of light on said light-sensitive electrically responsive devices by supplying a sequency of control functions including in sequence a gate function and a set function, said gate function operating said slide card holding means to position a slide in said path of light;

said master program advance actuator means including:

a. a program advance switch,

b. first pulse generating means for generating a gate pulse in response to actuation of said program advance switch,

c. second pulse generating means for generating a clear pulse a preset time after generation of said gate pulse,

d. third pulse generating means for generating a set pulse upon termination of the clear pulse;

a plurality of actuation control channel circuits, each uniquely connected to an associated one of said electrically responsive devices, each circuit including:

a. first bate means for assuming an enabled condition when light is impinging upon the associated electrically responsive device upon operation of said slide card holding means through said gate function, said first gate means being coupled to said master program advance actuator means to be operated after being enabled by said set function,

b. current control means adapted for connection to an operating device to control actuation current therein,

c. coupling means coupling said first gate means with said current control means after operation of said first gate means by said gate function to cause said current control means to assume a conductive condition, said coupling means including:

i. bistable memory means for storing the fact said first gate means was enabled until the time of said set pulse coupled to said first gate means and to said master program advance actuator means, said bistable memory means assuming a first state in response to generation of the clear pulse and assuming a second state in response to generation of the set pulse when said first gate means is in its enabled condition,

ii. second gate means for assuming an enabled condition when said bistable memory means is in its second state, said second gate means coupled to said current control means for causing said current control means to assume a conductive condition in response to generation of the gate pulse when said second gate means is in its enabled condition.

2. Apparatus as claimed in claim 1 in which:

said master program advance actuator means includes:

a. a program advance switch,

b. first pulse generating means for generating a gate pulse in response to actuation of said program advance switch,

c. second pulse generating means for generating a clear pulse a preset time after generation of said gate pulse,

d. third pulse generating means for generating a set pulse upon termination of the clear pulse;

and in which each said coupling means includes:

a. bistable memory means for storing the fact said first gate means was enabled until the time of said gate pulse coupled to said first gate means and to said master program advance actuator means, said bistable memory means assuming a first state in response to generation of the clear pulse and assuming a second state in response to generation of the set pulse when said first gate means is in its enabled condition,

b. second gate means for assuming an enabled condition when said bistable memory means is in its second state, said second gate means coupled to said current control means for causing said current control means to assume a conductive condition in response to generation of the gate pulse when said second gate means is in its enabled condition.

3. Apparatus as claimed in claim 1 in which said master program advance actuator means further com-

prises fourth pulse generating means for generating a toggle pulse upon generation of the gate pulse and in which said coupling means further comprises a power outlet connector, a power source means for supplying electrical power to said power outlet connector, power control means capable of assuming a first state in which said power outlet connector is connected to said power source means and capable of assuming a second state in which said power outlet connector is isolated from said power source means, and means for causing said power control means to alternately toggle between its first state and its second state in response to generation of a toggle pulse when said bistable memory device is in its second state.

4. Apparatus for controlling the selective actuation of a plurality of electrically actuated operating devices in combination with a right source and slide card holding means for positioning a slide card in the path of light from said source, which apparatus comprises:

a plurality of light-sensitive electrically responsive devices positioned in relation to said light source and said slide card holding means in alignment such that a plurality of control locations exist on a slide card in said holding means, each such location being uniquely associated in the path of light between said light source and one of said electrically responsive devices;

master program advance actuator means actuatable to operate the actuation of said operating devices selectively in response to the impingement of light on said light-sensitive electrically responsive devices by supplying a sequency of control functions including in sequence a gate function and a set function, said gate function operating said slide card holding means to position a slide in said path of light;

a plurality of actuation control channel circuits, each uniquely connected to an associated one of said electrically responsive devices, each circuit including:

a. first gate means for assuming an enabled condition when light is impinging upon the associated electrically responsive device upon operation of said slide card holding means through said gate function, said first gate means being coupled to said master program advance actuator means to be operated after being enabled by said set function,

b. current control means adopted for correction to an operating device to control actuation current therein,

c. coupling means coupling said first gate means with said current control means after operation of said first gate means by said gate function to cause said current control means to assume a conductive conductive condition;

a plurality of slave controllers, each slave controller including an actuation current circuit uniquely connected to one current control means, each slave controller further comprising:

a plurality of light-sensitive electrically responsive devices;

slide card holding means adapted to hold in alignment between said slave controller electrically responsive devices and a light source location a slide card having designated thereon a plurality of control locations, each control location uniquely associated with one of said slave controller electrically responsive devices;

a plurality of actuation control channel circuits, each uniquely connected to an associated one of said slave controller electrically responsive devices, each circuit including;

a. first gate means for assuming an enabled condition when light is impinging upon the associated electrically responsive device, said slave controller first gate means coupled to said slave controller master program advance actuator means,

b. current control means adapted for connection to an operating device to control actuation current therein,

c. coupling means coupling said slave controller first gate means with said slave controller current control means for causing said slave controller current control means to assume a conductive condition in response to actuation of said slave controller master program advance actuator means when said slave controller first gate means is in its enabled condition.

5. Apparatus as claimed in claim 4 in which:

said slave controller master program advance actuator means includes

a. a program advance switch,

b. first pulse generating means for generating a gate pulse in response to actuation of said program advance switch,

c. second pulse generating means for generating a clear pulse a preset time after generation of said slave controller gate pulse,

d. third pulse generating means for generating a set pulse upon termination of the slave controller clear pulse;

and in which each said slave controller coupling means includes:

and in which each said slave controller coupling means includes:

a. bistable memory means for storing the fact said slave controller first gate means was enabled until the time of said slave controller set pulse coupled to said slave controller first gate means and to said slave controller master program advance actuator means, said slave controller bistable memory means assuming a first state in response to generation of the slave controller clear pulse and assuming a second state in response to generation of the slave controller set pulse when said slave controller first gate means is in its enabled condition,

b. second gate means for assuming an enabled condition when said slave controller bistable memory means is in its second state, said slave controller second gate means coupled to said slave controller current control means for causing said slave controller current control means to assume a conductive condition in response to generation of the slave controller gate pulse when said slave controller second gate means is in its enabled condition.

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