(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2010/0072580 A1**
**Shaheen et al.** (43) **Pub. Date: Mar. 25, 2010**

(54) **ULTRA-THIN OXIDE BONDING FOR SI TO SI DUAL ORIENTATION BONDING**

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(21) Appl. No.: **12/620,523**

(22) Filed: **Nov. 17, 2009**

**Related U.S. Application Data**

(62) Division of application No. 11/453,444, filed on Jun. 14, 2006.

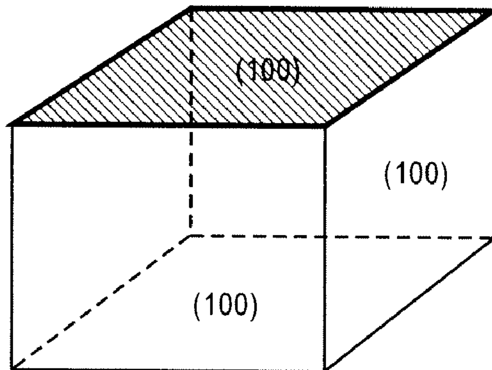
**Publication Classification**

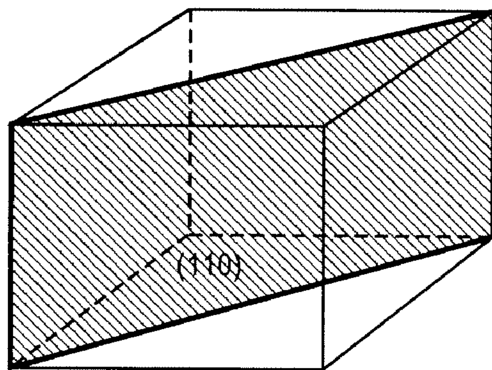
(51) **Int. Cl.**
***H01L 29/04*** (2006.01)

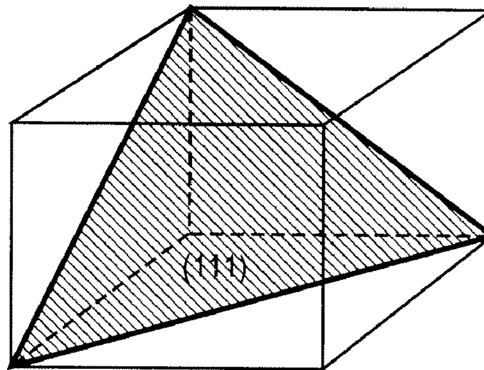
(52) **U.S. Cl.** ................................ **257/627**; 257/E29.004

(57) **ABSTRACT**

A multi-layered substrate with bulk substrate characteristics and processes for the fabrication of such substrates are herein disclosed. The multi-layered substrate can include a first layer, a second layer and an interfacial layer therebetween. The first and second layers can be silicon, germanium, or any other suitable material of the same or different crystal orientations. The interfacial layer can be an oxide layer from about 5 Angstroms to about 50 Angstroms.



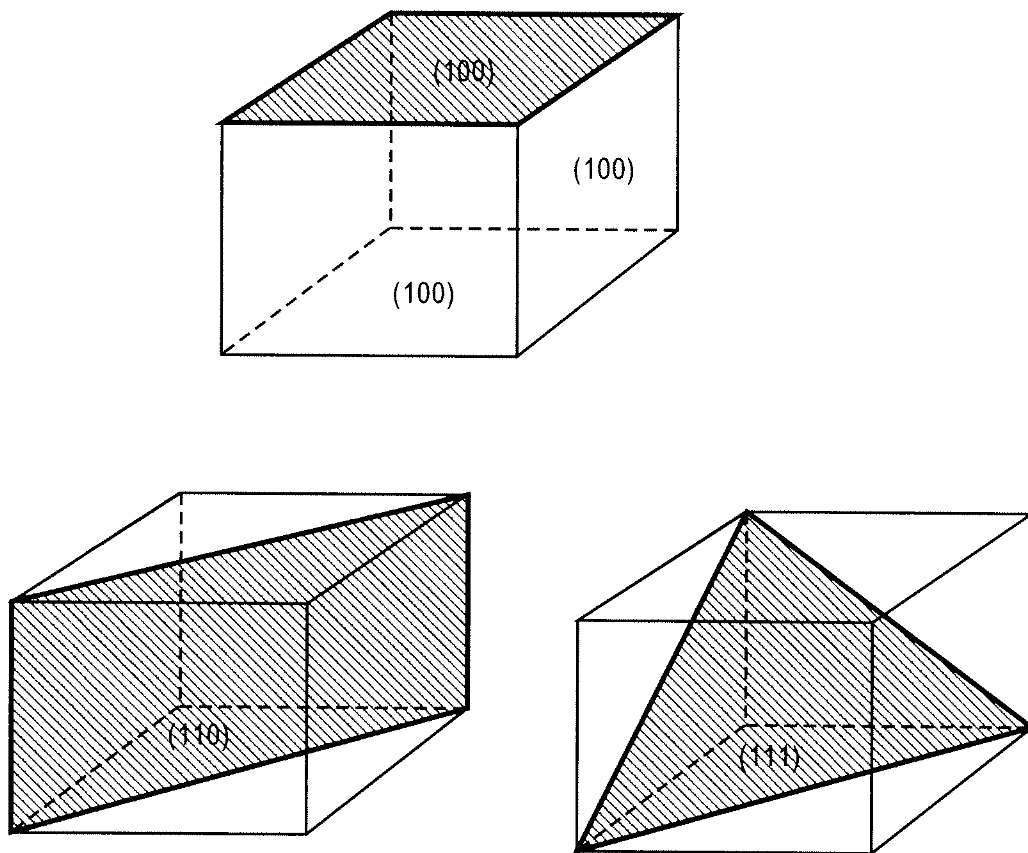



FIG. 1

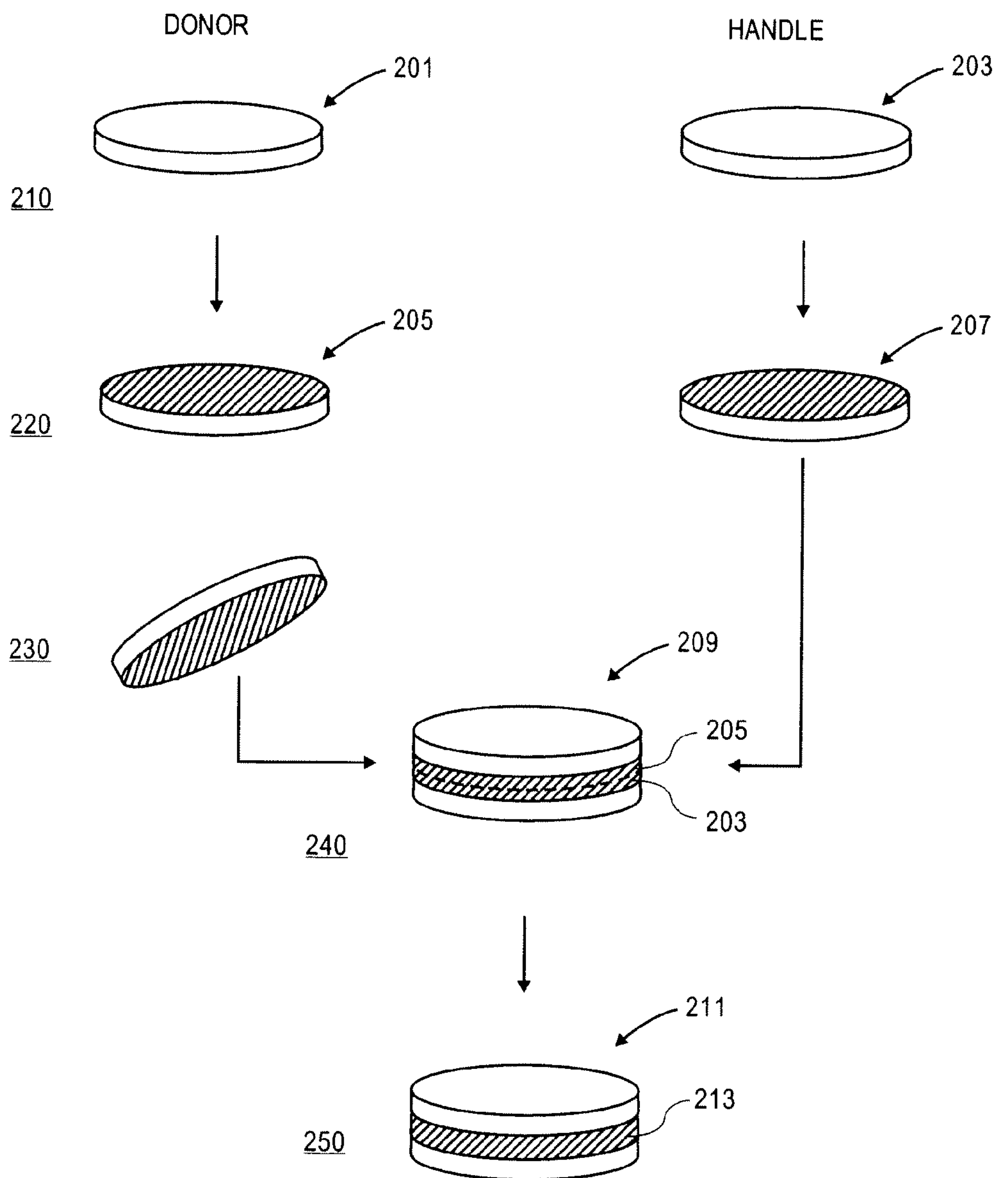



**FIG. 2**

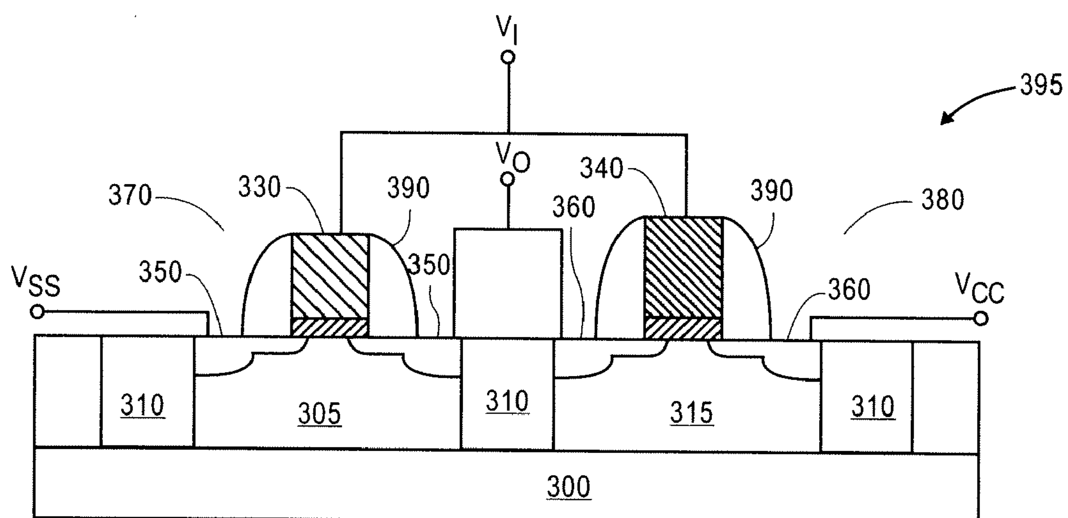



FIG. 3

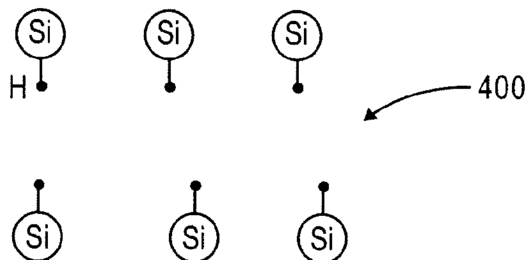



FIG. 4

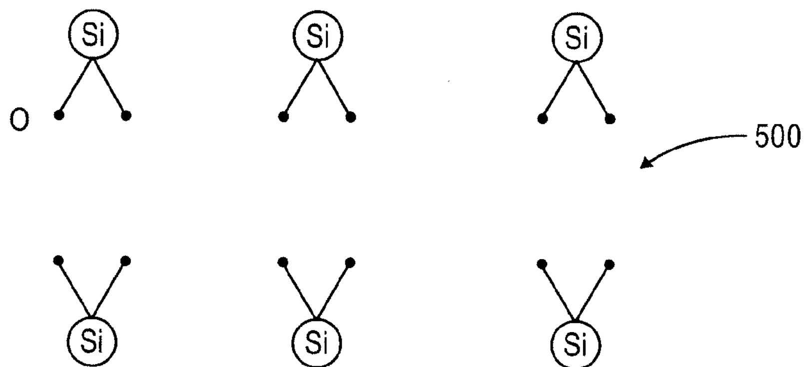



FIG. 5

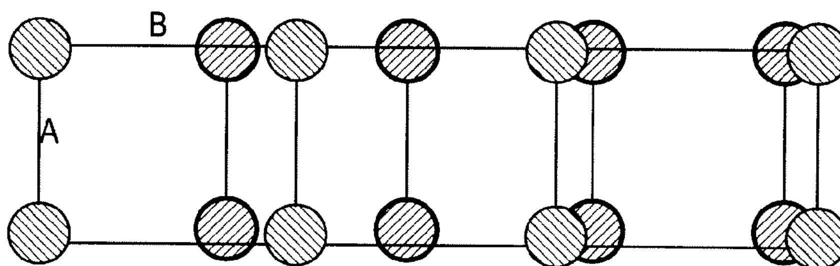



FIG. 6

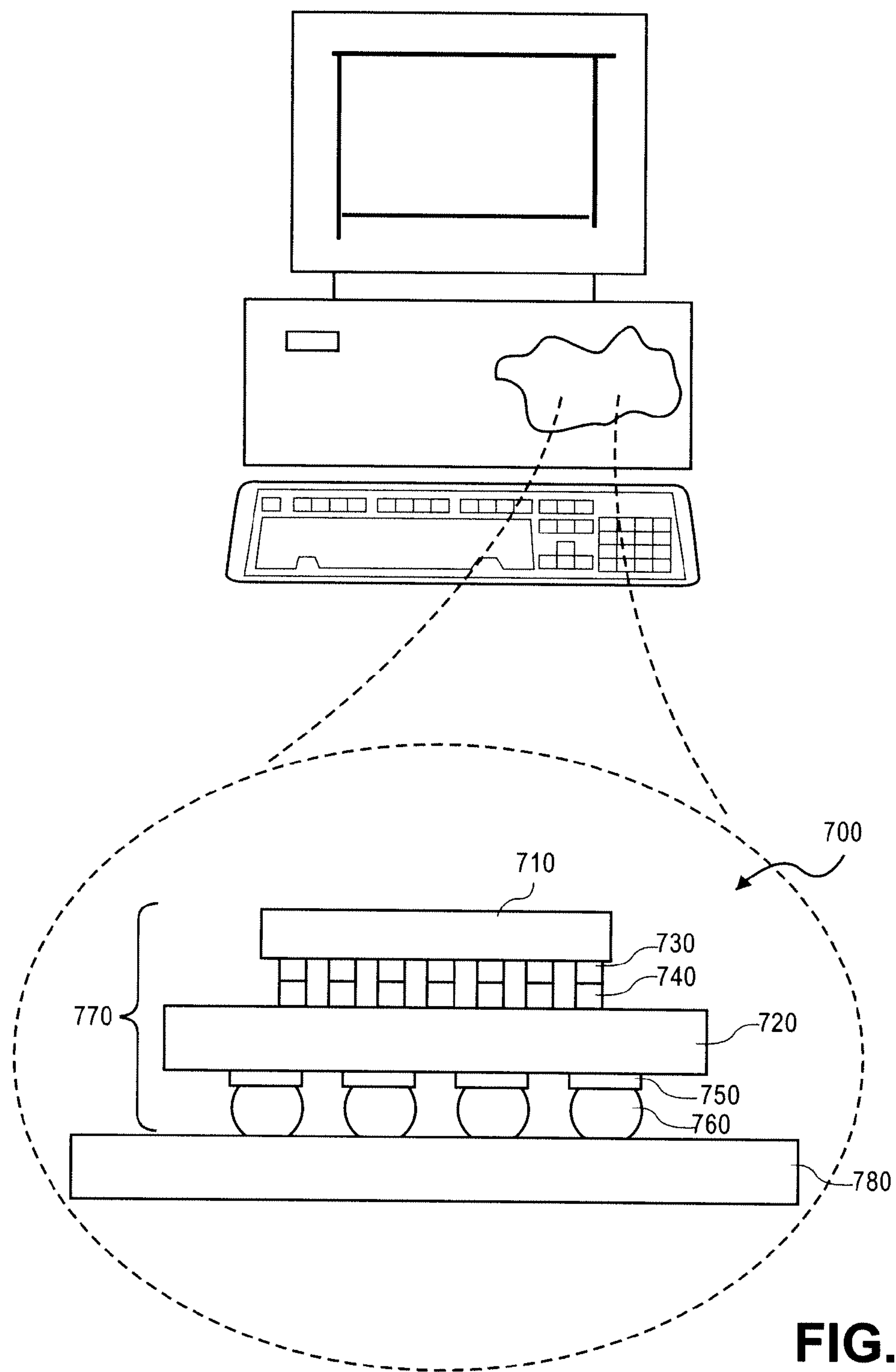



FIG. 7

# ULTRA-THIN OXIDE BONDING FOR SI TO SI DUAL ORIENTATION BONDING

## CROSS-REFERENCE TO RELATED APPLICATION

**[0001]** The application is a divisional of co-pending U.S. patent application Ser. No. 11/453,444, filed Jun. 14, 2006.

## FIELD

**[0002]** Semiconductor processes.

## BACKGROUND

**[0003]** Wafer-to-wafer bonding techniques are used to create substrates with varying layer-to-layer characteristics for a variety of different applications. For example, wafer-to-wafer bonding, i.e., wafer bonding, can allow the formation of device layer stacks that otherwise cannot be grown or deposited with conventional thin film methods with the same material qualities required for high device performance

**[0004]** Wafer bonding techniques typically employ at least two wafer substrates, referred to as a handle wafer and a donor wafer, as starting materials. Wafer bonding is generally done in three basic operations: (1) cleaning and surface activation of the handle wafer and the donor wafer prior to bonding; (2) bringing into contact the treated and cleaned surfaces of the handle wafer and the donor wafer; and (3) post-anneal processing to seal the bond.

**[0005]** In some applications, a substrate of varying layers having different crystal orientations is desired. "Crystal orientation" refers to the crystal lattice structure of materials used in the fabrication of semiconductor substrates. Crystal orientation planes of silicon are typically represented as (**100**), (**110**) and (**111**) and are representatively shown in FIG. **1**. Monocrystalline silicon is an anisotropic material, meaning that the properties of monocrystalline silicon change depending on the direction from which they are measured within the crystal lattice of silicon. This may be explained by the different atomic densities within each of the (**100**), (**110**), and (**111**) crystal planes that are illustrated in FIG. **1**. The atomic densities of the (**100**) crystal plane, the (**110**) crystal plane, and the (**111**) crystal plane are illustrated in FIG. **1**. Examples of properties that change with the direction in silicon include the Young's Modulus (a measure of the strength of the material), the mobility of electrons (or holes), the etch rate, and the oxidation rate. For example, the Young's modulus of silicon is 1.3 $e^{12}$ dynes/$cm^2$ in the (**100**) crystal plane, 1.7 $e^{12}$ dynes/$cm^2$ in the (**110**) crystal plane, and 1.9 $e^{12}$ dynes/$cm^2$ in the (**111**) crystal plane. As another example, the mobility of electrons in the (**100**) crystal plane is known to be greater than in the (**110**) crystal plane of silicon, resulting in a current drivability in the (**100**) direction that is approximately 15 percent (%) greater than the current drivability in the (**110**) direction.

**[0006]** Substrates of varying layers having different crystal orientations can have a high degree of lattice mismatch. "Lattice mismatch" is the percentage difference between atom spacings along a plane of the same crystallographic orientation as the interface plane in the respective bulk phases of the two materials. In certain instances, lattice mismatch can lead to device degradation in semiconductor devices. Thus, an interfacial layer is generally required to accommodate lattice mismatch between layers of different crystal orientations in multi-layered substrates.

**[0007]** In some wafer bonding techniques resulting in substrates of different crystal orientations, hydrophilic bonding can be used. For example, a thick layer of oxide is formed on a donor wafer. The oxide layer can be in the range from 300 Angstroms (Å) to 3000 Angstroms. The wafer surfaces are typically terminated in hydrophilic hydroxyl groups, such as Si—OH groups. The donor wafer is subsequently bonded to the handle wafer by contacting the treated surfaces of the respective wafers to each other with heat applied thereto. Prior to bonding, one of the wafers is implanted with hydrogen to establish the 'breakline' for predetermined thickness of the top silicon portion of the bonded wafer. When the bonded wafer is treated with heat, the implanted hydrogen line breaks and thus a wafer with an imbedded thick oxide layer is formed. Thus, the result is a hybrid crystal orientation substrate with a thick oxide layer in between the respective crystal orientation layers.

**[0008]** Imbedded thick oxide bonding produces a wafer with imbedded isolation (buried oxide, or BOX) which has different device characteristics than standard bulk silicon. This requires completely different circuit design. In addition, the interfacial oxide layer acts as an insulator and the resulting hybrid substrate has silicon-on-insulator (SOI) characteristics.

**[0009]** In some wafer bonding techniques resulting in substrates of different crystal orientations, hydrophobic bonding can be used. The process requires high temperatures and expensive equipment. For example, a handle wafer can be treated with hydrofluoric acid. A donor wafer can be implanted with hydrogen ions resulting in an implanted wafer. Before contacting the treated surfaces, the handle wafer must be subjected to a pre-anneal process to obtain a surface free of hydrogen (H) and hydroxyl (OH) groups. In some applications, the pre-anneal process is conducted at 650 degrees Celsius (C.). Similar to the handle wafer, the implanted wafer must be processed by a krypton-fluoride excimer laser to obtain a surface substantially free of H and OH groups. Thereafter, the handle wafer and the implanted wafer can be contacted for wafer bonding. The result is a substrate which may include layers of different crystal orientations formed by high temperature and laser treatment.

## BRIEF DESCRIPTION OF DRAWINGS

**[0010]** FIG. **1** illustrates crystal orientations.

**[0011]** FIG. **2** illustrates an embodiment of forming a multi-layer substrate with bulk substrate characteristics.

**[0012]** FIG. **3** illustrates an embodiment of a transistor on a multi-layer substrate with bulk substrate characteristics.

**[0013]** FIG. **4** illustrates an embodiment of hydrophobic bonding between two substrates.

**[0014]** FIG. **5** illustrates an embodiment of hydrophilic bonding between two substrates.

**[0015]** FIG. **6** illustrates an embodiment of lattice mismatch between two substrates with two different crystal orientations.

**[0016]** FIG. **7** shows a computer system including microprocessor enclosed by a package mounted to a printed circuit board.

## DETAILED DESCRIPTION

**[0017]** A multi-layered substrate with bulk substrate characteristics and processes for the fabrication of such substrates are herein disclosed. The multi-layered substrate can include

a first layer, a second layer and an interfacial layer therebetween. The first and second layers can be silicon, germanium, or any other suitable material of the same or different crystal orientations. The interfacial layer can be an oxide layer from about 3 Angstroms to about 100 Angstroms.

**[0018]** FIG. **2** illustrates an embodiment of forming a multi-layer substrate that, in one aspect, has bulk substrate characteristics. A first wafer **201** and a second wafer **203** may be the starting materials for forming a multi-layer substrate (**210**). In some embodiments, first wafer **201** is a donor wafer and second wafer **203** is a handle wafer, hereinafter referred to as donor wafer **201** and handle wafer **203**. Each of donor wafer **201** and handle wafer **203** can be a semiconductor material such as silicon, germanium, a combination of silicon and germanium, or any other suitable material (and combinations thereof) used in semiconductor fabrication processes. The materials may be doped with other materials such as, but not limited to, phosphorous (P), boron (B) and beryllium (Be), among other N or P dopant types. In some embodiments, donor wafer **201** may be implanted with hydrogen atoms.

**[0019]** In some embodiments, donor wafer **201** may have crystal orientation (**100**), (**110**) or (**111**). Independent of the wafer plane, the notch direction may be in the direction of [**100**], [**110**] or [**111**]. Similarly, in some embodiments, handle wafer **203** may have crystal orientation (**100**), (**110**) or (**111**) and independent notch directions of [**100**], [**110**] or [**111**]. Thus, donor wafer **201** and handle wafer **203** may comprise the same or different crystal orientations depending on the intended application of the resulting multi-layer substrate.

**[0020]** Oxide layers **205** and **207** can be formed on one or both of donor wafer **201** and handle wafer **203**, respectively (**220**). Examples of materials which can be used for oxide layers **205** and **207**, include but are not limited to, silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$), plasma oxide and chemical oxide, or high-dielectric constant based oxides such as hafnium oxide. Oxide layer formation can be performed by a variety of methods, including, but not limited to, ambient native growth, chemical growth, chemical vapor deposition (CVD), RF sputtering, atomic layer deposition (ALD), low pressure CVD, plasma-enhanced CVD or any other suitable process. It should be appreciated that in some embodiments, an oxide layer can be formed on the donor wafer, the handle wafer or both wafers.

**[0021]** In some embodiments, ambient native growth forms oxide layers **205** and **207**. Donor wafer **201** and handle wafer **203** may first be cleaned by such processes including, but not limited to, wet-chemistry wafer cleaning processes. In some embodiments, hydrogen fluoride (HF) and hydrogen-peroxide-based wet cleans can be used. For example, dilute HF, Standard Clean-1 (SC-1) and Standard Clean-2 (SC-2) can be used sequentially on wafers **201** and **203**. Wafers **201** and **203** can then be rinsed with deionized water with a resistivity of about 18 megaOhms centimeter. Subsequently, cleaned donor wafer **201** and handle wafer **203** may be left in ambient conditions for approximately six hours to approximately thirty-six hours for saturated growth. Ambient conditions can be room temperature (approximately 21° C. to 23° C.) at approximately one atmosphere. Ambient native growth can result in an oxide layer of, for example, approximately 8 Angstroms to approximately 25 Angstroms.

**[0022]** In some embodiments, donor wafer **201** and handle wafer **203** can be dipped in a solution for formation of oxide layers **205** and **207**. Examples of solutions include, but are not limited to, peroxide solutions, such as hydrogen peroxide ($H_2O_2$) solutions and SCI/SC2 solutions. Wafers **201** and **203** should be stripped of any native oxide that has grown in ambient conditions. Thus, a cleaning process, such as the one described previously, should be performed before formation of chemical oxide layers **205** and **207**. In one embodiment, cleaned donor wafer **201** and handle wafer **203** may be dipped into a bath of 7% solution of hydrogen peroxide for a time from between 60 seconds and 600 seconds to form oxide layers **205** and **207**, respectively. Dipping in peroxide can result in an oxide layer of, for example, approximately 15 Angstroms. In another embodiment, cleaned donor wafer **201** and handle wafer **203** may be dipped into baths of SC1 and SC2 solutions for a time from between 60 seconds and 600 seconds to form oxide layers **205** and **207**, respectively. Dipping in SC1/SC2 can result in an oxide layer of, for example, approximately 3 Angstroms.

**[0023]** In some embodiments, chemical vapor deposition forms oxide layers **205** and **207**. Wafers **201** and **203** should be stripped of any native oxide that has grown in ambient conditions. Thus, a cleaning process, such as the one described previously should be performed before formation of oxide layers **205** and **207**. An example of a process to grow this oxide would involve annealing at about 900° C. of Si in a flow of oxygen or steam (wet oxidation) for approximately 30 to100 seconds. This results in an oxide layer of, for example, from approximately 3 Angstroms to approximately 10 Angstroms.

**[0024]** After formation of oxide layers **205** and **207**, donor layer **201** can be brought into contact with handle layer **203** by "flipping" donor layer **201** onto handle layer **203** (**230**). Donor layer **201** should be situated relative to handle wafer **203** such that oxide layer **205** of donor layer **201** is in contact with oxide layer **207** of handle wafer **203** (**240**). Wafers **201** and **203** are brought into contact to initiate bonding (contact bonding) as point bonding or full face bonding. "Point bonding" is when the bonding is initiated at a single point and the bonding wave propagates across the wafer. "Full face bonding" is when pressure is applied across the whole wafer at the same time to induce bonding. After placing the wafers **201** and **203** in contact, a bond wave propagates until full bonding is achieved. Bond wave propagation occurs when two substances are put into contact with another at at least one point. A wave initiates to seal the remaining points so that that the two substances are molecularly bonded by weak van der Waals forces. Bonding can be achieved from about 30 seconds to about 2 minutes. Bonding can be done under atmospheric conditions or vacuum conditions. At this point, weak molecular forces, i.e., van der Waals forces, hold the bonded donor wafer **201** and handle wafer **203** together resulting in a bonded substrate **209**. Surface energy at the bonding interface is about 0.1 Joules per meter squared ($J/m^2$).

**[0025]** After contact bonding and bond wave propagation, a post-bonding anneal process can be applied to a resulting multi-layer substrate **211** to convert the weak molecular forces to chemical covalent bonds (**250**). "Anneal" is a high temperature process which can be employed in, for example, semiconductor fabrication processes. In some embodiments, a post-bonding anneal process can be in a range from approximately 400° C. to approximately 1200° C. for a time period between about 2 hours to about 10 hours. Although bonding is achieved in contact bonding, strengthening bonding to form covalent bonds (such as by post-bonding anneal processes) may be further applied to multi-layer substrate **211** to

strengthen the bond between donor wafer **201** and handle wafer **203**. After the post-bonding anneal process, the bond energy is increased to about 2.0 (J/$m^2$) and multi-layer substrate **211** may be subjected to further processing, such as grinding.

**[0026]** Multi-layer substrate **211** includes ultra-thin oxide layer **213**. Oxide layer **213** can be in a range from about 5 Angstroms to about 100 Angstroms, and more particularly, from about 5 Angstroms to about 50 Angstroms. In some embodiments, oxide layer **213** is approximately 5 Angstroms. Representative examples in which oxide layer **213** may be approximately 5 Angstroms include Logic transistor devices. In some embodiments, oxide layer **213** is approximately 15 Angstroms to 25 Angstroms. Representative examples in which oxide layer **213** may be approximately 15 to 50 Angstroms include floating body Memory transistor devices. During the post-anneal process (**250**), moisture or hydrogen can form water ($H_2O$) or hydrogen gas ($H_2$) which gets absorbed in oxide layer **213**, thus preventing formation of voids.

**[0027]** FIG. **3** illustrates an embodiment of a complementary metal-oxide-semiconductor (CMOS) transistor device formed on a multi-layer substrate. CMOS device **395** includes NMOS transistor **370** and PMOS transistor **380** on substrate **300** which, in some embodiments, may be a multi-layer substrate. Transistors **370** and **380** each include gate electrodes **330** and **340**, respectively, and side walls **390** adjacent to gate electrodes **330** and **340**. NMOS transistor includes p-type well **305** and junction regions **350** within substrate **300** and adjacent to gate electrode **330**. PMOS transistor includes n-type well **315** and junction regions **360** within substrate **300** and adjacent to gate electrode **340**. Regions **310** represent isolation areas between PMOS and NMOS transistor devices. CMOS devices are known by those skilled in the art.

**[0028]** "Voids" refer to local unbonded areas between two bonded surfaces. Accordingly, voids can accumulate in and around an interfacial layer between two substrates. Voids can result from particulate impurities or gases, particularly hydrogen gas or $H_2O$ vapor. In some applications, voids can result in incomplete bonding, low die-yield, low die quality and, in some cases, eventually device failure. In wafer bonding in which a thick oxide layer comprises the interfacial layer, i.e., 300 Angstroms to 3000 Angstroms, the thick oxide layer can absorb interfacial gases which result in voids. However, such thick oxide layers serve as insulators and isolate the underlying and overlying substrate materials from each other. Such configurations are typically referred to as silicon-on-insulator substrates. In some applications, the bonding process is preferably performed at room temperature to reduce the formation of voids. On the other hand, direct bonding, i.e., bonding without the employment of an oxide layer, can be performed at high temperatures, but at the risk of blistering of hydrogen-implanted wafers.

**[0029]** FIG. **4** depicts the chemistry of hydrophobic bonding, i.e., direct bonding between two wafers. In a post-bond anneal, Si—H reacts with Si—H to form Si—Si and $H_2$. Thus, at interface **400**, $H_2$ can become trapped forming voids. Additionally, in cases in which the wafers have different crystal orientations, misfit dislocations are expected.

**[0030]** FIG. **5** depicts the chemistry of hydrophilic bonding, i.e., bonding between two wafers with an oxide layer disposed therebetween, such as described with reference to FIG. **2**. In a post-bond anneal, Si—O reacts with Si—O to form Si—O—Si. In some embodiments, interface **500** is an ultra-thin oxide layer of approximately 5 Angstroms to 25 Angstroms. It is anticipated that any residual $H_2$ or $H_2O$ is substantially or completely absorbed in the interfacial oxide **400**. Also it is anticipated that the interface **400** oxide will accommodates crystal mismatch between different crystal orientations.

**[0031]** According to the above-described embodiments, ultra-thin oxide layer **213** allows multi-layer substrate **211** to behave as a bulk substrate thereby avoiding substrate isolation. SOI substrates exhibit different device characteristics than bulk silicon and each requires completely different circuit design. Bulk substrate characteristics include, but are not limited to, lack of floating body effects or self-heating. Thus, even though ultra-thin oxide layer **213** is interdisposed between wafer **201** and wafer **203**, ultra-thin oxide layer **213** is sufficiently thin to allow multi-layer substrate **211** to behave as a bulk substrate. Moreover, ultra-thin oxide layer **213** can absorb interfacial gases, such as $H_2$ and $H_2O$ formed during the post-bond anneal process, which gases could otherwise result in voids. Additionally, full bonding can be done at room temperature which avoids complications associated with high temperature pre-heating of implanted wafers, i.e., direct bonding

**[0032]** Also, ultra-thin oxide layer **213** can accommodate lattice mismatch between different crystal orientations. For example, bonding of (**100**) crystal orientation to (**110**) crystal orientation can result in a 40% mismatch. That is, one out of every four atoms are mismatched at the interface between (**100**) silica and (**110**) silica (see FIG. **6**). Thus, ultra-thin oxide layer **213** may be needed due to the anticipated high density of dislocation between atoms. Ultra-thin oxide layer **213** allows the bonding for largely mismatched materials without formation of misfit or threading dislocations. "Misfit dislocation" refers to the mismatch between individual atoms of different crystal orientations. "Threading dislocation" refers to non-equilibrium defects that raise the free energy of a layer. Threading dislocations are deleterious for physical performance.

**[0033]** FIG. **7** shows a cross-sectional side view of an integrated circuit package that is physically and electrically connected to a printed wiring board or printed circuit board (PCB) to form an electronic assembly. The electronic assembly can be part of an electronic system such as a computer (e.g., desktop, laptop, handheld, server, etc.), wireless communication device (e.g., cellular phone, cordless phone, pager, etc.), computer-related peripheral (e.g., printer, scanner, monitor, etc.), entertainment device (e.g., television, radio, stereo, tapes and compact disc player, video cassette recorder, motion picture expert group audio layer 3 player (MP3), etc.), and the like. FIG. **7** illustrates the electronic assembly as part of a desktop computer. FIG. **7** shows electronic assembly **700** including die **710**, physically and electrically connected to package substrate **720**. Die **710** is an integrated circuit die, such as a microprocessor die, having, for example, transistor structures interconnected or connected to power/ground or input/output signals external to the die through interconnect lines to contacts **730** on an external surface of die **710**. The die may be formed in accordance with known wafer processing techniques using as the substrate the substrate described with reference to FIG. **2**. Contacts **730** of die **710** may be aligned with contacts **740** making up, for example, a die bump layer on an external surface of package substrate **720**. On a surface of package substrate **720** opposite a surface including contacts **740** are land contacts **750**. Connected to each of land contacts **750** are solder bumps **760** that may be used to connect package **770** to circuit board **780**, such as a motherboard or other circuit board.

**[0034]** Although the foregoing description has specified certain processes and materials that may be used in the method of the present invention, those skilled in the art will

appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims. In addition, it is appreciated that wafer bonding to manufacture a silicon device is well known in the art. Therefore, it is appreciated that the figures provided herein illustrate only portions of an exemplary microelectronic device that pertains to the practice of embodiments of the present invention. Thus, the present invention is not limited to the structures described herein.

What is claimed is:

**1**. A device comprising:

a multi-layer substrate comprising a first layer, an interfacial layer and a second layer, the interfacial layer disposed between the first layer and the second layer, the multi-layer substrate having a characteristic of a bulk substrate when the interfacial layer is less than 15 Angstroms.

**2**. The device of claim **1**, wherein the first layer has a first crystal orientation and the second layer has a second crystal orientation.

**3**. The device of claim **2**, wherein the first crystal orientation is one of (**100**), (**110**) or (**111**).

**4**. The device of claim **2**, wherein the second crystal orientation is one of (**100**), (**110**) or (**111**).

**5**. The device of claim **1**, wherein the substrate bonded interface is substantially free of voids.

**6**. The device of claim **1**, wherein the interfacial layer is between 5 Angstroms and 25 Angstroms.

**7**. The device of claim **1**, wherein at least one of the first layer and second layer is hydrogen implanted.

* * * * *