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Jordan, Jr.

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[45] Aug. 7, 1973

[54] **MEMORY SELECTION APPARATUS**

[75] Inventor: **William F. Jordan, Jr.**, Wellesley, Mass.

[73] Assignee: **Honeywell, Inc.**, Minneapolis, Minn.

[22] Filed: **Dec. 7, 1970**

[21] Appl. No.: **95,904**

Related U.S. Application Data

[60] Division of Ser. No. 675,081, Oct. 4, 1968, Pat. No. 3,588,851, Continuation-in-part of Ser. No. 536,736, March 23, 1966, abandoned, Continuation-in-part of Ser. No. 536,921, March 23, 1966, abandoned.

[52] **U.S. Cl.** **307/215**, 307/213, 307/218, 307/270, 307/300

[51] **Int. Cl.. H03k 19/36**, H03k 19/24, H03k 17/04

[58] **Field of Search** ..... 307/213, 215, 218, 307/270, 280, 300, 299 A

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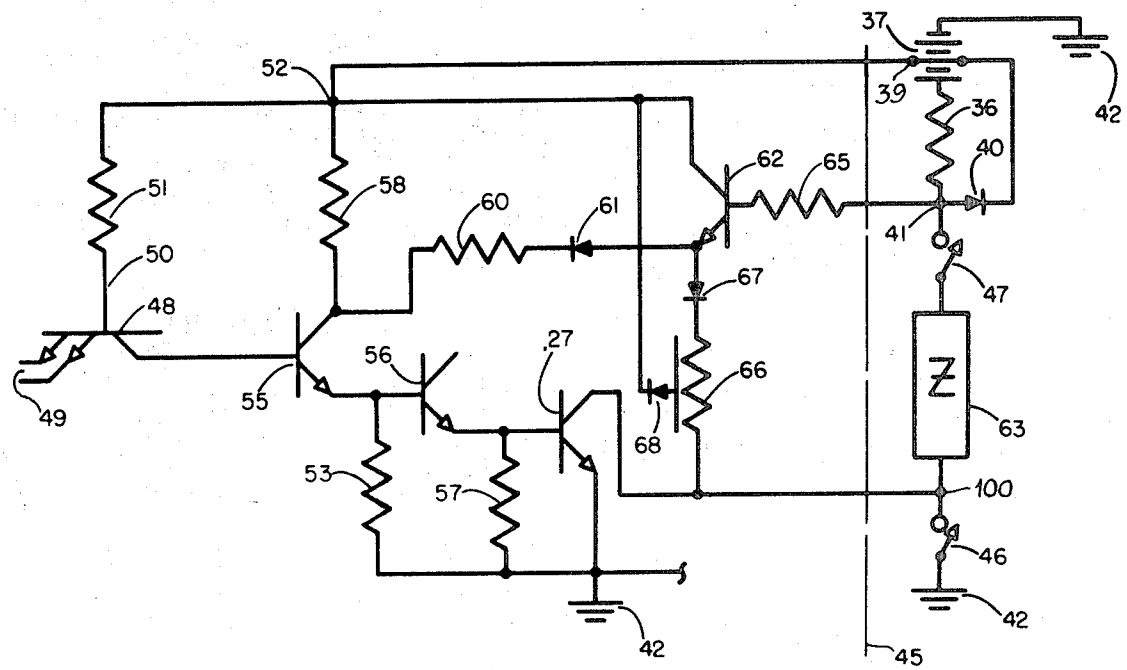
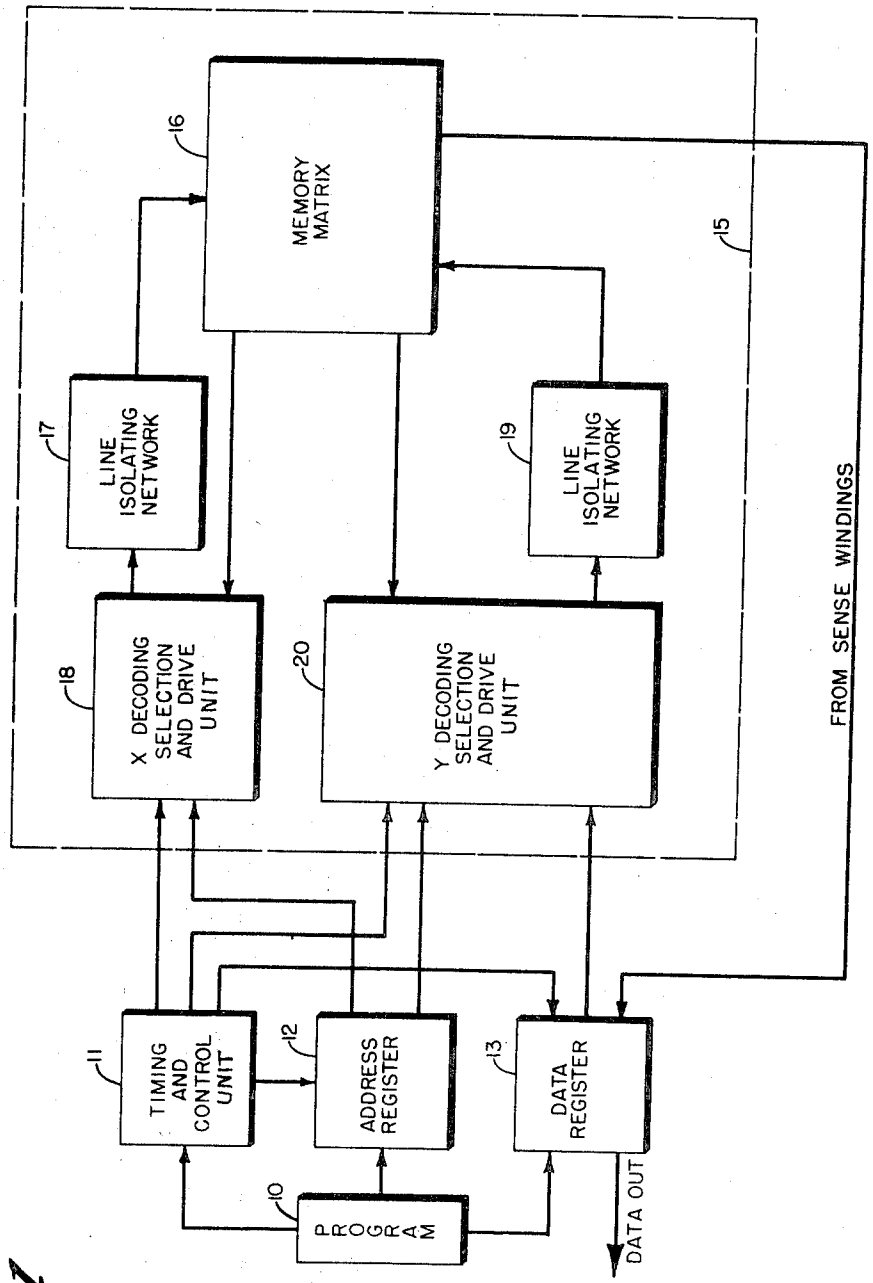
Primary Examiner—John W. Huckert
Assistant Examiner—L. N. Anagnos
Attorney—W. Hugo Liepmann and Fied Jacob

[57] **ABSTRACT**

Electronic selection circuits for operating coincident-current magnetic memories, and like apparatus, are provided for construction essentially entirely as integrated circuits, even the output drive stages. The circuits are arranged to transform ground referenced input signals to output signals for driving floating reactances without the transformers required in the prior art for voltage isolation. Further, the new circuits drive these reactive loads without excessive power dissipation or excessive transient voltages.

4 Claims, 9 Drawing Figures




MEMORY MATRIX
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LINE ISOLATING NETWORK
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LINE ISOLATING NETWORK
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X DECODING SELECTION AND DRIVE UNIT
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Y DECODING SELECTION AND DRIVE UNIT
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FROM SENSE WINDINGS
TIMING AND CONTROL UNIT
11
ADDRESS REGISTER
12
DATA REGISTER
13
PROGRAM
10
DATA OUT

Fig. 1

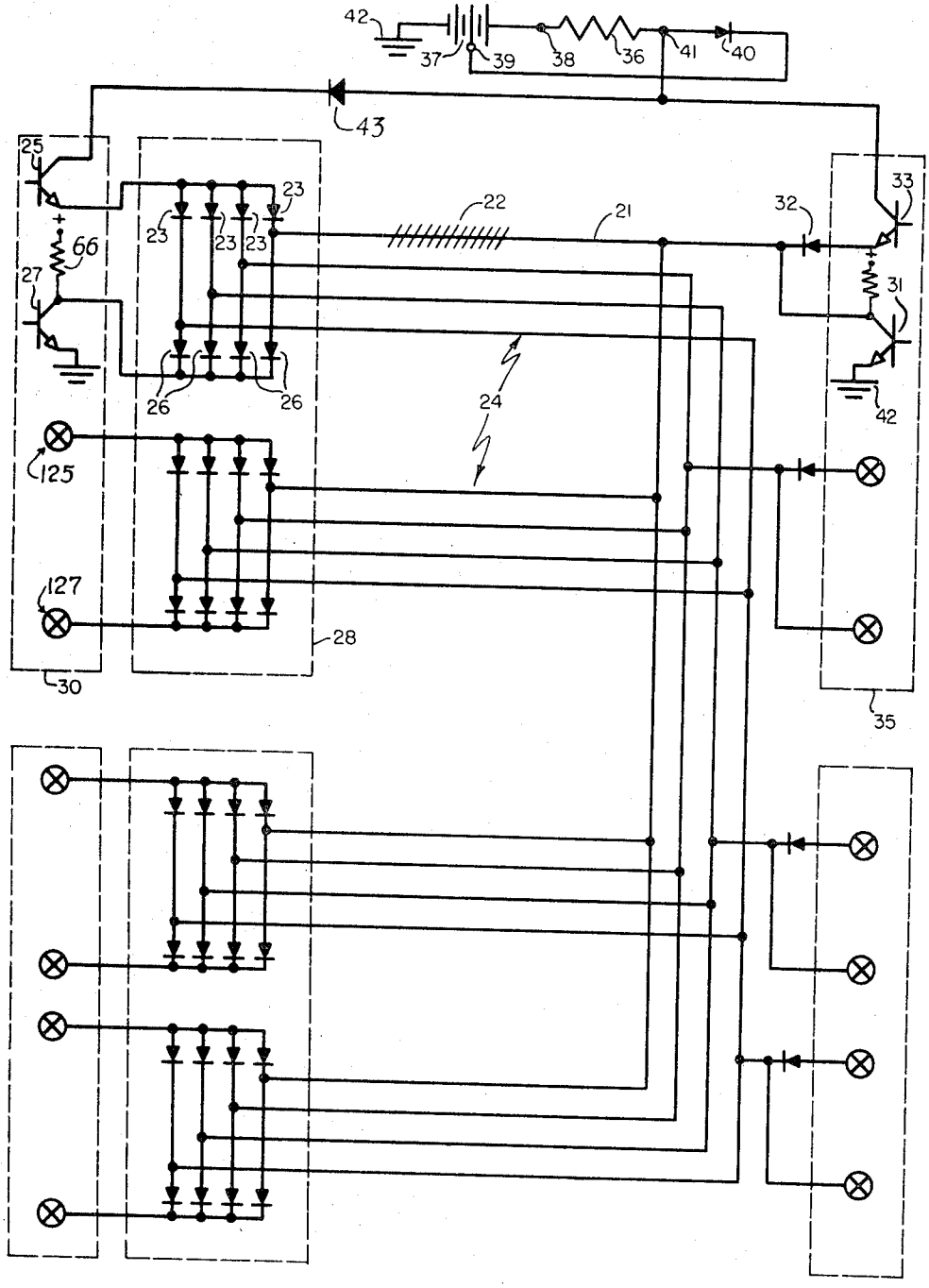
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Fig. 2

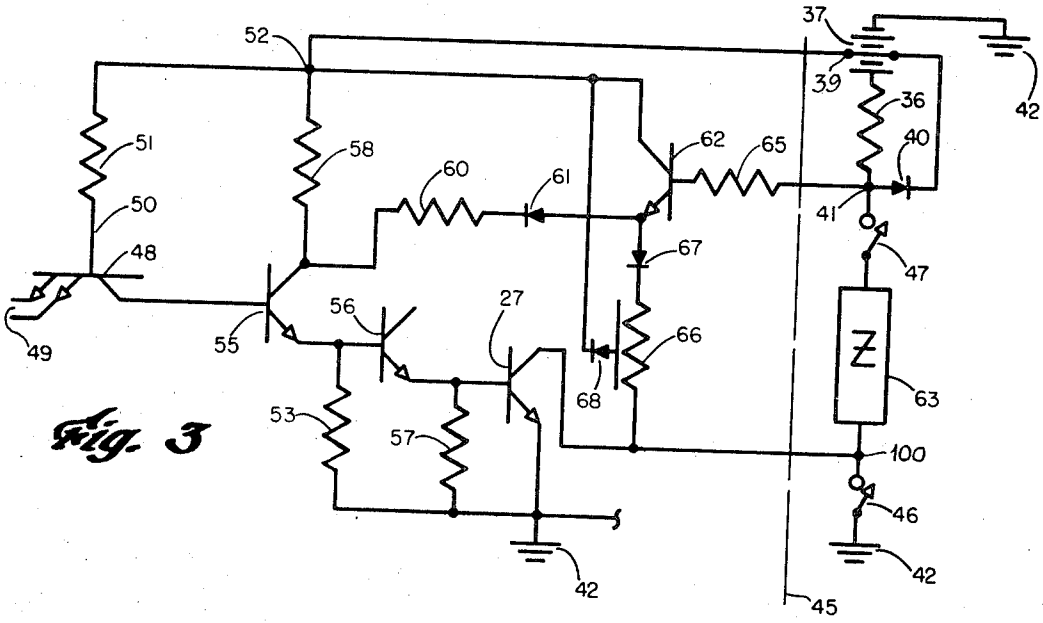
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Fig. 3

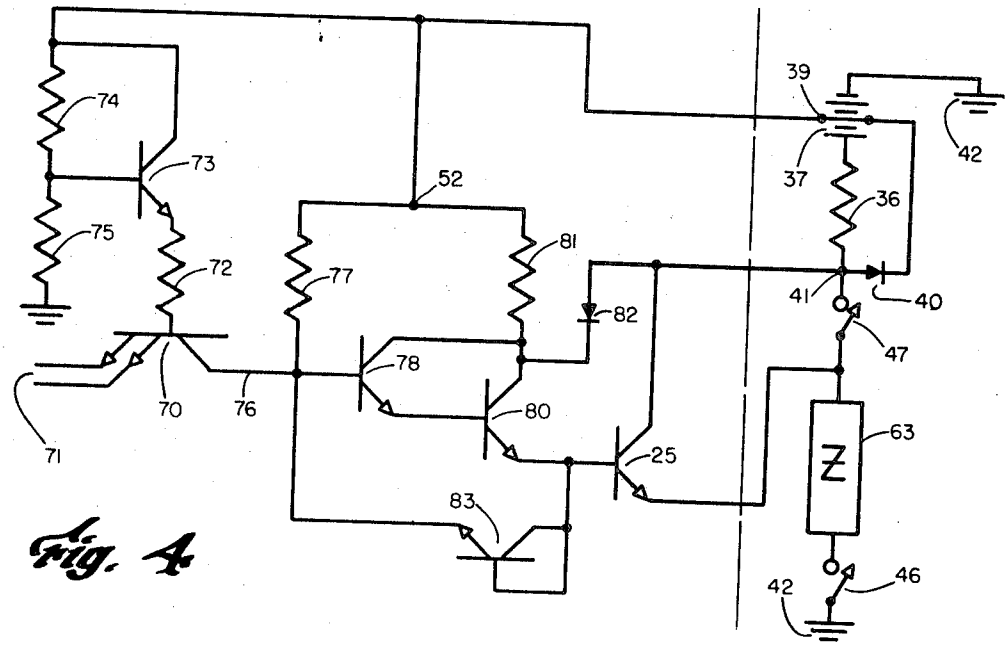
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Fig. 4

Fig. 5

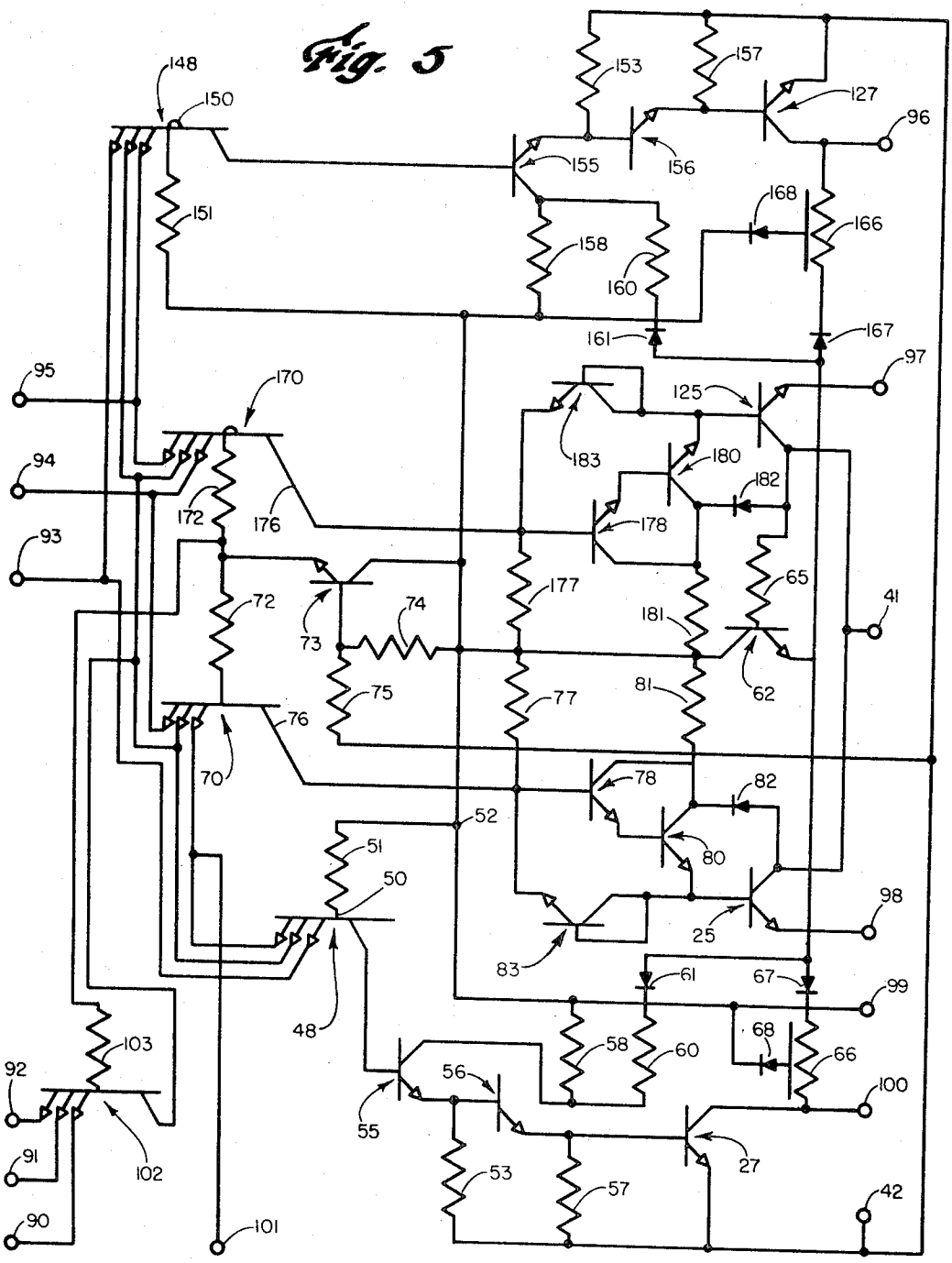
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Fig. 6

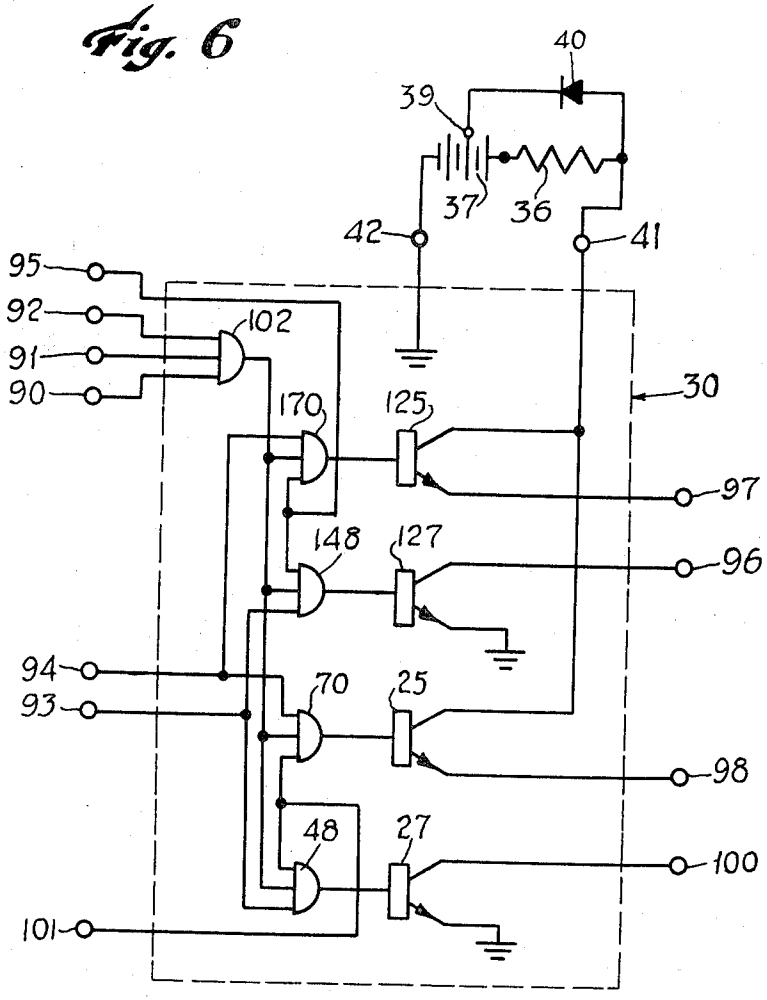
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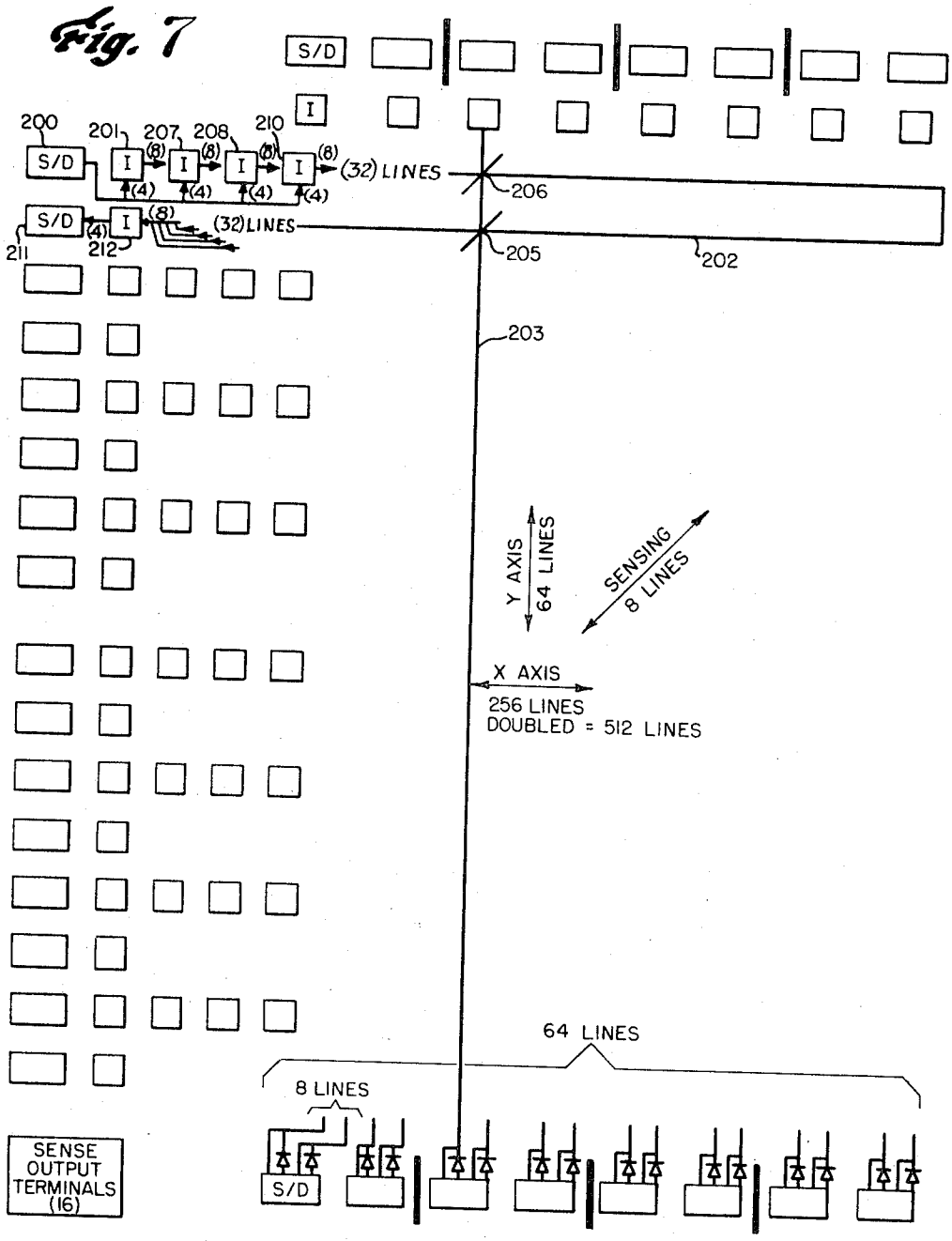
Fig. 7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I
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201
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S/D
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211
212
203
Y AXIS
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SENSING
8 LINES
X AXIS
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SENSE
OUTPUT
TERMINALS
(16)
S/D

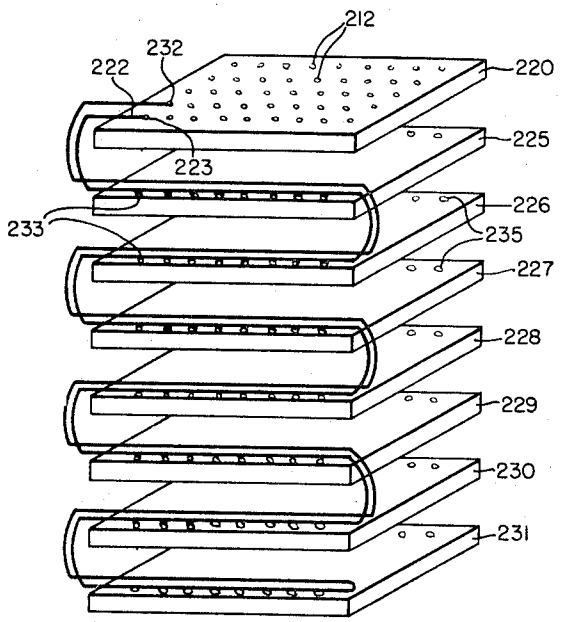
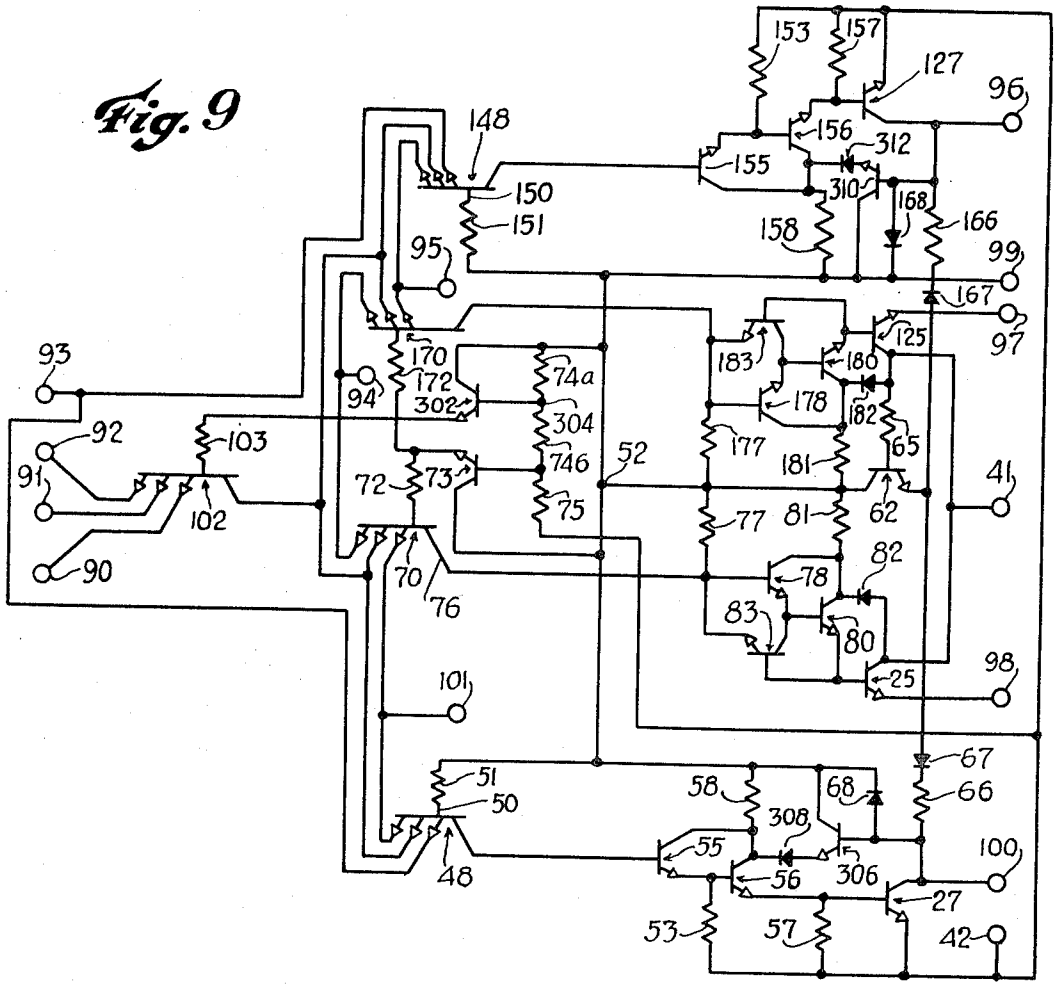


Fig. 8

Fig. 9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MEMORY SELECTION APPARATUS

This application is a division of Ser. No. 675,081, filed on Oct. 4, 1968, now U.S. Pat. No. 3,588,851, which application was a Continuation in Part of Ser. Nos. 536,736, and 536,921, both filed on Mar. 23, 1966 and owned by the Assignee hereof, and now abandoned.

This invention relates to selection circuits for operating coincidentcurrent magnetic memories and like electrical devices. In particular, it provides such circuits that can be fabricated essentially entirely with monolithic integrated construction even on a commercial scale, i.e., in relatively large quantity and at industry-wise competitive cost. The monolithic construction enables the circuits to be compact; and because signal paths therein are short, they are fast.

The selection circuits of the invention also provide advantages in performance and cost, whether constructed as integrated circuits or otherwise, e.g., with discrete components.

When used to operate a coincident current magnetic memory, the selection circuit performs the decoding, drive and switching operations with which a pulse of current of selected polarity is applied to one line of the memory in response to address and read-write control signals.

Integrated circuits are known to provide economies in cost and size for electronic circuits. However, they have limited tolerence to heat dissipation and to reverse voltage on semiconductor junctions. Also, inductors, and particularly coupled inductors as used in forming transformers, are not readily fabricated with integrated construction.

These problems have restricted the use of integrated circuits, particularly for operating coincident current memories. This is because such memories present reactive impedances to their driving circuits, which consequently must develop relatively large currents to switch such loads. Also, prior circuits have developed relatively large transient voltages when switching such loads, and it is costly and relatively difficult to fabricate semiconductor junctions by means of integrated circuit techniques which withstand such voltages. Another problem is that the voltage isolation desired in such circuits between the ground referenced input signals and the output signals, the potentials of which are load and time dependent, has heretofore been considered to be best handled by resort to isolation transformers. But transformers are not readily fabricated by means of integrated circuit techniques.

Also in the prior art, a conventional circuit for selecting one corethreading line in a core memory employs two voltage supplies of symmetrical voltages, i.e., $+v$ and $-v$. Two pairs of switches per line are operated to apply current from one of the two supplies to the line, according to the desired current direction. With this prior arrangement, faulty logic or a malfunction can place both supplies in series, which can result in destructive circuit damage, particularly to the transistors forming the switches.

Further, it is an unfortunate drawback that the leads from a coincident-current memory are necessarily abundant. These leads run to selection and driver components for providing read-write currents to the selected storage element. Due partly to the amount of lead length required, with inherent stray capacity and inductance, and partly to inductance and drive requirements of the storage elements, the necessary drive power has heretofore required utilization of a large number of "discrete" circuit elements.

As used herein, "discrete" elements are defined as circuit elements such as transistors, diodes, resistors, and capacitors that exist individually, in individual physical packages. This is in opposition to integrated circuit elements, which are formed simultaneously with other circuit elements and their interconnections in a single physical package. A monolithic integrated circuit is an operative configuration of interconnected components formed on a single block of semiconductor material. Commonly the block is a chip of silicon measuring about 1 to 10 square millimeters in area with the circuit formed by diffusion and evaporation techniques.

The use of discrete circuit elements produces a volume and packaging problem that makes it difficult to unite the drive and selection circuitry of a memory in really close proximity to, or in the same physical package or module with, the memory elements with which the circuit operates.

Now in accordance with the present invention, selection circuitry for magnetic storage media are provided which are adapted for economic construction essentially entirely as monolithic integrated circuits. This is obtained by a minimal power-dissipation form of circuit that can be incorporated in the same monolithic chip, if so desired, with the drivers for a plurality of drive lines of a magnetic core or like memory. In one embodiment, four drive transistors with their associated circuitry are incorporated in a single monolithic element.

The result of essentially complete utilization of integrated circuit elements for decoding, driving and line-isolating functions in accordance with the invention is a complete functional computer memory of surprisingly small size. If desired, the circuitry and the magnetic storage media can be packaged on a single printed circuit wiring board. One result is that many prior art interconnecting leads are eliminated, and others can be replaced with printed circuits; both providing greater stability and reliability. The reduced lead length results in decreased stray inductance and capacitance. Also, both operating speed and power requirements are improved.

It is an object of this invention to provide a memory selection circuit of comparatively low cost and comparatively small size. The circuit should be suited for large-scale commercial production. In particular, it is an object to provide such a circuit for operating a coincident-current magnetic memory.

Another object of the invention is to provide a coincident-current memory selection circuit suited for construction substantially entirely as an integrated circuit. Specifically, it is an object to provide the decoding, drive and switch portions of such a circuit suitable for monolithic integrated construction.

A further object of the invention is to provide circuits for operating coincident-current memories and like devices which have improved performance relative to prior circuits of this type. In particular, it is an object to provide such circuits that develop comparatively low transient voltages even when driving reactive loads. Another specific objective is that the circuits have relatively low vulnerability to destructive damage in the

event of component breakdown or erroneous operation.

A further object is to provide a selection circuit of the foregoing character operating with relatively high electrical efficiency, particularly having relatively low average power dissipation.

It is another object of the invention to provide a circuit of the above character capable of relatively fast switching of reactive loads, and in particular of core-threading memory lines.

It is also an object of the invention to provide a circuit of the above character providing efficient operation in response to ground-based input signals without the use of discrete inductive elements or transformers.

Further objects of the invention are to provide a sink drive circuit for driving one end of a line in a magnetic storage array and which can be implemented essentially entirely with integrated circuitry; and to provide a switch drive circuit for driving a second end of a line in a magnetic storage array that also can be implemented essentially entirely with integrated circuitry.

Other objects of the invention will in part be obvious and will in part appear hereinafter.

The invention accordingly comprises the features of construction, combinations of elements and arrangement of parts exemplified in the constructions hereinafter set forth and the scope of the invention is indicated in the claims.

SUMMARY OF THE INVENTION

In accordance with the invention, a selection circuit for operating a coincident-current magnetic memory and like electrical devices is provided that can be fabricated with integrated circuit techniques. The circuit has the low power dissipation and the freedom from excessive transient voltages desired for high reliability with integrated components. However, the circuit has active feedback paths automatically operative during turn-on transients to expedite this switching operation. Other elements of the circuit automatically operate during turn-off transients to hasten the return to the off condition.

In addition, the selection circuit applies current of a selected polarity to a core-threading memory line from a single supply, rather than from a symmetrical pair of supplies as in the prior art. With this new arrangement, erroneous switching operation does not produce the destructive damage likely with prior circuits.

These and other features described herein below enable memory selection circuits to be fabricated essentially entirely with monolithic integrated construction. Such circuits embodying the invention are highly compact and are well suited for relatively high volume manufacture at comparatively low cost. Further, they are capable of fast operation and they facilitate compact and electrically-efficient and low cost connection to the memory they operate.

BRIEF DESCRIPTION OF FIGURES

For a fuller understanding of the nature and object of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 is a functional block diagram of a digital computer;

FIG. 2 is a schematic representation of a portion of a selection circuit embodying the invention;

FIG. 3 is a simplified schematic representation of the sink circuit portion of FIG. 5;

FIG. 4 is a simplified schematic representation of the switch circuit portion of FIG. 5;

FIG. 5 is a schematic diagram of a selection circuit embodying the invention;

FIG. 6 is a functional symbolic representation of the FIG. 5 circuit,

FIG. 7 is a block diagram of a multi-bit core memory embodying features of the invention;

FIG. 8 is a simplified showing of a magnetic core stack embodying features of the invention; and

FIG. 9 is a schematic diagram of another selection circuit, similar to that of FIG. 5, embodying features of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1 is a block diagram representing a conventional digital computer. A "program" block **10** represents the input facilities that perform the programming functions. A timing and control unit **11**, an address register **12**, and a data register **13** all receive program instructions i.e., control signals. A fast access memory indicated generally at **15** includes the blocks within the dashed outline. Memory **15** is depicted as one of a large number of common and essentially identical units operated in conjunction with the same timing, address and data units.

Memory **15** generally comprises one or more memory matrices **16** and selection and drive units **18** and **20.** Each memory matrix usually contains many thousands of binary switch elements such as magnetic cores. The cores are threaded in a matrix on conductive leads termed lines. A specific core is selected by applying drive current on two lines both threading, i.e., having windings on, the specified core. Current is applied in one direction for a "write" operation and in the reverse direction for a "read" operation. Line isolating networks **17** and **19,** constructed for example, as conventional "two-diode-per-line" networks, provide a reduction in equipment by restricting current to a single desired path for both read and write operations. Current is applied to the lines by drive switches which in turn are enabled by decoding circuitry. Current is applied along one line by an "X decoding, selection, and drive unit" **18** and along the intersecting line by a "Y decoding, selection, and drive unit" **20.**

The only feature in FIG. 1 that distinguishes it from conventional computers is the position of the dashed line defining memory **15.** In accordance with one aspect of the present invention, all the functions indicated in memory **15** can be performed with circuits constructed substantially entirely as integrated circuits and hence capable of assembly in a remarkably small package — even, where desired, on the same circuit card which carries an array of cores. (This construction assumes that the memory matrix **16** is built up of plural planes of threaded magnetic cores, the cores in each plane being threaded with X and Y lines in a rectangular configuration of rows and columns, respectively.)

The block diagram, FIG. 1, depicts what is called a "2½D" memory organization. By way of comparison, one common early memory organization using magnetic cores is the "3D" system in which each core carries four windings: X-axis winding, Y-axis winding, inhibit winding and sense winding. In a "2½D" memory, the windings are reduced to three by eliminating

the inhibit winding and adding the inhibit function to the Y-axis input logic. In FIG. 1 this is indicated by the input to the Y unit 20 from data register 13. However, the decoding, selection, and drive circuits of the present invention can be utilized equally well in 3D and other memory organizations.

The interconnections between the registers 12 and 13 and the unit 11 and the memory 15 are not described in detail, nor are the programming, register and timing units described, since various conventional configurations of these components can be utilized within the scope of the invention.

FIG. 2 is a partial schematic representation of the inventive memory 15 depicting a few of the matrix lines 24 for one axis with magnetic storage elements 22 represented by short transverse marks on one matrix line 21. It will be understood that in practice a memory may have many more lines and each line threads a number of storage elements. Typically the storage elements run to over one thousand per line.

One end of each line 24 is connected through an isolating diode to a switch and through another isolating diode to a sink transistor. For example, one end of line 21 is connected through an isolating diode 23 to a switch transistor 25 and through an isolating diode 26 to a sink transistor 27. It is to be understood that all of the switch transistors 25 and sink transistors 27 are transistor switches. The terms "switch" and "sink" are arbitrarily chosen to distinguish the switched potential levels. The sink transistor switches to a common ground reference potential. The switch transistor switches to a potential, illustrated as positive, different from the common ground level. Isolating diodes 23 and 26 can be made in the form of a monolithic chip flat pack 28. That is, these diodes can be fabricated on a single chip of semiconductor material and the chip packaged as a conventional flat pack. In the embodiment illustrated, this flat pack 28 contains sixteen diodes connected to eight matrix lines. Switch 25 and sink 27 are also suitably made in the form of a monolithic chip 30 comprising two switches and two sinks. Monolithic chip 30 also includes decoding circuitry which will be described in detail with relation to FIGS. 3, 4 and 5.

With further reference to FIG. 2, lines 24 are also each connected at an opposite end to a further switch transistor and sink transistor. For example the upper most line 21 is connected to a sink transistor 31 and through a diode 32 to switch transistor 33. Sink transistor 31 and switch transistor 33 are formed in a monolithic chip 35 identical to chip 30. Diode 32 is a reverse voltage protection device to protect the base-emitter junction of switch transistor 33 against reverse voltage breakdown. Integrated circuit diodes 23 perform this function with respect to switch transistor 25. Diode 32 is preferably a discrete element since integrating it into chip 35 would significantly increase the thermal dissipation requirements of the chip.

The remainder of the circuitry in FIG. 2 is merely a repetition of what has been described with the exception of the electrical supply arrangement, at the top of the drawing, now to be described.

In order to draw a known current essentially independent of the memory impedance, it is generally desirable to operate a magnetic storage matrix from a constant current source or at least a source with some current regulation. This is commonly achieved by using a higher than necessary voltage with a current limiting resistor. When used with monolithic integrated circuits, this technique allows undesirably high voltages to appear between detail portions of the monolithic chip e.g., between two electrodes of a transistor. That is, the conventional supply arrangement of a higher than necessary voltage supply and a current limiting resistor results in the development of undesirably high voltages across the semiconductor material constituting the diodes 23 and 26 and the source and sink transistors.

In accordance with one feature of the invention depicted at the top of FIG. 2, a current source is provided by a discrete element current limiting resistor 36 connected at one end 38 to a source 37 of a relatively high voltage and clamped at the other end 41 by a discrete element diode 40 to a lower voltage at terminal 39. End 41 of resistor 36 is the current source terminal for the matrix lines. Clamp 40 prevents the voltage across the semiconductor elements 28, 30 and 35 from exceeding the lower voltage at the resistor end 41. It should be understood that the designation of elements such as the resistor 36 and diode 40 as discrete is not necessary to practice the invention; it merely denotes a preferred embodiment of the invention.

As also shown in FIG. 2, a further diode 43 is in series between the supply terminal 41 and the switch transistor 25. It is provided so that current applied to any line 24 from this supply terminal 41 passes through the same number of diodes regardless of the direction of the current in the line 24.

In operation, line 21 is selected with current directed from left to right (FIG. 2) by turning transistors 25 and 31 on. The resulting low resistance path from ground 42, through the emitter-collector circuits of transistors 31 and 25, to terminal 41 reverse biases clamp diode 40. The circuit then operates as though the clamp diode did not exist. When transistors 25 and 31 are turned off, the voltage at terminal 41 again rises to the clamp voltage, at which point diode 40 again conducts forward current, preventing further voltage increase.

It was previously supposed that with no current in line 21 at the instant the transistors were turned on, a voltage of about 24 volts was necessary to ensure a fast rise time, i.e., a rapid turning on of the transistors. Close observation and analysis of prior circuits in operation revealed that the voltage at terminal 41 in the absence of clamp 40 dropped immediately to about 14 volts as soon as any one of the switch transistors was turned on. The reason for the voltage drop was eventually determined as capacitive loading by the unswitched lines 24.

For example, as soon as transistor 25 is turned on, stray capacitance between all the lines connected to diodes 23, and from these lines to ground, discharges through those diodes and the conducting transistor 25. This produces significant clamping during the current rise time so that the voltage at terminal 41 does not attain the level at which diode 40 is conductive. Under these conditions, the addition of clamping diode 40 has little effect on rise time. However, the higher voltage from source 37 clamped with diode 40 through the current limiting resistor 36 is still desirable to provide a stable current through the selected lines after the transient rise interval.

The clamping diode 40 is of particular importance when all of the switches connected to the particular source are turned off, disconnecting all lines. In the ab-

sence of clamping diode 40 under this condition, the voltage at terminal 41 would rise to the full source voltage applying, in the illustrated example, 24 volts across the semiconductor elements to which it is connected. Clamping diode 40, however, prevents this voltage from ever exceeding a predetermined relatively low level, for example, 14 volts.

Thus, reviewing the circuit of FIG. 2, in each group of four memory lines 24 connected with a switch-sink transistor pair on a monolithic chip 30, one memory line 21 is selected with current directed from left to right by turning on transistors 25 and 31 and having transistors 27 and 33 turned off. This applies the voltage at resistor end 41 to the collector of transistor 25 with the result that current successively passes from the source 37 through resistor 36, diode 43, transistor 25 collector-emitter path, one diode 23, to the line 21 and through transistor 31, from its collector to emitter, to the common ground 42 to which the source 37 is returned.

Similarly, turning on only transistors 33 and 27 applies the same-magnitude current through line 21, but directed from right to left in FIG. 2. From the source 37, the current successively passes through the transistor 33, diode 32, line 21, one diode 26, and transistor 27.

In either of these operating conditions, the current in line 21 traverses resistor 36. However, the low impedance of the conducting pair of transistors 25 and 31 or 27 and 33, and of the elements between them, holds the voltage at the resistor end 41 to below the value at which the diode 40 conducts appreciable current.

When all transistors 25, 27, 31 and 33 are off, so that essentially no current is applied to any line 24 in circuit with them, the diode 40 is biased to conduction and clamps the voltage at the resistor end 41 to the desired maximum level. The resistor 36 conducts the diode clamping current.

With this arrangement, the voltage across the transistors 25, 27, 31 and 33, and across the diodes 23 and 26, never materially exceeds the value to which the diode 47 clamps the resistor end 41. Further, the dynamic range of voltages across these transistors and diodes is essentially only between this clamped voltage and the common ground 42.

If two transistors 25 and 27 or 31 and 33 should conduct simultaneously due to some fault, the current through them is limited to the same nominal value normally conducted. Hence, this fault condition is not materially different from the desired operating conditions described above inasmuch as two transistors are in series between the resistor 41 and the common ground 42 in both instances. As a result, this fault condition is not likely to damage any circuit components.

A further feature of the FIG. 2 circuit is that a single supply i.e., a single combination of the source 37, resistor 36 and clamping diode 40, is sufficient to operate many memory lines 24; there are 16 in the illustrated relatively simple embodiment. This results in a saving of circuit components with a corresponding saving in cost, weight, space and dissipation.

FIG. 5 is an essentially complete schematic representation of an embodiment of the selection circuit for block 30 in FIG. 2 and capable of monolithic integrated circuit construction; block 35 of FIG. 2 preferably employs identical circuitry. However, before considering FIG. 5, FIGS. 3, 4 and 6 pertaining to it will be described, starting with FIG. 6 which is a symbolic representation of the elementary logic functions performed with the FIG. 5 circuit.

In FIG. 6, three address signals are applied to terminals 90, 91, and 92 for selecting the block 30 out of a group of (2^3) or eight such blocks. The terminals 90, 91 and 92, when they receive assertion level signals, operate a coincidence gate 102 to apply an assertive output signal to one input terminal on each of four coincidence gates 48, 70, 148 and 170. The single output signal from each of these gates operates, when assertive, a transistor 27, 25, 127 and 125 respectively. These are the same transistors 27, 25, 127, 125 shown in FIG. 2.

A further address signal applied to terminal 95 in FIG. 6 enables the gates 170 and 148, and a like address signal applied to terminal 101 enables the two gates 70 and 48. The Read control pulse is applied to a terminal 94 to operate whichever of gate 70 and 170 is simultaneously receiving assertive signals on its other two input terminals. Likewise, a Write control pulse is applied to a terminal 93 to operate whichever gates 48 and 148 is simultaneously receiving assertive signals on its other two input terminals.

The FIG. 6 terminals 96, 97, 98 and 100 connect to the FIG. 2 diode block 28 as indicated in FIG. 2. The connection of the block 30 to the supply shown at the top of FIG. 2 is also indicated in FIG. 6.

Thus, by way of example, the coincidence of three assertive address signals at terminal 90, 91, and 92, and at terminal 95, plus a Write pulse at terminal 93, activate the coincidence circuit 148. Its resultant output signal turns on transistor 127 to provide a low-impedance path to ground from the terminal 96.

FIGS. 3 and 4 show portions of the FIG. 5 selection circuit. In the detail circuits of FIGS. 3, 4 and 5, the reference numerals 48, 70, 148, 170 and 102 used in FIG. 6 to denote coincidence gates are used with reference to multiple-emitter transistors that provide the logical coincidence function.

FIG. 3 shows the circuitry associated with the sink transistor 27 of FIG. 2 and represented in FIG. 6 with the gate 48 and transistor 27. The FIG. 3 impedance 63 represents the core memory, i.e., the core-threading lines 24 of FIG. 2, and the diodes 23 and 26 in the FIG. 2 block 28. The circuit applies current to this impedance when both the FIG. 3 sink transistor 27 is conducting and switch 47, which represents any one transistor switch such as the transistor switches 33 and 25 of FIG. 2, is closed (i.e., the switch transistor is conducting).

The circuit is basically an amplifier actuated when all inputs on leads 49 are positive. When actuated, for the purpose of reducing turn-on time, the circuit overdrives the transistor 27 until it becomes saturated. When the transistor 27 is turned off, the circuit discharges transient current from the inductive impedance 63 without subjecting any components to excessive, and hence potentially damaging, voltages or currents. Moreover the transient discharge path reduces system noise voltages. These features enable the circuit to attain fast operation with a relatively highly reactive load 63 with only relatively low dissipation requirements and relatively small peak voltages and currents, even during switching transients.

More specifically, a multi-emitter transistor 48 in FIG. 3 is connected at the input of the circuit to provide a selection function. It has two or more emitters

connected to inputs leads **49**. The base **50** is connected through a current limiting resistor **51** to a terminal **52** connected to the tap **39** on the source **37** described above with reference to FIG. **2**. The collector of transistor **48** is connected directly to the base of transistor **55**.

The collector of transistor **55** is connected through a resistor **58** to supply terminal **52** and also through resistor **60** to the cathode of a diode **61**. The anode of diode **61** is in turn connected to the emitter of a further transistor **62**. The emitter of transistor **55** is connected through a resistor **53** to common ground **42** and also by a direct connection to the base of transistor **56**.

Where the elements in the block **30** are fabricated on a single semiconductor chip, i.e., with monolithic integrated construction, common ground **42** is common to the reference substrate of the chip.

The emitter of transistor **56** is connected to the base of transistor **27** and also through a resistor **57** to the common ground **42**. Transistor **56** is connected with its collector floating for use as a diode. The emitter of transistor **27** is connected to common ground, while the collector is connected to an output terminal **100**. The collector of transistor **27** is also connected through a resistor **66** to the cathode of a diode **67**. The anode of diode **67** is connected to the emitter of transistor **62**. Transistor **62**, which may be shared by two or more of these circuits as shown in FIG. **5**, has a collector connected to supply terminal **52** and a base connected through a resistor **65** to supply terminal **41**.

In FIG. **3**, the dashed line **45** shows the division between the circuitry connected to transistor **27** and illustrated as fabricated on block **30** in FIG. **2**, and other memory circuitry connected with it. For example, switch **46** is representative of other sink transistor circuits, while switch **47** represents other switch transistor circuits. Resistor **36** and diode **40** are the same as those illustrated in FIG. **2** along with supply **37**.

Considering the operation of the FIG. **3** circuit, the multiple emitter transistor **48** serves as an input AND gate. All emitters on transistor **48**, which may be two as illustrated, or more, must be gated off by signals that are positive with respect to the potential of base electrode **50**, in order for sink transistor **27** to conductor. With all emitters of transistor **48** gated off, current from the positive supply terminal **52** passes through the bias resistor **51** and the forward-biased collector-base junction of transistor **48** to bias transistor **55** on, i.e., into conduction.

Transistor **55** provides gain and together with transistor **56** operates to provide noise immunity in the operation of transistor **27**. This is because transistor **56**, connected as a diode, provides an essentially current-independent voltage drop, thereby increasing the input signal necessary to operate transistor **27**. Hence the accumulated base-emitter drops of transistors **55, 56** and **27** is sufficiently large substantially to preclude noise voltages at the base of transistor **55** from causing operation of transistor **27**.

Resistor **57** provides a discharge path for the input capacity, more precisely for the stored charge, of transistor **27**, and a resistor **58** connected from the collector of transistor **55** to supply terminal **52** provides the operating current for transistor **55**.

Thus, when all inputs to the emitter of transistor **48** are positive relative to the base **50**, the transistor **55** conducts and switches the transistor **27** to conduction. Its collector then drops from its normally positive potential to a potential near the ground level at the emitter.

When the memory matrix, represented as load **63**, is not receiving current, terminal **41** will be clamped at approximately the same voltage as supply terminal **52**. This clamped voltage at terminal **41** is sufficiently positive to bias transistor **62** to conduct current from the supply terminal **52**, through diode **61** and resistor **62**, to the collector of transistor **55**. However, so long as transistor **55** is not conducting, this current through transistor **62** is nil. On the other hand, as soon as transistor **55** is switched to conduction and before transient conditions terminate so that the voltage at terminal **41** drops toward the steady state "on" value, transistor **62** provides additional current for the collector circuit of transistor **55**, increasing to the current in its collector and hence at its emitter; resistor **60** is suitably selected to provide an equal current path as provided through resistor **58**. The end result is increased drive current for sink transistor **27** and is referred to hereinafter as "overdrive".

When current is applied to the matrix by closure of the switch **47** and turning on of transistor **27** and the turn-on transients settle, the voltage at terminal **41**, connected to the base of transistor **62**, drops. This in turn reduces conduction of transistor **62**, thereby removing the overdrive current applied to the collector of transistor **55**. The purpose of this arrangement is to provide overdrive current during turn-on of sink transistor **27**. With resistor **60** and resistor **58** approximately equal, the initial drive current through transistor **27** is thereby nearly doubled. The subsequent automatic reduction in base drive current upon delivery of current to the matrix reduces the average power dissipation of the circuit.

The purpose of providing this overdrive to transistor **27** is to turn the transistor on quickly, thereby initiating the desired memory operation with minimal delay. This action is opposed by the inductive reactance of the memory load **63**. Further, once the inductive memory reactance is charged, the excessive drive that turns transistor **27** on quickly is unnecessary and, in fact, would result in undesirably high dissipation. The present circuit solves all these problems by providing overdrive automatically only during the turn-on transient. The circuit automatically initiates the overdrive current when transistor **55** turns on and automatically terminates it when the turn-on transient ends so that the voltage at the base of transistor **62** drops. In this manner, the FIG. **3** circuit provides the desired high drive to transistor **27** for rapid turn-on yet maintains the continuous operation of transistor **27** at a low level where dissipation is minimal.

With further reference to FIG. **3**, the base-collector junction of transistor **62** forms a diode that serves the additional function of a protective clamp shunting the clamp diode **40**. That is, in case of failure of a clamp diode **40**, the several transistors **62** associated with that diode take over its clamping function. Diodes **61** and **67** serve as reverse voltage protection for transistor **62**. Also, the collector of transistor **27** (connected to the matrix load **63**) is connected through resistor **66** and diode **67** to the emitter of transistor **62**. As described hereinafter, this provides a reference potential for unloading matrix capacitance when no current is applied to the matrix.

Diode 68 in FIG. 3 is intrinsic to the integrated monolithic construction of resistor 66 and acts as a diode with its anode connection distributed along resistor 66. In the construction of an integrated circuit, a resistor is formed by a region of semiconductor material of a given conductivity type, e.g. with a selected impurity. This region is separated from the rest of the circuit by a layer of opposite conductivity type semiconductor material which will be biased to a fixed potential during operation. Connection is made to the resistor by electrodes at two spaced points in the region, and the resistance is determined by the geometry and resistivity of the region. The semiconductive materials, their conductivity type characteristics, and the fixed potential are so selected that the junction formed between them is reverse biased during normal operation. This electrically isolates the element from the remainder of the integrated circuit. However, schematically, the diode 68 is essentially connected between the output terminal 100 and the supply terminal 52.

The intrinsic diode 68 is advantageous in damping inductive kicks from the matrix during switching of the current therein. That is, a high voltage swing in the forward direction will cause conduction of diode 68. The large area junction formed by the resistor 66 permits high peak current with low voltage drop, thereby providing good protection against overvoltage breakdown in transistor 27.

The FIG. 3 transistor 62 provides the further function of restoring the load 63 to a positive voltage after current therein is interrupted by turning transistor 27 off. During application of current to the load through transistor 27, the load is at the near-ground potential of the transistor collector. When the transistor is switched off, the base-emitter junction of transistor 62 is briefly forward-biased. Hence, this transistor conducts through resistor 66 and the shunt capacitance of the load 63. As a result, this stray capacitance becomes charged to near the voltage at terminal 41.

FIG. 4 is a more-detailed schematic representation of the FIG. 6 gate 70 and switch transistor 25, in which switch transistor 25 is the same as transistor 25 in FIG. 2. Transistor 25 is arranged as an emitter follower driven from a logical "AND" input stage. This input stage is a common base multiemitter input amplifier transistor 70 with gating but no inversion. In addition to providing the logical AND selection function, transistor 70 provides voltage gain. It drives the three emitter-follower transistors 78, 80 and 25 that provide an impedance transformation, with direct coupled semiconductor elements exclusively (i.e., no transformers or the like), from the ground-based input signals at transistor 70 to the floating emitter of transistor 25. The memory load 63 is connected from this emitter to ground through the sink transistor 27 in FIG. 3 or other switches 46 as shown in FIG. 4.

In particular, the plural emitters of transistor 70 are connected to input leads 71. The base of transistor 70 is connected through resistor 72 to a biasing supply that consists of a transistor 73 and voltage divider resistors 74 and 75. The divider resistors tend to track with temperature and supply a stable control to bias transistor 73, which operates as a constant voltage supply to transistor 70.

Collector 76 of transistor 70 is connected to supply terminal 52 through a resistor 77 and is connected directly to the base of transistor 78. Transistors 78, 80 and 25 are connected as a three-stage emitter follower for current gain and high input impedance. The collectors of transistor 78 and 80 are connected through a resistor 81 to supply terminal 52. The collector of transistor 25 is connected to supply terminal 41 and the emitter is connected to the matrix load 63. Switch 47 represents other switch transistor circuits.

As also shown in FIG. 4, a diode 82 is connected with its cathode to terminal 41 and its anode to the collectors of transistor 78 and 80. A further transistor 83 is connected as a diode with its cathode (the emitter) connected to collector 76 and its anode (the base and collector) connected to the base of transistor 25.

In the operation of the FIG. 4 circuit, gating transistor 70 provides voltage gain while transistors 78, 80 and 25 all provide current gain. Resistor 81 is selected to maintain saturation of transistor 25 during the switch "on" time and thereby minimize dissipation in the transistor. Diode 82 provides quick turn-on with the inductive load by increasing the drive current through transistor 80 during the turn-on transient. In particular, when the transistor 25 is turned on, transistor 80 is also on, with its collector near the potential of the transistor 25 emitter. Thus, when the switch 46 closes, the relatively high clamped voltage at terminal 41 forward biases diode 82 so that it delivers current to the transistor 80 collector in parallel with the current the transistor normally receives through the resistor 81. The sum of these two currents applied to the transistor 80 collector are applied to the base of transistor 25 and hence to the load 63 through the transistor 25 emitter. This overdriving turn-on operation stops when the turn-on transient of the load 63 stabilizes, allowing the voltage at the terminal 41 to decrease, with the result that the diode 82 is no longer significantly forward biased.

The transistor 83 in FIG. 4 functions as a turn-off diode that discharges parasitic capacity between transistor 80 and transistor 25 and stored charge in these transistors. This speeds up the turn-off transition, i.e., the cessation of current in the load 63 in response to corresponding signals applied to the input transistor 70. In addition, when the transistor 70 is not applying an assertive signal to transistor 78, so that transistor 25 should be non-conductive, the transistor 83 functions as a diode preventing the transistor 25 base from becoming charged positive, and hence maintains the transistor 25 reliably off.

In reviewing FIGS. 3 and 4, average operating power dissipation is greatly reduced by the use of the "overdrive circuits" for increasing drive only during turn-on transients. The "overdrive" is automatically cancelled as soon as full turn-on is achieved so that drive power is reduced to a "holding" level. In FIG. 3 the overdrive is provided by transistor 62 under control from terminal 41. As full load current is attained through the matrix load 63, the voltage at terminal 41 decreases, cutting off the overdrive. In FIG. 4, diode 82 provides the overdrive current to transistor 80, again in response to the voltage at terminal 41.

Referring now to FIG. 5, it shows a selection circuit which can be fabricated as a monolithic integrated circuit. That is, all the transistors, diodes, resistors, terminals and interconnections shown in FIG. 5 can be fabricated on a single body of semiconductor material with conventional bipolar integrated circuit materials and techniques. As indicated in FIG. 6, the circuit incorporates two sink circuits of FIG. 3 and two switch circuits

of FIG. 4. The discrete elements separated in FIGS. 3 and 4 dashed lines 45 are of course not shown in FIG. 5 as they are not part of the monolithic chip 30 (FIG. 2). It will further be noted that while all the other circuit elements of FIG. 3 are duplicated in FIG. 5, transistor 62 and resistor 65 only occur once in FIG. 5, when they are shared by both sink circuits. Likewise, transistor 73 and resistors 74 and 75 of FIG. 4 appear only once in FIG. 5 and are shared by the two switch circuits. For convenience, the duplicated circuit elements in FIG. 5 appear in one instance with the same numbers used in FIGS. 3 and 4, in the other instance using the same number plus one hundred so that, for example, the sink transistors appear as transistor 27 and transistor 127. The input AND gates are illustrated in FIG. 5 using transistors of three emitters each instead of two as shown in FIGS. 3 and 4. The number of emitters can be varied according to the demands of the input logic.

An additional input transistor 102 is shown in FIG. 5 with its base connected through resistor 103 to the emitter of transistor 73. Its collector is connected to one emitter of each of input gate transistors 48, 70, 170 and 148. Transistor 102 is a multiemitter transistor having three emitters connected to input terminals 90, 91 and 92 for address and data signals, an illustration of which was previously considered with reference to FIG. 6. Transistor 102 serves the dual function of reducing the required number of input emitters and the number of crossunder connections.

In this last respect it is pointed out that FIG. 5 shows literally the layout and connection crossunders for a specific embodiment of the monolithic integrated circuit. In the absence of the required resistive connection, each connection crossunder required the addition of an extraneous resistance (not shown). Since in monolithic integrated circuit design each added resistance for crossunder purposes is an additional component supplying no other beneficial result, it is worth considerable effort to minimize connection crossunders. Referring again to transistor 102, it will be seen that the crossunder connecting the emitter of transistor 73 to the base of transistor 102 can be accomplished with the current limiting resistor 103. The crossunder beneath the lead connecting the collector of transistor 102 to the input circuitry required the use of an extraneous resistance (not shown).

Terminals 93 and 94 for connection to read/write timing signals are connected with terminal 93 to one emitter of each of transistors 148 and 48 and terminal 94 to one emitter of each of transistors 170 and 70. Thus terminal 93 is connected to the sinks and terminal 94 is connected to the switches. Terminals 95 and 101 are further address input connections. Terminal 95 is connected to an emitter of each of transistors 148 and 170 and terminal 101 is connected to one emitter of each of transistors 48 and 70.

The other terminals of the FIG. 5 monolithic chip are terminal 41 for connection to the voltage developed with current limiting resistor 36 and supply source 37 as will be remembered with reference to the previous figures and which is clamped by diode 40 so that it cannot exceed a fixed voltage, for example, 14 volts. Terminal 99 is connected to terminal 52 internal to the monolithic circuit and is for connection to said fixed voltage, i.e., 14 volts. Terminal 42 is for connection to a common ground. Terminals 96 and 100 are connected to the collector electrodes of transistors 127 and 27 for sink connections to the memory matrix, and terminals 97 and 98 are connected to the emitter electrodes of transistors 125 and 25 for switch connections to the memory matrix. It will be seen that in some cases terminals 96, 97, 98 and 100 will be connected into the memory matrix through line isolating matrices such as integrated monolithic diode matrix 28 of FIG. 2. In other instances, as depicted by the partial showing of a monolithic selection and drive chip 35 in FIG. 2, the connection to the memory matrix will utilize only discrete element diodes, such as diode 32, connected to terminals 97 and 98, while the connections to terminals 96 and 100 could be direct connections.

The monolithic selection circuit of FIG. 5 connected to a current-limited and voltage-clamped supply source, as depicted at terminal 41 in FIG. 2, has the advantage of near fail-proof operation. The use of this single supply for both read and write currents prevents damage possible with prior schemes having separate read and write suppliers. Further, it is short-circuit proof in that any output can be shorted to ground without damage. The use of a common ground for input logic and for sink emitters enables the use of a standard 14-pin integrated circuit flat pack. (It will be noted that the terminals depicted in FIG. 5 total 14.) The circuit is also heavily protected against over-voltage transients by both internal and external diodes as previously described.

A comparison of the operational and other characteristics of the present integrated selection and drive circuit with the presently commercially produced circuit having the nearest operational characteristics and functions but using discrete element driver transistors operated from transformers is given in the following Table I:

	Prior Art	Monolithic Selection and Drive
Worst case X set-up time	20 nsec	30 nsec (switch)
Worst case turn-on delay		20 nsec (sink)
Worst case turn-off delay	90 nsec	50 nsec (sink)
Intercycle recovery time	100 nsec (transformer)	20 nsec (switch parasitic capacity)
Address input loading (per 8K bit, assuming load sharing)	6 ma	6 ma
Power dissipation	1300 mw	500 mw
Worst case saturation voltage	1.1 v	0.6 v
Worst case noise immunity (local ambient 60° C)	1.1 v	1.0 v
Maximum voltage	30 v	17 v
Maximum current	400 ma	400 ma
Packaging volume (actual)	4.125 in.^{3}	0.0625 in.^{3} (Two flat packs)

The integrated selection circuit of FIG. 5 provides internal stack capacity discharge paths as has been described. An idle stack is referenced to the fixed voltage of terminal 99, i.e., to 14 volts.

One problem in memory matrices which limits speed and increases power requirements is capacitive storage effects. The present invention minimizes this problem by minimizing interconnecting lead lengths, as has been previously described, and by the use of appropriate recovery circuits and operational sequence control for providing optimum potential recovery.

In a system such as will be further described in connection with FIG. 7, the Y lines are partially recovered through resistors such as resistor 66 of FIG. 3 associated with the sink transistors. This can be seen in FIG.

2 in which connected to the collector of each sink transistor 27 and 31 is a resistor referenced to a positive voltage. Referring back to FIG. 2 it will be seen that one of these resistors is connected at each end of each Y axis line, for example, line 21 is connected at one end through one of diodes 26 to the resistor in the collector circuit of transistor 27 and at the other end directly to the resistor in the collector circuit of transistor 31.

Referring again to FIG. 3 it will be seen that the referencing of these resistors is under the control of the voltage at terminal 41. When the transistors are switched to terminate the current applied to a Y line, e.g., line 21 in FIG. 2, and before current is applied to another Y line, the voltage at terminal 41 rises to the clamping voltage of diode 40. This clamped voltage is sufficiently positive to bias transistor 62 to conduction, thereby providing a recovery path to the positive potential at terminal 52 for the Y line 21. As a result, when current in a Y line is switched off, resistor 66 and transistor 62 (FIG. 3) operate automatically to raise the line from the near-ground potential applied to it during the application of current to a positive potential corresponding to the potential at terminal 52.

Thereafter, as soon as current is applied to a Y line, a voltage drop at terminal 41 disconnects the recovery path through transistor 62 to reduce power dissipation. As described below, a different recovery system is required for the X lines in the arrangement of FIG. 7 due to the additional diode matrices at both ends of each line.

FIG. 7 illustrates a typical memory matrix in accordance with the present invention. The matrix shown is described as an 8000 word memory with four bits per word. The number of bits per word can be increased by stacking as illustrated in FIG. 8.

Each block labeled "S/D", such as block 200, represents a single monolithic selection circuit as illustrated in FIG. 5. Each block labeled "I" such as block 201 represents a monolithic flat pack containing two eight-diode line isolating matrices as illustrated by block 28 in FIG. 2.

The X axis lines in the matrix go horizontally across the FIGURE and return as represented by single line 202. By doubling back in this manner it will be seen that each X axis line, as depicted by line 202, crosses each Y axis line twice. One of the Y axis lines is indicated by line 203 and since there are storage elements at all intersections, there are two elements represented as 205 and 206 at intersections of lines 202 and 203. Drive block 200 has four output connections connected in parallel to each of isolating blocks 201, 207, 208 and 210. These output connections are shown in FIG. 5 as output terminals 96, 97, 98 and 100. The interconnections are in the manner shown in FIG. 2 between blocks 30 and 28. Since eight isolating lines are available at the output of each isolating block there are a total of 32 X lines derived from the single drive block 200. It should be noted that the input lines to each isolating block from drive block 200 are parallel but the output lines, eight from each isolating block, go directly into the matrix without connection to other isolating blocks. Each X line, after traversing all of the Y lines twice, returns to another drive block 211. A single 16-diode isolating block 212 buffers the connection of the 32 return lines to drive block 211.

Isolating block 212 is not needed to prevent read/write interaction but rather is used to segment part of the matrix capacitance from each X line to reduce transient power dissipation. As shown in block 28 in FIG. 2, there are eight two-diode-per-line line isolators in each of the isolating blocks. Thus, as indicated at the top of FIG. 7 for one of the eight lines input to block 212, with 32 lines coming into isolating block 212, four lines are connected in common to each of the two-diode-per-line line isolators. This arrangement effectively disconnects three-quarters of the matrix capacitance from each X line during operation of any one line. The seven additional sets of 32 doubled lines shown in FIG. 7 are each identical to the one described.

No description of the Y axis lines is necessary since they are described in detail in connection with FIG. 2, which illustrates the Y axis lines for a one-bit matrix. It will be seen that the FIG. 2 configuration with 16 lines is repeated four times in FIG. 7 giving a total of 64 Y axis lines. The number of Y axis lines multiplied by each traversal of an X axis line across the matrix determines the number of intersections at which magnetic storage elements are located. Accordingly, the matrix illustrated in FIG. 7 has a total of 32,768 storage elements.

With further reference to FIG. 7, a sense line for each data bit has a winding on each storage element in the data bit and is connected to output terminals for supplying sense information to a data register. At least one sensing wire is required for each data bit. Thus with four data bits to each word, there will be four sense wires and eight sense wire output terminals. In an actual matrix as depicted by FIG. 7, two sense wires were used for each data bit giving a total of 16 sense output terminals.

These 32,768 cores are readily mounted on a single printed circuit card measuring about 5 × 11 inches and leaving enough additional space for mounting flat packs containing monolithic chips depicted by the "S/D" and "I" blocks in FIG. 7. However, the number of bits can be increased considerably without addition to the X drive circuitry by using additional magnetic matrix cards in stacked formation in which the different cards may be referred to as planes.

An illustrative embodiment of such an arrangement is depicted in FIG. 8, where the X axis drive and isolating circuits are arranged on a single stack card 220. This separate card for X axis drive can be utilized in stacks having various numbers of planes. The integrated X circuitry on the card 220 is represented by an arbitrary arrangement of spots 212 on the surface of the card with the X axis drive arrangement depicted in FIG. 8. These spots 212 represent the 56 monolithic chips mounted as flat packs on the card. X axis line 222 is connected to the X axis drive and isolating circuits in the same manner as the line 202 in FIG. 7. Thus it is connected at a first end 223 to an X axis drive connection on card 220 and then traverses through the Y axis lines on seven planes of matrix cards 225, 226, 227, 228, 229, 230 and 231. At card 231 line 222 reverses after traversing the card, recrosses the Y axis lines across all seven planes and returns to connect at its other end 232 to X axis drive circuitry on card 220.

The integrated Y axis circuitry is illustrated in FIG. 8 as mounted on the margins of the matrix cards of the respective planes and is represented by spots 233 and 235.

Referring back to the current supply source arrangement depicted in FIG. 2 using resistor 36 and diode 40,

it has been a previous practice to use separate current limiting resistors for each polarity at current, i.e., to use one or more separate resistors for write current and likewise for read current. It was found that this prior arrangement allowed unnecessarily high supply voltage inside the drive circuits. To prevent this, diode clamp 40 was added. This arrangement for each drive circuit resulted in considerable power loss through the clamps. It was then found possible to eliminate not only the greater part of this power loss, but also to reduce the number of required components by a significant factor. This is because memory matrices are commonly made up of groupings of drive circuits and associated matrix lines arranged such that within each group only one line can be operated at a time. An example of this is seen in the Y axis system of FIG. 7, where the Y axis contains four groups of 16 lines each. Each group is depicted in greater detail in FIG. 2 where it is shown that the lines are interconnected in a way that makes mutual exclusion a requirement, i.e., that allows current to be applied to only one line 24 at a time.

Consequently, in accordance with one aspect of the invention, a single resistor 36 and a single diode 40 are used for the current source operating all the drive circuits in one such mutually exclusive group. Since sometimes it is desirable to switch one end of a line slightly before or after the other end, the same current supply source is used only for the drive circuitry at one end of the lines in the group. In any case, each resistor-diode source combination operates with a plurality of lines, e.g., with 16 lines. In normal computer-type memory operation, one or another of the lines in a mutually exclusive group is driven over a substantial percentage of operating time. In addition, as long as one such line is driven from a given current source, the voltage at the respective terminal 41 will be below the clamp level and essentially no power will be lost in the clamp current. Thus, with a plurality of mutually exclusive load circuits connected to each clamped source as in FIG. 2, the clamps can be operated efficiently with low power loss.

FIG. 9 shows a modified embodiment of the selection circuit of FIG. 5. Circuit elements in FIG. 9 having identical counterparts in FIG. 5 are designated with the same reference numerals used in FIG. 5, whereas circuit elements in FIG. 9 not found in FIG. 5 are designated with reference numerals in the 300 count. The component layout of FIG. 9, which can be applied directly to the layout of the integrated circuit structure, differs slightly from FIG. 5 with the result that integrated circuit cross-overs are reduced.

The FIG. 9 circuit is sufficiently similar to FIG. 5 that a description of only the differences is in order. A first difference concerns the transistors 83 and 183 connected with the switch transistors 25 and 125, respectively. In FIG. 5, transistor 83 is connected with its collector and base tied together to operate as a diode. However, in FIG. 9 the transistor 83 collector is connected, separate from the base, to the base of transistor 80. Similarly, the transistor 183 collector is connected to the base of transistor 180.

The new connection of transistor 83 in FIG. 9 provides enhanced turnoff of transistor 25 by improved removal of stored charge from transistor 25 and from transistor 80 driving it. During the steady state condition where transistor 25 is conducting collector-emitter current, the transistor 83 emitter-base junction is reverse biased because the transistor 25 base is at a smaller positive voltage than the transistor 70 collector 76. Hence the transistor 83 has a relatively large impedance to its emitter from both its collector and its base.

However, when the emitter of transistor 70 is switched from a positive voltage to near ground in order to turn transistor 25 off, the transistor 70 collector also drops to near ground potential. The transistor 83 emitter-base junction is then forward biased. Hence the transistor conducts and removes, by way of its base, stored charge from transistor 25. The base-emitter diode of transistor 83 subsequently maintains an off potential at the base of transistor 25.

The turn-off operation also requires the removal of stored charge from transistor 80 driving transistor 25. The transistor 83 in FIG. 9, when conductive, provides a low impedance discharge path for this purpose from its collector, connected to the transistor 80 base, to its emitter. Thus the modified FIG. 9 circuit discharges the transistor 80 at its base, rather than at its emitter as with the FIG. 5 configuration.

The discharging operation of transistor 83 in FIG. 9 is "self-regulating". That is, when the transistor 83 collector-emitter impedance is sufficiently large so that some stored charge in transistor 80 is conducted to the transistor 80 emitter and discharged through transistor 83 by way of the transistor 83 base, the resultant additional base-emitter discharge current turns the transistor 83 on further. This reduces the transistor's collector-emitter impedance thereby hastening the transistor 80 discharge directly from its base through the collector of transistor 83.

With further reference to FIG. 9, a second difference from the FIG. 5 circuit is that the base resistor 103 connected with the input multiemitter transistor 102 (lower left side of FIG. 9) is returned to a larger positive voltage than in FIG. 5. This is done by the addition of an impedance buffer transistor 302 having its emitter connected to the resistor 103, its base connected to a further tap 304 on the resistor 74-resistor 75 voltage divider, and having its collector connected to the terminal 52 to which the supply applies positive direct voltage (see FIG. 4). This arrangement enhances the turn-on speed of the circuit by charging the stray capacitance that exists from the transistor 102 collector to ground to a more positive voltage than with the FIG. 5 arrangement. The transistor 302 serves essentially the same function for resistor 103 as the transistor 73 does for the resistor 72 connected with transistor 70, that is, it minimizes the effect on the voltage at the tap 304 due to variations in the current drawn by resistor 103.

A final difference between the FIG. 9 circuit and that of FIG. 5 is the addition of a transistor 306 and a diode 308 to develop the overdrive current applied to the sink transistor 27 during the turn-on transient. In particular, the resistor 60 and diode 61 shown in FIGS. 3 and 5 are omitted from the FIG. 9 circuit. The new transistor 306 senses the transistor 27 collector voltage at its base. When this voltage is sufficiently positive, which occurs with initiation of turn-on operation, transistor 306 applies overdrive current, from the supply terminal 52, by way of the transistor 306 collector-emitter path and through the diode 308 to the collectors of both transistors 56 and 55. The diode 308 serves the same reverse-voltage protection function as the diode 61 of FIG. 5. And the use of the transistor 56 as

a transistor in FIG. 9 rather than as a diode in FIG. 5 provides additional gain. More important, however, the elimination of resistor 60 from FIG. 3 and FIG. 5 decreases power dissipation.

With this new arrangement, the feedback circuit providing the turn-on overdrive current is responsive to the transistor 27 collector voltage. In the arrangement of FIGS. 3 and 5 on the other hand, the voltage at the source terminal 41 controls this overdrive current.

In sum, the invention described above provides memory selection circuits capable of extensive fabrication with monolithic integrated circuit structure. The invention thereby provides important savings in size and weight over prior circuits. The integrated circuit capability of the inventive circuit also enables it to be constructed at comparatively low cost, particularly on a large scale.

It should be noted that the circuits of the invention are not necessarily limited to operation with memories. Their logical decoding and driving functions can be applied to other electrical devices. Also the "magnetic storage medium" as used herein comprehends magnetic cores, magnetic film, plated wires, plated rods and other magnetic media suited for data storage. Generally the magnetic media should be operative as small selectable elements having a magnetic characteristic exhibiting a hysteresis loop for switching purposes.

The circuits provided by the invention also have advantageous performance, particularly in terms of power dissipation, operating speed, ability to drive reactive loads and to withstand the resultant dynamic changes in output voltage and current. These advantages are realized substantially independent from the type of construction, e.g., discrete components or integrated components, employed.

While the invention has been described in relation to specific embodiments, various modifications thereof will be apparent to those skilled in the art and it is intended to cover the invention broadly within the spirit and scope of the appended claims.

Having described the invention, what is claimed as new and secured by Letters Patent is:

1. A monolithic integrated circuit formed in a single block of semiconductor material, said circuit comprising:
   1. conductive means formed in said single block of semiconductor material and including at least two input terminals, an output terminal, and a supply terminal,
   2. an output transistor formed in said single block of semiconductor material and having its emitter-collector path serially connected betwen said output terminal and said supply terminal,
   3. semiconductor impedance transforming means formed in said single block of semiconductor material and having an input lead and an output lead, said output lead connected with the base of said output transistor,
   4. semiconductor coincidence means formed in said single block of semiconductor material and having input leads coupled to said input terminals and an output lead coupled to said input lead of said transforming means, said semiconductor coincidence means in response to signals applied to said input terminals enabling said transforming means and controlling the emitter-controller conduction of said output transistor,
   5. semiconductor feedback means formed in said single block of semiconductor material and receiving a feedback signal corresponding to the signal at at least one terminal selected from said output terminal and said supply terminal, said semiconductor feedback means responsive to said feedback signal for applying a selective overdrive signal to said transforming means for accelerating the switching operation of said output transistor, and
   6. impedance means including a resistor and diode having its anode connection distributed along said resistor, said impedance means coupled to said semiconductor feedback means and said output transistor for damping inductive kick during switching of said output transistor.

2. A circuit as defined in claim 1 wherein said semiconductor impedance means includes a first transistor having its base as an input lead and a second transistor having its emitter as an output lead, said first transistor when conductive enabling said second transistor, said second transistor when conductive providing an enabling input to said base of said output transistor.

3. A circuit as defined in claim 2 wherein said semiconductor coincidence means includes a third transistor having multiple emitters and a collector, said multiple emitters coupled to said input terminal, said collector coupled to said base of said first transistor, said third transistor in response to signals applied to said input terminals enabling said first transistor to conduction.

4. A circuit as defined in claim 3 wherein said semiconductor feedback means includes a fourth transistor having a base and an emitter, said base coupled to said supply terminal, said emitter coupled to said impedance means and to the collector of said first transistor, said fourth transistor when conductive applying a selective overdrive signal to said collector of said first transistor for accelerating the switching operation of said output transistor.

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