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(54) Title: A PROGRAMMABLE TWO-PHASE NON-OVERLAPPING CLOCK SIGNAL SELF-GENERATOR

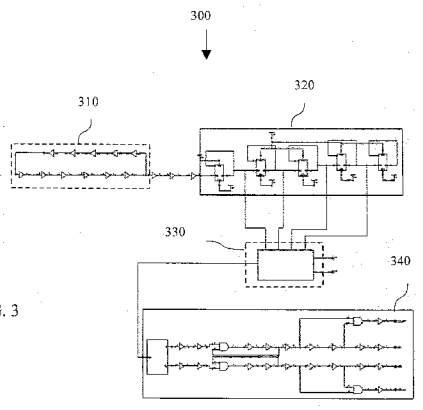

FIG. 3

(57) Abstract: The present invention relates to a clock generator circuit (300) that is programmable and capable of self-generating two-phase non-overlapping clock signals for switch capacitor circuit applications. This clock generator circuit (300) has a wide frequency range and allows for selection of several frequency rates by controlling the digital inputs of a multiplexer (330). Besides the multiplexer (330), the proposed circuit includes a ring oscillator (310), frequency dividers (320) and a two-phase non- overlapping clock circuit (340). The internal ring oscillator (310) generates an oscillation signal and sends the signal to the frequency dividers (320). These frequency dividers (320) generate series of clock signals at different frequencies. Through the multiplexer (330), one of the clock signals is selected and transferred to the non- overlapping clock circuit (340). The non-overlapping clock signal generator (340) includes toggle flip-flop, NAND gates, delay and buffer cells.

WO 2011/025360 A1

A PROGRAMMABLE TWO-PHASE NON-OVERLAPPING CLOCK SIGNAL SELF-GENERATOR

FIELD OF INVENTION

The present invention relates, to a programmable two-phase non-overlapping clock signal generator. More particularly a programmable two-phase non-overlapping clock signal generator for switch capacitor circuit applications.

BACKGROUND OF THE INVENTION

Switched capacitor circuits have broad applications in integrated circuits (ICs). They play a very important role in analog signal processing block such as sensor interface, summing amplifier, switched-capacitor integrator, voltage comparator and so forth. A switched capacitor circuit requires non-overlapping clock signals for transferring the charge into and out of the capacitors. This is to reduce the voltage errors during on and off switching during operation of switched capacitor circuits. For wide range switched-capacitor circuit applications, programmable frequency is useful.

The non-overlapping clock signals are derived from a master clock signal and they typically have inverting and non-inverting clock signals, wherein the first and the second phases are within one period clock cycle. A small delay between transition of these inverting and non-inverting clock signals ensures they are non-overlapping signals. Such described waveforms are the so called two-phase non-overlapping clock signals.

A commonly used method for generating non-overlapping clock signals consists of an array of cross-coupled logic gates. In that approach, the master clock signal is split into two paths. Each path contains a chain of NAND or NOR logic gates and inverters. The

outputs of each chain are cross-coupled back to the input, as shown in FIG. 1. The non-overlapping clock signals arise due to the propagation time delay in the logic gates. FIG. 2 shows a timing diagram of the output two-phase non-overlapping clock signals of FIG. 1.

In U. S Pat. No. 6,653,881 B2, dated Nov. 25, 2003 inventors Ho Dai Truong and Chong Ming Lin disclosed a system and method for generating and optimizing clock signals with non-overlapping edges on a chip using a unique programmable on-chip clock generator. Overlapping of the edges of the clocking signals is avoided by adjusting an amount of delay introduced in the on-chip clock generator circuit. The proposed programmable non -overlapping clock signal generator disclosed receives the primary clock signal from an external source. The circuit is programmable for controlling the delay of the clock edge. The non-overlapping clock signals are produced through NOR gates and inverter.

In U. S Pat. No. 5,955,906, dated Sep. 21, 1999, inventor Hiroshi Yamaguchi, discloses a non-overlapping two-phase signal generator that includes an oscillator to produce an oscillation signal of period 2t. This simple circuit non-overlapping clock signal generator consists of NAND (or NOR) gate and a time delay circuit. The programmable non- overlapping clock signal generator implements the Miller current-starved inverter ring oscillator. The generator is programmable on capacitor values for reducing frequency at ring oscillator and produces the non-overlapping clock signals through JK flip-flop

In U. S Pat. No. 5,867,453, dated Feb. 2, 1999, inventors Shyh Jye Wang, Chi Chiang Wu and Hsing Chien Huang, disclose a non-overlapping clock signal generator with a programmable delay circuit. This is to ensure and control a non-overlapping space between the first clock signal and the second clock signal.

Furthermore, in U.S Pat. No. 5,818,276, dated Oct. 6, 1998 inventors Douglas A. Garrity, Patrick L. Rakers and Andrea Eberhardt disclose a non-overlapping clock signal that comprises of six NOR gates and an inverter. This configuration circuit

claims to increase the time for circuit operation by minimizing delays between non-overlapping clock signals and simultaneously transiting rising edges of clock signal.

The published paper, 'A low-cost programmable clock generator for switched-capacitor circuit applications', authored by W. F Lee and P.K. Chan, published in year 2006, presents improved-circuit techniques that allow the design of low-cost programmable clock generator using a ring oscillator for low-frequency switched-capacitor applications. The paper proposed a Miller current-starved inverter ring oscillator with programmable capacitor values to reduce frequency of the oscillator.

SUMMARY OF THE INVENTION

In an embodiment, the present invention is a programmable self-generating two-phase non-overlapping clock signal generator, particularly for switched capacitor circuit applications. This clock generator has a wide frequency range and allows for selection of several frequency rates by controlling the digital inputs of a multiplexer. Besides multiplexer, the proposed circuit includes a ring oscillator, a set of frequency dividers and a two-phase non-overlapping clock circuit. The internal ring oscillator generates an oscillation signal and sends the signal to the frequency dividers. These frequency dividers generate a series of clock signals at different frequencies. Through the multiplexer, one of the clock signals is selected and transferred to the non-overlapping clock signal generator. This non-overlapping clock signal generator produces two-phase non-overlapping clock signals.

In an embodiment, the clock signal generator produces four clock signals Φ_1, Φ_{1p}, Φ_2, and Φ_{2p}; wherein Φ_1 and Φ_2 have an 180° difference phase shift and a delay between clock transitions, while, Φ_{1p} and Φ_{2p} turn off before Φ_1 and Φ_2 respectively. Other types of two-phase non-overlapping signals may be generated.

In an embodiment, the non-overlapping clock circuit includes toggle flip-flop, NAND

gates, delay cells and buffer cells. Other types of components may also be used.

The programmable non-overlapping clock signal generator is a self generator and implements a typical ring oscillator composed of inverters. The generator is programmable for selection of the operating frequency at the frequency divider providing a wide frequency range and allowing for selection of several frequency rates. Such a programmable generator is useful particularly for wide range switched-capacitor circuit applications.

The present invention consists of certain novel features and a combination of parts hereinafter fully described and illustrated in the accompanying drawings and particularly pointed out in the appended claims; it being understood that various changes in the details may be possible without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following drawings, same reference numbers generally refer to the same parts throughout. The drawings are not necessarily to scale, instead emphasis is placed upon illustrating the principles of the invention. The various embodiments and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims and accompanying drawings wherein:

FIG. 1 illustrates a schematic diagram of a prior art non-overlapping clock signal generator.

FIG. 2 illustrates a timing diagram of output signals of the circuit at FIG.1.

FIG. 3 illustrates a schematic diagram of a programmable two-phase non-overlapping clock signal self-generator, according to an embodiment of the invention.

FIG. 4 is a flow chart illustrating the operation of the circuit at FIG. 3.

FIG. 5 is a timing diagram of the output signals of circuit FIG. 3.

DETAILED DESCRIPTION OF THE INVENTION

The following description presents several preferred embodiments of the present invention in sufficient detail such that those skilled in the art can make and use the invention.

Before describing in detail embodiments that are in accordance with the present invention, it should be noted that all of the figures are drawn for ease of explanation of the basic teachings of the present invention only. The extension of the figures with respect to the number, position, relationship and dimension of the parts of the preferred embodiment will be within the skill of the art after the following teachings of the present invention have been read and understood. Further, the exact dimensions and dimensional proportions to conform to specific force, weight, strength and similar requirements will likewise be within the skill of the art after the following teachings of the present invention have been read and understood.

FIG. 3 illustrates a schematic diagram for the proposed programmable two-phase non-overlapping clock signal self generator (300). This circuit includes an inverter ring oscillator (310), frequency dividers (320), a multiplexer (330) and a non-overlapping clock signal generator circuit (340).

The functionality of this invention is summarized in the flowchart shown in FIG. 4. As described in the first block (410), the ring oscillator (310) consists of multiple complementary metal-oxide-semiconductor (CMOS) based inverter cells and they must be in odd numbers in order to produce oscillation signal. The frequency of this oscillation signal depends on the size of transistor in inverter cells. To have several set of frequency signals in the next stage, this ring oscillator (410) is designed at optimum frequency.

As described in the second block (420), several sets of frequency dividers (320) are used in this invention to generate multiple reference frequencies. The configuration for this frequency divider (320) is a series of standard D flip-flop divide-by-2, with the data input driven by the negated of the flip flop. N number of D flip-flop gives 2^N division.

As described in the third block (430), an N-to-1 multiplexer (330) is used to select the required frequency signal, such that the generator is programmable.

As described in the fourth block (440) the output from the multiplexer (330) is passed to an input terminal of a non-overlapping clock signal generator (340).

As described in the fifth block (450), this generator (340) includes toggle (T) flip-flop, two NAND gates, and plurality of delay cells and buffer cells. T flip-flop generates two non-overlapping clock signals and then these signals are split to give two-phase non overlapping clock signals, Φ_1, and Φ_2, through delay cells in cross-coupled manner. The clock signals of Φ_{1p} and Φ_{2p} are generated through NAND gate with inputs of before and after delay cells. The produced clock signals are shown in FIG. 4. The generator circuit (340) may be designed to provide other types of signals from the selected input from the multiplexer (330).

As to further discussion of the manner of usage and operation of the present invention, the same should be apparent from the above description. Accordingly, no further discussion relating to the manner of usage and operation will be provided.

While the foregoing description presents preferred embodiments of the present invention along with many details set forth for purpose of illustration, it will be understood by those skilled in the art that many variations or modifications in details of design, construction and operation may be made without departing from the present invention as defined in the claims. The scope of the invention is as indicated by the appended claims and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

CLAIMS

1. A programmable two-phase non-overlapping clock signal self-generator circuit (300), comprising :

a ring oscillator (310) for producing an oscillation signal at a predetermined frequency;

a set of frequency dividers (320) for receiving the oscillation signal and converting to a plurality of clock signals at predefined frequencies;

a multiplexer (330) for receiving the plurality of clock signals and selecting a required clock signal from within the plurality of clock signals; and

a clock signal generator (340) for receiving the required clock signal to generate two-phase non-overlapping clock signals.

2. A programmable two-phase non-overlapping clock signal self-generator circuit according to claim 1, wherein the clock signal generator (340) includes toggle flip-flop, NAND gates, delay cells and buffer cells.

3. A programmable two-phase non-overlapping clock signal self-generator circuit according to claim 1, wherein the non-overlapping clock signals are for switched-capacitor circuit applications.

4. A programmable two-phase non-overlapping clock signal self-generator circuit according to claim 2, wherein the two-phase non-overlapping clock signals are four clock signals, namely Φ_1, Φ_{1p}, Φ_2, and $\Phi_{2p,}$ such that the Φ_1 and the Φ_2 have an 180° difference phase shift and a delay between clock transitions, while, the Φ_{1p} and the Φ_{2p} turn off before the Φ_1 and the Φ_2 respectively.

5. A method for self-generating programmable two-phase non-overlapping clock signals, comprising the steps of:

producing an oscillation signal at a predetermined frequency, by a ring oscillator

(310);

feeding the oscillation signal to a set of frequency dividers (320) for producing a plurality of clock signals at predefined frequencies;

feeding the plurality of clock signals to a multiplexer (330) for selecting a required clock signal from within the plurality of clock signals;

feeding the required clock signal to a non-overlapping clock signal generator (340); and

converting the required clock signal into two-phase non-overlapping clock signals, in the signal generator (340).

6. A method according to claim 5, wherein the non-overlapping clock signal generator (340) includes toggle flip-flop, NAND gates, delay cells and buffer cells.

7. A method according to claim 5, wherein the two-phase non-overlapping clock signals are for switched-capacitor circuit applications.

8. A method according to claim 6, wherein the two-phase non-overlapping clock signals are four clock signals, namely Φ_1, Φ_{1p}, Φ_2, and $\Phi_{2p,}$ such that the Φ_1 and the Φ_2 have an 180^o difference phase shift and a delay between clock transitions, while, the Φ_{1p} and the Φ_{2p} turn off before the Φ_1 and the Φ_2 respectively.

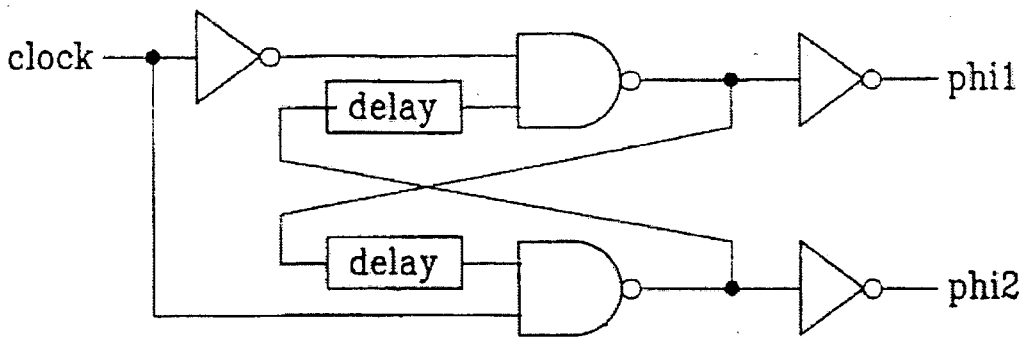

FIG. 1

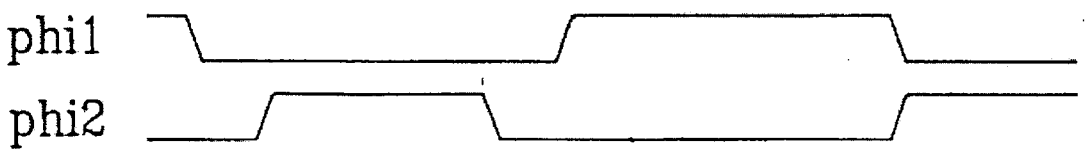

FIG. 2

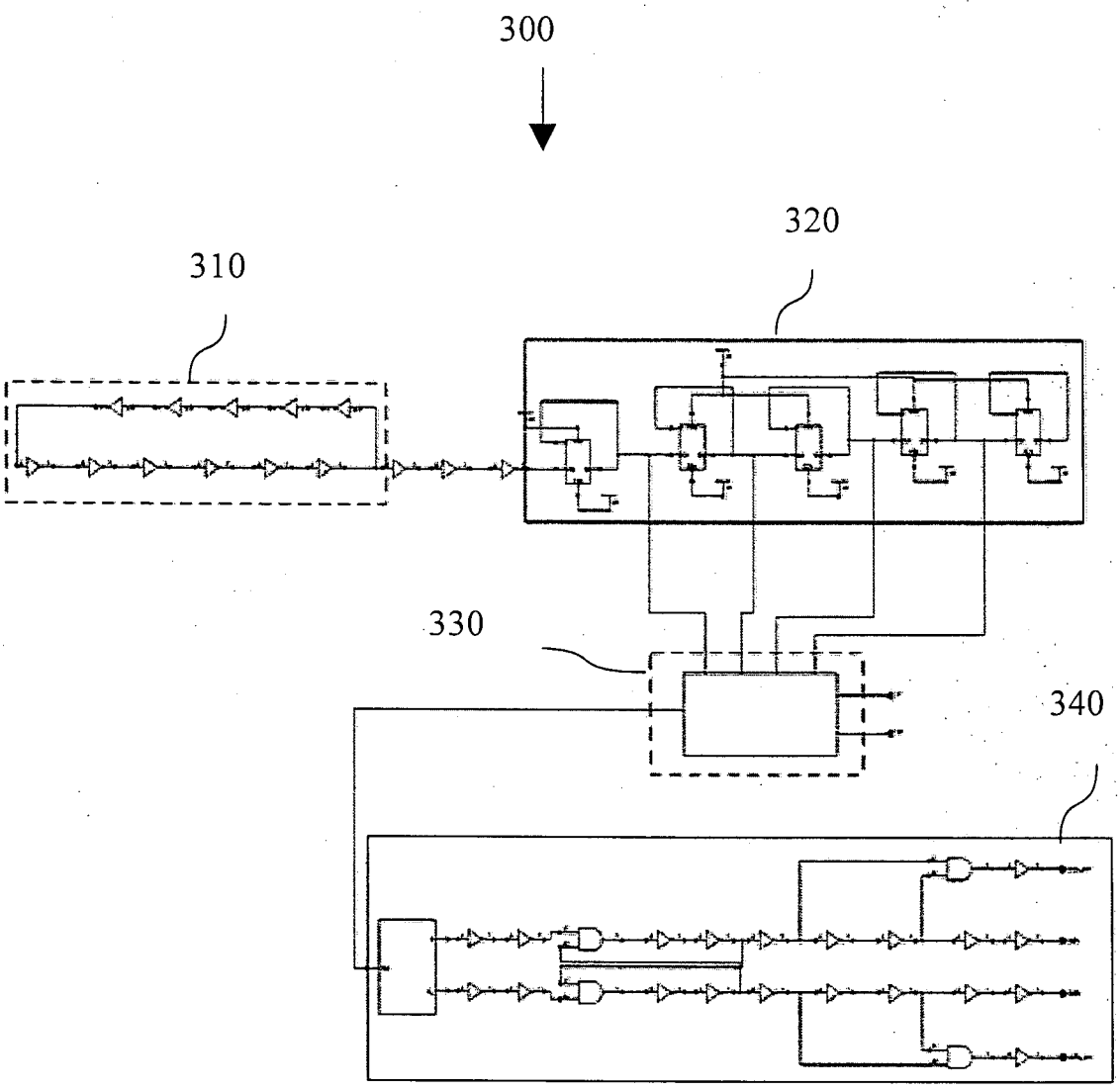

FIG. 3

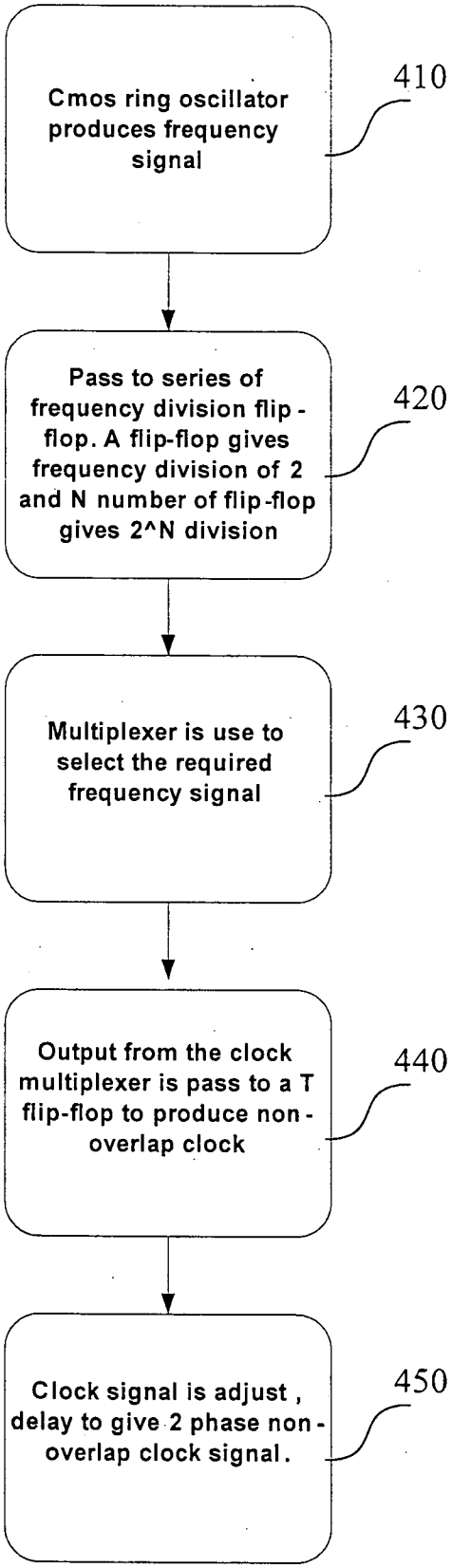
Cmos ring oscillator produces frequency signal
410
Pass to series of frequency division flip-flop. A flip-flop gives frequency division of 2 and N number of flip-flop gives 2^N division
420
Multiplexer is use to select the required frequency signal
430
Output from the clock multiplexer is pass to a T flip-flop to produce non-overlap clock
440
Clock signal is adjust, delay to give 2 phase non-overlap clock signal.
450

FIG. 4

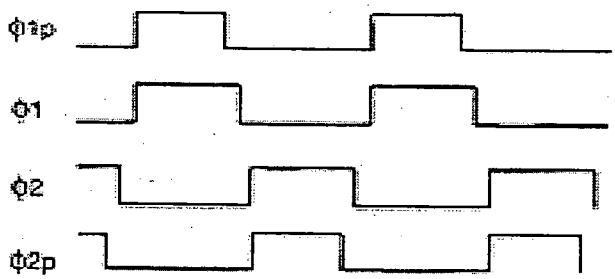

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2010/000151

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H03K 5/15 (2006.01) ***G06F 1/06*** (2006.01) ***G06F 7/487*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPODOC & WPI (abstracts), GOOGLE keywords:TWO PHASE, NON OVERLAPPING, RING OSCILLATOR, MULTIPLEXER, FREQUENCY DIVIDER, SWITCH CAPACITOR, PHASE SHIFT and other terms and phrases

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6950490 B1 (KOH ET AL) 27 September 2005 Abstract, column 1 line 20 – column 2 line 27, column 3 lines 20-55, column 5 lines 4-15, column 5 lines 50-67, Figs. 1, 2A, 2B, 4.	1-8
X	US 5955906 A (YAMAGUCHI) 21 September 1999 Abstract, column 1 lines 11-67, column 3 lines 30-67, Figs. 4A, 4B, 5A, 5B.	1-8

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 November 2010	11 NOV 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **BAYER MITROVIC** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 2164

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/MY2010/000151

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	6950490	NONE	
US	5955906	JP	10070442

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX