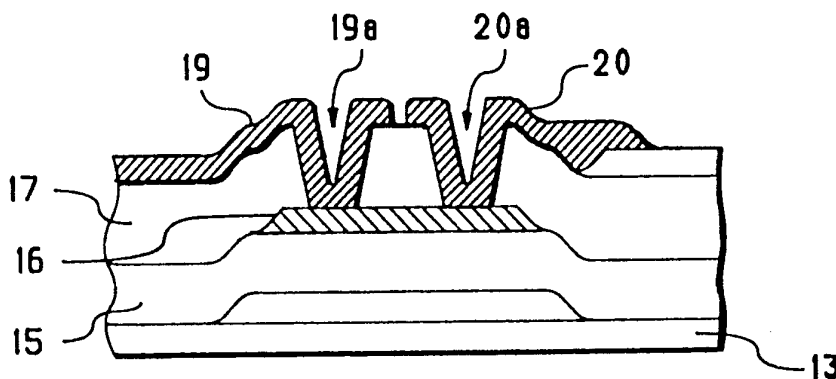


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(21) International Application Number: PCT/CA92/00520 (22) International Filing Date: 1 December 1992 (01.12.92) (71) Applicant (for all designated States except US): LITTON SYSTEMS CANADA LIMITED [CA/CA]; 25 City View Drive, Etobicoke, Ontario M9W 5A7 (CA). (72) Inventor; and (75) Inventor/Applicant (for US only): FARRELL, James, F. [CA/CA]; 159 Beaverbend Crescent, Etobicoke, Ontario M9W 5A7 (CA). (74) Agent: PERRY, Stephen, J.; Sim & McBurney, 330 University, Suite 701, Toronto, Ontario M5G 1R7 (CA).		(81) Designated States: CA, JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>
(54) Title: IMPROVED STRUCTURE FOR CdSe TFT (57) Abstract <p>A thin film transistor, comprising: a glass substrate; a gate electrode deposited on the substrate; a gate insulator layer deposited on the substrate so as to overlie the gate electrode; a thin film semiconductor channel layer deposited on the gate insulator layer and substantially aligned with the gate electrode; a passivation layer deposited on the gate insulator layer so as to overlie the thin film semiconductor channel layer; a pair of via holes etched through the passivation layer to the semiconductor channel layer; and a pair of source and drain electrodes deposited on the passivation layer and extending through the via holes for contacting the semiconductor channel layer.</p>		



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IMPROVED STRUCTURE FOR CdSe TFTField of the Invention

This invention relates in general to thin film transistors (TFTs), and more particularly to an improved structure for CdSe thin film transistors for use in an active matrix liquid crystal display.

Background of the Invention

Thin film transistor-based active matrix liquid crystal displays are now in production at a number of large electronics companies. These displays, used for personal television and lap-top computer screens, use amorphous silicon as the semiconductor.

Each dot in an active matrix liquid crystal display (AMLCD) acts as an analog sample and hold circuit, for sampling the video data and holding it until the next data refresh cycle. The ability of an AMLCD to present good video pictures is directly related to the accuracy of the sample and hold circuits at each dot or pixel. The TFT must have sufficiently high on-conductance to fully charge the pixel capacitance during the line address time, while having sufficiently low off-conductance to hold the charge accurately for the refresh period of the display.

Amorphous silicon TFTs used in early displays were known for their low leakage current in the "off" state while exhibiting enough "on" current to fully charge the pixel capacitance and activate the liquid crystal. Amorphous silicon is rather a low mobility semiconductor however, so as the number of addressable lines in AMLCDs has increased, and the line address time has decreased, methods to increase the "on" current of the TFTs have been investigated.

The current output of amorphous silicon TFTs can be increased by simply increasing the gate voltage swings, increasing the channel width to length ratio, or by using a high dielectric constant gate insulator to decrease the channel capacitance.

One prior art TFT design is disclosed in U.K. Patent GB 2087147 (National Research Development Corporation). As will be discussed in greater detail below, this prior art design suffers from the disadvantage that the thin metal source and drain layers can be contaminated prior to deposition of the semiconductor channel layer. Furthermore, once the semiconductor channel layer is deposited and patterned, it must be crystallized since it is formed of polycrystalline material. During crystallizing, the semiconductor material is subjected to high temperatures so that the source and drain contact material tends to diffuse into the semiconductor channel material and shortens the channel length.

In addition, when used as an AMLCD, an additional lithography step is required to ensure adequate current carrying capability of the source contact.

Summary of the Invention

According to the present invention, an AMLCD design is provided in which the source and drain electrodes are deposited for connection to the semiconductor channel layer as the last step of the fabrication process. This avoids unwanted diffusion of the source and drain metallic contacts into the semiconductor material. Furthermore, according to the invention, the source and drain electrodes may be made of a desired thickness for increased current conduction, and no extra lithography step is required. In addition, the problem of organic contamination from residual lift-off photoresist, which arises in the prior art system disclosed in the UK Patent, does not occur.

Various aspects of the present invention are as follows:

A thin film transistor, comprising:

- a) a glass substrate;
- b) a gate electrode deposited on said substrate;
- c) a gate insulator layer deposited on said

substrate so as to overly said gate electrode;

d) a thin film semiconductor channel layer deposited on said gate insulator layer and substantially aligned with said gate electrode;

5 e) a passivation layer deposited on said gate insulator layer so as to overly said thin film semiconductor channel layer; and

f) a pair of source and drain electrodes deposited on said passivation layer and extending through a portion of said passivation layer for contacting said semiconductor channel layer.

A method of fabricating a thin film transistor, comprising the steps of:

15 a) providing a substrate;

b) depositing a gate electrode on said substrate;

c) depositing a gate insulator layer on said substrate so as to overly said gate electrode;

20 d) depositing a thin film semiconductor channel layer on said gate insulator layer so as to be substantially aligned with said gate electrode;

e) depositing a passivation layer on said gate insulator layer so as to overly said thin film semiconductor channel layer;

25 f) etching a pair of via holes through said passivation layer to said semiconductor channel layer; and

g) depositing a pair of source and drain electrodes on said passivation layer so as to extend through said via holes for contacting said semiconductor channel layer.

An active matrix liquid crystal display, comprising:

a) a first polarizing layer;

35 b) a first glass substrate deposited on said first polarizing layer;

c) a plurality of gate electrodes deposited on

said first glass substrate;

d) a gate insulator layer deposited on said first glass substrate so as to overly said gate electrodes;

5 e) a plurality of thin film semiconductor channel layers deposited on said gate insulator layer and substantially aligned with respective ones of said plurality of gate electrodes;

10 f) a passivation layer deposited on said gate insulator layer so as to overly respective ones of said plurality of thin film semiconductor channel layers;

g) a plurality of pairs of via holes etched through said passivation layer to respective ones of said semiconductor channel layers;

15 h) a plurality of pairs of source and drain electrodes deposited on said passivation layer and extending through respective ones of said pairs of via holes for contacting respective ones of said semiconductor channel layers;

20 i) a plurality of select lines for interconnecting said plurality of metallic gate electrodes;

25 j) a plurality of data lines arranged orthogonally to said select lines for interconnecting said plurality of metallic source electrodes;

k) a plurality of rectangular pixel output pads intermediate respective ones of said orthogonally arranged select lines and data lines and connected to respective ones of said drain electrodes;

30 l) a first alignment layer deposited on said substrate so as to overly said select lines, said data lines and said rectangular pixel output pads;

m) a layer of liquid crystal material overlying said first alignment layer;

35 n) a second polarizing layer;

o) a second glass substrate deposited on said second polarizing layer;

p) a light shielding/contrast enhancement layer deposited on said second glass substrate;

q) a plurality of colour filters spun on to said light shielding/contrast enhancement layer, said plurality of colour filters being thereafter patterned to align with respective ones of said rectangular pixel output pads and then cured;

r) a planarization layer deposited on said plurality of colour filters;

s) a conductive backplane electrode deposited on said planarization layer; and

t) a second alignment layer intermediate said backplane electrode and said layer of liquid crystal material.

Brief Description of the Drawings

A detailed description of the preferred embodiment and of the prior art is provided herein below, with reference to the following drawings, in which:

Figure 1 is a plan view showing a prior art TFT array for AMLCD;

Figure 2 is a sectional view showing the prior art in Figure 1 taken along the line II-II thereof;

Figure 3 is a simplified schematic diagram of the sample and hold structure of the TFT shown in Figures 1 and 2;

Figures 4a, 4b and 4c show successive steps in the fabrication process of a TFT according to the preferred embodiment of the present invention;

Figure 5 is a graph showing current-voltage characteristics of the TFT according to the preferred embodiment of the present invention; and

Figure 6 is a cross sectional view of an AMLCD incorporating the TFTs of the present invention.

Detailed Description of the Preferred Embodiment and Prior Art

Figures 1 and 2 show structures of an inverted TFT

(Figure 2) and a TFT array (Figure 1) obtained by arranging a plurality of such inverted TFTs on an insulating substrate. The plurality of TFTs 1 are arranged on a transparent insulating substrate 2, such as glass, in the form of a matrix. Gate electrodes 3 of each TFT 1 are commonly connected through gate line 4 so as to form select lines of the array. Source electrodes 5 of each TFT 1 are commonly connected to source lines 6 to form data lines of the array. Drain electrode 7 of each TFT 1 is connected to a transparent electrode 8 which is formed as a rectangular pixel output pad between the gate lines 4 and source lines 6 of the array.

Turning to the cross-sectional view of Figure 2, the profile of a TFT 1 is shown comprising a series of overlapping layers. The metallic gate electrode 3 is deposited on transparent glass substrate 2. A gate insulator layer 9 is then deposited on the glass substrate 2 so as to overlie the gate electrode 3. The gate insulating layer 9 may consist of silicon oxide or silicon nitride, or other suitable insulating material. Next, the source and drain electrodes 5 and 7 are deposited on the gate insulating layer 9, and a layer of semiconductor material 10 is then deposited so as to overlap the source and drain electrodes 5 and 7, forming a thin-film semiconductor channel therebetween.

The prior art pixel cell design shown in Figure 3 corresponds to the structure of Figure 1, and includes a storage capacitor 12 which is formed by the overlap of the output pad 8 with a previously scanned gate.

Finally, a passivation layer 11 is deposited over the entire structure.

In order to cause the semiconductor layer 10 to overlap the source and drain electrodes, the semiconductor layer must be thicker than the thickness of the metallic source and drain electrodes 5 and 7. In order to avoid the deposition of an excessively thick semiconductor layer which would be inappropriate for thin

film applications, the metallic contacts 5 and 7 are made thin. However, according to the prior art, for large displays, the data lines must be built up at source or data lines in order to provide sufficient current carrying capabilities. Therefore, according to the prior art TFT design of Figure 2, an additional lithography step is required to add thicker metal to region 6.

Other disadvantages of the illustrated prior art TFT are that the thin metal source and drain electrodes 5 and 7 can become contaminated in the time between the lithography step implemented to deposit these layers and the time that semiconductor layer 10 is deposited thereover. In order to remove the contaminated areas, ion beam etching or sputter etching is required to remove the contamination. Unfortunately, these additional etching procedures can cause damage to the interface between the semiconductor layer 10 and oxide layer 9.

Furthermore, when the semiconductor layer 10 is deposited and patterned, it must be crystallized since it is formed from polycrystalline material. During the crystallizing step, the semiconductor material is subjected to high temperatures which can cause diffusion of the metallic source and drain contacts into the semiconductor material, thereby shortening the active channel length of the TFT 1.

The TFT design of the present invention avoids the extra metal lithography step required during fabrication of the illustrated prior art TFT. The TFT design of the present invention also minimizes any contamination of the source and drain contacts, thereby alleviating the necessity to conduct ion beam etching or sputter etching for cleaning the contacts. Finally, the TFT design according to the present invention avoids unwanted diffusion of the metallic source and drain contact material into the semiconductor.

Turning now to Figures 4a, 4b and 4c illustrating the fabrication steps according to the present invention,

a layer of chromium (Cr) is deposited on a Corning 7059 glass substrate 13, and patterned to form gate electrode 14. A 5000 Å film of PECVD SiO_x, serving as the gate insulator 15, is then deposited, followed by a 500 Å layer of the evaporated CdSe semiconductor. After annealing, the semiconductor layer 16 is patterned and then passivated with a SiO_x layer 17. Following this, indium tin oxide (ITO) is deposited and patterned to form the pixel output pad 18.

10 The final two steps in the process of the present invention are to open up contact vias 19a and 20a in the passivation oxide, deposit the source/drain metal, and pattern the metal to form the source and drain electrodes 19 and 20. The contact vias are formed by a dry etch process using reactive gases. Since conductivity properties of the semiconductor are disturbed when the semiconductor is uncovered as a result of the reactive ion etch, a sputter etch is performed, according to the present invention, to etch away contaminated areas. A final anneal is then performed to ensure good ohmic contact between the semiconductor 16 and the source and drain electrodes 19 and 20.

 Since the source and drain electrodes 19 and 20 are contacted to the semiconductor layer 16 as the last step of the process according to the present invention, unwanted diffusion of the source and drain metal into the semiconductor layer is eliminated. The source and drain electrodes 19 and 20 can easily be made as thick as required for achieving proper current carrying capabilities, since the prior art problem of step coverage of the semiconductor over the source and drain electrodes does not arise in the TFT design according to the present invention. Furthermore, the problem of organic contamination of the source and drain contacts which results from residual lift-off photoresist in the fabrication process according to the prior art, does not occur in the process according to the present invention

since the via holes 19a and 20a are formed by an etch process.

Typical I-V characteristics for the TFT of the present invention are shown in Figure 5.

5 The highest temperature used in the process according to the present invention is 400°C., allowing for the use of readily available low cost substrates. Proximity printing is effected using lithographic exposure to pattern each layer, resulting in the creation
10 of features with as little as 12 micron resolution.

Turning to Figure 6, the overall construction of a liquid crystal cell according to the present invention, is shown in profile. The active matrix LCD (AMLCD) comprises a plurality of TFT devices as shown in Figure
15 4c arranged on a polarizer 21. Liquid crystal material 23 (i.e. nematic liquid) is confined between alignment layers 22 and 24.

A glass substrate 31 and top polarizer 32 are provided, onto which a black chromium (CrO_x) grid 27 is
20 deposited and patterned to form a light shielding/contrast enhancement layer. Then, the first colour filter (e.g. red filter 28) is spun on, patterned and cured. This process is then repeated for the next two colours (e.g. green filter 29 and blue filter 30).
25 The colour filters 28-30 are fabricated using dyed polyimide material. Finally, the filter is planarized with clear polyimide to form planarization layer 26 and then deposited with ITO layer 25 which forms the back plane electrode.

30 The colour AMLCD of Figure 6, using CdSe TFTs according to the present invention, has applications in military land vehicles and avionics. However, it is contemplated that commercial applications of the invention are, in fact, extremely broad, including
35 displays for lap top and desk top computers, and other applications in which an active matrix display may be used to replace a CRT. The drive electronics (not shown)

used to control the display can be identical to those used in prior art amorphous silicon AMLCDs. Furthermore, the TFT fabrication process according to the present invention utilizes equipment and methods common to the amorphous silicon process, the main exceptions being that CdSe is evaporated instead of plasma deposited as in the prior art amorphous silicon technology, and that proximity printing is used due to the larger features possible with the CdSe design.

It is believed that this compatibility with existing amorphous silicon fabrication techniques and driver chip technology, coupled with the increasingly apparent limitations of prior art amorphous silicon TFTs, will speed the development of new applications for CdSe based AMLCDs such as discussed herein throughout avionics and other industries requiring thin film AMLCDs.

Other embodiments and variations of the invention are possible within the sphere and scope of the claims appended hereto.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE
PROPERTY OF PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A thin film transistor, comprising:
 - 5 a) a glass substrate;
 - b) a gate electrode deposited on said substrate;
 - c) a gate insulator layer deposited on said substrate so as to overly said gate electrode;
 - 10 d) a thin film semiconductor channel layer deposited on said gate insulator layer and substantially aligned with said gate electrode;
 - e) a passivation layer deposited on said gate insulator layer so as to overly said thin film semiconductor channel layer; and
 - 15 f) a pair of source and drain electrodes deposited on said passivation layer and extending through a portion of said passivation layer for contacting said semiconductor channel layer.
- 20 2. The thin film transistor of claim 1, further comprising a pair of via holes etched through said passivation layer to said semiconductor channel layer through which said pair of source and drain electrodes
- 25 extend for contacting said semiconductor channel layer.
3. The thin film transistor of claim 1, wherein said gate electrode is fabricated from chromium.
- 30 4. The thin film transistor of claim 1, wherein said gate insulator layer is fabricated from SiO_x .
5. The thin film transistor of claim 4, wherein said gate insulator layer is approximately 5000 Å in
- 35 thickness.
6. The thin film transistor of claim 1, wherein

said thin film semiconductor channel layer is fabricated from CdSe.

7. The thin film transistor of claim 6, wherein
5 said thin film semiconductor channel layer is approximately 500 Å in thickness.

8. The thin film transistor of claim 1, wherein
10 said passivation layer is fabricated from SiO_x.

9. The thin film transistor of claim 1, further
comprising a pixel output pad intermediate respective
portions of said passivation layer and said drain
electrode.

15 10. A method of fabricating a thin film transistor,
comprising the steps of:

- a) providing a substrate;
- b) depositing a gate electrode on said
20 substrate;
- c) depositing a gate insulator layer on said
substrate so as to overly said gate electrode;
- d) depositing a thin film semiconductor channel
layer on said gate insulator layer so as to be
25 substantially aligned with said gate electrode;
- e) depositing a passivation layer on said gate
insulator layer so as to overly said thin film
semiconductor channel layer;
- f) etching a pair of via holes through said
30 passivation layer to said semiconductor channel layer;
and
- g) depositing a pair of source and drain
electrodes on said passivation layer so as to extend
through said via holes for contacting said semiconductor
35 channel layer.

11. The method of claim 10, wherein said step of

etching said pair of via holes comprises subjecting said passivation layer to at least one reactive ion etching gas.

5 12. The method of claim 11, further comprising sputter etching said semiconductor layer for cleaning contamination prior to depositing said pair of source and drain electrodes.

10 13. An active matrix liquid crystal display, comprising:

a) a first polarizing layer;

b) a first glass substrate deposited on said first polarizing layer;

15 c) a plurality of gate electrodes deposited on said first glass substrate;

d) a gate insulator layer deposited on said first glass substrate so as to overly said gate electrodes;

20 e) a plurality of thin film semiconductor channel layers deposited on said gate insulator layer and substantially aligned with respective ones of said plurality of gate electrodes;

25 f) a passivation layer deposited on said gate insulator layer so as to overly respective ones of said plurality of thin film semiconductor channel layers;

g) a plurality of pairs of via holes etched through said passivation layer to respective ones of said semiconductor channel layers;

30 h) a plurality of pairs of source and drain electrodes deposited on said passivation layer and extending through respective ones of said pairs of via holes for contacting respective ones of said semiconductor channel layers;

35 i) a plurality of select lines for interconnecting said plurality of gate electrodes;

j) a plurality of data lines arranged

orthogonally to said select lines for interconnecting said plurality of source electrodes;

k) a plurality of rectangular pixel output pads intermediate respective ones of said orthogonally arranged select lines and data lines and connected to respective ones of said drain electrodes;

l) a first alignment layer deposited on said substrate so as to overly said select lines, said data lines and said rectangular pixel output pads;

m) a layer of liquid crystal material overlying said first alignment layer;

n) a second polarizing layer;

o) a second glass substrate deposited on said second polarizing layer;

p) a light shielding/contrast enhancement layer deposited on said second glass substrate;

q) a plurality of colour filters spun on to said light shielding/contrast enhancement layer, said plurality of colour filters being thereafter patterned to align with respective ones of said rectangular pixel output pads and then cured;

r) a planarization layer deposited on said plurality of colour filters;

s) a conductive backplane electrode deposited on said planarization layer; and

t) a second alignment layer intermediate said backplane electrode and said layer of liquid crystal material.

14. The active matrix liquid crystal display of claim 13, wherein said colour filters are fabricated from dyed polyimide material.

15. The active matrix liquid crystal display of claim 13, wherein said light shielding/contrast enhancement layer is fabricated from CrO_x .

16. The active matrix liquid crystal display of claim 13, wherein said backplane electrode is fabricated from indium tin oxide.
- 5 17. The active matrix liquid crystal display of claim 13, wherein each one of said plurality of gate electrodes is fabricated from chromium.
- 10 18. The active matrix liquid crystal display of claim 13, wherein said gate insulator layer is fabricated from SiO_x .
- 15 19. The active matrix liquid crystal display of claim 18, wherein said gate insulator layer is approximately 5000 Å in thickness.
- 20 20. The active matrix liquid crystal display of claim 13, wherein each of said thin film semiconductor channel layers is fabricated from CdSe.
21. The active matrix liquid crystal display of claim 20, wherein each of said thin film semiconductor channel layers is approximately 500 Å in thickness.
- 25 22. The active matrix liquid crystal display of claim 13, wherein said passivation layer is fabricated from SiO_x .
- 30

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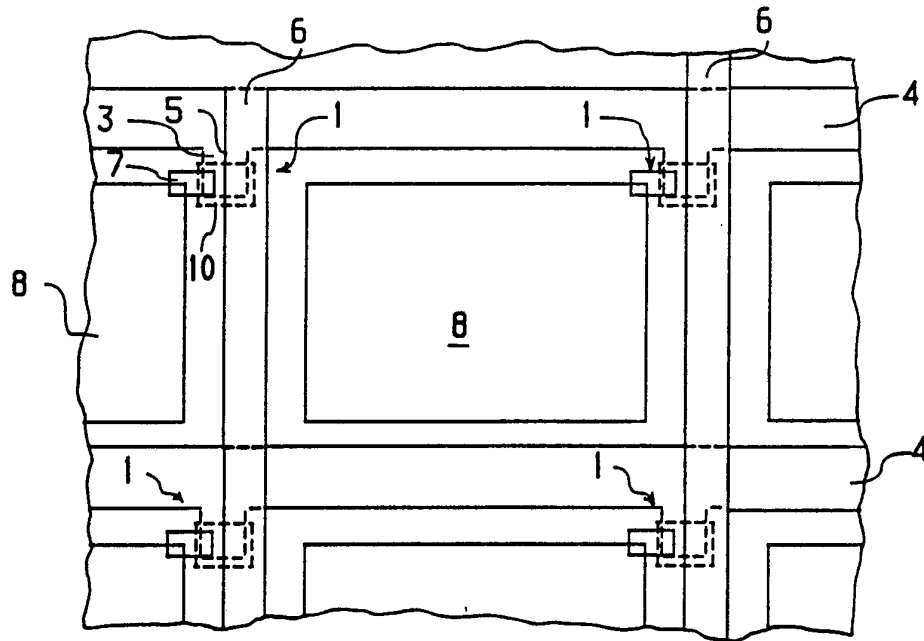


FIG. 1. (PRIOR ART)

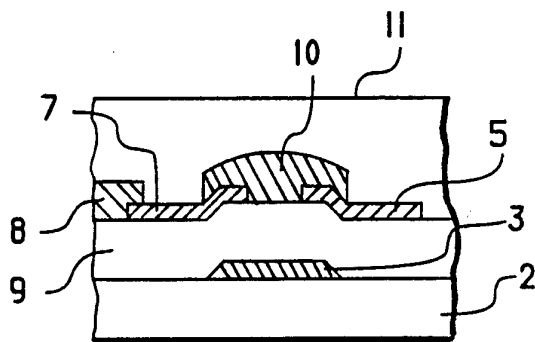


FIG. 2. (PRIOR ART)

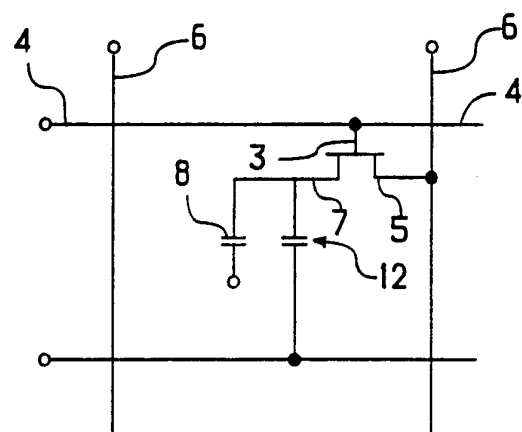


FIG. 3. (PRIOR ART)

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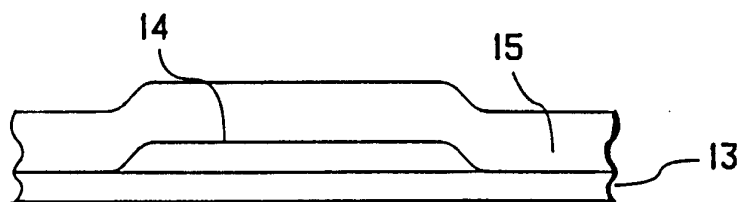


FIG. 4.A.

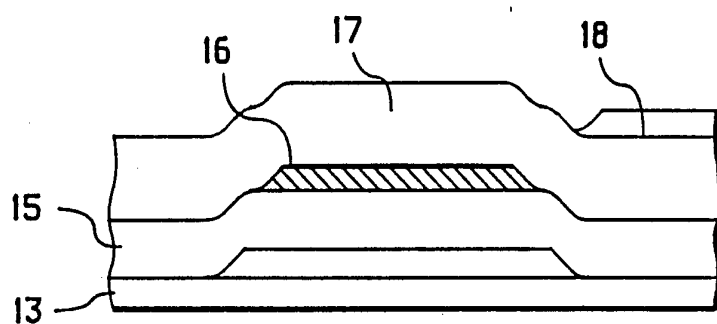


FIG. 4.B.

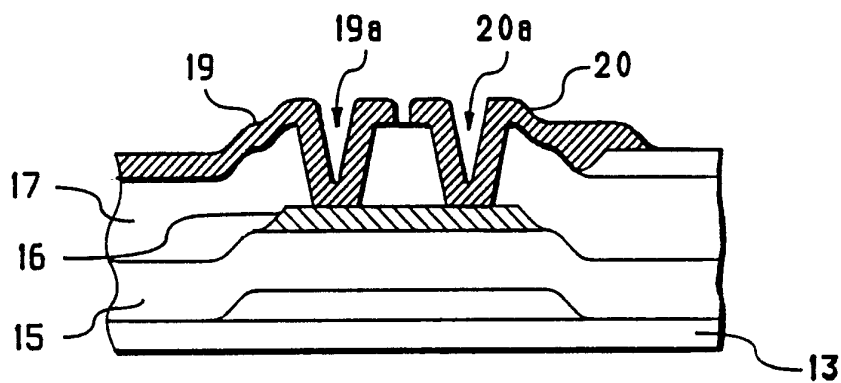


FIG. 4.C.

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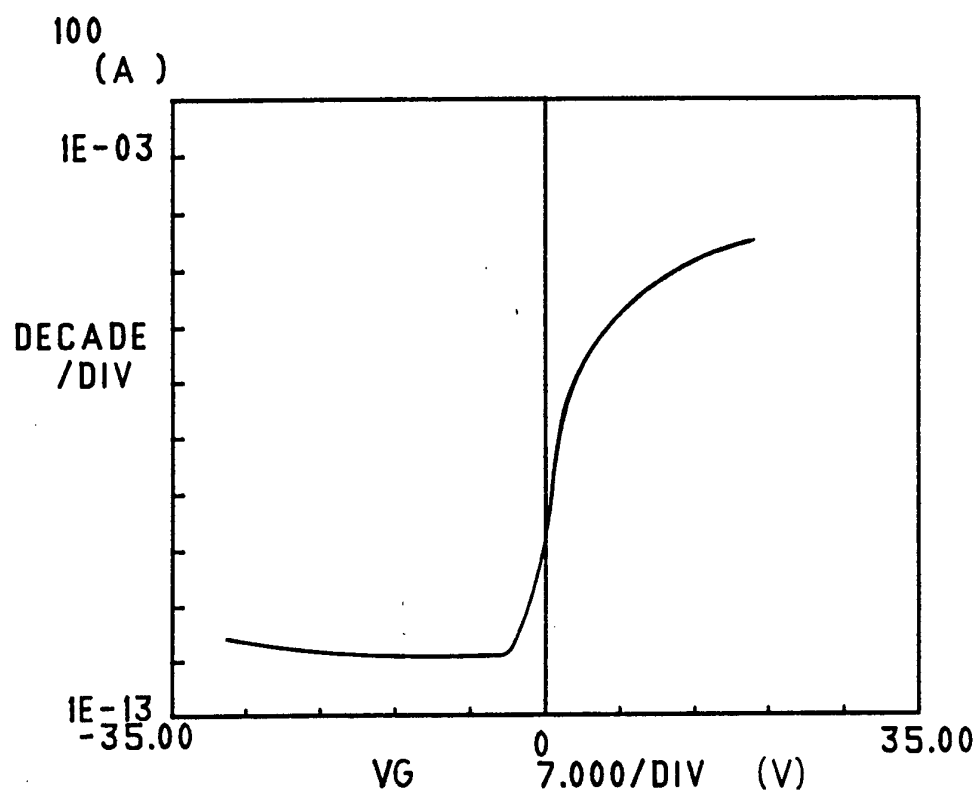


FIG.5.

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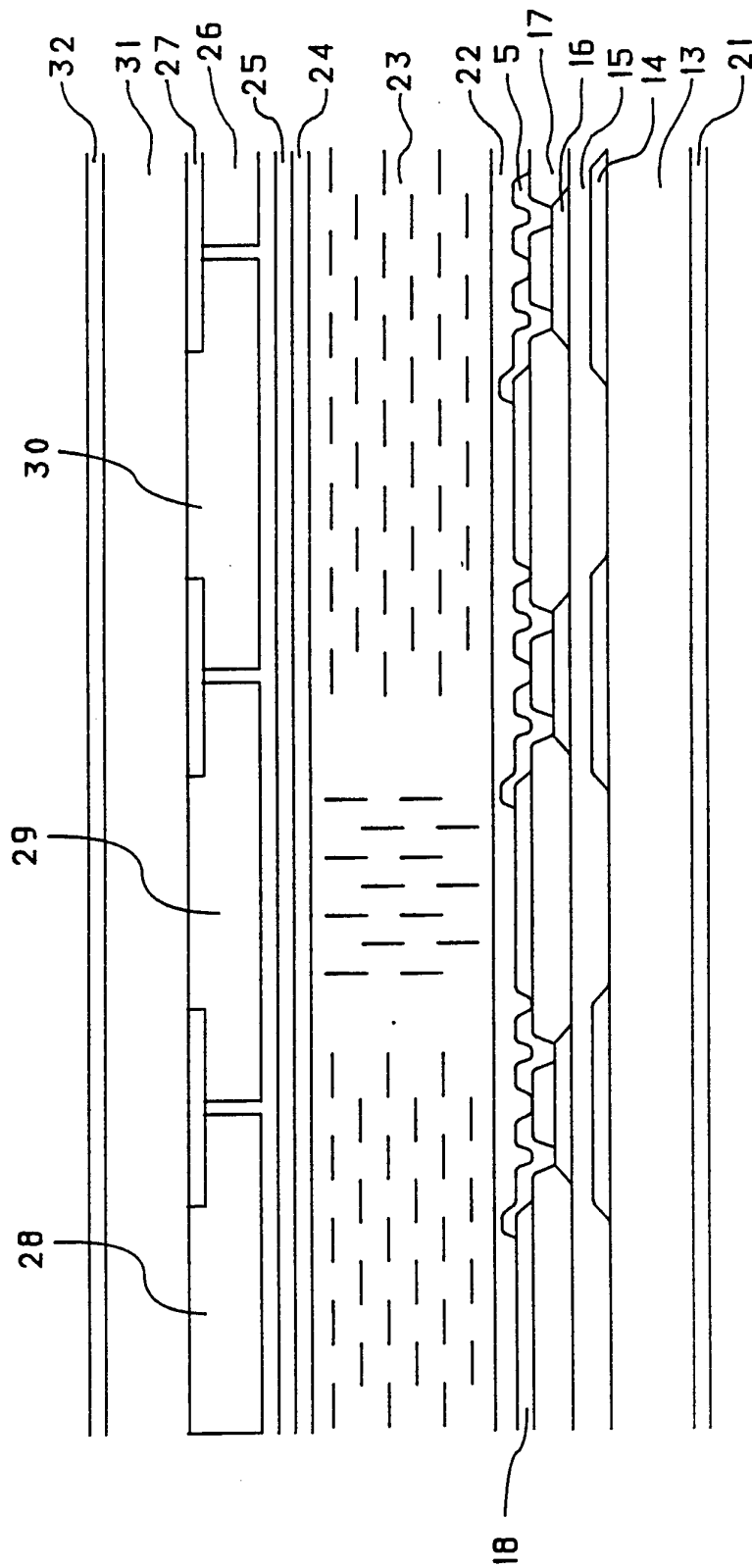


FIG. 6.

SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International Application No

PCT/CA 92/00520

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC Int.Cl. 5 H01L29/784		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
Int.Cl. 5	H01L ; G02F	
Documentation Searched other than Minimum Documentation to the extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 174 (E-612)24 May 1988 & JP,A,62 281 369 (MATSUSHITA ELECTRIC IND CO LTD) 7 December 1987	1,2,9,10
Y	see abstract ---	13,16
Y	CONFERENCE RECORD OF THE 1985 INTERNATIONAL DISPLAY RESEARCH CONFERENCE SAN DIEGO, CAL. OCTOBER 15-17, 1985 pages 18 - 23 T. SUNATA ET AL 'A LARGE AREA, HIGH RESOLVING POWER ACTIVE MATRIX COLOR LCD ADDRESSED BY a-SI TFTs' see abstract; figure 4 --- -/--	13,16
<p>¹⁰ Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search 23 JUNE 1993	Date of Mailing of this International Search Report 02.07.93	
International Searching Authority EUROPEAN PATENT OFFICE	Signature of Authorized Officer MIMOUN B.J.	

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category ^a	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X	US,A,5 010 027 (POSSIN ET AL) 23 April 1991 see column 3, line 6 - line 40; figures 2,3 see column 5, line 13 - column 6, line 10 ---	1,3-5,8
X	PATENT ABSTRACTS OF JAPAN vol. 10, no. 221 (E-424)(2277) 2 August 1986 & JP,A,61 058 271 (HITACHI LTD) 25 March 1986 see abstract ---	1
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 564 (E-860)14 December 1989 & JP,A,12 35 384 (MATSUSHITA ELECTRIC IND CO LTD) 20 September 1989 see abstract ---	1,23, 10-12
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-5010027	23-04-91	None	