



(51) International Patent Classification:

H01L 21/687 (2006.01) *H01L 21/673* (2006.01)
H01L 21/683 (2006.01)

(21) International Application Number:

PCT/US2017/062248

(22) International Filing Date:

17 November 2017 (17.11.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/424,159 18 November 2016 (18.11.2016) US
15/815,673 16 November 2017 (16.11.2017) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **THIRUNAVUKARASU, Sriskantharajah**;
54 Canberra Drive, Unit 07-25, Singapore 768440 (SG).
VAYYAPRON, Shoju; F8, Swarna Heavens Apt., Upkar
Lyt., Prashanth Ext, Whitefield, Bangalore 560066 (IN).
MAHADEV, Anand; Jayaleela, No. 98/78/8, Kodigehal-
li-Tindlu main, GD Layout, Vidyananyapura, Bangalore
560097 (IN). **KALYANASUNDARAM, Shankeerthan**;
49/1 Jinananda Mawatha, Kotahena, 13, Western Province,

Colombo 01300 (LK). **PEH, Eng Sheng**; Block 436, Jurong
West Ave 1, #08-454, Singapore 640436 (SG).

(74) Agent: **TABOADA, Alan** et al.; MOSER TABOADA,
1030 Broad Street, Suite 203, Shrewsbury, New Jersey
07702 (US).

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

(54) Title: HYBRID SUBSTRATE CARRIER

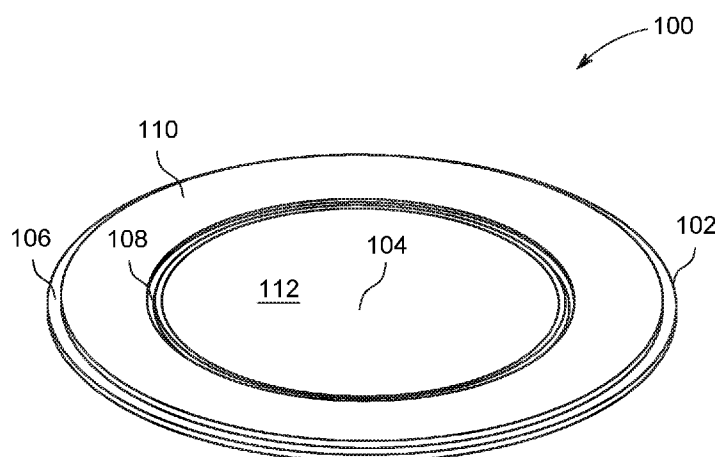


FIG. 1

(57) Abstract: Embodiments of a hybrid substrate carrier are provided herein. In some embodiments, a substrate carrier includes: a carrier ring having an inner ledge adjacent a central opening of the carrier ring; and a carrier plate having a diameter greater than central opening and configured to rest upon the inner ledge, wherein the carrier plate includes an electrode disposed beneath a support surface to electrostatically clamp a substrate to the support surface of the carrier plate.

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

HYBRID SUBSTRATE CARRIER

FIELD

[0001] Embodiments of the present disclosure generally relate to semiconductor substrate processing systems.

BACKGROUND

[0002] Integrated circuit production has been migrating from 200 mm to 300 mm substrates, or wafers, for several years. The move allows the creation of up to 2.5 times more chips on a single wafer and can enable chipmakers to lower the cost of producing the increasingly powerful semiconductors demanded by today's Information Age applications. However, the inventors believe that not all semiconductors will ever be produced on 300 mm wafers. Although chip capacity is transitioning to 300 mm wafers, the inventors believe that 200 mm wafers will not disappear in the near future. Specifically, the inventors believe that fabs running 200 mm wafers may continue to be used at least for the indefinite future to fabricate a variety of devices, for example, specialty memories, image sensors, display drivers, microcontrollers, analog products, and MEMS-based devices. The inventors further believe that some chipmakers may desire to have a mix of chip production running 300 mm and 200 mm wafers on 300 mm and 200 mm tools respectively.

[0003] Thus, the inventors have provided embodiments of substrate carriers for multiple-sized substrates for use in substrate processing systems.

SUMMARY

[0004] Embodiments of a hybrid substrate carrier are provided herein. In some embodiments, a substrate carrier includes: a carrier ring having an inner ledge adjacent a central opening of the carrier ring; and a carrier plate having a diameter greater than central opening and configured to rest upon the inner ledge, wherein the carrier plate includes an electrode disposed beneath a support surface to electrostatically clamp a substrate to the support surface of the carrier plate.

[0005] In some embodiments, a substrate carrier includes: a carrier ring having an inner ledge adjacent a central opening of the carrier ring, an outer ledge, and a

substantially planar upper surface disposed between the inner and outer ledges; and a carrier plate having a diameter greater than central opening and configured to rest upon the inner ledge, wherein the carrier plate includes an electrode to electrostatically clamp a substrate to the carrier plate; wherein a lower surface of the carrier plate and a lower surface of the carrier ring are substantially coplanar when the carrier plate is disposed on the inner ledge; and wherein the carrier plate has a thickness less than a thickness of the carrier ring. In some embodiments, the carrier plate has a diameter less than 200 mm, and a sidewall of the carrier ring at the interface of the upper surface and the inner ledge is disposed along a diameter that is greater than 200 mm to define a gap between the edge of a 200 mm wafer (when disposed on the carrier plate) and the sidewall.

[0006] In some embodiments, a substrate carrier includes: a carrier ring having an inner ledge adjacent a central opening of the carrier ring, an outer ledge, a substantially planar upper surface disposed between the inner and outer ledges, and a substantially planar lower surface opposite the upper surface, wherein the inner ledge is stepped and has an inner portion having a lesser thickness than an outer portion of the inner ledge; and a carrier plate having a diameter greater than central opening and configured to rest upon the inner ledge, wherein the carrier plate includes a lower portion having a diameter less than the central opening and radially extending protrusion configured to rest on the inner portion of the inner ledge of the carrier ring such that the lower portion sits within the central opening, and wherein the carrier plate includes an electrode to electrostatically clamp a substrate to the carrier plate; wherein a lower surface of the carrier plate and a lower surface of the carrier ring are substantially coplanar when the carrier plate is disposed on the inner ledge; and wherein the carrier plate has a thickness less than a thickness of the carrier ring.

[0007] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative

embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0009] Figure 1 is an isometric view of a hybrid substrate carrier in accordance with at least some embodiments of the present disclosure.

[0010] Figure 2 is a partial isometric view of the hybrid substrate carrier of Figure 1 in accordance with at least some embodiments of the present disclosure.

[0011] Figure 3 is a partial isometric view of the hybrid substrate carrier of Figure 1 in accordance with at least some embodiments of the present disclosure and having a substrate disposed thereon.

[0012] Figure 4 is a top view of a carrier plate for a substrate carrier in accordance with at least some embodiments of the present disclosure.

[0013] Figure 5 is a top view of a carrier ring in accordance with at least some embodiments of the present disclosure.

[0014] Figure 6 is a top view of a hybrid substrate carrier having the carrier plate mounted on the carrier ring in accordance with at least some embodiments of the present disclosure.

[0015] Figure 7 is a cross-sectional side view of a portion of a hybrid substrate carrier in accordance with at least some embodiments of the present disclosure.

[0016] Figure 8 is detailed a cross-sectional side view of a portion of the hybrid substrate carrier of Figure 7 in accordance with at least some embodiments of the present disclosure.

[0017] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0018] Embodiments of a hybrid substrate carrier are provided herein. Embodiments of the present disclosure advantageously enable 200 mm wafers to be run with little or no hardware modifications while maintaining process transparency and stable defect performance on 300 mm platforms and process chambers. In addition, embodiments of the present disclosure advantageously allow flexibility to increase the capacity of 200 mm wafer production on existing available 300 mm tools and switching back to 300 mm wafer production effortlessly. Moreover, the hybrid substrate carrier is reusable and designed to prevent wafer level arcing.

[0019] Embodiments of the hybrid bridge carrier are designed to chuck 200 mm electrostatically and transit seamlessly across processing chambers in 300 mm platforms. Thus, no downtime is incurred to switch production from 300 mm to 200 mm wafers. Embodiments of the hybrid bridge carrier are process transparent and compatible to most 300 mm multi-chamber systems in microelectronic device production. Moreover, embodiments of the present disclosure advantageously provide significant cost savings and minimum production scheduled downtime for substrate handler conversion in enabling 200 mm wafer production on 300 mm platforms and process chambers. For example, embodiments of the hybrid bridge carrier are compatible with 300 mm multi-chamber systems, such as physical vapor deposition (PVD) chambers, chemical vapor deposition (CVD) chambers, etching chambers, and the like.

[0020] Figure 1 is an isometric view of a hybrid substrate carrier in accordance with at least some embodiments of the present disclosure. Figure 2 is a partial isometric view of the hybrid substrate carrier of Figure 1 enlarged to more clearly illustrate the hybrid substrate carrier. Figure 3 is a partial isometric view of the hybrid substrate carrier of Figure 1 having a substrate disposed thereon. As shown in Figures 1-3, a hybrid substrate carrier (e.g., substrate carrier 100) includes a carrier ring 102 and a carrier plate 104 configured to rest within the carrier ring 102.

[0021] In some embodiments, the carrier ring 102 includes an outer ledge 106 disposed along the outer peripheral edge of the carrier ring 102. The outer ledge

106 may advantageously facilitate handling (e.g., storage and/or movement) of the carrier ring 102 (and the substrate carrier 100 as a whole). Thus, the outer ledge is configured for handling by substrate handling equipment (such as 300 mm substrate handling equipment). In some embodiments, the outer ledge 106 is free or substantially free of openings formed therethrough. The carrier ring 102 includes an inner ledge 108 disposed along the inner peripheral edge of the carrier ring 102. In some embodiments, the inner ledge 108 is free or substantially free of openings formed therethrough. An upper surface 110 of the carrier ring 102 disposed between the outer ledge 106 and the inner ledge 108 is raised above the respective upper surfaces of the outer ledge 106 and the inner ledge 108. In some embodiments, the upper surface 110 is substantially planar. In some embodiments, the body of the carrier ring 102 is free or substantially free of openings formed therethrough. The carrier ring may be fabricated from quartz. The separable carrier ring 102 advantageously may be easily cleaned separate from the carrier plate 104.

[0022] Figure 5 is a top view of a carrier ring in accordance with at least some embodiments of the present disclosure. Figure 5 depicts a top view of the carrier ring 102 showing the outer ledge 106, upper surface 110, and inner ledge 108 surrounding a central opening 502 of the carrier ring 102. As depicted in Figure 5, the carrier ring 102 can be free of holes or openings formed through the body of the carrier ring 102.

[0023] Returning to Figures 1-3, the carrier plate 104 is sized and configured such that the outer peripheral edge of the carrier plate 104 rests upon at least a portion of the inner ledge 108 of the carrier plate 104 to fill and/or cover the central opening of the carrier ring 102 (e.g., 502 in Figure 5). The carrier plate 104 need not be mechanically coupled to the carrier ring 102. Thus, in some embodiments, no bolts, clamps, screws, adhesives, brazing, welding, or the like is provided to couple the carrier plate 104 to the carrier ring 102. The carrier plate 104 includes a substantially planar substrate support surface 112 to support a substrate thereon. For example, Figure 3 depicts a substrate 302 disposed atop the carrier plate 104. The substrate carrier 100 may advantageously be configured to support a smaller substrate (such as a 200 mm wafer) atop the carrier plate 104 and radially inward of the upper surface 110 of the carrier ring 102.

[0024] The carrier plate 104 may be made of a highly thermally conductive material (e.g., aluminum nitride, AlN, or silicon carbide, SiC) to maintain robust thermal conductivity from an underlying substrate support through the carrier plate 104 to a substrate disposed thereon. The highly thermally conductive material (e.g., aluminum nitride, AlN, or silicon carbide, SiC) further advantageously can withstand high temperature applications in most wafer processing chambers.

[0025] The carrier plate further has electrostatic chucking capability for excellent wafer bonding and heat transmission from/to an underlying substrate support. For example, the carrier plate 104 includes an electrode, such as an embedded electrode, suitable for electrostatically clamping a substrate to the carrier plate 104. As depicted in the top view of a carrier plate as shown in Figure 4, the carrier plate 104 may include an electrode 402. In some embodiments, and as illustrated, the electrode 402 may comprise a first electrode 406 and a second electrode 408. For example, the first and second electrodes 406, 408 may be half-moon, or semi-circular, electrodes. Other electrode configurations are suitable as well.

[0026] The electrostatic chucking capability advantageously provides excellent substrate bonding to the carrier plate 104 and enhances heat transfer between a substrate mounted on the carrier plate 104 and a substrate support upon which the substrate carrier is disposed. The electrode 402 (or first and second electrodes 406, 408) may be charged or discharged to respectively clamp or release a substrate from the carrier plate 104 at a charging/discharging station (not shown).

[0027] Figure 6 is a top view of a hybrid substrate carrier (e.g., substrate carrier 100) having a carrier plate (e.g., carrier plate 104) mounted on a carrier ring (e.g., carrier ring 102) in accordance with at least some embodiments of the present disclosure. As shown in Figure 6, the outer diameter of the carrier plate 104 is smaller than the inner diameter of the interface between the upper surface 110 of the carrier ring 102 and the inner ledge 108 of the carrier ring 102.

[0028] Figure 7 is a cross-sectional side view of a portion of a hybrid substrate carrier in accordance with at least some embodiments of the present disclosure. As shown in Figure 7, in some embodiments, the carrier ring 102 includes a lower surface 702 that is parallel to the upper surface 110 such that the overall profile of

the carrier ring 102 is substantially flat, or planar (excluding the outer and inner ledges 106, 108). In some embodiments, the substantially planar lower surface 702 extends from the outer diameter to the inner diameter of the carrier ring 102 such that the outer and inner ledges 106, 108 are defined by reduced thickness of the carrier ring 102 such that upper surfaces of the outer and inner ledges 106, 108 are not coplanar with the upper surface 110.

[0029] Figure 8 is detailed a cross-sectional side view of a portion of the hybrid substrate carrier of Figure 7 in accordance with at least some embodiments of the present disclosure. As shown more clearly in Figure 8, the carrier ring 102 is configured to support the carrier plate 104 on the inner ledge 108 of the carrier ring 102. In some embodiments, a lower surface 704 of the carrier plate 104 may be substantially coplanar with the lower surface 702 of the carrier ring 102. In some embodiments, the inner ledge 108 has a thickness such that an upper surface of a substrate (e.g., substrate 302) disposed on the carrier plate (such as a standard wafer, e.g., a 200 mm wafer) is coplanar or substantially coplanar with the upper surface 110. For example, a thickness 822 of the carrier ring 102 is greater than a thickness 824 of the carrier plate 104. In some embodiments, the thickness 822 is greater than the thickness 824 by an amount substantially equal to a thickness of a substrate 302 to be supported, such that a combined thickness 826 of the carrier plate 104 and the substrate 302 is substantially equal to the thickness 822 of the carrier ring 102.

[0030] In some embodiments, the inner edge of the inner ledge 108 of the carrier ring 102 (e.g., sidewall 802 at the interface between upper surface 110 and the inner ledge 108) has a diameter that is greater than the diameter of the substrate disposed on the carrier plate 104. For example, the upper surface of the carrier plate 104, the inner ledge 108, and the sidewall 802 define a pocket in which the substrate may be disposed during use. In embodiments where the carrier plate 104 is designed to support a 200 mm wafer, the carrier plate 104 can have a diameter that is slightly less than the substrate to provide an overhang 804. In some embodiments, the overhang 804 may be about 1 mm (e.g., the carrier plate 104 may have a diameter of about 198 mm). The sidewall 802 may be disposed along a diameter greater than that of the substrate to be supported to define a radial gap

806 between the sidewall 802 and the edge of the substrate. In some embodiments, the radial gap 806 may be about 2.5 mm.

[0031] The support surface 112 of the carrier plate 104 is disposed above the inner ledge 108 to define a gap 808 between the plane of the support surface (e.g., and the overhanging bottom surface of the substrate when present) and the plane of the upper surface of the inner ledge 108.

[0032] In some embodiments, the inner ledge 108 may be stepped, for example, having an inner portion 810 having a lesser thickness than an outer portion 812 of the inner ledge 108. In such embodiments, the carrier plate 104 may include a corresponding radially extending protrusion 814 configured to rest on the inner portion 810. In such embodiments, the carrier plate 104 has a lower portion having a diameter less than the central opening (e.g., 502 in Figure 5) such that the carrier plate 104 sits within the central opening and the radially extending protrusion 814 rests upon the inner portion 810 of the inner ledge 108. A gap 816 is disposed between the sidewall of the carrier plate 104 below the radially extending protrusion 814 and the sidewall of the inner ledge 108 adjacent the central opening 502. In some embodiments, the outer portion 812 of the inner ledge 108 has a diameter greater than the radially extending protrusion 814 to define a gap 818 between the outermost diameter of the radially extending protrusion 814 and the step of the inner ledge 108. In some embodiments, the radially extending protrusion 814 has a thickness 820 that is greater than the reduction in thickness of the inner ledge 108 at the step, such that the plane of the support surface 112 is elevated relative to the upper surface of the outer portion 812 of the inner ledge 108 to provide the gap 808 discussed above.

[0033] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A substrate carrier, comprising:
a carrier ring having an inner ledge adjacent a central opening of the carrier ring; and
a carrier plate having a diameter greater than central opening and configured to rest upon the inner ledge, wherein the carrier plate includes an electrode disposed beneath a support surface to electrostatically clamp a substrate to the support surface of the carrier plate.
2. The substrate carrier of claim 1, further comprising:
an outer ledge disposed along the outer peripheral edge of the carrier ring.
3. The substrate carrier of claim 1, further comprising:
an upper surface of the carrier ring disposed radially outward of the inner ledge, wherein the upper surface of the carrier ring is raised above an upper surface of the inner ledge.
4. The substrate carrier of claim 1, wherein the carrier ring and the carrier plate are not coupled together.
5. The substrate carrier of claim 1, wherein at least one of:
the carrier ring is fabricated from quartz; or
wherein the carrier plate is made of a highly thermally conductive material.
6. The substrate carrier of claim 1, wherein the carrier plate is made of a highly thermally conductive material, and wherein the highly thermally conductive material is aluminum nitride or silicon carbide.
7. The substrate carrier of any of claims 1 to 6, wherein the carrier ring is configured to be handled by 300 mm substrate handling equipment and the carrier

plate is configured to support a substrate having a diameter less than 300 mm radially inward of an upper surface of the carrier ring.

8. The substrate carrier of claim 7, wherein the carrier plate is configured to support a substrate having a diameter of about 200 mm.

9. The substrate carrier of any of claims 1 to 6, wherein the electrode comprises a first electrode and a second electrode.

10. The substrate carrier of claim 9, wherein the first and second electrodes are half-moon, or semi-circular, electrodes.

11. The substrate carrier of any of claims 1 to 6, wherein the outer diameter of the carrier plate is smaller than the inner diameter of an interface between an upper surface of the carrier ring and the inner ledge of the carrier ring.

12. The substrate carrier of any of claims 1 to 6, wherein the carrier ring includes a lower surface that is parallel to an upper surface of the carrier ring such that the carrier ring is substantially flat.

13. The substrate carrier of claim 12, further comprising an outer ledge disposed along the outer peripheral edge of the carrier ring, wherein the lower surface extends from the outer diameter to the inner diameter of the carrier ring such that the outer and inner ledges are defined by a reduced thickness of the carrier ring and such that upper surfaces of the outer and inner ledges are not coplanar with the upper surface.

14. The substrate carrier of any of claims 1 to 6, wherein a thickness of the carrier plate is less than a thickness of the carrier ring.

15. The substrate carrier of claim 14, wherein the thickness of the carrier ring is greater than the thickness of the carrier plate by an amount substantially equal to a

thickness of a substrate to be supported, such that a combined thickness of the carrier plate and the substrate to be supported is substantially equal to the thickness of the carrier ring.

1/5

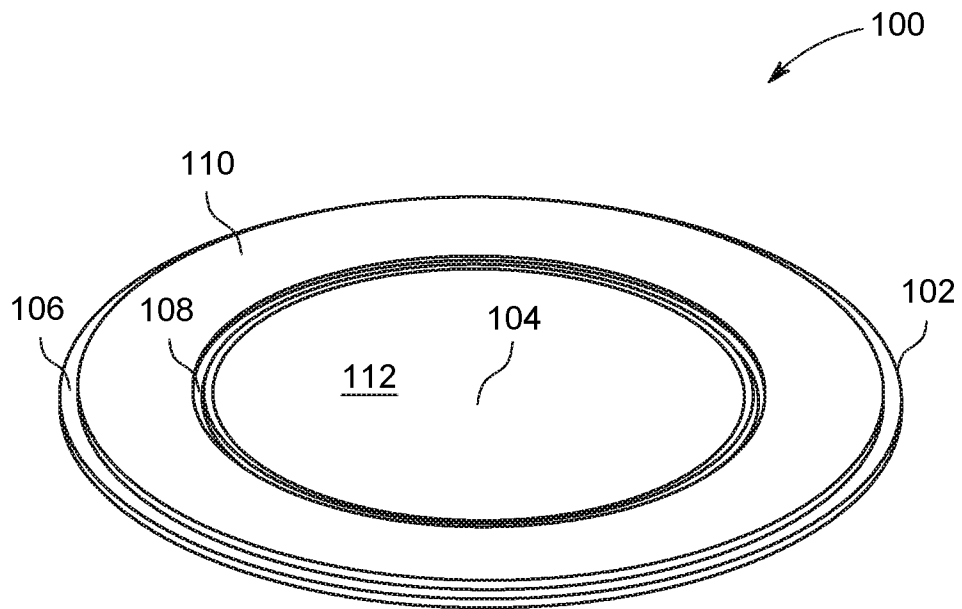


FIG. 1

2/5

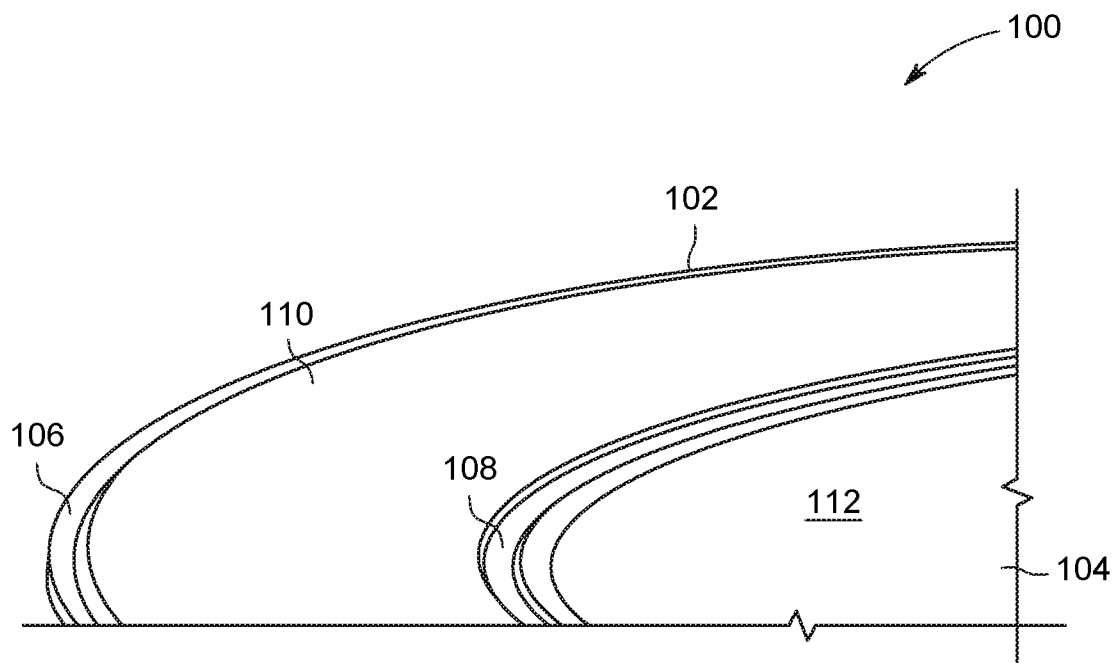


FIG. 2

3/5

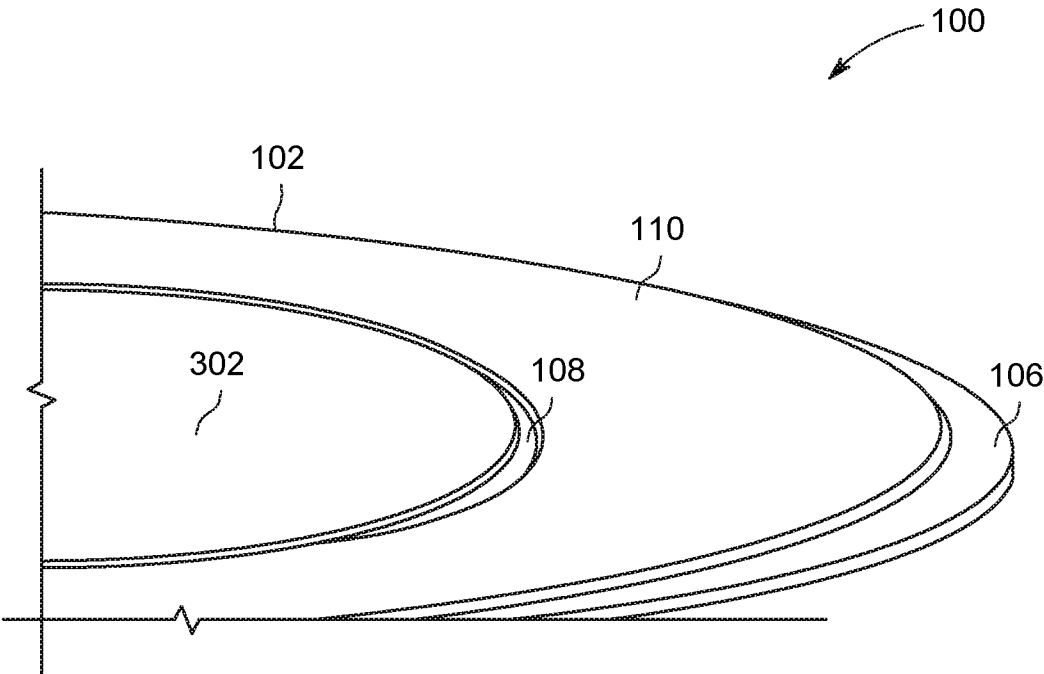


FIG. 3

4/5

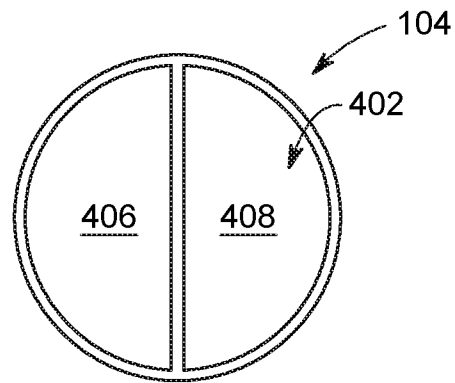


FIG. 4

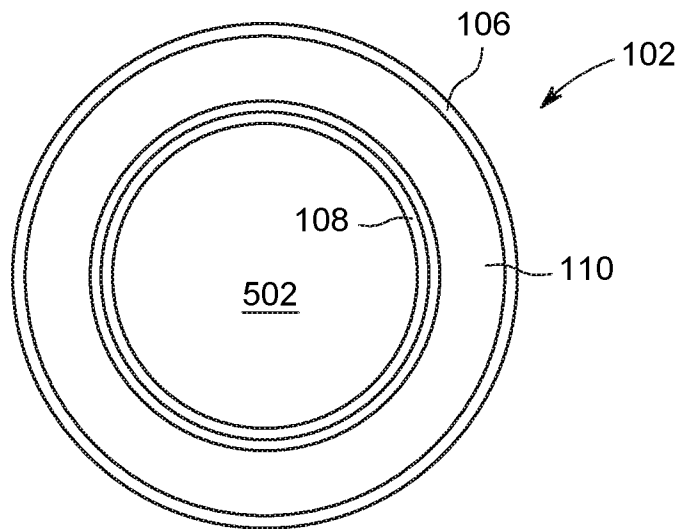


FIG. 5

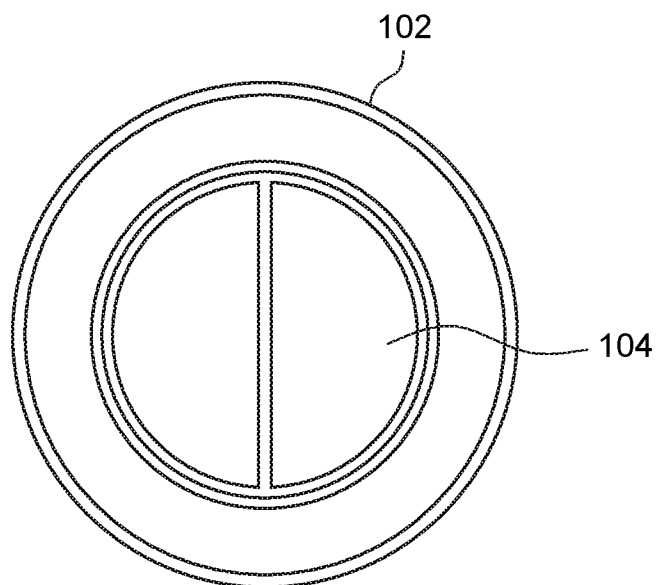


FIG. 6

5/5

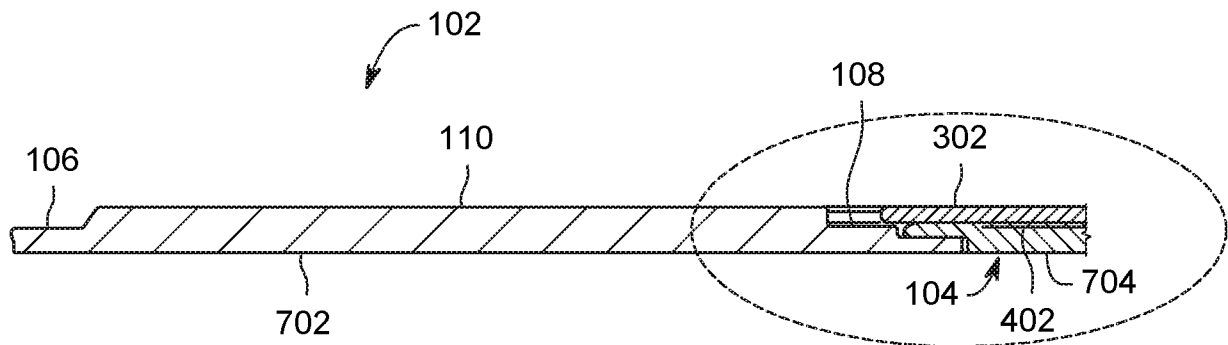


FIG. 7

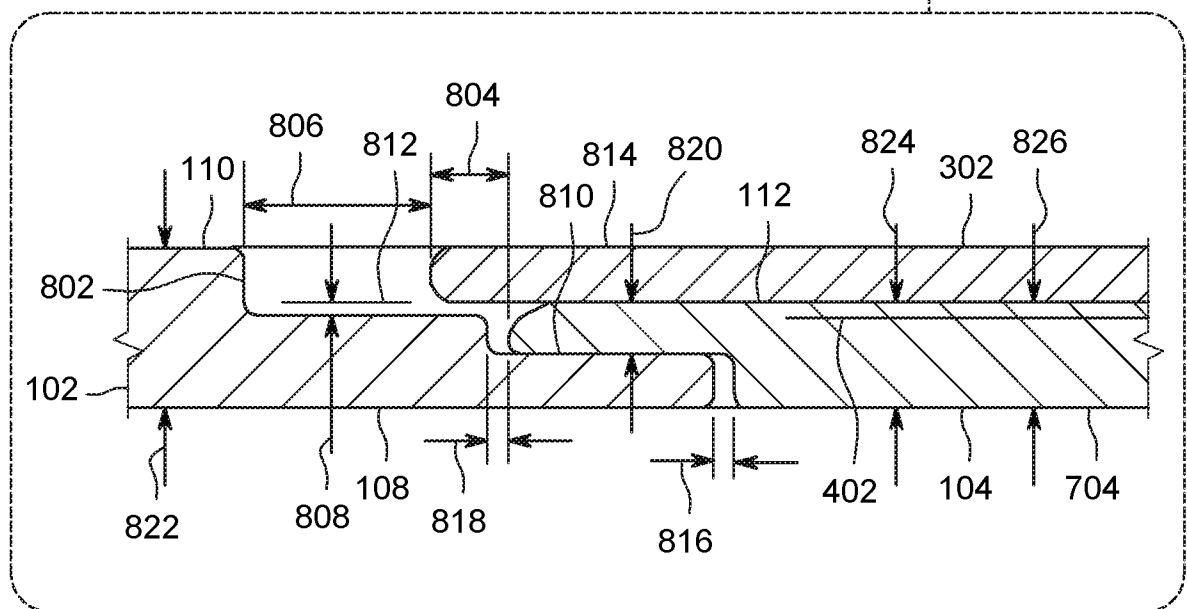


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/062248**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/687(2006.01)i, H01L 21/683(2006.01)i, H01L 21/673(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/687; C23C 16/04; H02N 13/00; C23F 1/00; H01T 23/00; B24B 37/04; B24B 41/04; C23C 16/00; H01L 21/683; H01L 21/673

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: substrate, carrier, ring, plate, inner, outer, ledge, electrode, support, surface, electrostatically, clamp, diameter, central, opening

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0020629 A1 (TSAI et al.) 23 January 2014 See paragraphs [0022]-[0035]; and figures 1, 2A-2B, 3.	1-15
Y	US 5986874 A (ROSS et al.) 16 November 1999 See column 4, lines 1-26; and figures 2-3.	1-15
A	EP 1046464 A1 (OBSIDIAN, INC.) 25 October 2000 See paragraphs [0072]-[0074]; and figures 10-11.	1-15
A	US 2003-0029571 A1 (GOODMAN et al.) 13 February 2003 See paragraphs [0156]-[0185]; and figures 16-27.	1-15
A	US 2007-0258186 A1 (MATYUSHKIN et al.) 08 November 2007 See paragraphs [0031]-[0045]; and figures 4A-4B.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 March 2018 (12.03.2018)

Date of mailing of the international search report

12 March 2018 (12.03.2018)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Dal Kyong

Telephone No. +82-42-481-8440



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/062248

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0020629 A1	23/01/2014	CN 104428885 A	18/03/2015
		CN 104428885 B	12/09/2017
		KR 10-1774213 B1	04/09/2017
		KR 10-2015-0038129 A	08/04/2015
		SG 11201408298V A	27/02/2015
		TW 201405701 A	01/02/2014
		TW I570835 B	11/02/2017
		US 9252002 B2	02/02/2016
		WO 2014-014822 A1	23/01/2014
US 5986874 A	16/11/1999	JP 2002-502555 A	22/01/2002
		KR 10-0578281 B1	11/05/2006
		WO 98-56102 A1	10/12/1998
EP 1046464 A1	25/10/2000	JP 2000-296457 A	24/10/2000
		TW 496814 B	01/08/2002
		US 6276998 B1	21/08/2001
		US 6645050 B1	11/11/2003
US 2003-0029571 A1	13/02/2003	DE 69813014 T2	12/02/2004
		EP 1036406 A2	20/09/2000
		EP 1036406 B1	02/04/2003
		EP 1308989 A2	07/05/2003
		EP 1308989 A3	26/12/2007
		JP 2001-522142 A	13/11/2001
		KR 10-0660416 B1	22/12/2006
		KR 10-2001-0031715 A	16/04/2001
		US 2002-0043337 A1	18/04/2002
		US 2005-0183829 A1	25/08/2005
		US 6454865 B1	24/09/2002
		US 6893507 B2	17/05/2005
		WO 99-23691 A2	14/05/1999
		WO 99-23691 A3	05/08/1999
US 2007-0258186 A1	08/11/2007	CN 101093811 A	26/12/2007
		CN 101093811 B	25/04/2012
		CN 101093812 A	26/12/2007
		CN 101887865 A	17/11/2010
		CN 101887865 B	19/06/2013
		CN 102593031 A	18/07/2012
		CN 102593031 B	16/09/2015
		JP 2007-300057 A	15/11/2007
		JP 2007-300119 A	15/11/2007
		JP 5069452 B2	07/11/2012
		JP 5183092 B2	17/04/2013
		KR 10-1380879 B1	02/04/2014
		KR 10-1387598 B1	23/04/2014
		KR 10-2007-0105828 A	31/10/2007
		KR 10-2007-0105929 A	31/10/2007

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/062248Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

TW 200807606 A	01/02/2008
TW 200809999 A	16/02/2008
TW I357629 B	01/02/2012
TW I463588 B	01/12/2014
US 2012-0285619 A1	15/11/2012
US 8226769 B2	24/07/2012
US 8663391 B2	04/03/2014