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CONDUCTIVE LAYER PRE-PATTERNING AND SUBSTRATE CORE STRUCTURE FORMED ACCORDING TO THE
METHOD

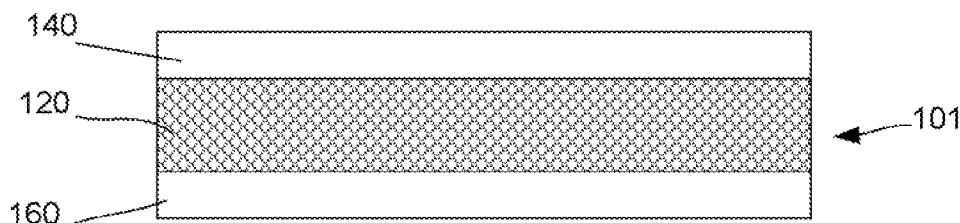


Fig. 1

(57) Abstract: A method of fabricating a substrate core structure comprises: providing first and second patterned conductive layers defining openings therein on each side of a starting insulating layer; providing a first and a second supplemental insulating layers onto respective ones of a first and a second patterned conductive layer; laser drilling a set of via openings extending through at least some of the conductive layer openings of the first and second patterned conductive layers; filling the set of via openings with a conductive material to provide a set of conductive vias; and providing a first and a second supplemental patterned conductive layer onto respective ones of the first and the second supplemental insulating layers, the set of conductive vias contacting the first supplemental patterned conductive layer at one side thereof, and the second supplemental patterned conductive layer at another side thereof.

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A Method of Forming a Substrate Core Structure
Using Microvia Laser Drilling and Conductive Layer Pre-Patterning
And Substrate Core Structure Formed According to the Method

FIELD

[0001] Embodiments of the present invention relate generally to the field of multilayer substrate core structure fabrication, and, in particular, to methods for fabricating such a board by laser drilling microvias therein.

BACKGROUND

[0002] A multilayer substrate core structure may be conventionally fabricated by first providing a copper clad core. The copper clad core (CCL) may be a laminate that is copper clad on one or two sides depending on application needs. An example of such a fabrication process is shown in Figs. 1-8. As seen in Fig. 1, a two sided CCL 101 is first provided including an insulating laminate 12 and top and bottom copper films 140 and 160, respectively. As seen in Fig. 2, the top and bottom copper films 140 and 160 are pre-patterned according to pre-determined interconnect patterns to be provided onto the laminate 120, such as by way of etching, to provide patterned copper films 150 and 170. Thereafter, as seen in Fig. 3, dielectric layer, such as ABF layers 190 and 210 (Ajinomoto Build-Up Film), are laminated onto the patterned copper films 150 and 160, and, as seen in Fig. 4 to provide a first intermediate laminate 180. As seen in Fig. 4, the first intermediate laminate 180 is then provided with through holes 201 by way of mechanical drilling and desmearing to provide a second intermediate laminate 220. The desmearing involves using a desmear solution to process the board to dissolve and remove any smears caused by drilling. As seen in Fig. 5, the through-holes 201 and the top and bottom surfaces of the intermediate laminate 220 are then plated, such as by way of plating, to provide a plated intermediate laminate 240 with plated through holes 260. As seen in Fig. 6, the plated intermediate laminate 240 may be subjected thereafter to PTH plugging with a conductive material 250 such as copper to yield a plugged intermediate laminate 280. In a next stage, as shown in Fig. 7, the plugged intermediate laminate 280 may be lid plated with a conductive material such as copper to provide lids 270 and 290 on a top and bottom surface thereof, the plating occurring on the top and bottom plating existing on laminate 280 of Fig. 6 to yield a

lid plated intermediate laminate 300. Thereafter, the copper existing at the top and bottom surfaces of lid plated intermediate laminate 30 is patterned, such as by way of etching, to yield the wiring board 320 as shown in Fig. 8.

[0003] Prior art substrates are typically built on the base of a thick core (for example one having a thickness of about 0.7 mm (not including any build-up or conductive layers). The prior art core build up process can be lengthy. Taking a four layer core as an example, the macro process stages of a prior art fabrication process may include all of: core baking and cleaning, core copper patterning, copper roughening, ABF lamination, plated through hole drilling, desmear, copper plating, copper roughening, plated through hole plugging, surface flattening, copper plating, and finally, copper patterning. However, mechanical plated through hole drilling can be the most expensive single process in the fabrication of a prior art multilayer substrate core structure. The need for plugging as explained above can add more to the manufacturing costs according to the prior art.

[0004] Disadvantageously, substrate core structures for substrate core structures according to the prior art can be costly, and can carry high manufacturing costs as a result of the use of mechanical drilling technology. These costs can skyrocket where the substrate core structures are miniaturized and scaled for future applications. In addition, mechanical drilling is not suitable for producing holes smaller than about 150 microns.

[0005] The prior art fails to provide a cost-effective, expedient and reliable method of providing a multilayer substrate core structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figs 1-8 show stages of forming a substrate core structure according to the prior art;

[0007] Figs. 9a-9f show stages of forming a multilayer substrate core structure according to a first embodiment;

[0008] Figs. 10a-10f show stages of forming a multilayer substrate core structure according to a second embodiment;

[0009] Figs. 11a-11g show stages of forming a multilayer substrate core structure according to a third embodiment;

[0010] Fig. 12 is a schematic view of an embodiment of a system incorporating a multilayer substrate core structure as shown in either of Figs. 9f, 10f or 11g.

[0011] For simplicity and clarity of illustration, elements in the drawings have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Where considered appropriate, reference numerals have been repeated among the drawings to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

[0012] In the following detailed description, a method of fabricating a substrate core structure, such as a substrate core structure, a substrate core structure formed according to the method, and a system including the substrate core structure, are disclosed. Reference is made to the accompanying drawings within which are shown, by way of illustration, specific embodiments by which the present invention may be practiced. It is to be understood that other embodiments may exist and that other structural changes may be made without departing from the scope and spirit of the present invention.

[0013] The terms on, onto above, below, and adjacent as used herein refer to the position of one element relative to other elements. As such, a first element disposed on, onto, above, or below a second element may be directly in contact with the second element or it may include one or more intervening elements. In addition, a first element disposed next to or adjacent a second element may be directly in contact with the second element or it may include one or more intervening elements. In addition, in the instant description, figures and/or elements may be referred to in the alternative. In such a case, for example where the description refers to Figs. X/Y showing an element A/B, what is meant is that Fig. X shows element A and Fig. Y shows element B. In addition, a "layer" as used herein may refer to a layer made of a single material, a layer made of a mixture of different components, a layer made of various sub-layers, each sub-layer also having the same definition of layer as set forth above.

[0014] Aspects of this and other embodiments will be discussed herein with respect to Figs. 9a-12 below. Figs. 9a-9f show stages for the fabrication of a multilayer substrate core structure according to a first method embodiment involving the lamination of a single sided copper clad core onto a patterned starting insulating layer followed by laser through-via drilling and subtractive patterning. Figs. 10a-10f show stages for the fabrication of a multilayer substrate core structure according to a

second method embodiment involving the lamination of two single sided copper clad cores onto a patterned starting insulating layer followed by laser through via drilling and subtractive patterning. Figs. 11a-11g show stages for the fabrication of a multilayer substrate core structure according to a third embodiment involving the use of via plugging and semi-additive patterning. Fig. 12 shows a system incorporating a multilayer substrate core structure according to an embodiment. The figures, however, should not be taken to be limiting, as are intended for the purpose of explanation and understanding.

[0015] Referring to Figs. 9a, 10a and 11a, method embodiments include providing a starting insulating layer 10. The starting insulating layer may include any one of well known core insulating/dielectric materials, such as, for example, glass epoxy resin or bismaleimide-triazine (BT), or ABF. Preferably, the starting insulating layer comprises a fiber reinforced glass epoxy resin. According to one embodiment, as shown in Figs. 9a, 10a, and 11a, the starting insulating layer 10 may include initial conductive layers 12 and 13 thereon, such as conductive layers made of copper. In the shown embodiments of Figs. 9a, 10a, and 11a, the starting insulating layer 10 may be part of a conventional copper clad core or CCL 14.

[0016] Referring next to Figs. 9b, 10b and 11b, method embodiments include providing a first patterned conductive layer 19 on one side of the starting insulating layer 10, and a second patterned conductive layer 20 on another side of the starting insulating layer 10. For all three embodiments shown, providing the first/second patterned conductive layer may include patterning the initial conductive layer 12/13 by way of etching. Embodiments, however, are not limited to the provision of first/second patterned conductive layers by way of subtractive patterning, and include within their scope the provision of patterned conductive layers in any one of well known manners, such as, for example, by way of semi-additive patterning. According to embodiments, each of the first patterned conductive layer 19 and the second patterned conductive layer 20 define conductive layer openings 38 therein as a result of the patterning process.

[0017] Referring next to Figs. 9c, 10c and 11c, method embodiments include providing a first supplemental insulating layer 26 onto the first patterned conductive layer 19, and a second supplemental insulating layer 28 onto the second patterned conductive layer 20 as shown. A supplemental insulating layer according to

embodiments may include the same material as the one used for the starting insulating layer as noted above. According to an embodiment, provision of a supplemental insulating layer may include laminating the supplemental insulating layer onto a corresponding patterned conductive layer. In the embodiment of Fig. 9c, the first supplemental insulating layer 26 may be laminated onto the first patterned conductive layer 19 along with a first supplemental conductive layer 40 disposed on one side of the first supplemental insulating layer 26. For example, according to the first embodiment, a combination of the first supplemental insulating layer 26 and the first supplemental conductive layer 40 may comprise a single sided copper clad core 42. The single sided copper clad core 42 is shown in the embodiment of Fig. 9c as being provided onto the first patterned conductive layer 19 such that the supplemental insulating layer 26 is disposed between the first patterned conductive layer 19 and the first supplemental conductive layer 40 as shown. A thickness range of the conductive layer 40 may be between about 10 microns and about 50 microns. In the embodiment of Fig. 10c, the first/second supplemental insulating layer 26/28 may be laminated onto the first/second patterned conductive layer 19/20 along with a first/second supplemental conductive layer 40/44 disposed on one side of the first/second supplemental insulating layer 26/28. The first/second supplemental insulating layers 26/28 are shown in the embodiment of Fig. 10c as being provided onto the first patterned conductive layer 19/20 such that the supplemental insulating layer 26/28 is disposed between the first/second patterned conductive layer 19/20 and the first/second supplemental conductive layer 40/44 as shown. The first/second supplemental conductive layers 40/44 may include thin conductive layers such as thin copper (having a thickness of less than about 10 microns, and preferably less than about 5 microns. In the embodiment of Fig. 11c, on the other hand, the first and second supplemental insulating layers 26 and 28 are shown as having been provided onto the starting layer 14 without any conductive layers being provided thereon.

[0018] Referring next to Figs. 9d, 10d and 11d, embodiments include laser drilling a set of through via openings 46 extending from a side of the second supplemental insulating layer 28 farthest from the second patterned conductive layer 20, up to a side of the first supplemental insulating layer 26 farthest from the first patterned conductive layer 19, such that the via openings 46 extend through at least

some of the conductive layer openings 38 of the first patterned conductive layer 19 and of the second patterned conductive layer 20. It is clear from Figs. 9d, 10d and 11d that, by pre-patterning the first and second conductive layers 12 and 13 (Figs. 9a, 10a and 11a) prior to laser drilling, the necessity to drill through layers of conductive material while providing the through via openings 46 is advantageously obviated. Although laser drilling of some of the material of the patterned conductive layers 19 and 20 may take place during laser drilling of the via openings, especially at the edges of some of the openings 38, in order to accommodate a possibly larger size of the via openings 46 than a size of the conductive layer openings 38 accommodating the via openings 46, such drilling would be minimal compared to a laser drilling that would have to take place if the conductive layers 12 and 13 (Figs. 9a, 10a and 11a) were not pre-patterning. For laser drilling, a carbon dioxide gas laser beam, an ultraviolet laser beam or an excimer laser beam may be used. Referring now still to Fig. 9d, the shown method embodiment involves laser drilling the via openings such that the openings extend to the first supplemental conductive layer 40. Referring next to Fig. 10d, the shown method embodiment involves laser drilling the via openings such that the openings extend through the second supplemental conductive layer 44 to the first supplemental conductive layer 40. Referring finally to Fig. 11d, the shown method embodiment involves laser drilling the via openings such that the openings extend through the second supplemental insulating layer 26, the conductive layer openings 38, the starting insulating layer 10, and the first supplemental insulating layer 28 as shown. According to embodiments, the laser drilling of via openings results in laser drilled via openings which may exhibit, as shown in Figs. 9f, 10f and 11g, a conical configuration.

[0019] Referring next to Figs. 9e, 10e and 11e, embodiments include filling the set of via openings 46 with a conductive material 16 to provide a set of conductive vias 18 as shown. Preferably, the conductive material 16 includes copper, but it may also include other conductive materials as would be within the knowledge of one skilled in the art. In the embodiments of Figs. 9e and 10e, filling the conductive vias may include plating, such as copper plating. For the embodiment of Fig. 9e, after filling of the via openings 46, for example by way of plating, filling the via openings 46 may involve providing a second supplemental conductive layer 48 on one side of the second supplemental insulating layer 28. For the embodiment of Fig. 10e, after

filling the via openings 46, for example by way of plating, filling the via openings 46 may involve plating first and second extra conductive layers 50 and 52 onto respective ones of the first and second supplemental conductive layer 40 and 44. The additional plated conductive layers 48 in Fig. 9e and 50 and 52 in Fig. 10e may later be patterned as will be described in further detail in relation to Figs. 9f and 10f, respectively. Referring next to the embodiment of Fig. 11e, filling the via openings 46 may involve first plating the via openings 46 and the exposed surfaces of the first and second supplemental insulating layers 26 and 28 to achieve plating layers 54 on the walls of the via openings 46 and on the exposed surfaces of the first and second supplemental insulating layers 26 and 28 as shown. Referring still to the embodiment of Fig. 11e, filling the set of via openings 46 may further include plugging the via openings with a plugging material 60 in a well known manner after providing the plating layers 54 to provide plated plugged conductive vias 18 as shown.

[0020] Referring next to Figs. 9f, 10f and 11f-g, embodiments include providing a first supplemental patterned conductive layer 56 onto the first supplemental insulating layer 26, and a second supplemental patterned conductive layer 58 onto the second supplemental insulating layer 28 such that the set of conductive vias 18 contacts the first supplemental patterned conductive layer 56 at one side thereof, and the second supplemental patterned conductive layer 58 at another side thereof. According to the embodiment of Fig. 9f, the shown method may involve patterning the first supplemental conductive layer 40 and the second supplemental conductive layer 44 of Fig. 9e, such as, for example, by way of subtractive patterning involving, for example, etching, to yield the first supplemental patterned conductive layer 56 and the second supplemental patterned conductive layer 58. According to the embodiment of Fig. 10f, the shown method may involve patterning a combination of the first supplemental conductive layer 40 and the first extra conductive layer 50 by way of subtractive patterning involving, for example, etching, to yield the first supplemental patterned conductive layer 56. The embodiment of Fig. 10f may further involve patterning a combination of the second supplemental conductive layer 44 and the second extra conductive layer 52 by way of subtractive patterning involving, for example, etching, to yield the second supplemental patterned conductive layer 58. For the embodiment of Figs. 11f-g, on the other hand, providing

the first and second supplemental patterned conductive layers 56 and 58 may include using semi-additive patterning onto the plating layers 54 present on respective ones of the first and second supplemental insulating layers. A semi-additive process is a well known process according to which, for example, a photoresist may be deposited on the plating layer 54, which photoresist may then be exposed to light and developed, whereby a resist pattern may be formed while leaving, on the plating layers 54, a non-mask region corresponding to the pattern of the first and/or second supplemental patterned conductive layer. By means of electroplating, the plating layer may be used as a seed layer to stack an electroplated film in the non-mask regions. The resist pattern may then be removed by etching, and thereafter the electroless plating film which was till then covered with the resist pattern, may be removed by etching. In this way, the first and second supplemental patterned conductive layers 56 and 58 may be formed according to the third embodiment as shown in Fig. 11g.

[0021] Embodiments as shown by way of example with respect to Figs. 9a-9f, 10a-10f or 11a-11g, may respectively yield a multilayer substrate core structure 100 as shown in Fig. 9f, a multilayer substrate core structure 200 as shown in Fig. 10f, and a multilayer substrate core structure 300 as shown in Fig. 11g. Boards 100/200/300 each include the starting insulating layer 10, first patterned conductive layer 19 on one side of the starting insulating layer 10, and second patterned conductive layer on another side of the starting insulating layer 10. The boards 100/200/300 additionally include: first and second supplemental insulating layers 26 and 28 disposed, respectively, on the first and second patterned conductive layer 19 and 20; first and second supplemental patterned conductive layers 56 and 58 disposed, respectively, on the first and second supplemental insulating layers 26 and 28; and a set of conductive through vias 18 provided in corresponding laser-drilled via openings extending from the second supplemental patterned conductive layer 58 to the first supplemental patterned conductive layer 56, the via openings extending through the first patterned conductive layer 19 and the second patterned conductive layer 20 as shown. According to some embodiments, the set of conductive vias 18 may include a plated conductive material therein. According to one embodiment as shown in Fig. 11g, the set of conductive vias 18 may include a plugging material 60

therein. According to some embodiments, the set of conductive vias may include a skip via, such as skip via 64 of Figs. 9f/10f/11g, and/or a padless via (not shown).

[0022] Although the substrate core structure structures shown in Figs. 9f, 10f and 11g, respectively, show only two supplemental insulating layers, two conductive vias and four sets of patterned conductive layers, embodiments are not so limited, and include within their ambit the provision of as many supplemental insulating layers, conductive vias, and patterned conductive layers as necessary in order to arrive at a desired substrate core structure structure. The provision of the various additional elements noted above, including the supplemental insulating layers, conductive vias, and sets of patterned conductive layers may be effected as noted above either with respect to the first embodiment as shown in Figs. 9a-9f, with respect to the second embodiment as shown in Figs. 10a-10f, or with respect to the third embodiment as shown in Figs. 11a-11g.

[0023] Advantageously, embodiments provide a method to enable building multilayer substrate core structures by way of laser drilled through via openings using pre-patterned conductive build-up layers on the starting insulating layer of the board. Embodiments address a new multilayer substrate core structures and a method of building the same in which the costly plated through hole structure is replaced with the low cost laser drilled microvias. Embodiments effectively address among other things the problems of: (1) high cost prior art substrate core structures which use mechanical drilling technology by replacing the costly mechanically drilled plated through holes with low cost laser drilled microvias; (2) the need to laser drill through conductive layers such as copper by achieving low cost, shorter processing times, and high reliability of a laser drilled via core structure that obviates the need to laser drill through a thickness of the conductive layers. An embodiment provides a lower cost method of fabrication than prior art methods by not only replacing the prior art plated through hole regime with laser drilled through microvias, but also by reducing the core dielectric material thickness (by virtue of the generally reduced via dimensions and line and space features possible according to embodiments). In addition, laser drilling according to embodiments allows for higher starting insulating layer connection density as compared with prior art structures, owing to small via sizes and pitches, thus allowing for smaller sized vias and smaller pitches, in this way leading to an improved design and to scalable miniaturization at low cost.

Laser drilling according to embodiments features high alignment accuracy and through-put (up to about 1000 vias/sec), a wide range of possible via sizes, and low cost (about 2 cents per about 60 to about 100 vias). The combination of high alignment accuracy and small via size make possible, for example for a four layer core structure, via diameters of about 50 microns at the bottom and of about 140 microns at the top, pad sizes of about 170 microns at the top and about 100 microns at the bottom, which sizes are much less than typical plated through hole sizes including diameters of about 250 microns and pad sizes of about 400 microns. Pitches according to embodiments may further be much less than typical through hole pitches of about 475 microns. Moreover, embodiments lead to substrate core structure substrate structures having potentially smaller form factors (by virtue of potentially smaller pitches, pad sizes, via dimensions), and a potentially smaller z-height (by virtue of potentially finer routing through the thickness of the insulating layers, which may lead to thinner insulating layers and/or the use of a smaller amount of insulating layers). Additionally, embodiments advantageously allow the provision of a padless via structure in the core layers. Embodiments further allow conductive material, such as copper, pre-patterning in the inner core layers to accommodate for lamination and cladding accuracy and enable skip via connection. This is because, according to embodiments, the via openings in different metal layers are formed simultaneously.

[0024] Referring to Fig. 12, there is illustrated one of many possible systems 900 in which embodiments of the present invention may be used. In one embodiment, the electronic assembly 1000 may include a substrate core structure structure, such as structure 100 of Fig. 9f or structure 200 of Fig. 10f or structure 300 of Fig. 11g. Assembly 1000 may further include a microprocessor. In an alternate embodiment, the electronic assembly 1000 may include an application specific IC (ASIC). Integrated circuits found in chipsets (e.g., graphics, sound, and control chipsets) may also be packaged in accordance with embodiments of this invention.

[0025] For the embodiment depicted by Fig. 12, the system 900 may also include a main memory 1002, a graphics processor 1004, a mass storage device 1006, and/or an input/output module 1008 coupled to each other by way of a bus 1010, as shown. Examples of the memory 1002 include but are not limited to static random access memory (SRAM) and dynamic random access memory (DRAM).

Examples of the mass storage device 1006 include but are not limited to a hard disk drive, a compact disk drive (CD), a digital versatile disk drive (DVD), and so forth.

Examples of the input/output module 1008 include but are not limited to a keyboard, cursor control arrangements, a display, a network interface, and so forth. Examples of the bus 1010 include but are not limited to a peripheral control interface (PCI) bus, and Industry Standard Architecture (ISA) bus, and so forth. In various embodiments, the system 90 may be a wireless mobile phone, a personal digital assistant, a pocket PC, a tablet PC, a notebook PC, a desktop computer, a set-top box, a media-center PC, a DVD player, and a server.

[0026] The various embodiments described above have been presented by way of example and not by way of limitation. Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many variations thereof are possible without departing from the spirit or scope thereof.

WHAT IS CLAIMED IS:

1. A method of fabricating a substrate core structure comprising:
 - providing a starting insulating layer;
 - providing a first patterned conductive layer on one side of the starting insulating layer, and a second patterned conductive layer on another side of the starting insulating layer, each of the first patterned conductive layer and the second patterned conductive layer defining conductive layer openings therein;
 - providing a supplemental insulating layer onto the first patterned conductive layer, and a second supplemental insulating layer onto the second patterned conductive layer;
 - laser drilling a set of via openings extending from a side of the second supplemental insulating layer farthest from the second patterned conductive layer to a side of the first supplemental insulating layer farthest from the first patterned conductive layer such that the via openings extend through at least some of the conductive layer openings of the first patterned conductive layer and the second patterned conductive layer ;
 - filling the set of via openings with a conductive material to provide a set of conductive vias;
 - providing a first supplemental patterned conductive layer onto the first supplemental insulating layer and a second supplemental patterned conductive layer onto the second supplemental insulating layer, the set of conductive vias contacting the first supplemental patterned conductive layer at one side thereof, and the second supplemental patterned conductive layer at another side thereof.
2. The method of claim 1, wherein filling the set of via openings includes plating.
3. The method of claim 2, wherein filling the set of via openings further includes plugging after plating such that the set of conductive vias includes plated plugged conductive vias.
4. The method of claim 1, wherein the starting insulating layer and the supplemental insulating layer each comprise at least one of a glass epoxy resin and bismaleimide-triazine (BT).
5. The method of claim 1, wherein providing the first patterned conductive layer and the second patterned conductive layer includes:

providing, respectively, a first initial conductive layer on one side of the starting insulating layer and a second initial conductive layer on an opposite side of the starting insulating layer to yield a core layer; and

patterning respective ones of the first initial conductive layer and the second initial conductive layer to yield the first and second patterned conductive layers.

6. The method of claim 1, wherein providing the first supplemental insulating layer and the second supplemental insulating layer includes laminating.

7. The method of claim 1, wherein providing the first supplemental patterned conductive layer includes:

providing a first supplemental conductive layer on one side of the first supplemental insulating layer prior to providing the first supplemental insulating layer onto the first patterned conductive layer, such that, after providing the first supplemental insulating layer onto the first patterned conductive layer, the first supplemental insulating layer is disposed between the first patterned conductive layer and the first supplemental conductive layer, the set of via openings extending to the first supplemental conductive layer.

8 The method of claim 7, wherein:

providing the first supplemental patterned conductive layer includes patterning the first supplemental conductive layer to yield the first supplemental patterned conductive layer; and

providing the second supplemental patterned conductive layer includes:

providing an second supplemental conductive layer on one side of the second supplemental insulating layer after filling the set of via openings; and

patterning the second supplemental conductive layer to yield the second supplemental patterned conductive layer.

9. The method of claim 7, wherein providing the second supplemental patterned conductive layer includes providing an second supplemental conductive layer on one side of the second supplemental insulating layer prior to providing the second supplemental insulating layer onto the second patterned conductive layer, such that, after providing the second supplemental insulating layer onto the second patterned conductive layer, the second supplemental insulating layer is disposed between the second patterned conductive layer and the second supplemental conductive layer,

the set of via openings extending through the second supplemental conductive layer to the first supplemental conductive layer.

10. The method of claim 9, wherein the first supplemental conductive layer and the second supplemental conductive layer have a thickness below about 2 microns.

11. The method of claim 9, wherein:

providing the first supplemental patterned conductive layer includes:

plating a first extra conductive layer onto the first supplemental conductive layer; and

patterning a combination of the first supplemental conductive layer and the first extra conductive layer to yield the first supplemental patterned conductive layer; and

providing the second supplemental patterned conductive layer includes:

plating a second extra conductive layer onto the second supplemental conductive layer; and

patterning a combination of the second supplemental conductive layer and the second extra conductive layer to yield the second supplemental patterned conductive layer.

12. The method of claim 3, wherein:

plating includes providing plating layers to cover walls of the set of via openings and exposed surfaces of respective ones of the first supplemental insulating layer and second supplemental insulating layer; and

providing the first supplemental patterned conductive layer and the second supplemental patterned conductive layer includes using semi-additive patterning onto plating layers disposed on respective ones of the first supplemental insulating layer and the second supplemental insulating layer.

13. The method of claim 5, wherein the core layer is a double-sided copper clad core.

14. A multilayer substrate core structure including:

a starting insulating layer;

a first patterned conductive layer on one side of the starting insulating layer, and a second patterned conductive layer on another side of the starting insulating layer;

a first supplemental insulating layer on the first patterned conductive layer;

a second supplemental insulating layer on the second patterned conductive layer;

a first supplemental patterned conductive layer on the first supplemental insulating layer;

a second supplemental patterned conductive layer on the second supplemental insulating layer;

a set of conductive vias provided in corresponding laser-drilled via openings extending from the second supplemental patterned conductive layer to the first supplemental patterned conductive layer, the via openings further extending through the first patterned conductive layer and the second patterned conductive layer.

15. The substrate core structure of claim 14, wherein the set of conductive vias include a plated conductive material therein.

16. The substrate core structure of claim 14, wherein the set of conductive vias include a plugging material therein.

17. The substrate core structure of claim 14, wherein the set of conductive vias includes a skip via.

18. The substrate core structure of claim 14, wherein the set of conductive vias includes a padless via.

19. The substrate core structure of claim 14, wherein the starting insulating layer and the supplemental insulating layer each comprise at least one of a glass epoxy resin and bismaleimide-triazine (BT).

20. A system comprising:

an electronic assembly including:

a multilayer substrate core structure including:

a starting insulating layer;

a first patterned conductive layer on one side of the starting insulating layer, and a second patterned conductive layer on another side of the starting insulating layer;

a first supplemental insulating layer on the first patterned conductive layer;

a second supplemental insulating layer on the second patterned conductive layer;

a first supplemental patterned conductive layer on the first supplemental insulating layer;

a second supplemental patterned conductive layer on the second supplemental insulating layer;

a set of conductive vias provided in corresponding laser-drilled via openings extending from the second supplemental patterned conductive layer to the first supplemental patterned conductive layer, the via openings further extending through the first patterned conductive layer and the second patterned conductive layer; and

a main memory coupled to the electronic assembly.

21. The system of claim 20, wherein the set of conductive vias include an plated conductive material therein.

22. The system of claim 20, wherein the set of conductive vias include a plugging material therein.

23. The system of claim 20, wherein the set of conductive vias includes a skip via.

24. The system of claim 20, wherein the set of conductive vias includes a padless via extending through the starting insulating layer.

25. The system of claim 20, wherein the starting insulating layer and the supplemental insulating layer each comprise at least one of a glass epoxy resin and bismaleimide-triazine (BT).

26. A method of fabricating a substrate core structure comprising:

providing a starting insulating layer;

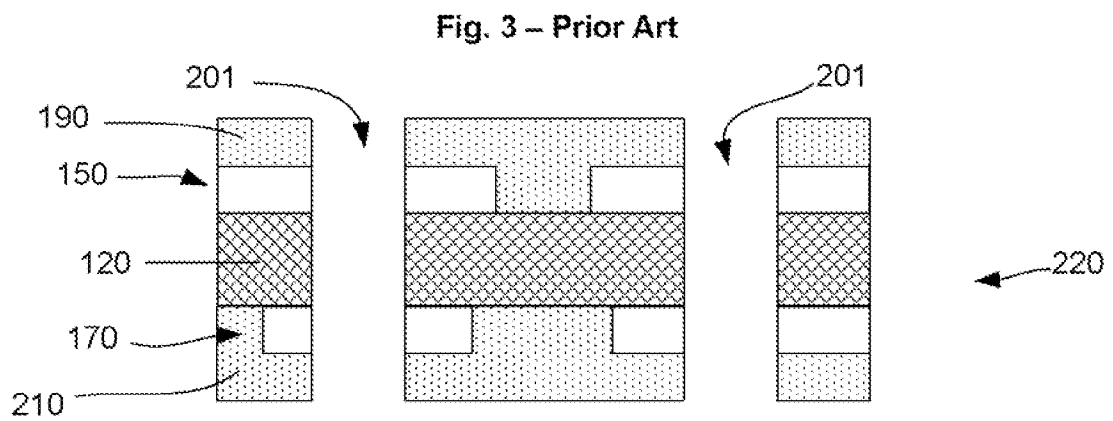
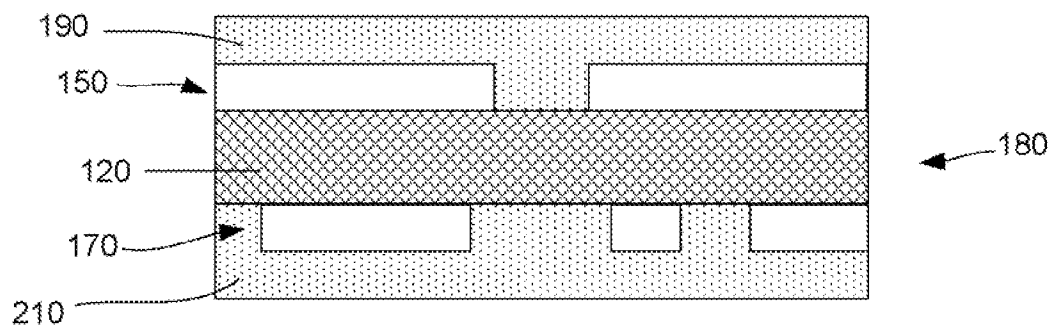
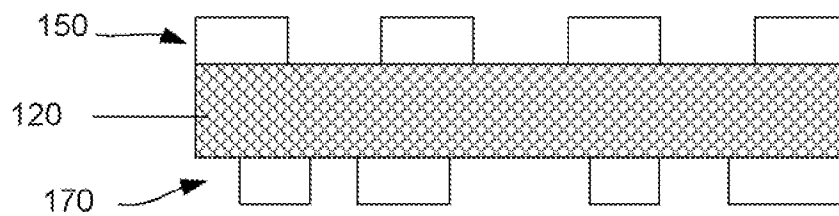
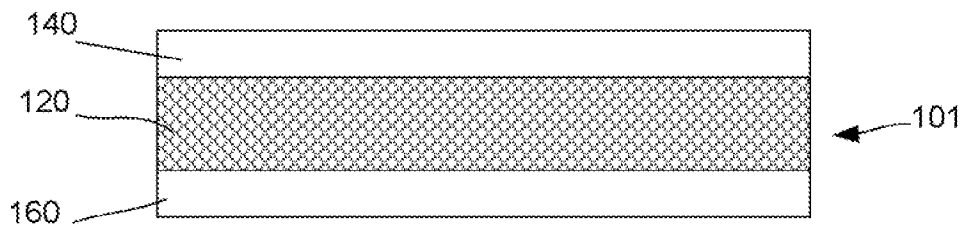
providing a patterned conductive layer on one side of the starting insulating layer, the first patterned conductive layer defining conductive layer openings therein;

providing a supplemental insulating layer onto the first patterned conductive layer;

laser drilling a set of via openings extending from a side of the supplemental insulating layer farthest from the patterned conductive layer to a side of the starting insulating layer farthest from the patterned conductive layer such that the via openings extend through at least some of the conductive layer openings of the patterned conductive layer;

filling the set of via openings with a conductive material to provide a set of conductive vias,

27. The method of claim 26, wherein the set of via openings includes a padless via.
28. The method of claim 26, wherein the set of via openings includes a skip via.
29. The method of claim 1, wherein filling the set of via openings includes plating.
30. The method of claim 2, wherein filling the set of via openings further includes plugging after plating such that the set of conductive vias includes plated plugged conductive vias.



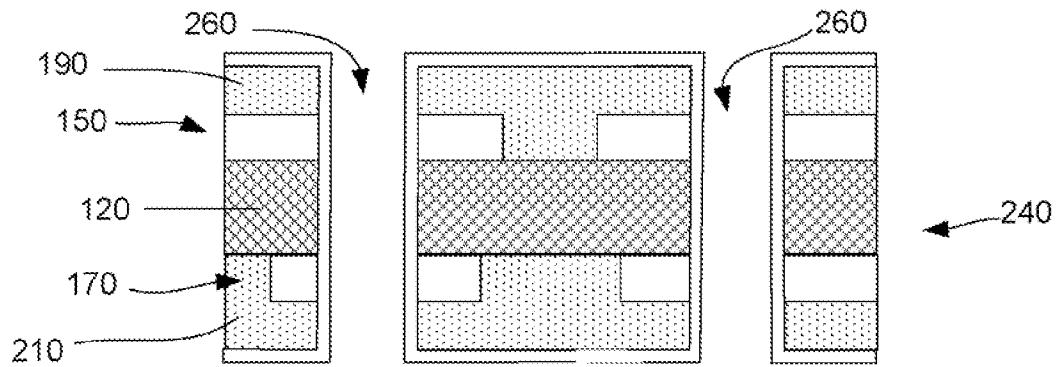


Fig. 5 - Prior Art

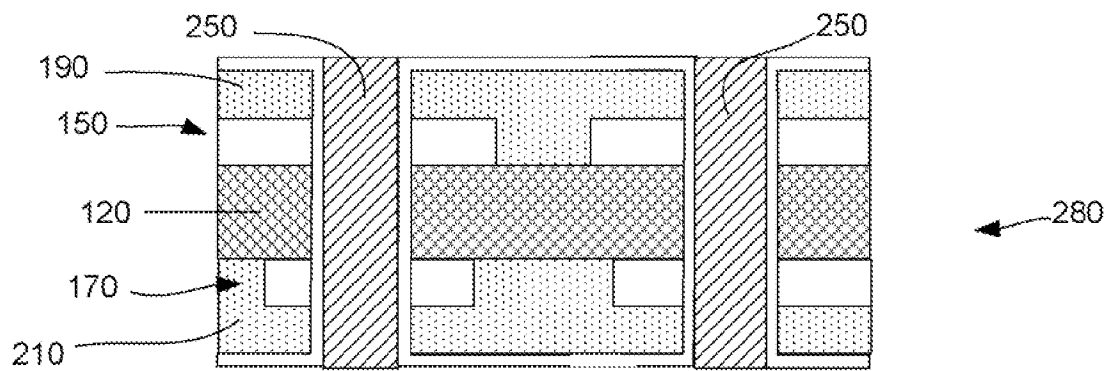


Fig. 6 - Prior Art

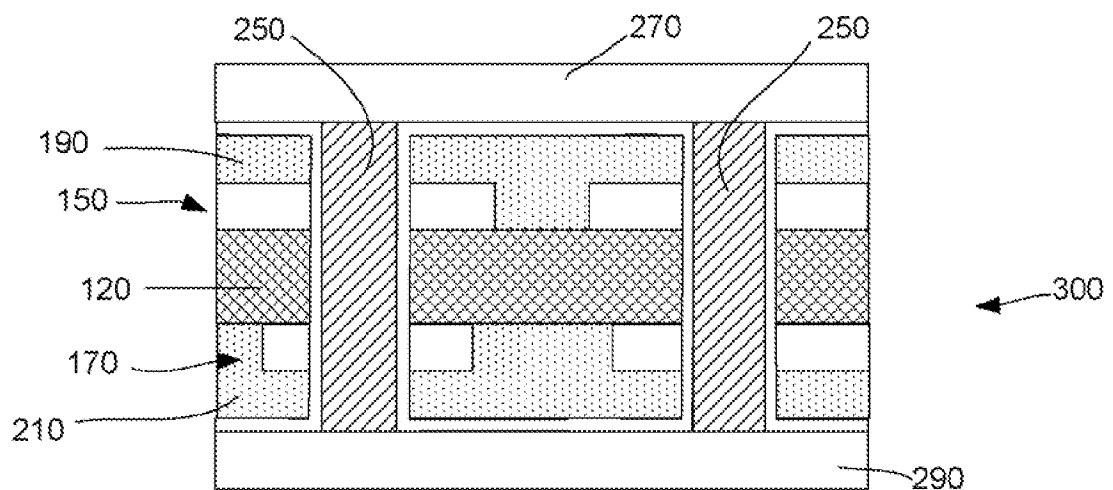


Fig. 7 - Prior Art

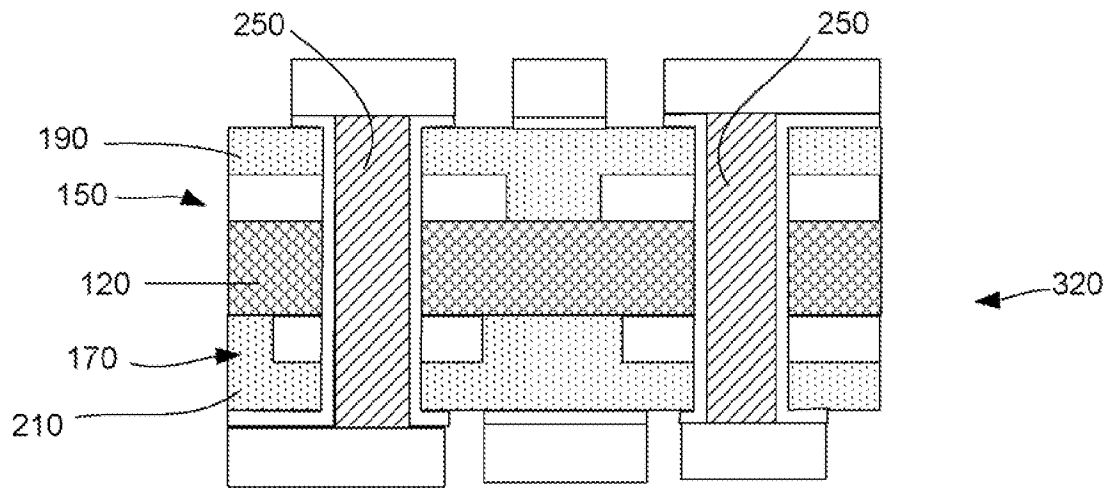


Fig. 8 – Prior Art

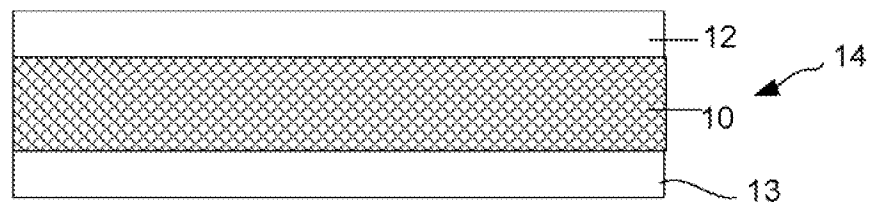


Fig. 9a

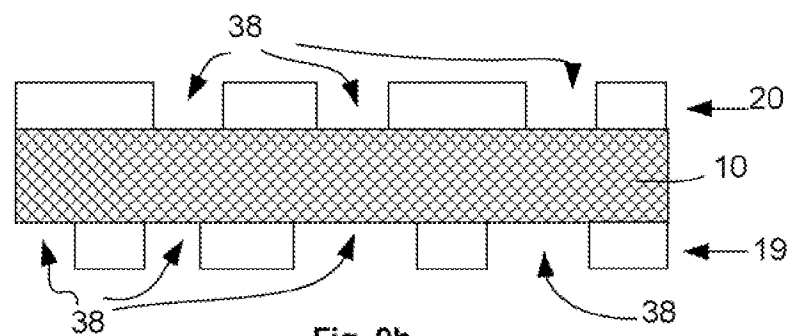
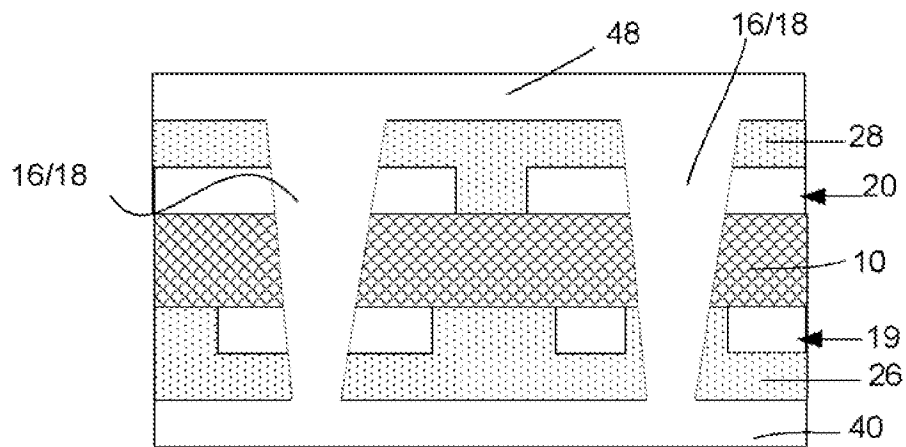
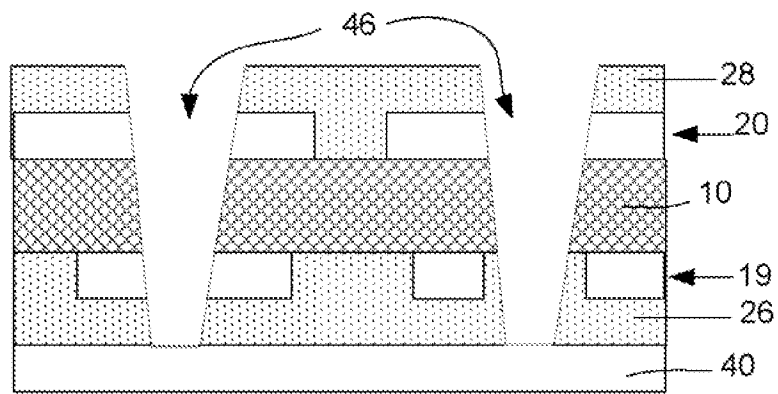
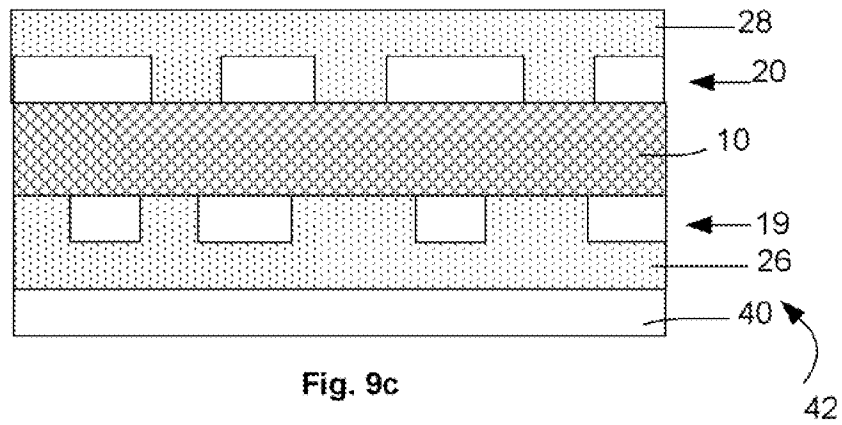


Fig. 9b



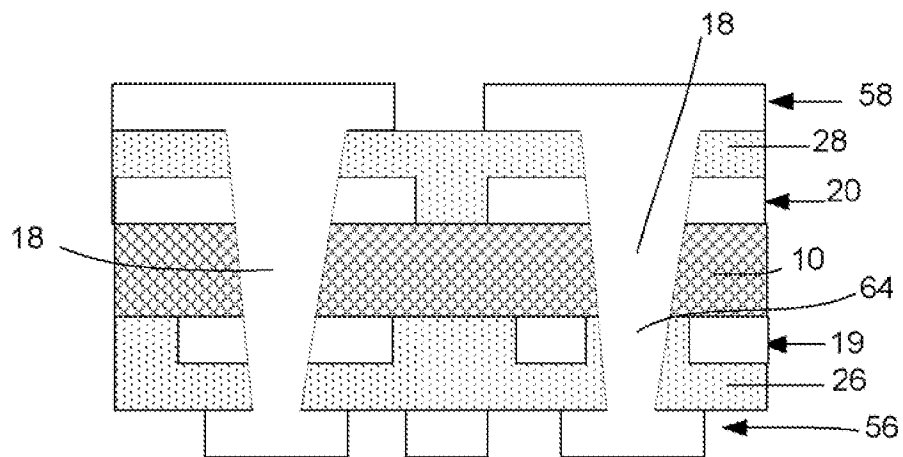


Fig. 9f

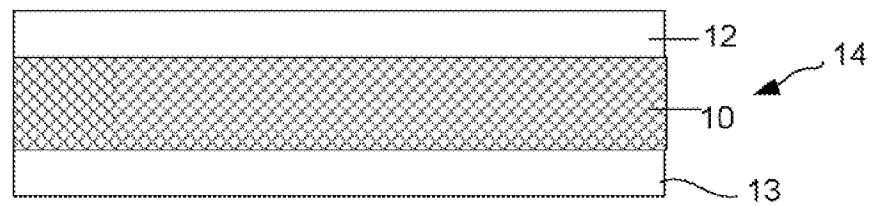


Fig. 10a

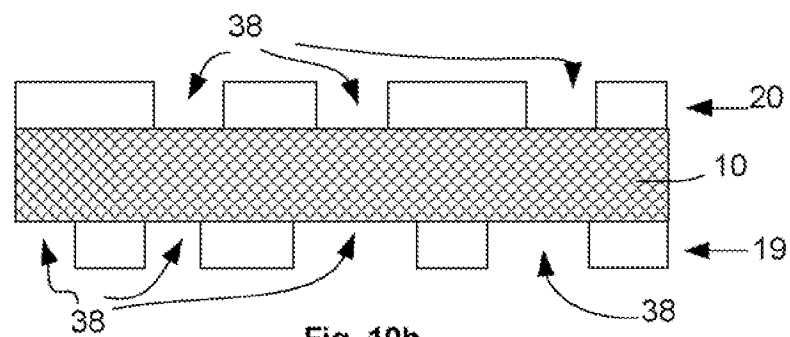


Fig. 10b

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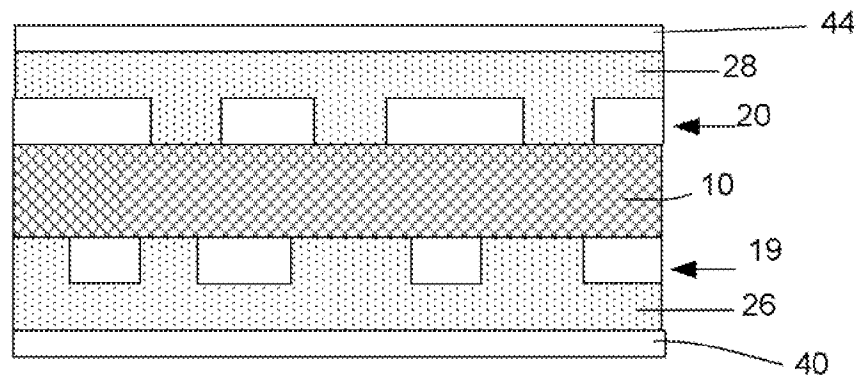


Fig. 10c

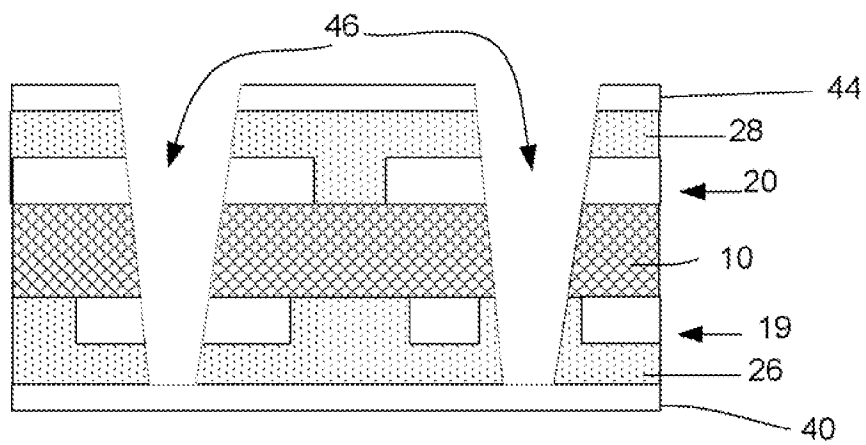


Fig. 10d

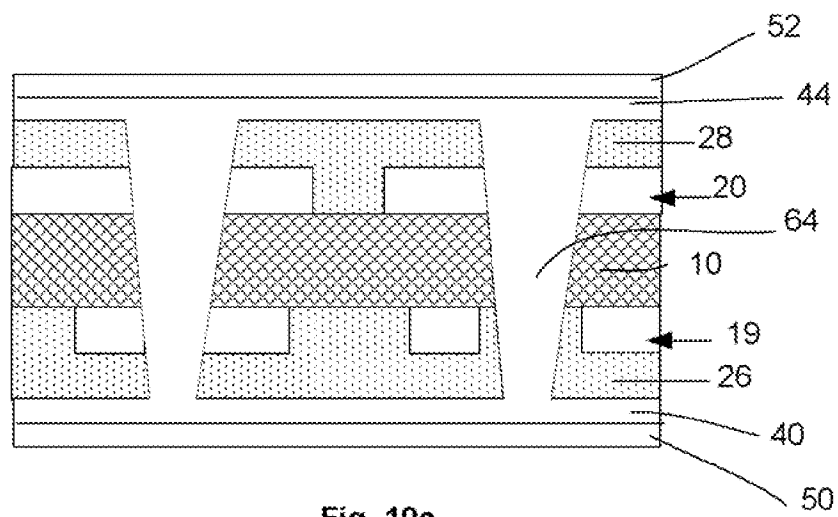


Fig. 10e

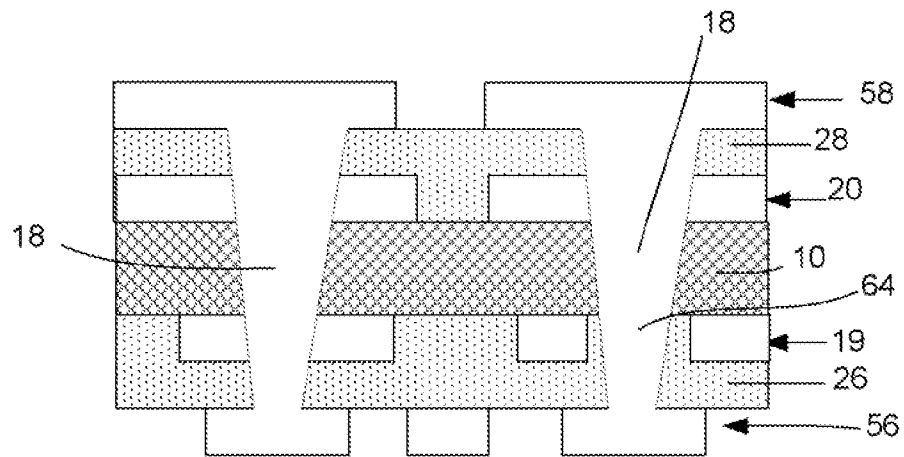


Fig. 10f

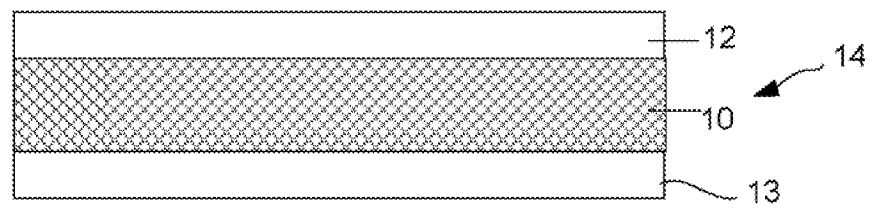


Fig. 11a

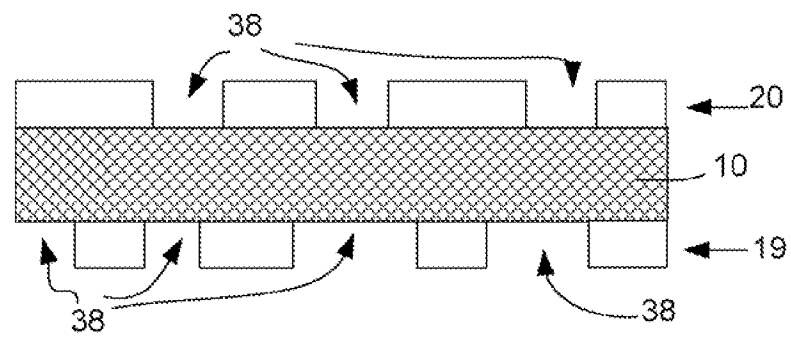


Fig. 11b

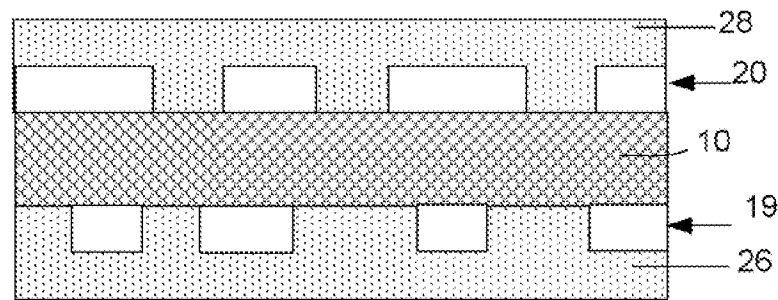


Fig. 11c

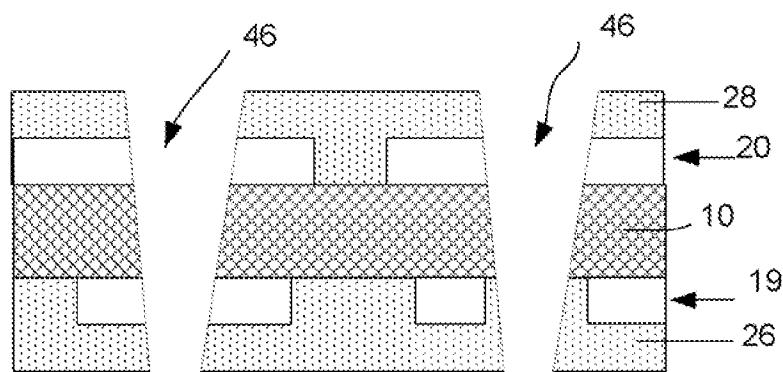


Fig. 11d

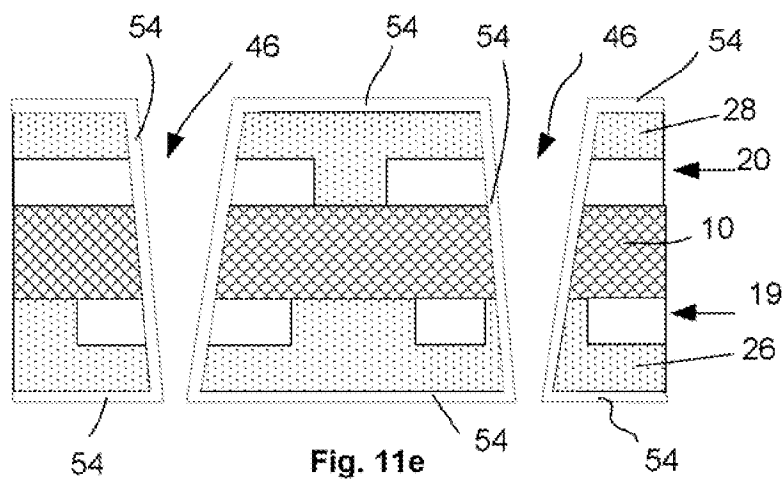


Fig. 11e

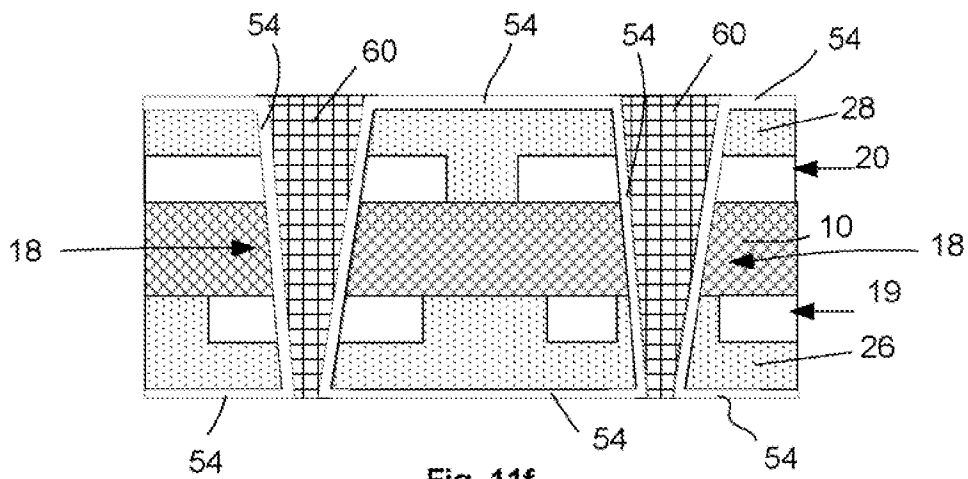


Fig. 11f

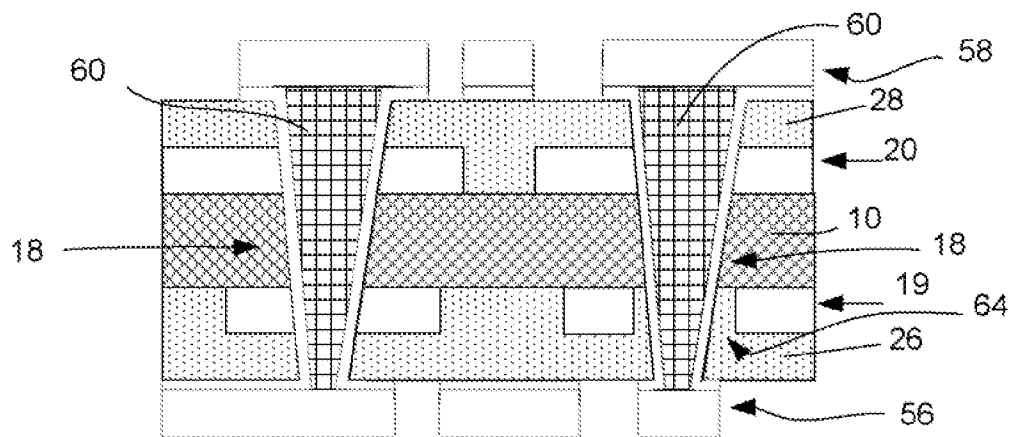


Fig. 11g

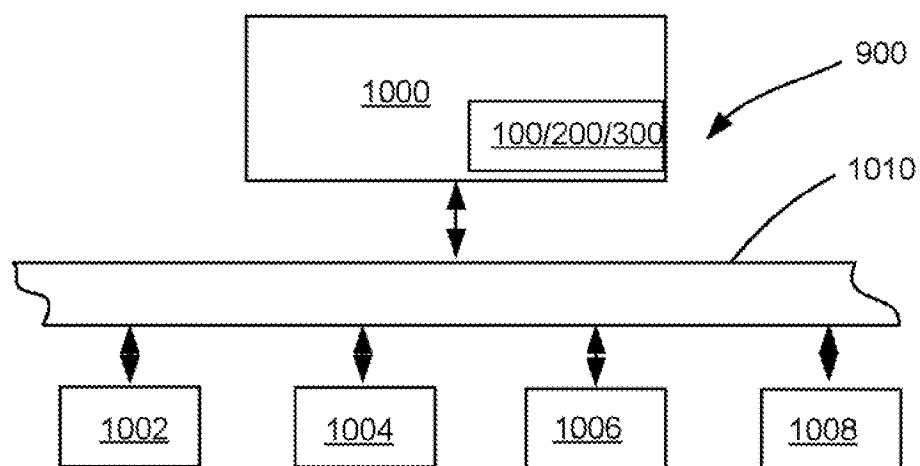


Fig. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/068111**A. CLASSIFICATION OF SUBJECT MATTER****H05K 3/46(2006.01)i, H05K 3/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) & Keyword: "via, multilayer, paste"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2005-005417 A (SHINKO SEISAKUSHO:KK) 06 January 2005 See the Abstract and Figs. 1,3	1,4-11,13-14,16-20, 22-28
Y		2-3,12,15,21,29-30
Y	KR10-2007-0034766 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 29 March 2007 See the Abstract	2-3,12,15,21,29-30



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 SEPTEMBER 2008 (26.09.2008)

Date of mailing of the international search report

26 SEPTEMBER 2008 (26.09.2008)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
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gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Jong Hee

Telephone No. 82-42-481-8500



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/068111

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2005-005417 A	06.01.2005	JP 2005-005417 A2	06.01.2005
=====	=====	=====	=====
KR 10-2007-0034766 A	29 03 2007	None	
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