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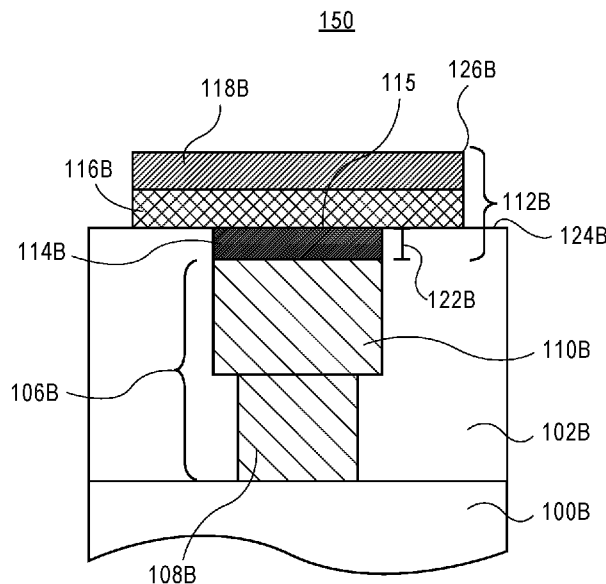


FIG. 1B

(57) Abstract: Approaches for fabricating self-aligned pedestals for resistive random access memory (RRAM) elements and devices, and the resulting structures, are described. In an example, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the conductive interconnect and in the ILD layer. The first electrode layer has an uppermost surface substantially co-planar with an uppermost surface of the ILD layer. A resistance switching layer is disposed on the uppermost surface of the first electrode layer and on a portion of the uppermost surface of the ILD layer. A second electrode layer is disposed on the resistance switching layer.



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**APPROACHES FOR FABRICATING SELF-ALIGNED PEDESTALS FOR RRAM DEVICES AND
THE RESULTING STRUCTURES**

TECHNICAL FIELD

5 Embodiments of the invention are in the field of integrated circuit fabrication and, in particular, approaches for fabricating self-aligned pedestals for resistive random access memory (RRAM) elements and devices, and the resulting structures.

BACKGROUND

10 For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory devices on a chip, lending to the fabrication of products with
15 increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

 Embedded SRAM and DRAM have problems with non-volatility and soft error rates, while embedded FLASH memories require additional masking layers or processing steps during manufacture, require high-voltage for programming, and have issues with endurance and
20 reliability. Nonvolatile memory based on resistance change is known as RRAM or ReRAM. Although commonly anticipated as a replacement technology for flash memory, the cost benefit and performance benefit of RRAM have not been obvious enough to most companies to proceed with the replacement. Also, for low voltage non-volatile embedded applications, operating voltages less than 1V and compatible with CMOS logic processes may be desirable but
25 challenging to achieve.

 Thus, significant improvements are still needed in the area of nonvolatile memory device manufacture and operation. In particular, significant improvements are still needed in the area of non-volatile memory arrays and their integration with logic processors.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a cross-sectional view of a resistive random access memory (RRAM) element.

5 Figure 1B illustrates a cross-sectional view of an RRAM element, in accordance with an embodiment of the present invention.

Figure 2 illustrates cross-sectional views of various operations in a method of fabricating an RRAM element, in accordance with an embodiment of the present invention.

10 Figure 3A illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, in accordance with an embodiment of the present invention.

Figure 3B illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, in accordance with an embodiment of the present invention.

Figure 4A illustrates a cross-sectional view of an RRAM element having an electrode on a recessed conductive line or via, in accordance with an embodiment of the present invention.

15 Figure 4B illustrates a cross-sectional view of another RRAM element having an electrode on a recessed conductive line or via, in accordance with another embodiment of the present invention.

Figure 4C illustrates a cross-sectional view of an RRAM element having damascene portions, in accordance with another embodiment of the present invention.

20 Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector, in accordance with an embodiment of the present invention.

Figure 6 illustrates schematic views of several options for positioning an RRAM element in an integrated circuit, in accordance with an embodiment of the present invention.

25 Figures 7A and 7B illustrate a schematic and corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element, in accordance with an embodiment of the present invention.

Figure 8 illustrates an operational schematic representing a changing of states for an anionic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention.

Figure 9 illustrates a schematic representation of resistance change in a conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention.

Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 12 illustrates a schematic of a memory bit cell which includes a metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention.

Figure 13 illustrates a block diagram of an electronic system, in accordance with an embodiment of the present invention.

Figure 14 illustrates a computing device in accordance with one embodiment of the invention.

Figure 15 illustrates an interposer that includes one or more embodiments of the invention.

DESCRIPTION OF THE EMBODIMENTS

Approaches for fabricating self-aligned pedestals for resistive random access memory (RRAM) elements and devices, and the resulting structures, are described. In the following description, numerous specific details are set forth, such as specific RRAM material regimes and structure architectures, in order to provide a thorough understanding of embodiments of the

present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as operations associated with embedded memory, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made.

Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

One or more embodiments of the present invention are directed to methods for integrating RRAM memory arrays into a logic processor. Specific embodiments are directed to self-aligned pedestal for scaled RRAM elements and devices fabricated therefrom. Particular embodiments may be suitable for fabricating embedded non-volatile memory (e-NVM). Approaches described herein may provide a fabrication pathway for high performance RRAM cells and increase the potential of using scaled RRAM cells for future e-NVM needs, such as for integration in system on chip (SoC) products.

In accordance with an embodiment of the present invention, an RRAM element thin film stack is integrated using electrode materials that are otherwise difficult to etch. In one such embodiment, integration approaches described herein can be implemented to improve an alignment between top and bottom electrodes in an RRAM element to allow for fabrication of scaled RRAM devices. In a particular example, noble or noble-like metals may be integrated as bottom electrodes in a back-end-of-line (BEOL) process. In one such embodiment, such a noble

metal electrode is self-aligned to a copper (Cu) based metallization structure. One or more embodiments enable a reduction in a required number of lithography operations.

To provide context, improvements in switching memory performance for both filamentary as well as interfacial RRAM devices may be achieved by integrating noble metals into the devices, e.g., in electrode layers, especially at the regions where switching takes place. Noble and noble-like metals provide high work function and are non-reactive to an RRAM oxide. However, noble metals are typically not easy to etch, often requiring integration via damascene process flows. A damascene process flow, however, involves additional lithography process operations and also risks misalignment with a metallization structure such as a copper metallization structure.

In an embodiment, one or more of the above described issues is addressed by implementation of a self-aligned structure with a recess in metallization, such as a recess in a copper metallization structure, to form a bottom electrode of an RRAM element. In one such embodiment, a thickness of the self-aligned electrode can be engineered to act as an internal ballast. Embodiments may be implemented to improve performance and reliability of RRAM memory, increasing its potential for use as embedded non-volatile memory (e-NVM).

Structural embodiments of the present invention may be contrasted against structures resulting from current or conventional integrations schemes. For example, Figure 1A illustrates a cross-sectional view of an RRAM element.

Referring to Figure 1A, an RRAM element for an RRAM device is shown as fabricated using a conventional integration scheme. The resulting structure includes a conductive interconnect 106A disposed in an inter-layer dielectric (ILD) layer 102A disposed above a substrate 100A. An RRAM element stack 112A is disposed on the conductive interconnect 106A. The RRAM element stack 112A includes a bottom electrode 114A, an oxide switching layer 116A, and a top electrode 118A. The bottom electrode 114A is typically a noble metal layer which is housed in an etch stop layer 120A. The arrangement of Figure 1A places a typically high work function pedestal (bottom electrode) set in the etch stop layer 102A. Such

pedestal integration typically involves several processing operations, including at least one lithography masking operation. As a result, misalignment of the pedestal can limit pitch scaling.

By contrast to the structure of Figure 1A, Figure 1B illustrates a cross-sectional view of an RRAM element, in accordance with an embodiment of the present invention. In one such embodiment, a pedestal or bottom electrode is integrated as self-aligned to a conductive interconnect or via, such as a copper interconnect or via. The fabrication may avoid use of a lithography operation, and may enhance lateral scaling (increased density) opportunities as a result of the self-alignment to the conductive interconnect or via since issues associated with misalignment are mitigated or altogether eliminated.

Referring to Figure 1B, a resistive random access memory (RRAM) device 150 includes a conductive interconnect 106B disposed in an ILD layer 102B disposed above a substrate 100B. An RRAM element 112B is disposed on the conductive interconnect 106B. The RRAM element includes a first electrode layer 114B disposed on the conductive interconnect 106B and in the ILD layer 102B. The first electrode layer 114B has an uppermost surface 115 substantially coplanar with an uppermost surface 124B of the ILD layer 102B. The first electrode layer 114B can be viewed as being disposed in a recess 122B between an uppermost surface of the conductive interconnect 106B and the uppermost surface 124B of the ILD layer 102B. A resistance switching layer 116B is disposed on the uppermost surface 115 of the first electrode layer 114B and on a portion of the uppermost surface 124B of the ILD layer 102B. A second electrode layer 118B is disposed on the resistance switching layer 116B. In one embodiment, the second electrode layer 118B and the resistance switching layer 116B have a common vertical sidewall profile 126B, as is depicted in Figure 1B.

In an embodiment, the conductive interconnect 106B includes a conductive line 110B which may or may not be continuous with an underlying via 108B. In one such embodiment, the conductive line 110B is further coupled to a second RRAM element sharing the first electrode layer 114B with the RRAM element 112B, as is described below in association with Figure 3A. In another embodiment, the conductive interconnect 106B is a single conductive via structure

(e.g., not having partitioned line 110B and via 108B portions), as is described below in association with Figure 3B.

In an embodiment, the conductive interconnect 106B includes a barrier layer and a conductive fill material within the barrier layer, as is described below in association with Figures 4A and 4B. In one such embodiment, an uppermost surface of the conductive fill material and an uppermost surface of the barrier layer are recessed below the uppermost surface 124B of the ILD layer 102B. The first electrode layer 114B is disposed on the uppermost surface of the conductive fill material and on the uppermost surface of the barrier layer, as is described below in association with Figure 4A. In another such embodiment, an uppermost surface of the conductive fill material is recessed below the uppermost surface 124B of the ILD layer 102B. An uppermost surface of the barrier layer is substantially co-planar with the uppermost surface 124B of the ILD layer 102B. The first electrode layer 114B is disposed on the uppermost surface of the conductive fill material and between portions of the barrier layer extending above the uppermost surface of the conductive fill layer, as is described below in association with Figure 4B.

Referring again to Figure 1B, and as used throughout the present disclosure, exemplary material combinations for the first electrode layer 114B, the resistance switching layer 116B, and the second electrode layer 118B are described below in association with Figures 7A and 8-11. In one embodiment, the first electrode layer 114B includes a noble metal species, such as Pd or Pt. In one embodiment, the second electrode layer 118B includes a transition metal species, such as W, V, Cr, or Ir. In one embodiment, the first electrode layer 114B includes a noble metal species, and the second electrode layer 118B includes a transition metal species. In one embodiment, the resistance switching layer is an oxide-based material layer including a dielectric oxide material (e.g., such as a layer of HfO_2 , as is described in association with Figures 7A and 7B) or a conductive oxide material (e.g., as described below in association with Figures 8 and 9).

Referring again to Figure 1B, and as used throughout the present disclosure, in an embodiment, one or more interlayer dielectrics (ILDs), such as ILD layer 102B, are included in

an RRAM device structure. Such ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant. In cases where a stack of ILD layers is implemented, etch stop materials may be included as intervening dielectric layers between the ILD layers. Such etch stop layers may be composed of dielectric materials different from the interlayer dielectric material. In some embodiments, an etch stop layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials, such as silicon carbide. Alternatively, other etch stop layers known in the art may be used depending upon the particular implementation. The etch stop layers may be formed by CVD, PVD, or by other deposition methods.

Referring again to Figure 1B, and as used throughout the present disclosure, in an embodiment, the metal lines (such as 110B) and vias (such as 108B) are composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers (such as Ta or TaN layers) between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

Referring again to Figure 1B, and as used throughout the present disclosure, in an embodiment, substrate 100B is a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are

not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

It is to be appreciated that the layers and materials described in association with to Figure 1B, and as used throughout the present disclosure, are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate 100B represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. In one embodiment, the illustrated structure depicted in Figure 1B is fabricated on underlying transistor or other semiconductor device layer(s) formed in or above the substrate 100B. In another embodiment, the illustrated structures depicted in Figure 1B are fabricated on underlying lower level interconnect layers formed above the substrate 100B.

A process flow may include fabrication of a self-aligned pedestal for scaled RRAM. As an example, Figure 2 illustrates cross-sectional views of various operations in a method of fabricating an RRAM element, in accordance with an embodiment of the present invention.

Referring to part (A) of Figure 2, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect 200 in an inter-layer dielectric (ILD) layer 102B formed above a substrate 100B. The conductive interconnect 200 has an uppermost surface 201 substantially co-planar with an uppermost surface 124B of the ILD

layer 102B. In an embodiment, the conductive interconnect 200 includes an upper metal line 202 on a conductive via 108B, as is depicted in part (A) of Figure 2. In other embodiments, the conductive interconnect 200 is a uniform conductive via. In an embodiment, the conductive interconnect 200 is fabricated using a damascene or dual damascene integration process.

5 Referring to part (B) of Figure 2, at least a portion of the uppermost surface 201 of the conductive interconnect 200 is recessed below the uppermost surface 124B of the ILD layer 102B. The recessing provides recessed conductive interconnect 106B having recessed portion 110B. The recessing is performed to an extent 122B below the uppermost surface 124B of the ILD layer 102B.

10 Referring to part (C) of Figure 2, subsequent to the recessing, a first electrode material layer 204 is formed over the ILD layer 102B and over the recessed portion 110B of the conductive interconnect. In an embodiment, the first electrode material layer 204 is or includes a noble metal and is deposited using a CVD process, a PVD process, an electroplating process, or an electroless plating process.

15 Referring to part (D) of Figure 2, the first electrode material layer 204 is planarized to form a first electrode layer 114B on the recessed portion 110B of the conductive interconnect 106B. The first electrode layer 114B has an uppermost surface 115 substantially co-planar with the uppermost surface 124B of the ILD layer 102B. In an embodiment, the first electrode material layer 204 is planarized using a chemical mechanical polishing (CMP) process.

20 Referring to part (E) of Figure 2, a resistance switching layer 116B is formed on the uppermost surface 115 of the first electrode layer 114B. A second electrode layer 118B is formed on the resistance switching layer 116B.

In one embodiment, forming the resistance switching layer 116B and forming the second electrode layer 118B includes first forming a blanket resistance switching material layer on the
25 first electrode layer 114B. A second electrode material layer is then formed on the resistance switching material layer. The second electrode material layer and the resistance switching material layer are then etched (e.g., subtractive patterning) to form the second electrode layer

118B and the resistance switching layer 116B, respectively. In one such embodiment, the etching process involves first patterning of a resist layer and/or hardmask layer formed above the second electrode material layer.

In one embodiment, recessing at least the portion of the uppermost surface of the conductive interconnect 200/202 below the uppermost surface 124B of the ILD layer 102B to form 106B/110B includes recessing the entire uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer. In a specific embodiment, both a barrier layer and a conductive fill material are recessed, as is described below in association with Figure 4A. In another embodiment, recessing at least the portion of the uppermost surface of the conductive interconnect 200/202 below the uppermost surface 124B of the ILD layer 102B to form 106B/110B includes recessing the only a portion uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer. In a specific embodiment, a barrier layer is not recessed while a conductive fill material is recessed, as is described below in association with Figure 4B.

A self-aligned pedestal may be fabricated for a metal line. As an example, Figure 3A illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, in accordance with an embodiment of the present invention.

Referring to Figure 3A, a conductive interconnect housed in an ILD 300 includes a first electrode layer 302 (e.g., a self-aligned pedestal) thereon. The conductive interconnect is a conductive line coupled to a first RRAM element 304 and a second RRAM element 304. In a specific embodiment, the dashed circles represent second electrode/resistance switching layer stacks which share a common first electrode layer 302.

A self-aligned pedestal may be fabricated for a metal via. As an example, Figure 3B illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, in accordance with an embodiment of the present invention.

Referring to Figure 3B, a conductive interconnect is a via housed in an ILD 310. Each via is discrete and includes a first electrode layer 312 (e.g., a self-aligned pedestal) thereon. Each

conductive interconnect is a conductive via coupled to a single corresponding RRAM element

314. In a specific embodiment, the dashed circles represent second electrode/resistance switching layer stacks.

Both a barrier layer and a conductive fill material may be recessed in the fabrication of a self-aligned pedestal. As an example, Figure 4A illustrates a cross-sectional view of an RRAM element having an electrode on a recessed conductive line or via, in accordance with an embodiment of the present invention.

Referring to Figure 4A, a conductive interconnect 404 is disposed in an ILD layer 402 disposed above a substrate 400. The conductive interconnect 404 includes a barrier layer 406 and a conductive fill material 408 within the barrier layer 406. An uppermost surface 450 of the conductive fill material 408 and an uppermost surface 452 of the barrier layer 406 are recessed below an uppermost surface 454 of the ILD layer 402. A first electrode layer 410 is disposed on the uppermost surface 450 of the conductive fill material 408 and on the uppermost surface 452 of the barrier layer 406. A resistance switching layer 412 is disposed on the first electrode layer 410. A second electrode layer 414 is disposed on the resistance switching layer 412. In one embodiment, dielectric sidewall spacers 416, such as silicon nitride spacers, are formed on the sidewalls of the second electrode layer 414 and the resistance switching layer 412, as is depicted in Figure 4A.

In an embodiment, the uppermost surface 450 of the conductive fill material 408 and the uppermost surface 452 of the barrier layer 406 are recessed below the uppermost surface 454 of the ILD layer 402 to approximately the same extent, as is depicted in Figure 4A. In another embodiment, the uppermost surface 450 of the conductive fill material 408 is recessed to a greater extent than the barrier layer 406. In yet another embodiment, the uppermost surface 450 of the conductive fill material 408 is recessed to a lesser extent than the barrier layer 406.

A conductive fill material, but not a barrier layer, may be recessed in the fabrication of a self-aligned pedestal. As an example, Figure 4B illustrates a cross-sectional view of another

RRAM element having an electrode on a recessed conductive line or via, in accordance with another embodiment of the present invention.

Referring to Figure 4B, a conductive interconnect 424 is disposed in an ILD layer 402 disposed above a substrate 400. The conductive interconnect 424 includes a barrier layer 426 and a conductive fill material 408 within the barrier layer 426. An uppermost surface 460 of the conductive fill material 408 is recessed below an uppermost surface 454 of the ILD layer 402. However, an uppermost surface 462 of the barrier layer 426 is not or is essentially not recessed below the uppermost surface 454 of the ILD layer 402. Accordingly, the uppermost surface 462 of the barrier layer 426 is substantially co-planar with the uppermost surface 454 of the ILD layer 402. A first electrode layer 430 is disposed on the uppermost surface 460 of the conductive fill material 408, between portions of the barrier layer 426 extending above the uppermost surface 460 of the conductive fill layer 408. A resistance switching layer 412 is disposed on the first electrode layer 430 and on the uppermost surface 462 of the barrier layer 426. A second electrode layer 414 is disposed on the resistance switching layer 412. In one embodiment, dielectric sidewall spacers 416, such as silicon nitride spacers, are formed on the sidewalls of the second electrode layer 414 and the resistance switching layer 412, as is depicted in Figure 4B.

The above described RRAM material stack formed above a self-aligned pedestal may be fabricated through subtractive patterning of the upper layers of the RRAM stack materials, as is depicted in the examples above. In another aspect, however, the upper layers of an RRAM element may be fabricated in a damascene-like fabrication scheme. As an example, Figure 4C illustrates a cross-sectional view of an RRAM element having damascene portions, in accordance with another embodiment of the present invention.

Referring to Figure 4C, a resistive random access memory (RRAM) device includes a conductive interconnect 404/424 (e.g., one such interconnect described in association with Figure 4A or Figure 4B) disposed in a first inter-layer dielectric (ILD) layer 402 disposed above a substrate 400. A second ILD layer 440 is disposed above the first ILD layer 402. The second

ILD layer 440 has an opening exposing the conductive interconnect 404/424 from a top down perspective. The opening has sidewalls, for example the sloped sidewalls depicted in Figure 4C.

An RRAM element is disposed on the conductive interconnect 404/424. The RRAM element includes a first electrode layer 410/430 (e.g., one such first electrode layer described in association with Figure 4A or Figure 4B) disposed on the conductive interconnect 404/424 and in the first ILD layer 402. The first electrode layer 410/430 has an uppermost surface 470 substantially co-planar with an uppermost surface 454 of the first ILD layer 402. The RRAM element also includes a resistance switching layer 442 disposed in the opening of the second ILD layer 440, on the uppermost surface 470 of the first electrode layer 410/430 and along the sidewalls of the opening of the second ILD layer 440. The RRAM element also includes a second electrode layer 444 disposed in the opening of the second ILD layer 440, on the resistance switching layer 442. In one embodiment, the resistance switching layer 442 is further disposed on a portion of the uppermost surface 454 of the first ILD layer 402, as is depicted in Figure 4C. It is to be appreciated that an etch stop layer may be disposed between the first ILD layer and the second ILD layer 440.

In an embodiment, forming the resistance switching layer 442 and forming the second electrode layer 444 includes first forming a second ILD material on or above the first ILD layer 402. An opening is then formed in the second ILD material to form second ILD layer 440, exposing the first electrode layer 410/430. The opening has sidewalls. A resistance switching material layer is then formed over the second ILD layer 440 and in the opening. A second electrode material layer is formed on the resistance switching material layer. The second electrode material layer and the resistance switching material layer are then planarized to form the resistance switching layer 442 on the first electrode layer 410/430 and along the sidewalls of the opening, and to form the second electrode layer 444 on the resistance switching layer 442.

In an aspect, a conductive interconnect of an associated RRAM element stack may be coupled to a drain region of an underlying select transistor disposed on a substrate. As an

example, Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector, in accordance with an embodiment of the present invention.

Referring to Figure 5, a memory structure 500 includes a transistor 502 disposed in or above an active region 504 of a semiconductor substrate 506. The transistor 502 includes a gate electrode 508 with source/drain regions 510 on either side of the gate electrode 508, and in active region 504 of substrate 506. In an embodiment, the source/drain region 510 on the left-hand side of Figure 5 is a source region, and the source/drain region 510 on the right-hand side of Figure 5 is a drain region. An RRAM element 514 is coupled to the drain region of the transistor 502, but not to the source region of the transistor 502. The arrangement enables driving of the RRAM element 514 by the drain side only. The RRAM element 514 and portions of the transistor 502 may be included in an inter-layer dielectric (ILD) layer 550, as is depicted in Figure 5.

The RRAM element 514 includes a top (second) electrode layer 520, a resistance switching layer 522, and a bottom (first) electrode layer 524. In an embodiment, the first electrode layer 524 is a self-aligned pedestal as described above. The RRAM element 514 is, in an embodiment, included as an interrupting feature along a conductive drain contact 530. In one such embodiment, corresponding gate contact 534 and source contact 532 are not coupled to, or interrupted by the RRAM element 514, as is depicted in Figure 5. It is to be appreciated that although the RRAM element 514 is shown generically along the drain contact 530 without a lateral reference, the actual layer in which the RRAM element 514 is included may be viewed as an interconnect layer (e.g., M1, M2, M3, M4, etc.) corresponding to a logic region in another area of the substrate 506. It is also to be appreciated that additional interconnect layer(s) may be formed on top of the structure 500 shown in Figure 5, e.g., using standard dual damascene process techniques that are well-known in the art.

In an embodiment, transistor 502 is a metal-oxide-semiconductor field-effect transistor (MOSFET or simply MOS transistor), fabricated on a substrate. In various implementations of the invention, the MOS transistors described herein may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as

double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors.

In an embodiment, each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer of each MOS transistor is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide.

An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the invention, a pair of sidewall spacers 552 may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions.

In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further
5 embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

To provide further context, integrating memory directly onto a microprocessor chip would be advantageous since it enables higher operation speeds compared to having physically
10 separate logic and memory chips. Unfortunately, traditional charge-based memory technologies such as DRAM and NAND Flash are now facing severe scalability issues related to increasingly precise charge placement and sensing requirements. As such, embedding charge-based memory directly onto a high performance logic chip is not very attractive for future technology nodes. However, a memory technology that does have the potential to scale to much smaller geometries
15 compared to traditional charge-based memories is resistive random access memory (RRAM), since it relies on resistivity rather than charge as the information carrier. However, in order to exploit the potential benefits of a high performance logic chip with embedded RRAM memory, an appropriate integrated logic plus RRAM structure and fabrication method is needed. Embodiments of the present invention include such structures and fabrication processes.

20 Relating to one or more embodiments described herein, it is to be appreciated that traditional DRAM memory is facing severe scaling issues and, so, other types of memory devices are being actively explored in the electronics industry. One future contender is RRAM devices. Embodiments described herein include a fabrication method for embedding RRAM bit cell arrays into a logic process technology. Embodiments described may be advantageous for
25 processing schemes involving the fabrication of logic processors with embedded memory arrays.

In an aspect, an RRAM element may be included in an integrated circuit in regions typically referred to as back end or back end of line (BEOL) layers of the integrated circuit. As

examples, Figure 6 illustrates schematic views of several options for positioning an RRAM element in an integrated circuit, in accordance with an embodiment of the present invention.

Referring to Figure 6, five examples (A)-(E) of an RRAM cell situated above a second metal logic layer (M2) or higher are provided. In each case, a memory region 600 and a logic region 602 of an integrated circuit are depicted schematically. Each memory region 600 and logic region 602 is associated with a corresponding transistor (or group of transistors) 604 or 606, respectively. Stacks of metallization layers (as housed in encompassing dielectric layer or layers 697) include metal lines 608 and vias 610 that are generally alternating. Thus, all arrangements depicted include an RRAM element disposed above a second metal line (M2) in the stack. The RRAM element typically includes a resistance switching layer, such as a conductive oxide memory layer, sandwiched between a bottom electrode and a top electrode, and may be formed in an opening of an insulating layer. The described arrangements can enable integration of both logic and memory on a same die versus stand-alone memory. Although depicted at a very high level conceptual view for the sake of illustrating general placement options, it is to be appreciated that, in accordance with an embodiment of the present invention, elements labeled RRAM in Figure 6 may include a self-aligned pedestal or electrode, examples of which are described above in association with Figure 1B, part (E) of Figure 2, Figures 3A and 3B, Figures 4A-4C and Figure 5.

Referring again to Figure 6, in a first example (A), an RRAM element is fabricated on top of a unique via 650 intended for memory devices. In a second example (B), an RRAM element is fabricated first and an upper unique via 660 contacts the RRAM from above. In a third example (C), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full via depth, between metal lines. In a fourth example (D), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full metal line height. In a fifth example (E), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full interconnect level (via

plus metal line). Accordingly, in an embodiment, an RRAM element or an array of RRAM elements can be embedded in a logic chip.

In another aspect, upon fabrication of an RRAM element having a self-aligned pedestal or electrode, the RRAM may be subjected to an intentional one-time “break-down” process for filament formation in the resulting RRAM device fabricated from the RRRAM memory element. To illustrate the above aspect, Figures 7A and 7B illustrate a schematic and corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element, in accordance with an embodiment of the present invention.

Referring to Figure 7A, a material stack 700 includes a bottom electrode (BE) 702, an oxide layer 704 such a hafnium oxide layer (HfO_2 , which may be considered a dielectric oxide layer), and a top electrode (TE) 706. Oxide vacancies 708 may be depicted as circles in Figure 7A. Oxide RRAM cell filament formation begins with a stoichiometric oxide layer 704 which is subjected to a forming (soft breakdown) operation (1) to provide a low resistance state (LRS). A first reset operation (2) is then performed to provide switching to a high resistance state (HRS). A set operation (3) is then performed to return to the LRS. Performing operations (1)-(3) involves motion of oxygen vacancies and redox phenomena. Plot 710 of Figure 7B illustrates the I-V characteristics association with operations (1), (2) and (3) of Figure 7A.

In another aspect, an RRAM element or device may be an anionic-based conductive oxide memory element. Figure 8 illustrates an operational schematic representing a changing of states for an anionic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention. Referring to Figure 8, a memory element 800 includes an electrode/conductive oxide/electrode material stack. The memory element 800 may begin in a less conductive state (1), with the conductive oxide layer being in a less conductive state 804A. An electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 800 in a more conductive state (3), with the conductive oxide layer being in a more conductive state 804B. An electrical pulse, such as a duration of a negative bias

(4) may be applied to again provide memory element 600 having the less conductive state (1).

Thus, electrical pulsing may be used to change resistance of the memory element 800.

As such, in an embodiment, a memory element includes an anionic-based conductive oxide layer sandwiched between two electrodes. Resistivity of the conductive oxide layer in low field (when device is read) is, in some embodiments, in the range found typical of conductive films of metal compounds, e.g. TiAlN. For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of 0.1 Ohm cm – 10 kOhm cm when measured at low field. Resistivity of the film is tuned depending in the memory element size to achieve final resistance value in the range compatible with fast read. Composition of the conductive oxide layer may be tuned in such a way that a small change in its composition results in a large change in resistance. Resistance change occurs, in some embodiments, due to a Mott transition, e.g., when injected/extracted charge causes phase transition in the conductive oxide layer between more and less resistive phase configurations. In other embodiments, the resistance change can be induced by changing the concentration of oxygen vacancies in the conductive oxide layer.

As an example of one approach, Figure 9 illustrates a schematic representation of resistance change in an anionic-based conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention. Referring to Figure 9, a memory element 900 is shown as deposited (A). The memory element includes a conductive oxide layer 904 between a palladium (Pd) electrode 902 and a tungsten (W) electrode 906. Oxygen atoms and oxygen vacancies may be distributed as shown in (A). Referring to (B) of Figure 9, upon application of a positive bias, the memory element 900 can be made more conductive. In that state, oxygen atoms migrate to the electrode 906, while vacancies remain throughout the layer 904. Referring to (C) of Figure 9, upon application of a negative bias, the memory element can be made less conductive. That that state, oxygen atoms are distributed more evenly throughout layer 904. Accordingly, in an embodiment, effective composition (e.g., the location of oxygen atoms versus vacancies) of a conductive oxide layer is modified to change resistance of a memory element. In a specific

embodiment, an applied electrical field, which drives such compositional change, is tuned to values approximately in the range of $1e6$ - $1e7$ V/cm. Referring again to Figure 9, although surface stage are demonstrated, it is to be appreciated that if filament formation is used, such as described in association with Figures 7A and 7B, vacancies will penetrate the film to a greater
5 extent.

As mentioned briefly above, in an embodiment, one electrode in a memory element including an anionic-based conductive oxide layer is a noble metal based electrode, while the other electrode in is a transition metal for which some of the lower valence oxides are conductive (e.g., to act as an oxygen reservoir). That is, when oxygen atoms migrate to the transition metal
10 oxide, the resulting interfacial transition metal oxide formed remains conductive. Examples of suitable transition metals which form conductive oxides include but are not limited to, W, V, Cr, or Ir. In other embodiments, one or both of the electrodes is fabricated from an electro-chromic material. In other embodiments, one or both of the electrodes is fabricated from a second, different conductive oxide material. In an embodiment, examples of suitable conductive oxides
15 include, but are not limited to: ITO ($In_2O_{3-x}SnO_{2-x}$), In_2O_{3-x} , sub-stoichiometric yttria doped zirconia ($Y_2O_{3-x}ZrO_{2-x}$), or $La_{1-x}Sr_xGa_{1-y}Mg_yO_{3-x-0.5(x+y)}$. In another embodiment, the conductive oxide layer is composed of a material with two or more metal elements (e.g., as contrasted to common RRAM memories using one metal such as found in binary oxides, such as HfO_x or TaO_x). In such ternary, quaternary, etc. alloys, the metals used are from adjacent columns of the
20 periodic table. Specific examples of suitable such conductive oxides include, but are not limited to: Y and Zr in $Y_2O_{3-x}ZrO_{2-x}$, In and Sn in $In_2O_{3-x}SnO_{2-x}$, or Sr and La in $La_{1-x}Sr_xGa_{1-y}Mg_yO_3$. Such materials may be viewed as compositions selected to have aliovalent substitution to significantly increase the number of oxygen vacancies. It is to be appreciated that in some embodiments the change of resistance of such electrode during programming can contribute to
25 the total resistance change.

In an embodiment, examples of suitable noble metals include, but are not limited to Pd or Pt. In a specific embodiment, a more complex, yet still all-conductive, stack includes an

approximately 10nm Pd first electrode layer, an approximately 3nm $\text{In}_2\text{O}_{3-x}$ and/or SnO_{2-x} conductive oxide layer, and a second electrode stack composed of approximately 20nm tungsten/10nm Pd/100nm TiN /55nm W.

In another aspect, an RRAM element or device may be a cationic-based conductive oxide memory element. As an example, Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention. Referring to Figure 10, memory element 1000 may begin in a more conductive state (1), with a cationic-based conductive oxide layer being in a more conductive state 1004A. An electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 1000 in a less conductive state (3), with the cationic-based conductive oxide layer being in a less conductive state 1004B. An electrical pulse, such as a duration of a negative bias (4) may be applied to again provide memory element 1000 having the more conductive state (1). Thus, electrical pulsing may be used to change resistance of the memory element 1000. Polarity applied is such as to attract active cations of in the memory layer to the intercalation electrode under negative bias.

As such, in an embodiment, a memory element includes a cationic-based conductive oxide layer sandwiched between two electrodes. Resistivity of the cationic-based conductive oxide layer in low field (when device is read) is, in some embodiments, can be as low as found typical of conductive films of metal compounds, e.g. TiAlN. For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of 0.1 Ohm cm – 10 kOhm cm when measured at low field (measured for the specific thickness used in the stack). Resistivity of the film is tuned depending in the memory element size to achieve final resistance value in the range compatible with fast read.

As an example of one approach, Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies (such as lithium cation vacancies) in the conductive oxide layer, in accordance with an embodiment of the present invention.

Referring to Figure 11, a memory element 1100 is shown as deposited (A). The memory element includes a cationic-based conductive oxide layer 1104 between a bottom electrode 1102 and a top electrode 1106. In a specific example, the layer 1104 is a lithium cobalt oxide layer, described in greater details below, and lithium atoms and lithium vacancies are distributed as shown in (A). Referring to (B) of Figure 11, upon application of a negative bias, the memory element 1100 can be made more conductive. In that state, lithium atoms migrate to the top electrode 1106, while vacancies remain throughout the layer 1104. Referring to (C) of Figure 11, upon application of a positive bias to one of the electrodes, the memory element can be made less conductive. In that state, lithium atoms are distributed more evenly throughout layer 1104. Accordingly, in an embodiment, effective composition (e.g., the location of lithium atoms (or cations) versus vacancies) of a cationic-based conductive oxide layer is modified to change resistance of a memory element, in some embodiments due to stoichiometry-induced Mott transition. In a specific embodiment, an applied electrical field, which drives such compositional change during write operation, is tuned to values approximately in the range of $1\text{e}6\text{-}1\text{e}7$ V/cm.

In an embodiment, referring again to Figure 11, the cationic-based conductive oxide layer 1104 is composed of a material suitable for cation-based mobility within the layer itself. In a specific exemplary embodiment, layer 1104 of Figure 11 part (A) is composed of lithium cobalt oxide (LiCoO_2). Then, in part (B), the corresponding layer becomes lithium deficient (e.g., $\text{Li}_{<0.75}\text{CoO}_2$) when a negative bias is applied and lithium atoms (e.g., as cations) migrate toward electrode 1106. By contrast, in part (C), the corresponding layer becomes lithium rich (e.g., $\text{Li}_{>0.95}\text{CoO}_2$) when a positive bias is applied and lithium atoms (e.g., as cations) migrate away from electrode 1106. In other embodiments, other suitable compositions with cationic conductivity include, but are not limited to, LiMnO_2 , $\text{Li}_4\text{TiO}_{12}$, LiNiO_2 , LiNbO_3 , $\text{Li}_3\text{N:H}$, LiTiS_2 (all of which are lithium atom or Li^+ mobility based), Na β -alumina (which is sodium atom or Na^+ mobility based), or AgI , RbAg_4I_5 , AgGeAsS_3 (all of which are silver atom or Ag^+ mobility based). In general, these examples provide materials based on cation mobility or migration,

which is typically much faster than anionic-based mobility or migration (e.g., for oxygen atoms or O^{2-} anions).

In an embodiment, referring again to Figure 11, one electrode (e.g., bottom electrode 1102) in a memory element including a cationic conductive oxide layer is a noble metal based electrode. In one embodiment, examples of suitable noble metals include, but are not limited to palladium (Pd) or platinum (Pt). In a specific embodiment, a memory stack includes a bottom electrode composed of an approximately 10 nanometer thick Pd layer. It is to be understood that use of the terms “bottom” and “top” for electrodes 1102 and 1106 need only be relative and are not necessarily absolute with respect to, e.g., an underlying substrate.

In an embodiment, referring again to Figure 11, the other electrode (e.g., top electrode 1106) in a memory element including a cationic conductive oxide layer is an “intercalation host” for migrating cations. The material of the top electrode is a host in a sense that the material is conductive with or without the presence of the migrating cations and is not substantially altered in the absence or presence of the migrating cations. In an exemplary embodiment, the top electrode is composed of a material such as, but not limited to, graphite, or metal chalcogenides such as disulfides (e.g., TaS_2). Such materials are conductive as well as absorbing of cations such as Li^+ . This is in contrast to an electrode for an anionic based conductive oxide which may include a metal with a corresponding conductive oxide to accommodate migrating oxygen atoms or anions.

Referring again to the description associated with Figures 8-11 above, a stack of conductive layers including a conductive metal oxide layer may be used to fabricate as memory bit cell. For example, Figure 12 illustrates a schematic of a memory bit cell 1200 which includes a metal-conductive oxide-metal RRAM memory element 1210, in accordance with an embodiment of the present invention. Such an RRAM memory element may be suitable for manufacture on a substrate in common with logic regions of the substrate.

Referring to Figure 12, the RRAM memory element 1210 may include a first conductive electrode 1212 with a conductive metal oxide layer 1214 adjacent the first conductive electrode

1212. A second conductive electrode 1216 is adjacent the conductive metal oxide layer 1214.

The second conductive electrode 1216 may be electrically connected to a bit line 1232. The first conductive electrode 1212 may be coupled with a transistor 1234. The transistor 1234 may be coupled with a wordline 1236 and a source line 1238 in a manner that will be understood to those skilled in the art. The memory bit cell 1200 may further include additional read and write circuitry (not shown), a sense amplifier (not shown), a bit line reference (not shown), and the like, as will be understood by those skilled in the art, for the operation of the memory bit cell 1200. It is to be appreciated that a plurality of the memory bit cells 1200 may be operably connected to one another to form a memory array, wherein the memory array can be incorporated into a non-volatile memory region of a substrate in common with a logic region. It is to be appreciated that the transistor 1234 may be connected to the second conductive electrode 1216 or the first conductive electrode 1212, although only the latter is shown. In accordance with an embodiment of the present invention, one of the second conductive electrode 1216 or the first conductive electrode 1212 is a self-aligned electrode formed on a recessed conductive interconnect.

Figure 13 illustrates a block diagram of an electronic system 1300, in accordance with an embodiment of the present invention. The electronic system 1300 can correspond to, for example, a portable system, a computer system, a process control system, or any other system that utilizes a processor and an associated memory. The electronic system 1300 may include a microprocessor 1302 (having a processor 1304 and control unit 1306), a memory device 1308, and an input/output device 1310 (it is to be appreciated that the electronic system 1300 may have a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 1300 has a set of instructions that define operations which are to be performed on data by the processor 1304, as well as, other transactions between the processor 1304, the memory device 1308, and the input/output device 1310. The control unit 1306 coordinates the operations of the processor 1304, the memory device 1308 and the input/output device 1310 by cycling through a set of operations that cause

instructions to be retrieved from the memory device 1308 and executed. The memory device 1308 can include a memory element having a conductive oxide and electrode stack as described in the present description. In an embodiment, the memory device 1308 is embedded in the microprocessor 1302, as depicted in Figure 13. In an embodiment, the processor 1304, or
5 another component of electronic system 1300, includes an array of RRAM devices having a self-aligned conductive pedestal or electrode.

Figure 14 illustrates a computing device 1400 in accordance with one embodiment of the invention. The computing device 1400 houses a board 1402. The board 1402 may include a number of components, including but not limited to a processor 1404 and at least one
10 communication chip 1406. The processor 1404 is physically and electrically coupled to the board 1402. In some implementations the at least one communication chip 1406 is also physically and electrically coupled to the board 1402. In further implementations, the communication chip 1406 is part of the processor 1404.

Depending on its applications, computing device 1400 may include other components
15 that may or may not be physically and electrically coupled to the board 1402. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass,
20 an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1406 enables wireless communications for the transfer of data to and from the computing device 1400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that
25 may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1406 may implement

any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1400 may include a plurality of communication chips 1406. For instance, a first communication chip 1406 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1206 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1404 of the computing device 1400 includes an integrated circuit die packaged within the processor 1404. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1406 also includes an integrated circuit die packaged within the communication chip 1406. In accordance with another implementation of an embodiment of the invention, the integrated circuit die of the communication chip includes RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In further implementations, another component housed within the computing device 1400 may contain a stand-alone integrated circuit memory die that includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In various implementations, the computing device 1400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-

top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1400 may be any other electronic device that processes data.

Accordingly, one or more embodiments of the present invention relate generally to the
5 fabrication of embedded microelectronic memory. The microelectronic memory may be non-volatile, wherein the memory can retain stored information even when not powered. One or more embodiments of the present invention relate to the fabrication of RRAM memory arrays integrated into a logic processor. Such arrays may be used in an embedded non-volatile memory, either for its non-volatility, or as a replacement for embedded dynamic random access memory
10 (eDRAM). For example, such an array may be used for 1T-1R memory or 2T-1R memory (R = resistor) at competitive cell sizes within a given technology node.

Figure 15 illustrates an interposer 1500 that includes one or more embodiments of the invention. The interposer 1500 is an intervening substrate used to bridge a first substrate 1502 to a second substrate 1504. The first substrate 1502 may be, for instance, an integrated circuit die.
15 The second substrate 1504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1500 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1500 may couple an integrated circuit die to a ball grid array (BGA) 1506 that can subsequently be coupled to the second substrate 1504. In some embodiments, the first and
20 second substrates 1502/1504 are attached to opposing sides of the interposer 1500. In other embodiments, the first and second substrates 1502/1504 are attached to the same side of the interposer 1500. And in further embodiments, three or more substrates are interconnected by way of the interposer 1500.

The interposer 1500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy
25 resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same

materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 1508 and vias 1510, including but not limited to through-silicon vias (TSVs) 1512. The interposer 1500 may further include embedded devices 1514, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1500. In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1500.

Thus, embodiments of the present invention include approaches for fabricating self-aligned pedestals for resistive random access memory (RRAM) elements and devices, and the resulting structures.

In an embodiment, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the conductive interconnect and in the ILD layer. The first electrode layer has an uppermost surface substantially co-planar with an uppermost surface of the ILD layer. A resistance switching layer is disposed on the uppermost surface of the first electrode layer and on a portion of the uppermost surface of the ILD layer. A second electrode layer is disposed on the resistance switching layer.

In one embodiment, the conductive interconnect is a conductive line further coupled to a second RRAM element sharing the first electrode layer with the RRAM element.

In one embodiment, the conductive interconnect is a conductive via.

In one embodiment, the conductive interconnect includes a barrier layer and a conductive fill material within the barrier layer.

In one embodiment, an uppermost surface of the conductive fill material and an uppermost surface of the barrier layer are recessed below the uppermost surface of the ILD layer. The first electrode layer is disposed on the uppermost surface of the conductive fill material and on the uppermost surface of the barrier layer.

5 In one embodiment, an uppermost surface of the conductive fill material is recessed below the uppermost surface of the ILD layer. An uppermost surface of the barrier layer is substantially co-planar with the uppermost surface of the ILD layer. The first electrode layer is disposed on the uppermost surface of the conductive fill material and between portions of the barrier layer extending above the uppermost surface of the conductive fill layer.

10 In one embodiment, the conductive interconnect is coupled to a drain region of an underlying select transistor disposed on the substrate.

In one embodiment, the first electrode layer includes a noble metal species.

In one embodiment, the second electrode layer includes a transition metal species.

In one embodiment, the resistance switching layer is an oxide-based material layer
15 including a dielectric oxide material or a conductive oxide material.

In an embodiment, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in a first inter-layer dielectric (ILD) layer disposed above a substrate. A second ILD layer is disposed above the first ILD layer. The second ILD layer has an opening exposing the conductive interconnect, the opening having sidewalls. An RRAM
20 element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the conductive interconnect and in the first ILD layer. The first electrode layer has an uppermost surface substantially co-planar with an uppermost surface of the first ILD layer. The RRAM element also includes a resistance switching layer disposed in the opening of the second ILD layer, on the uppermost surface of the first electrode layer and along
25 the sidewalls of the opening of the second ILD layer. The RRAM element also includes a second electrode layer disposed in the opening of the second ILD layer, on the resistance switching layer.

In one embodiment, the resistance switching layer is further disposed on a portion of the uppermost surface of the first ILD layer.

In one embodiment, the conductive interconnect is a conductive line further coupled to a second RRAM element sharing the first electrode layer with the RRAM element.

5 In one embodiment, the conductive interconnect is a conductive via.

In one embodiment, the conductive interconnect includes a barrier layer and a conductive fill material within the barrier layer.

In one embodiment, an uppermost surface of the conductive fill material and an uppermost surface of the barrier layer are recessed below the uppermost surface of the first ILD layer, and the first electrode layer is disposed on the uppermost surface of the conductive fill material and on the uppermost surface of the barrier layer.

In one embodiment, an uppermost surface of the conductive fill material is recessed below the uppermost surface of the first ILD layer, an uppermost surface of the barrier layer is substantially co-planar with the uppermost surface of the first ILD layer, and the first electrode layer is disposed on the uppermost surface of the conductive fill material and between portions of the barrier layer extending above the uppermost surface of the conductive fill layer.

In one embodiment, the conductive interconnect is coupled to a drain region of an underlying select transistor disposed on the substrate.

In one embodiment, the first electrode layer includes a noble metal species.

20 In one embodiment, the second electrode layer includes a transition metal species.

In one embodiment, the resistance switching layer is an oxide-based material layer including a dielectric oxide material or a conductive oxide material.

In an embodiment, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate. The conductive interconnect has an uppermost surface substantially co-planar with an uppermost surface of the ILD layer. The method also includes recessing at least a portion of the uppermost surface of the conductive interconnect below the uppermost surface of

the ILD layer. The method also includes, subsequent to the recessing, forming a first electrode material layer over the ILD layer and over the conductive interconnect. The method also includes planarizing the first electrode material layer to form a first electrode layer on the recessed portion of the conductive interconnect, the first electrode layer having an uppermost surface substantially co-planar with the uppermost surface of the ILD layer. The method also includes forming a resistance switching layer on the uppermost surface of the first electrode layer. The method also includes forming a second electrode layer on the resistance switching layer.

In one embodiment, forming the resistance switching layer and forming the second electrode layer includes forming a resistance switching material layer on the first electrode layer. A second electrode material layer is then formed on the resistance switching material layer. The second electrode material layer and the resistance switching material layer are then etched to form the second electrode layer and the resistance switching layer, respectively.

In one embodiment, forming the resistance switching layer and forming the second electrode layer includes forming a second ILD layer above the ILD layer. An opening is then formed in the second ILD layer exposing the first electrode layer. The opening has sidewalls. A resistance switching material layer is then formed over the second ILD layer and in the opening. A second electrode material layer is formed on the resistance switching material layer. The second electrode material layer and the resistance switching material layer are then planarized to form the resistance switching layer on the first electrode layer and along the sidewalls of the opening, and to form the second electrode layer on the resistance switching layer.

In one embodiment, recessing at least the portion of the uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer includes recessing the entire uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer.

CLAIMS

What is claimed is:

1. A resistive random access memory (RRAM) device, comprising:
5 a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate; and
an RRAM element disposed on the conductive interconnect, the RRAM element comprising:
a first electrode layer disposed on the conductive interconnect and in the ILD layer,
the first electrode layer having an uppermost surface substantially co-planar with
10 an uppermost surface of the ILD layer;
a resistance switching layer disposed on the uppermost surface of the first electrode layer and on a portion of the uppermost surface of the ILD layer; and
a second electrode layer disposed on the resistance switching layer.
- 15 2. The RRAM device of claim 1, wherein the conductive interconnect is a conductive line further coupled to a second RRAM element sharing the first electrode layer with the RRAM element.
3. The RRAM device of claim 1, wherein the conductive interconnect is a conductive via.
- 20 4. The RRAM device of claim 1, wherein the conductive interconnect comprises a barrier layer and a conductive fill material within the barrier layer.
5. The RRAM device of claim 4, wherein an uppermost surface of the conductive fill material
25 and an uppermost surface of the barrier layer are recessed below the uppermost surface of the ILD layer, and wherein the first electrode layer is disposed on the uppermost surface of the conductive fill material and on the uppermost surface of the barrier layer.

6. The RRAM device of claim 4, wherein an uppermost surface of the conductive fill material is recessed below the uppermost surface of the ILD layer, wherein an uppermost surface of the barrier layer is substantially co-planar with the uppermost surface of the ILD layer, and wherein
5 the first electrode layer is disposed on the uppermost surface of the conductive fill material and between portions of the barrier layer extending above the uppermost surface of the conductive fill layer.
7. The RRAM device of claim 1, wherein the conductive interconnect is coupled to a drain
10 region of an underlying select transistor disposed on the substrate.
8. The RRAM device of claim 1, wherein the first electrode layer comprises a noble metal species.
9. The RRAM device of claim 8, wherein the second electrode layer comprises a transition metal
15 species.
10. The RRAM device of claim 1, wherein the resistance switching layer is an oxide-based material layer comprising a dielectric oxide material or a conductive oxide material.
11. A resistive random access memory (RRAM) device, comprising:
20 a conductive interconnect disposed in a first inter-layer dielectric (ILD) layer disposed above a substrate;
a second ILD layer disposed above the first ILD layer, the second ILD layer having an opening exposing the conductive interconnect, the opening having sidewalls; and
25 an RRAM element disposed on the conductive interconnect, the RRAM element comprising:

a first electrode layer disposed on the conductive interconnect and in the first ILD layer, the first electrode layer having an uppermost surface substantially co-planar with an uppermost surface of the first ILD layer;

a resistance switching layer disposed in the opening of the second ILD layer, on the uppermost surface of the first electrode layer and the sidewalls of the opening of the second ILD layer; and

a second electrode layer disposed in the opening of the second ILD layer, on the resistance switching layer.

12. The RRAM device of claim 11, wherein the resistance switching layer is further disposed on a portion of the uppermost surface of the first ILD layer.

13. The RRAM device of claim 11, wherein the conductive interconnect is a conductive line further coupled to a second RRAM element sharing the first electrode layer with the RRAM element.

14. The RRAM device of claim 11, wherein the conductive interconnect is a conductive via.

15. The RRAM device of claim 11, wherein the conductive interconnect comprises a barrier layer and a conductive fill material within the barrier layer.

16. The RRAM device of claim 15, wherein an uppermost surface of the conductive fill material and an uppermost surface of the barrier layer are recessed below the uppermost surface of the first ILD layer, and wherein the first electrode layer is disposed on the uppermost surface of the conductive fill material and on the uppermost surface of the barrier layer.

17. The RRAM device of claim 15, wherein an uppermost surface of the conductive fill material is recessed below the uppermost surface of the first ILD layer, wherein an uppermost surface of the barrier layer is substantially co-planar with the uppermost surface of the first ILD layer, and wherein the first electrode layer is disposed on the uppermost surface of the conductive fill material and between portions of the barrier layer extending above the uppermost surface of the conductive fill layer.

18. The RRAM device of claim 11, wherein the conductive interconnect is coupled to a drain region of an underlying select transistor disposed on the substrate.

19. The RRAM device of claim 11, wherein the first electrode layer comprises a noble metal species.

20. The RRAM device of claim 19, wherein the second electrode layer comprises a transition metal species.

21. The RRAM device of claim 11, wherein the resistance switching layer is an oxide-based material layer comprising a dielectric oxide material or a conductive oxide material.

22. A method of fabricating a resistive random access memory (RRAM) device, the method comprising:

forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate, the conductive interconnect having an uppermost surface substantially co-planar with an uppermost surface of the ILD layer;

recessing at least a portion of the uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer;

subsequent to the recessing, forming a first electrode material layer over the ILD layer and over the conductive interconnect;

planarizing the first electrode material layer to form a first electrode layer on the recessed portion of the conductive interconnect, the first electrode layer having an uppermost

5 surface substantially co-planar with the uppermost surface of the ILD layer;

forming a resistance switching layer on the uppermost surface of the first electrode layer; and forming a second electrode layer on the resistance switching layer.

23. The method of claim 22, wherein forming the resistance switching layer and forming the
10 second electrode layer comprises:

forming a resistance switching material layer on the first electrode layer;

forming a second electrode material layer on the resistance switching material layer; and

etching the second electrode material layer and the resistance switching material layer to form the second electrode layer and the resistance switching layer, respectively.

15

24. The method of claim 22, wherein forming the resistance switching layer and forming the second electrode layer comprises:

forming a second ILD layer above the ILD layer;

forming an opening in the second ILD layer exposing the first electrode layer, the opening

20 having sidewalls;

forming a resistance switching material layer over the second ILD layer and in the opening;

forming a second electrode material layer on the resistance switching material layer;

planarizing the second electrode material layer and the resistance switching material layer to form the resistance switching layer on the first electrode layer and along the sidewalls of
25 the opening, and to form the second electrode layer on the resistance switching layer.

25. The method of claim 22, wherein recessing at least the portion of the uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer comprises recessing the entire uppermost surface of the conductive interconnect below the uppermost surface of the ILD layer.

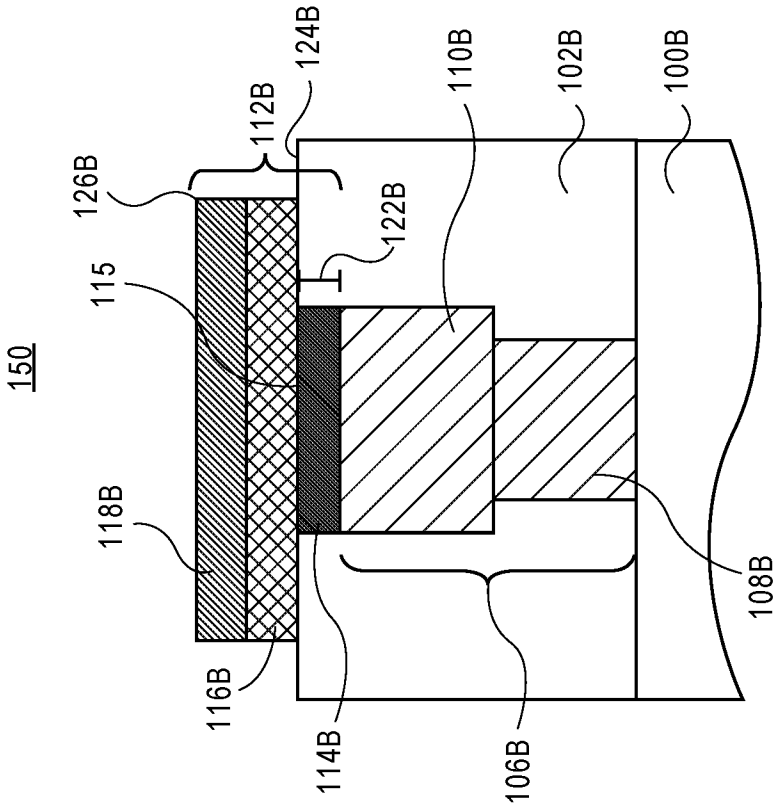


FIG. 1B

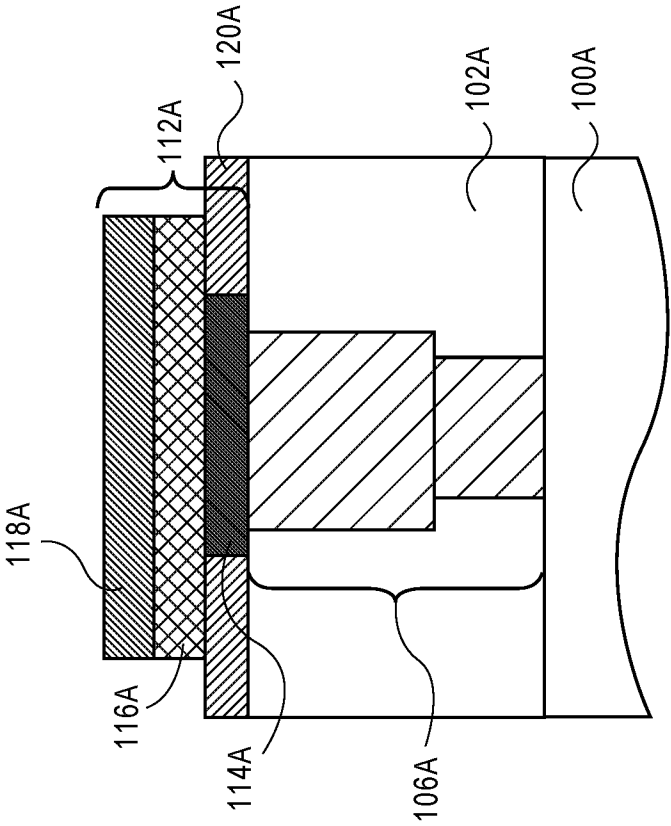


FIG. 1A

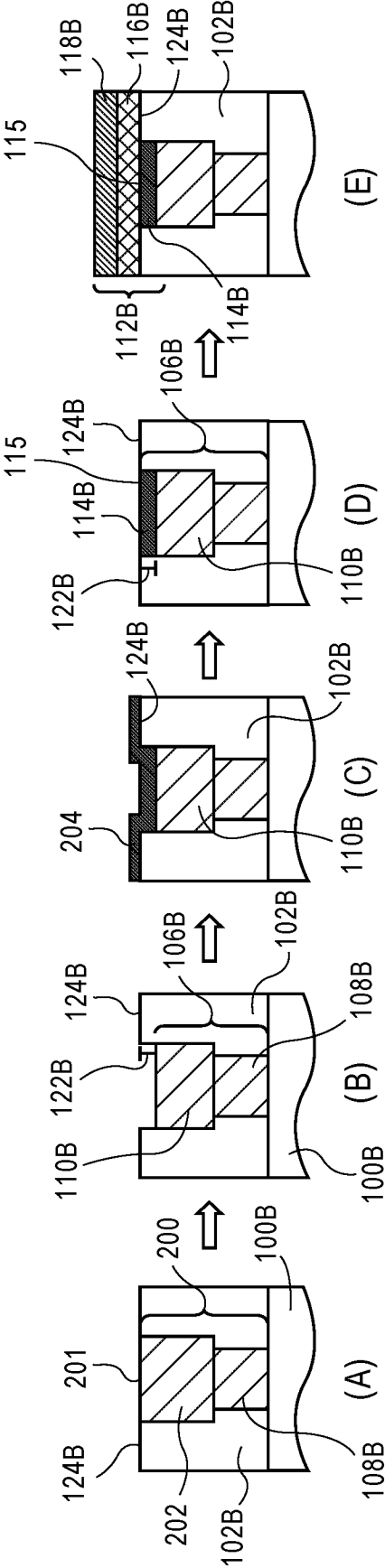


FIG. 2

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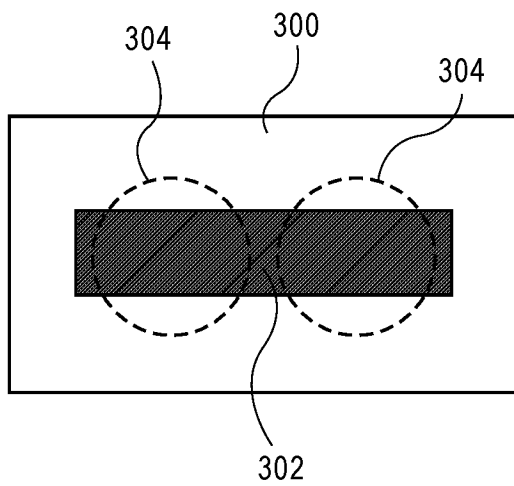


FIG. 3A

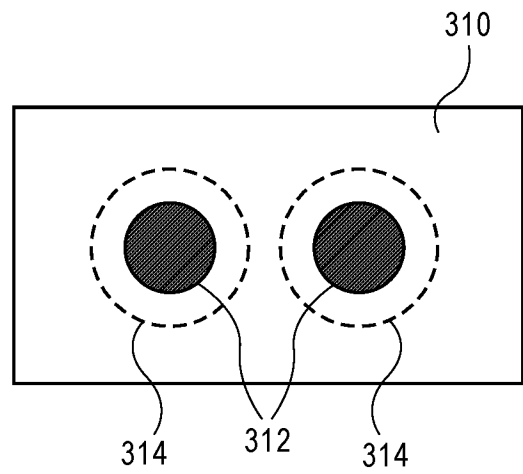


FIG. 3B

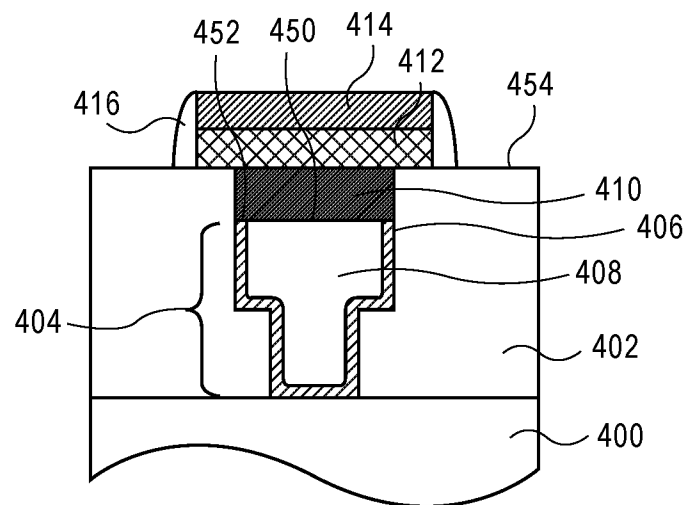


FIG. 4A

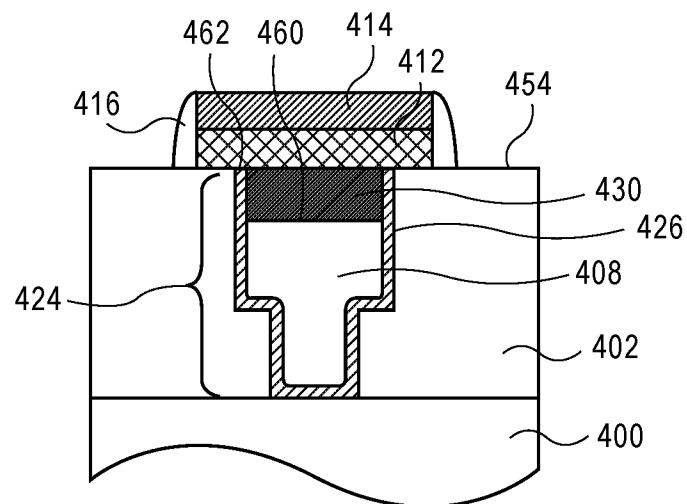


FIG. 4B

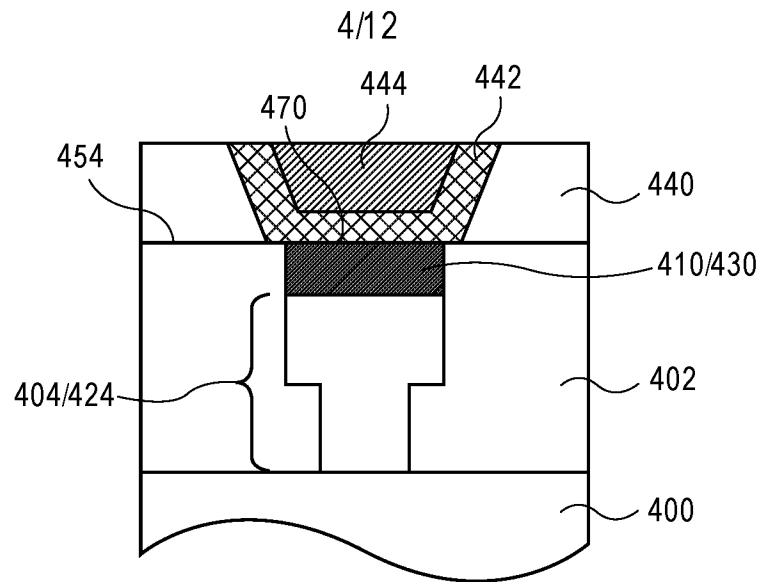


FIG. 4C

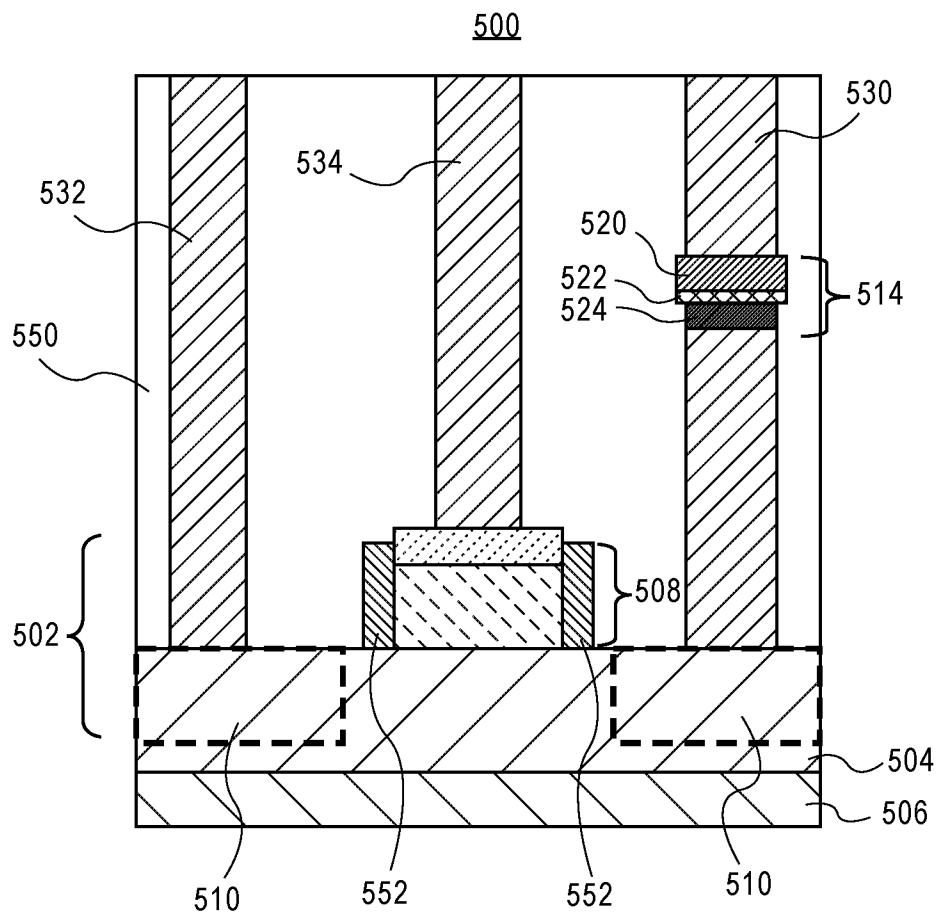


FIG. 5

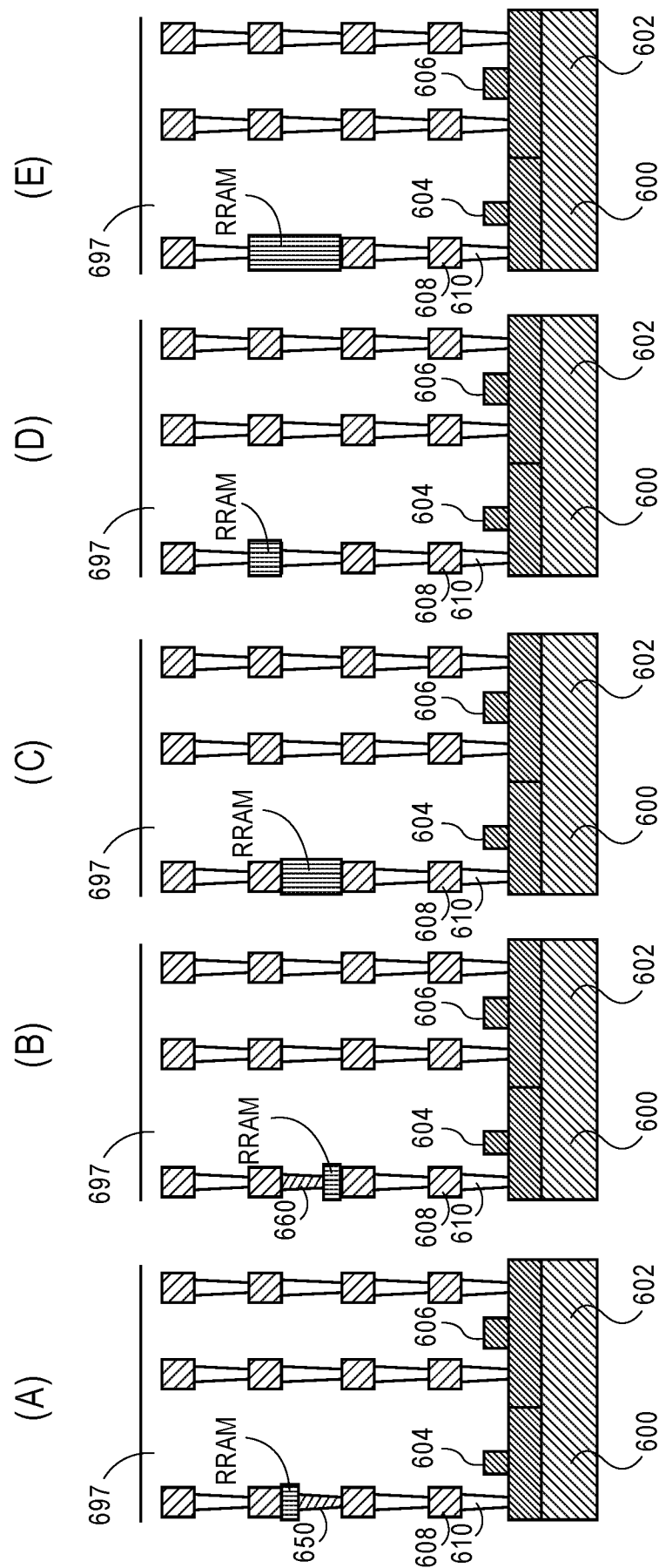
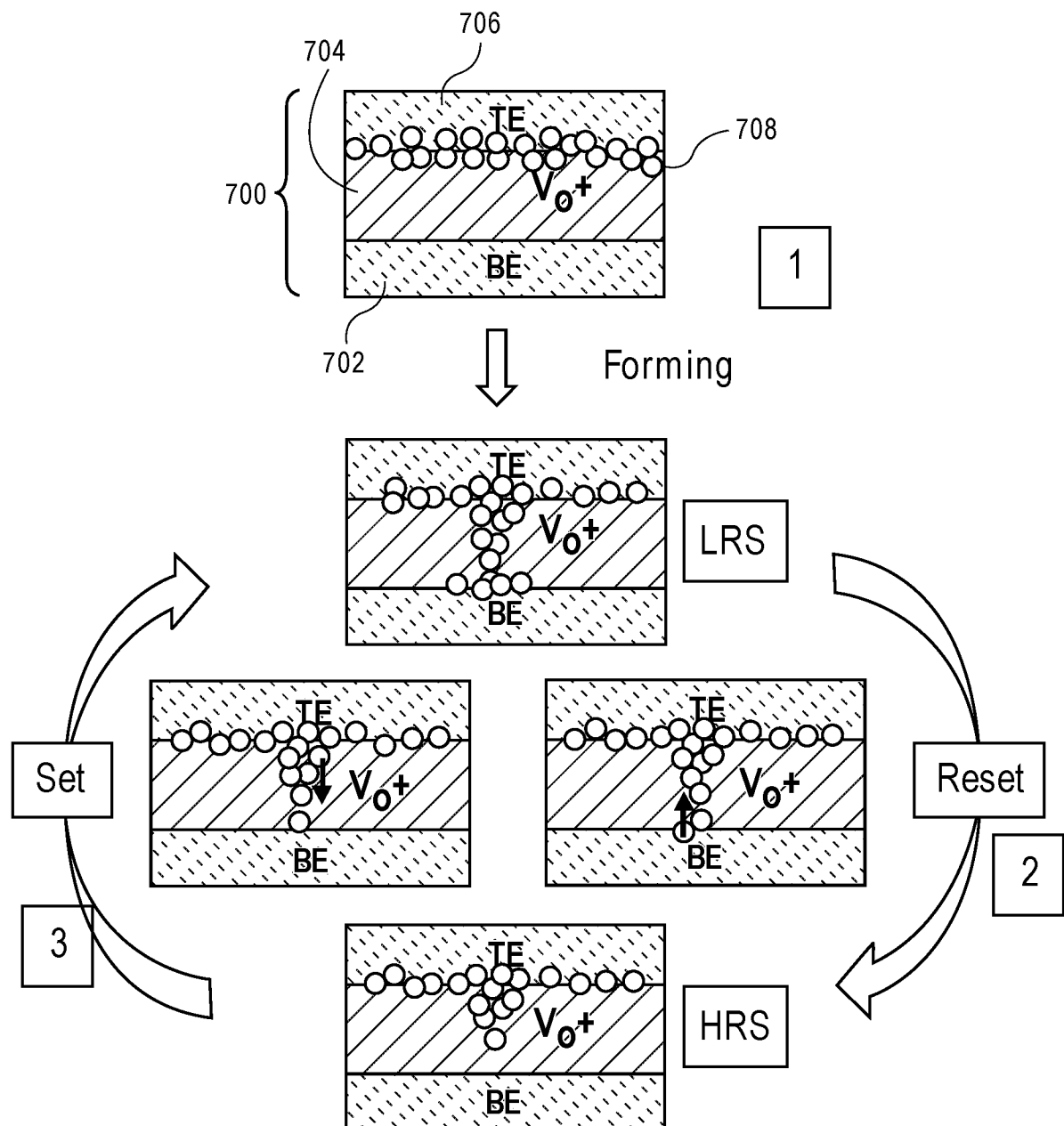
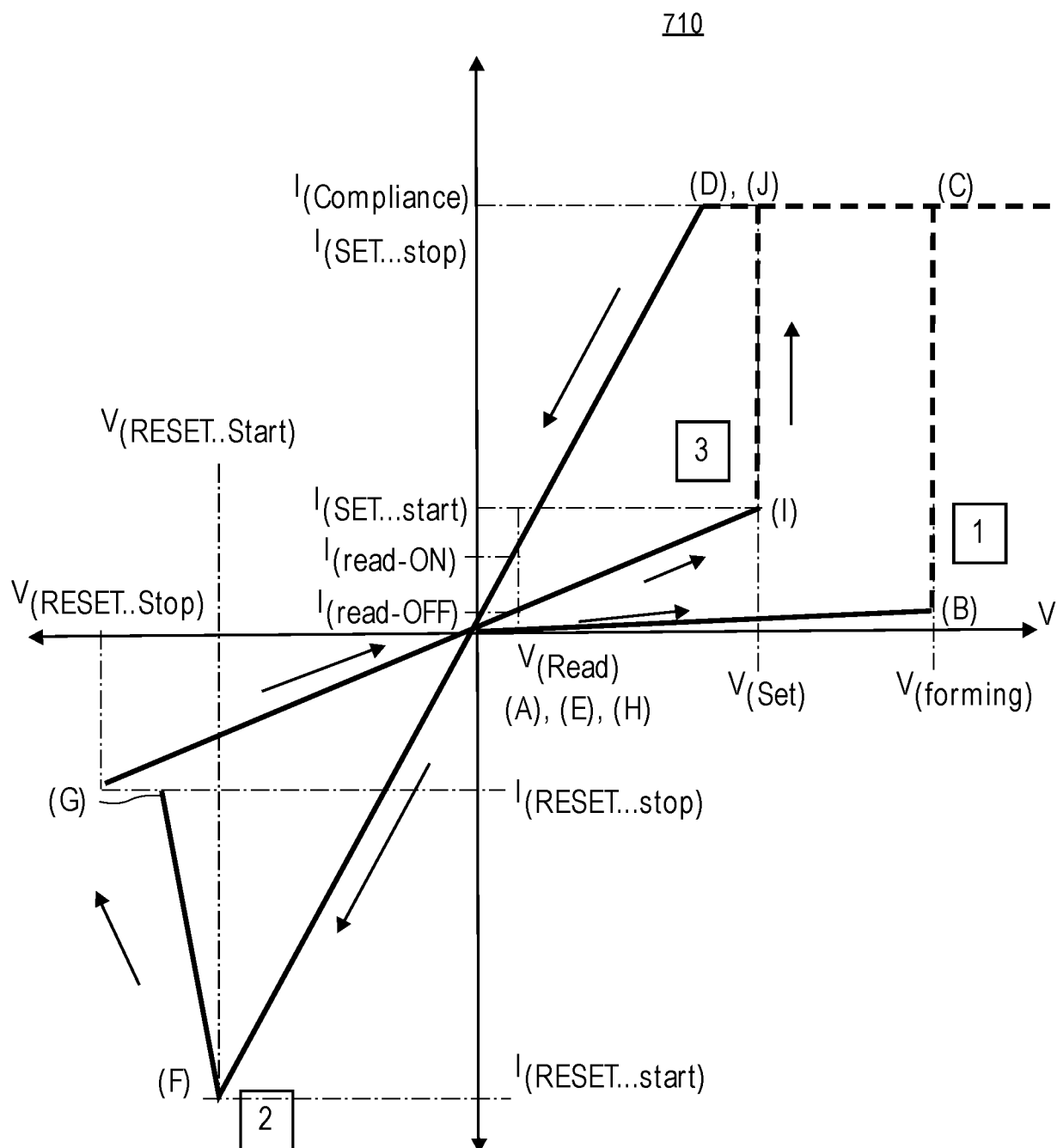


FIG. 6

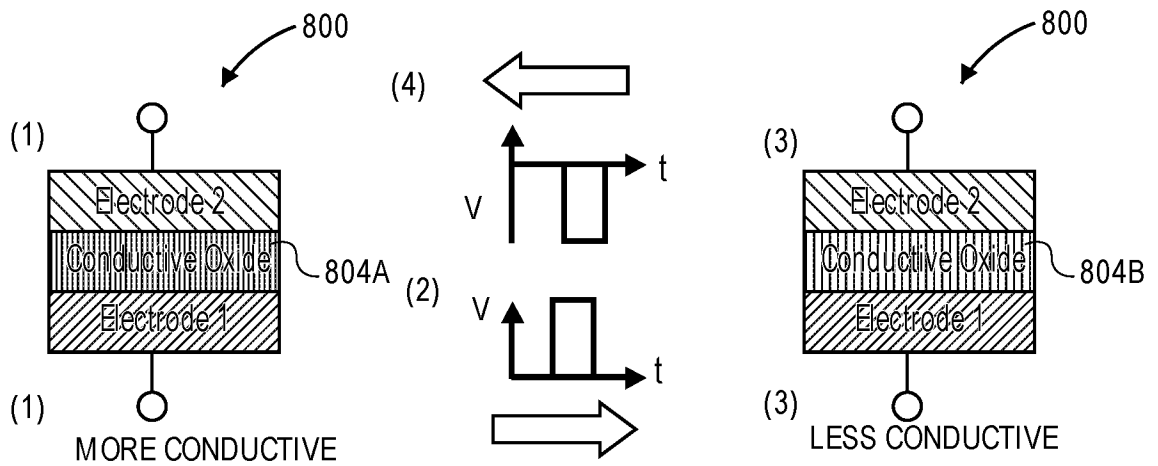
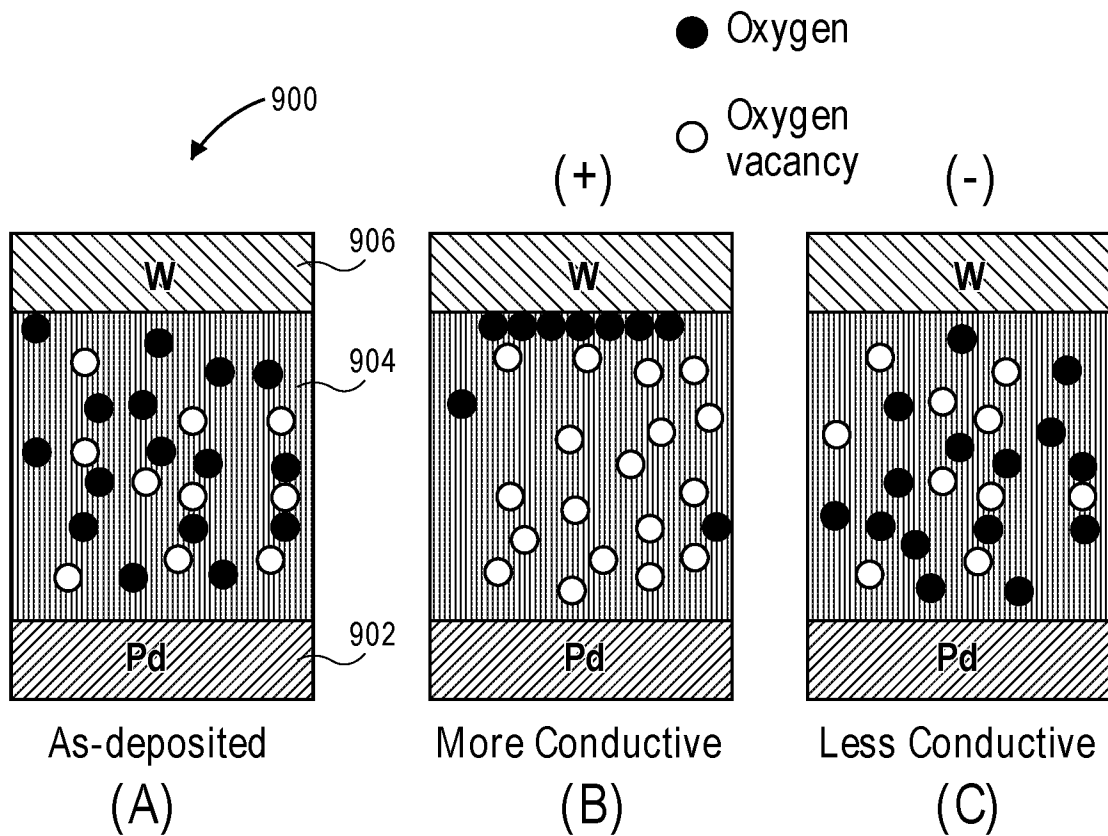
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**FIG. 7A**

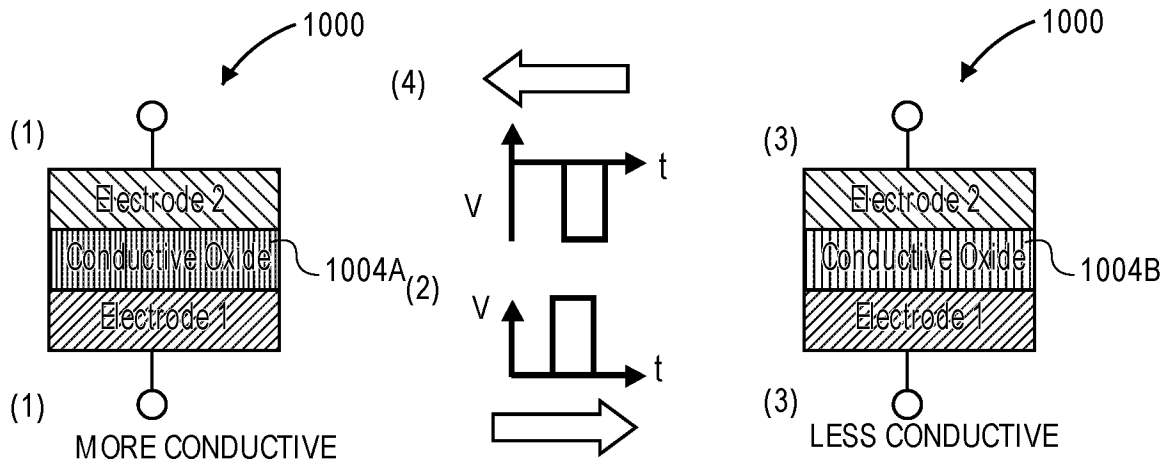
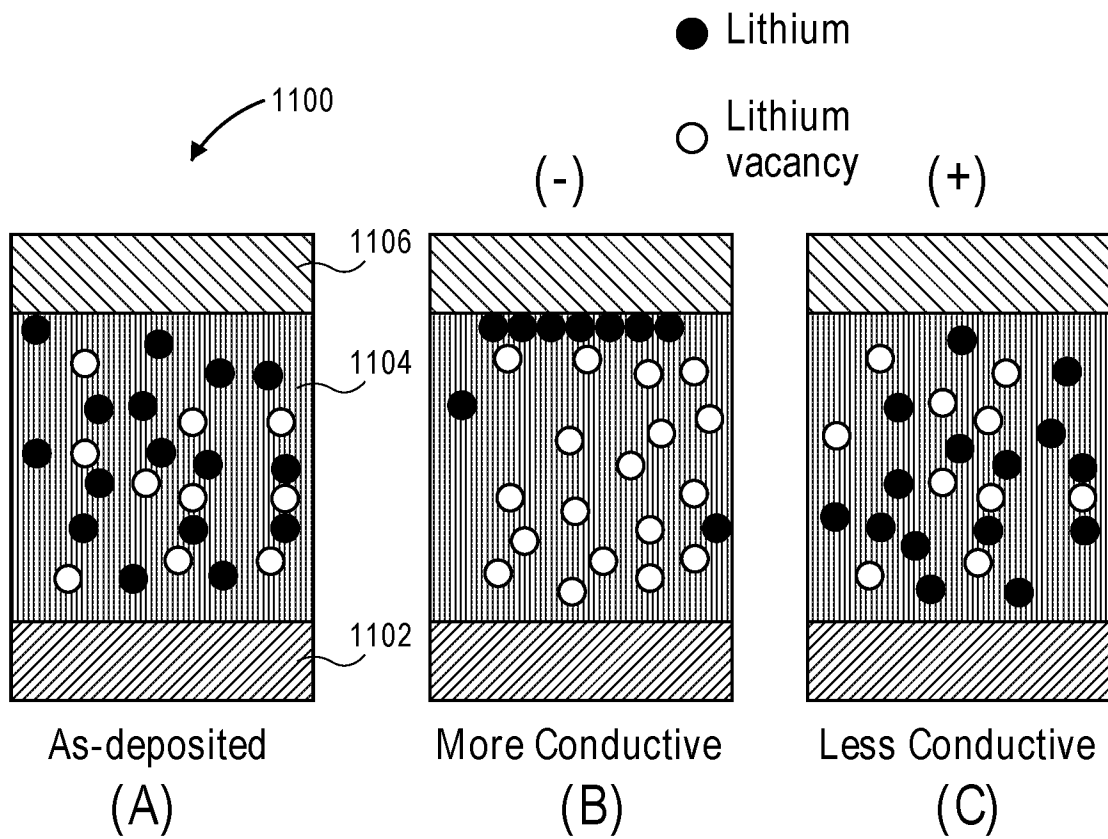
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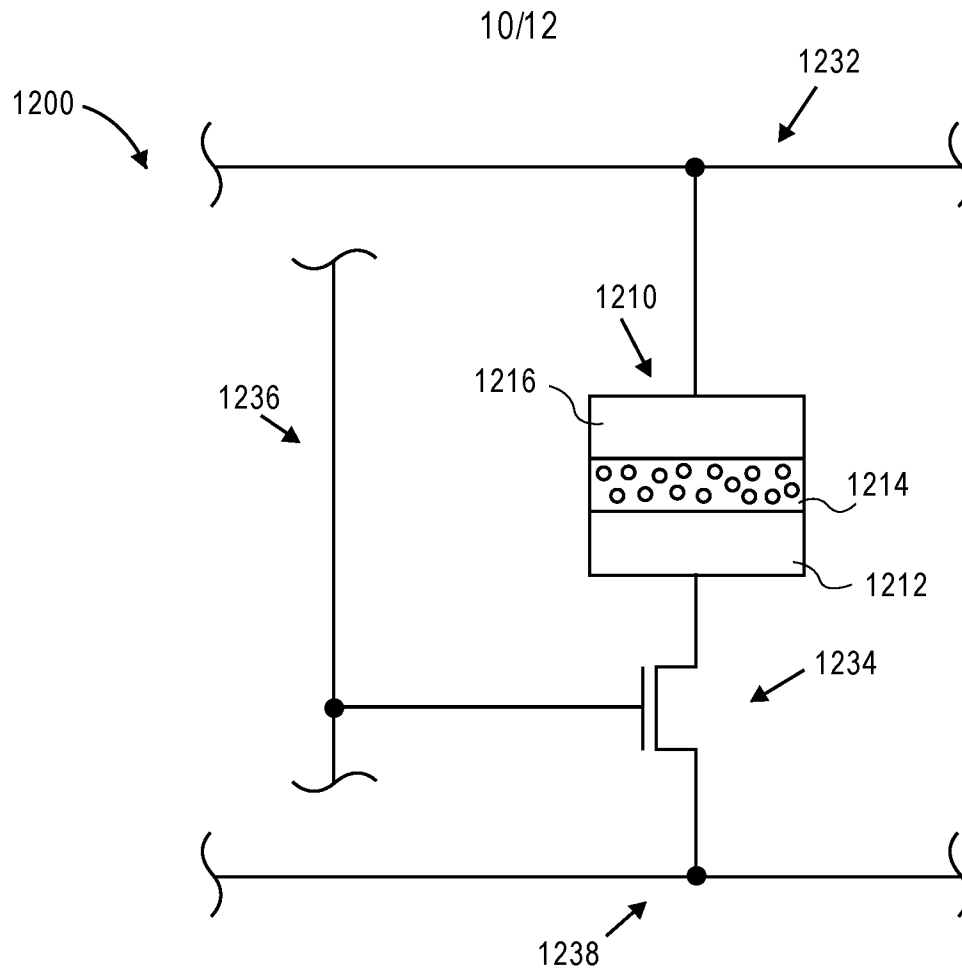
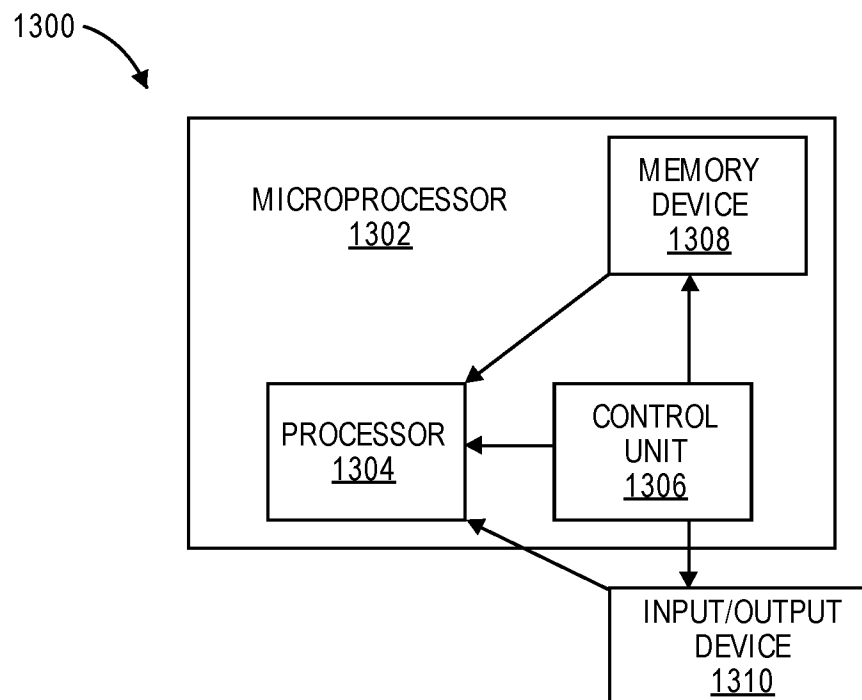
**FIG. 7B**

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**FIG. 8****FIG. 9**

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**FIG. 10****FIG. 11**

**FIG. 12****FIG. 13**

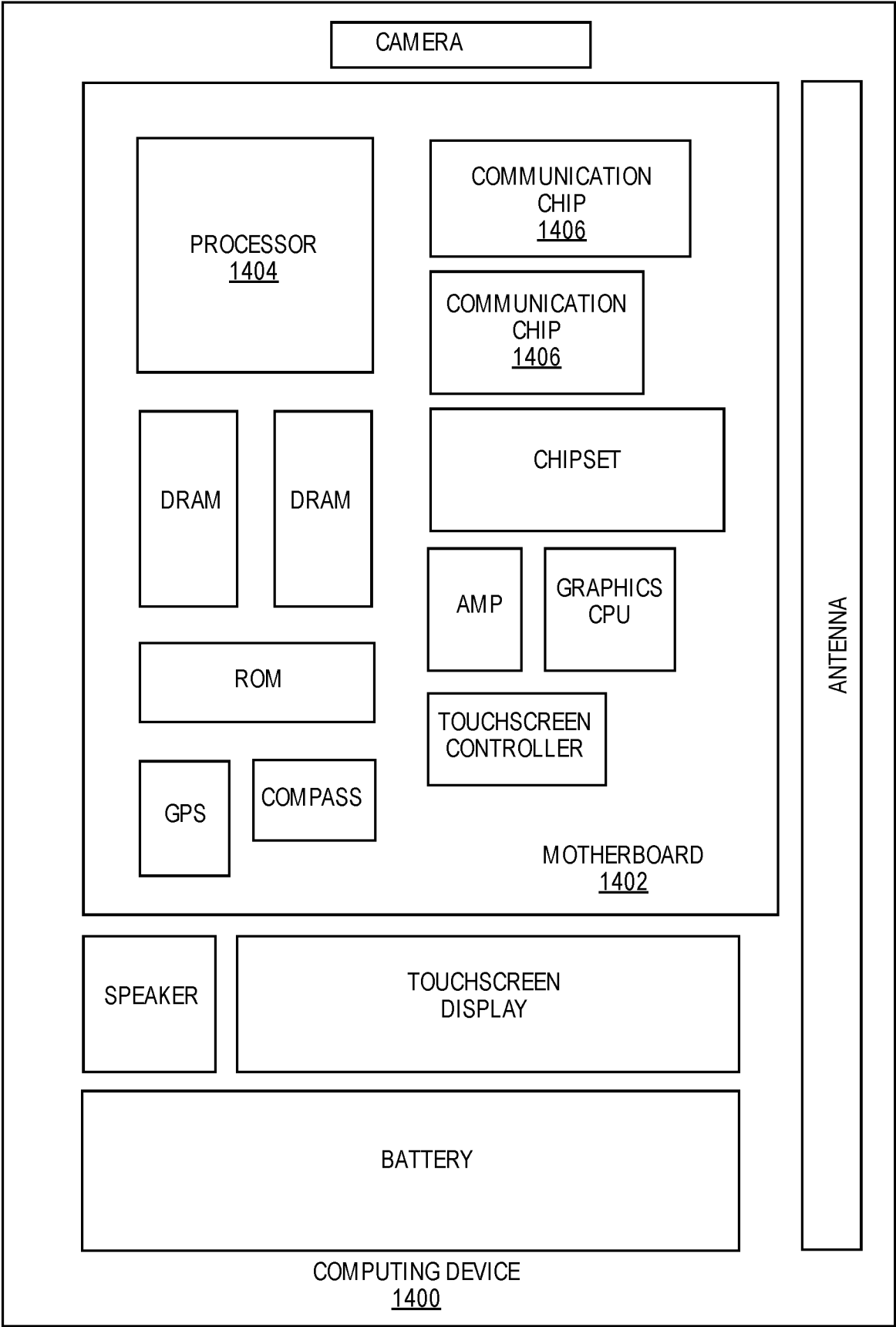


FIG. 14

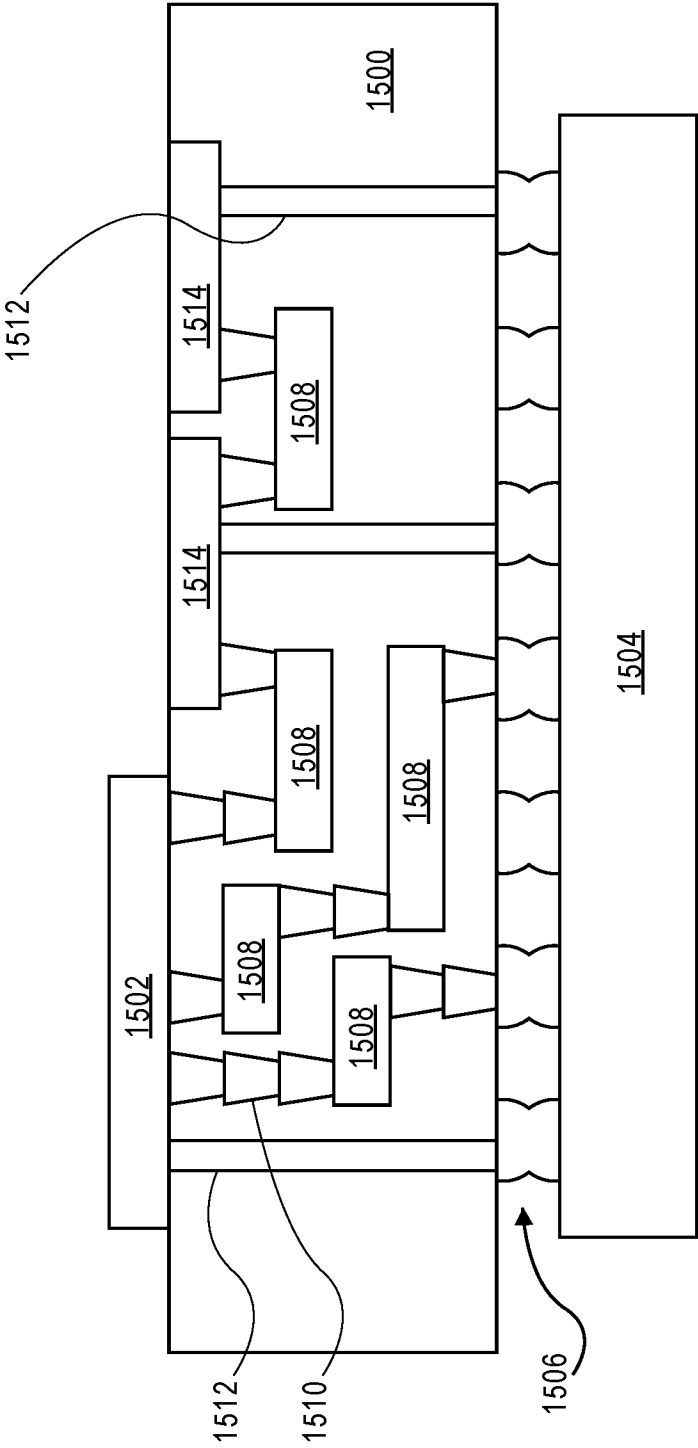


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040030**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i, H01L 27/10(2006.01)i, H01L 45/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; H01L 21/4763; H01L 45/00; H01L 47/00; H01L 23/538; H01L 21/00; H01L 27/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: resistive random access memory(RRAM), inter-layer dielectric(ILD), layer, conductive interconnect, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9178144 B1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 03 November 2015 See column 3, line 45 - column 4, line 15; column 4, lines 23-34; column 5, lines 8-61; column 7, lines 17-26; column 9, lines 36-62; column 10, lines 1-15; column 10, line 53 - column 11, line 15; and figures 2-3, 6, 14, 17-18.	1-7, 11-18, 22-25
Y		8-10, 19-21
Y	US 2014-0166961 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 19 June 2014 See paragraphs [0014]-[0016]; and figure 1A.	8-10, 19-21
A	US 7923285 B2 (ERH-KUN LAI et al.) 12 April 2011 See column 2, line 56 - column 7, line 44; and figures 1-2h.	1-25
A	US 8536558 B1 (SHYUE SENG (JASON) TAN et al.) 17 September 2013 See column 6, line 10 - column 7, line 62; and figures 18-29.	1-25
A	US 7833898 B2 (YU JIN LEE) 16 November 2010 See column 3, line 16 - column 4, line 65; and figures 1A-1E.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 March 2017 (23.03.2017)

Date of mailing of the international search report

23 March 2017 (23.03.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040030

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