A circuit (68) suitable to be utilized in an electronic ignition system or the like which receives periodic signal information and which is caused to ignore this information during a portion of each period a predetermined time interval after initiation of each period. The circuit comprises a blanking circuit (70) which is responsive to control signals generated from the input signal information at the predetermined time interval after initiation thereof to produce a blanking signal the duration of which last during the portion of the period and a coincidence gate (72) that is inhibited by the blanking signal but enabled during the remaining portion of each period to pass the signal information between an input (102) and output (98) thereof.
FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

<table>
<thead>
<tr>
<th>Code</th>
<th>Country</th>
<th>Code</th>
<th>Country</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT</td>
<td>Austria</td>
<td>KP</td>
<td>Democratic People’s Republic of Korea</td>
</tr>
<tr>
<td>AU</td>
<td>Australia</td>
<td>LI</td>
<td>Liechtenstein</td>
</tr>
<tr>
<td>BE</td>
<td>Belgium</td>
<td>LK</td>
<td>Sri Lanka</td>
</tr>
<tr>
<td>BR</td>
<td>Brazil</td>
<td>LU</td>
<td>Luxembourg</td>
</tr>
<tr>
<td>CF</td>
<td>Central African Republic</td>
<td>MC</td>
<td>Monaco</td>
</tr>
<tr>
<td>CG</td>
<td>Congo</td>
<td>MG</td>
<td>Madagascar</td>
</tr>
<tr>
<td>CH</td>
<td>Switzerland</td>
<td>MW</td>
<td>Malawi</td>
</tr>
<tr>
<td>CM</td>
<td>Cameroon</td>
<td>NL</td>
<td>Netherlands</td>
</tr>
<tr>
<td>DE</td>
<td>Germany, Federal Republic of</td>
<td>NO</td>
<td>Norway</td>
</tr>
<tr>
<td>DK</td>
<td>Denmark</td>
<td>RO</td>
<td>Romania</td>
</tr>
<tr>
<td>FI</td>
<td>Finland</td>
<td>SE</td>
<td>Sweden</td>
</tr>
<tr>
<td>FR</td>
<td>France</td>
<td>SN</td>
<td>Senegal</td>
</tr>
<tr>
<td>GA</td>
<td>Gabon</td>
<td>SU</td>
<td>Soviet Union</td>
</tr>
<tr>
<td>GB</td>
<td>United Kingdom</td>
<td>TD</td>
<td>Chad</td>
</tr>
<tr>
<td>HU</td>
<td>Hungary</td>
<td>TG</td>
<td>Togo</td>
</tr>
<tr>
<td>JP</td>
<td>Japan</td>
<td>US</td>
<td>United States of America</td>
</tr>
</tbody>
</table>
NOISE BLANKER CIRCUIT FOR USE WITH ELECTRONIC IGNITION SYSTEMS OR THE LIKE

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to electronic ignition systems or the like and more particularly to a noise blanker circuit for use therein to inhibit false signals from being generated due to system noise transients.

Description of the Prior Art

Electronic ignition systems which are operated in timed relationship to an automobile engine rpm for controlling a charge and discharge of an ignition coil to generate spark to operate the engine are well known in the art. Some contemporary ignition systems utilize adaptive dwell to control the power dissipated in the high energy ignition coil according to engine rpm. For example, Fig. 1 illustrates an adaptive dwell ignition system wherein the dwell current in the ignition coil is initiated anywhere from 25% - 90% after the initiation of a firing cycle depending upon the engine rpm and the current ramp time of the ignition coil as is generally understood. Because the ignition coil is a high energy device the current through the coil ramps very fast since the RL time constant of the coil is very low. Hence, voltage noise transients can be produced across the windings of the coil that may be equal to 2,000 volts or more. It has been observed that these voltage transients can be both inductively and capacitively coupled to the inputs of the ignition system and have a deleterious effect on the operation thereof. For example, in normal operation of the ignition system the coil dwell current is produced some time after the first 25% time period of the firing cycle and is allowed to ramp up through the coil to a maximum current value at which time...
the current is limited. At the end of the firing cycle, in response to the initiation of the next succeeding firing cycle, a spark command signal is generated by the ignition system to cause the coil to be discharged which creates the spark necessary to operate the engine. It has been observed that due to the low RL time constant to the coil that the dwell current therethrough produces voltage transients across the windings of the coil to cause the ignition system to generate what appears to be a valid spark command signal. This can cause a misspark or no spark to occur at the correct time during the firing cycle period which may damage the engine. These voltage transients normally decay to a sufficiently low level within 1-1/2 milliseconds after initiation of the coil current.

Thus, there is a need for a blanking circuit to be utilized in combination with an electronic ignition system or the like that requires a minimal number of components for blanking out a portion of each periodic signal input supplied thereto for a predetermined time interval after initiation of each period in order to prevent false output signals from occurring at the output of the system due to noise transients.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a blanking circuit for use with an electronic ignition system or the like to inhibit noise transients coupled to the inputs of the system from deleteriously affecting the operation thereof.

In accordance with the above and other objects there is provided a noise blanking circuit in combination with an adaptive dwell ignition system which charges and discharges an ignition coil in response to input signals supplied in an input thereof in time relationship to the operation of
an engine. The noise blanking circuit is responsive to the ignition system generating a dwell current for inhibiting the system from responding to noise transients occurring thereafter until such time that the magnitude of the dwell current reaches a predetermined value. The noise blanking circuit comprises a blanking signal circuit for providing a blanking signal for a predetermined time interval after initiation of the dwell current and a coincidence circuit responsive to an input thereof at all times except when the blanking signal is supplied thereto which inhibits the operation of the coincidence circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial block and schematic diagram of an adaptive dwell ignition system;

Fig. 2 illustrates waveforms useful for understanding the operation of the blanking circuit of the preferred embodiment of the invention; and

Fig. 3 is a schematic diagram of a blanking circuit of the preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Turning to Fig. 1 there is shown adaptive dwell electronic ignition system 10 which is suitable to be manufactured in integrated circuit form of which the operation is generally understood by those skilled in the art. Electronic ignition system 10 receives timing signals at inputs 12 and 14 which are generated in timed relationship to an automobile engine and provides dwell current at output terminal 16 to charge ignition coil 18 to a predetermined maximum current level at which level the current is limited prior to the ignition system generating a fire command to cause discharge of the ignition coil to generate spark in the engine. Briefly, in response to the
timing signals supplied thereto, a generally square wave output signal is produced at the output of comparator 20 at node 22 in the form as shown by waveform A of Fig. 2. Therefore, in response to the ignition timing signals crossing a zero axis in a positive direction, the output of comparator 20 goes positive to clock D-flip-flop 24 to produce a logic one at the Q output thereof to render current source 26 operative. Current source 26 as well as current source 28 are connected at node 30 to capacitor 32 such that this capacitor is caused to be discharged at a rate proportional to 31 until such time that the voltage potential thereacross decreases below the bias voltage V1 which causes comparator 34 to reset flip-flop 24. As flip-flop 24 is reset current source 26 is rendered nonconductive to allow charging of capacitor 32 at a rate proportional to the current I supplied from current source 28. Bias voltage V1 has a magnitude which under normal engine and ignition system operating conditions cause capacitor 32 to be discharged for 25% and charged for the remaining 75% of each firing cycle time interval. Hence, logic gate 36 is inhibited during the first quarter cycle of each firing cycle as an input thereto is provided by the Q output from flip-flop 24. Thus, predriver amplifier 38 is maintained in a nonconductive state so that dwell current cannot be produced at output terminal 16 of ignition system 10 during the first 25% of each firing cycle. Capacitor 32 is also coupled to the noninverting input of comparator 40 to produce an output therefrom until such time that the capacitor is discharged to a value equal to the bias voltage Vh. A coincidence gate 42 is provided for rendering current source 44 operative to discharge an adaptive dwell capacitor 46 whenever the inputs thereto are at a logic one level. All of the inputs to coincidence gate 42 will be at a logic one whenever the engine is: (1) operating (not in a stall condition), (2) the output from comparator 40 is high and (3) the Q output
of D flop 24 is at a logic one. Hence, adaptive dwell capacitor 46 is discharged by current source 44 during the first quarter cycle of each firing cycle. Thereafter, with coincidence gate 42 being inhibited, the potential across the adaptive dwell capacitor is maintained substantially constant until coincidence gate 48 is enabled by the current through the ignition coil 18 being limited at time t₃ (Fig. 2C) which enables current source 50 to charge the adaptive dwell capacitor 46 at a rate proportional to the current supplied thereto until time t₄ when the ignition coil 18 is discharged. Amplifier 38 is maintained in an off condition until such time that the magnitude of the potential appearing across capacitor 32 exceeds the threshold magnitude across adaptive dwell capacitor 46 which provides an output from comparator 52 to AND gate 54. Assuming that the Q output of flip-flop 24 is high (which occurs during the last 75% of each firing cycle time interval) coincidence gate 36 is enabled by the output from AND gate 54 to turn on preamplifier 38 to provide base drive to the external Darlington power amplifier 56 which produces dwell current in ignition coil 18. Simultaneously, a dwell signal is generated at the output of logic gate 58 whenever dwell current flows in ignition coil 18. The dwell current ramps up through ignition coil 18 between t₁-t₃ (Fig. 2C) until a voltage is developed across sense resistor 60, which is applied at terminal 62 to the noninverting input of comparator 64, becomes greater than the potential V_{ref} which is applied to the inverting input thereof. Thus, when the voltage across sense resistor exceeds V_{ref} comparator 64, which has an output coupled to output terminal 16, linearly regulates the current through amplifier 56 to limit the current through ignition coil 18. Simultaneously, an output is generated from comparator 64 to coincidence gate 66 which produces a logic output signal I\text{LIMIT} to enable coincidence gate 48. At time t₄, in response to the timing signals at
terminals 12 and 14 crossing a zero axis in a positive direction, the output from comparator 20 is switched to an upper level state (waveform A, Fig. 2) which again clocks flip-flop 24 whereby the Q output goes to a logic zero state to inhibit coincidence gate 36 which in turn renders amplifiers 38 and 56 nonconductive to discharge the coil.

A problem arises in ignition system 10 due to the high energy ignition coil producing a high voltage transients across the secondary winding thereof whenever the coil is turned on as is shown at time t₁ of Fig. 2. These voltage transients produce erroneous switching of comparator 20 and can adversely affect the operation of the ignition system. Blanking circuit 68 illustrated in Fig. 3 prevents these voltage transients from effecting the operation of the ignition system as will be hereinafter explained.

Blanking circuit 68 is adapted to be coupled between node 22 and the clock input of D-flip-flop 24 and comprises a blanking circuit portion 70 and a coincidence circuit 72 which utilize known integrated injection logic (I²L) technology for fabrication of the coincidence gates hereinafter referred to. Blanking circuit portion 70 includes a current mirror circuit 74, transistor 76 and coincidence gate 78. Current mirror 74 and transistor 76 form a comparator circuit with current mirror 74 including transistors 80 and 82 with transistor 80 being connected as a diode having its collector connected in common to the base thereof. The emitter of transistor 80 is connected to a reference potential the magnitude of which is equal to one-half Vref where Vref is equivalent to the magnitude at which the current through ignition coil 18 is limited. A current source 84 sources current to the collector and base of transistor 80 and has a magnitude associated therewith which is substantially equal to the magnitude supplied by current source 86 to node 88. Transistor 82 of current mirror 74 has its collector
coupled to node 88, its base connected in common with the base of transistor 80 and its emitter coupled to node 62, across sense resistor 60. The output of current mirror 74 is taken at the collector of transistor 82 and is supplied to transistor 76 which has its base connected to node 88 and its emitter to ground reference. Coincidence gate 78, the input of which is coupled to the collector of transistor 76 and to electronic ignition system 10, receives a dwell signal (waveform B of Fig. 2) therefrom.

Coincidence gate 78 has a pair of outputs connected across the input and output of coincidence gate 90 and to the respective inputs of coincidence gates 92 and 94 respectively of coincidence circuit 72. The output of comparator 20 is coupled at node 102 to the inputs of coincidence gates 90 and 92. The output of coincidence gate 92 is connected to an input of coincidence gate 96 and output of which is connected to the clock input of flip-flop 24 via lead 98. The output of coincidence gate 94 is connected to the input of coincidence gate 100 with the output thereof cross-connected to the input of coincidence gate 96 which has a second output cross-connected to the input of gate 100.

Referring to Fig. 2 the operation of blanking circuit 68 can be fully described. For explanation purposes, it is assumed that the timing signal supplied to input terminals 12 and 14 of ignition system 10 have crossed a zero axis in a negative direction at time \( t_0 \) such that the output from comparator 20 (waveform A, Fig. 2) has switched to a low level state which corresponds to a "zero" logic input at node 102 of logic circuit 68. Assuming, at \( t_0 \), the potential across capacitor 32 is less than the threshold potential appearing across adaptive dwell capacitor 46, amplifier 38 is in a nonconductive state such that a logic zero appears at the output of gate 58 which corresponds to the dwell signal (waveform B, Fig. 2) being zero at time \( t_0 \). Without a dwell control signal, no dwell current flows in ignition coil 18 as seen by waveform C of Fig. 2.
whereby the voltage across sense resistor 60 is nominally zero. In this state, transistor 82 of current mirror 74 is in a saturated state such that transistor 76 is rendered nonconductive. This provides a logic "one" to the input of coincidence gate 78. Hence, with the dwell control signal (waveform B of Fig. 2) being applied to the input of coincidence gate 78, the output therefrom is at a logic one which allows the output of coincidence circuit 72 to follow the input supplied thereto at node 102 wherein the output via lead 98 at time t₀ is forced to go to a low state (waveform E of Fig. 2). Thus, as long as the dwell control signal is zero, the output from logic circuit 72 follows the output signal appearing at the output of comparator 20. At time t₁, when amplifier 38 is rendered conductive to produce dwell current to ignition coil 18, the dwell control signal (waveform B of Fig. 2) goes from a logic zero state to a logic one state which thereby causes the outputs of coincidence gate 78 to go to a logic zero. Hence, the output of coincidence circuit 72 is latched in a low level output condition whereby the circuit cannot respond to any changes in the output level state of the output signal supplied from comparator 20 to the input thereof at node 102. Therefore, the corrected input to the clock input of D-type flip-flop 24 remains in a low level state from time t₀ to time t₂ regardless of the output level state of comparator 20. Hence, the voltage transients which appear on the output of comparator 20 (waveform A, Fig. 2) do not appear at the output of logic circuit 72, the corrected input to flip-flop 24 of ignition system 10. However, at time t₂ when the current through ignition coil 18 has ramped up to a value which produces a voltage across sense resistor 60 substantially equal to one-half V_{ref}, current mirror 74 becomes balanced such that any incremental change in the coil current causes base current drive to be supplied to the base of transistor 76 to render this transistor conductive to supply a logic zero
to the input of coincidence gate 78. Thereafter, coincidence circuit 72 will respond to the output signal state from comparator 20 since the output of coincidence gate 78 is now a logic one. Thus, at time $t_4$, when the output of comparator 20 goes to a high level output state the output from logic gate 96 correspondingly changes to a high output level state.

Hence, what has been described above, is a novel blanking circuit for use in combination with an adaptive dwell electronic ignition system wherein a predetermined time delay is generated after initiation of dwell current wherein any input signals supplied to the ignition system are blanked which inhibit noise transients from erroneously causing the ignition system to generate spark command signals. This time delay is generated by sensing the ignition coil current and causing the ignition system to remain in a latched state until such time that the magnitude of the coil current has reached approximately one-half its final value. Typically this time delay occurs for approximately two milliseconds following ignition coil turn on which is sufficient to allow any voltage transients caused by the ignition coil being turned on to decay down to a sufficiently low enough level as not to deleteriously affect the ignition system.
Claims

1. A circuit having an input and an output which is responsive to periodic input signals applied to the input for transferring the same to the output at which is connected load circuit means, the circuit being made non-responsive to changes in the input signals which can occur during a portion of each period of each individual input signal a predetermined time interval after initiation of each periodic input signal due to noise transients being coupled onto each periodic input signal, comprising:
   blanking circuit means responsive to control signals generated in response to each periodic input signal for producing a blanking signal at an output thereof during the portion of each period; and
   coincidence circuit means having an input and output, said input being coupled both to said output of said blanking circuit means and the input of the circuit, said output being coupled to the output of the circuit, said coincidence circuit means transferring the periodic input signals between said input and output except during the portion of each period when said coincidence circuit means is inhibited by said blanking signal.

2. The circuit of claim 1 wherein said blanking circuit means includes:
   comparator means having an output which is responsive to the magnitude of one of said control signals reaching a predetermined value sometime after the predetermined time interval after initiation of each individual periodic input signal for changing the signal appearing at said output from a first level state to a second level state; and
   a first coincidence gate coupled to said output of said comparator means and receiving a second one of the control signals for producing said blanking signal at said
output of said blanking circuit means upon coincidence of
said second control signal and said output signal from said
comparator means being in said first level state.

3. The circuit of claim 2 wherein said comparator
means includes:

- a current mirror circuit adapted to receive said
  first control signal and a reference potential at
  respective inputs, said current mirror circuit supplying an
  output current at an output thereof in response to said
  magnitude of said first control signal exceeding the
  magnitude of said reference potential; and

- output circuit means coupled between said output
  of said current mirror circuit and said output of said
  comparator means for causing the output of said comparator
  to switch to said second output level in response to said
  current supplied by said current mirror circuit to the
  input thereof, said output circuit including a transistor
  having first, second and control electrodes, said first
  electrode being coupled to a terminal at which is supplied
  ground reference potential, said second electrode being
  coupled to said output of said comparator means, said
  control electrode being coupled to said output of said
  current mirror circuit.

4. The circuit of claim 3 wherein said first
coinincidence gate having a second output coupled to said
coinincidence circuit means.

5. The circuit of claim 4 wherein said coinincidence
coinincidence circuit means includes:

- a second coinincidence gate having an input and
  output, said input being coupled to said input of said
  coinincidence circuit means;

- third and fourth coinincidence gates each having an
  input and an output, said input of said third coinincidence
  gate means being coupled to said input of said coinincidence
circuit means, said input of said fourth coincidence gate
being coupled to said second output of said first
coincidence gate and to said output of said second
coincidence gate; and

latch circuit means having first and second
inputs respectively coupled to said outputs of said third
and fourth coincidence gates and an output coupled to said
output of the coincidence circuit means.

6. In an ignition system responsive to periodic
timing signal information generated in timed relationship
to an engine rpm for producing dwell current a predeter-
mined time interval after initiation of each timing signal
information period to an ignition coil, a circuit for
cauusing the ignition system to ignore the timing signal
input information for a predetermined portion of each
period occurring after the predetermined time interval when
the dwell current is initiated, comprising:
a blanking circuit responsive to the dwell
current being produced for producing a blanking signal at
an output the duration of which lasts for said predeter-
mined portion of each period; and

a coincidence circuit having an input coupled to
said output of said blanking circuit and receiving said
timing signal information and an output, said coincidence
circuit being inhibited by said blanking signal whereby the
timing signal information is not transferred to the output
thereof.

7. The circuit of claim 6 wherein said blanking
circuit means includes:

comparator means having an output which is
responsive to the magnitude of a control signal supplied
thereto reaching a predetermined value sometime after the
predetermined time interval after initiation of each
individual periodic input signal for changing the output
signal appearing at said output from a first level state to a second level state; and
a first coincidence gate coupled to said output of said comparator means and receiving said dwell control signal indicative of said dwell current for producing said blanking signal at said output of said blanking circuit means upon coincidence of said dwell control signal and said comparator means output being in said first level state.

8. The circuit of claim 7 wherein said comparator means includes:
a current mirror circuit adapted to receive said first control signal and a reference potential at respective inputs, said current mirror circuit supplying an output current at an output thereof in response to said magnitude of said first control signal exceeding the magnitude of said reference potential; and
a transistor having first, second and control electrodes, said first electrode being coupled to a terminal at which is supplied a ground reference potential, said second electrode being coupled to said output of said comparator means, said control electrode being coupled to said output of said current mirror circuit.

9. The circuit of claim 8 wherein said first coincidence gate having a second output coupled to said coincidence circuit means.

10. The circuit of claim 9 wherein said coincidence circuit means includes:
a second coincidence gate having an input and output, said input being coupled to said input of said coincidence circuit means;
third and fourth coincidence gates each having an input and an output, said input of said third coincidence gate means being coupled to said input of said coincidence
circuit means, said input of said fourth coincidence gate being coupled to said second output of said first coincidence gate and to said output of said second coincidence gate; and

5 latch circuit means having first and second inputs respectively coupled to said outputs of said third and fourth coincidence gates and an output coupled to said output of the coincidence circuit means.
FIG 2

FIG 3
### I. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both National Classification and IPC:

- INT. CL. F 02P 3/04
- H 03K 17/16
- U.S. CL. 123/618, 645; 307/542

### II. FIELDS SEARCHED

<table>
<thead>
<tr>
<th>Classification System</th>
<th>Classification Symbols</th>
</tr>
</thead>
<tbody>
<tr>
<td>U.S.</td>
<td>123/609, 618, 644, 645</td>
</tr>
<tr>
<td></td>
<td>307/542, 544</td>
</tr>
</tbody>
</table>

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched:

### III. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of Document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to Claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>US, A, 3,052,850, PUBLISHED 04 SEPT. 1962 PLUHR.</td>
<td>1-10</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 3,898,482, PUBLISHED 05 AUG. 1975, HOLT, JR.</td>
<td>1-10</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 3,960,129, PUBLISHED 01 JUNE 1976, HOFER ET AL.</td>
<td>1-10</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 4,008,698, PUBLISHED 22 FEB. 1977, GARTNER.</td>
<td>1-10</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 4,246,200, PUBLISHED 03 FEB. 1981, SUGIURA ET AL.</td>
<td>1-10</td>
</tr>
</tbody>
</table>

* Special categories of cited documents:
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier document but published on or after the international filing date
  - "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  - "O" document referring to an oral disclosure, use, exhibition or other means
  - "P" document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"A" document member of the same patent family

### IV. CERTIFICATION

Date of the Actual Completion of the International Search: 28 July 1982

Date of Mailing of this International Search Report: 18 Aug 1982

International Searching Authority: ISA/US

Signature of Authorized Officer: T. M. Argenbright