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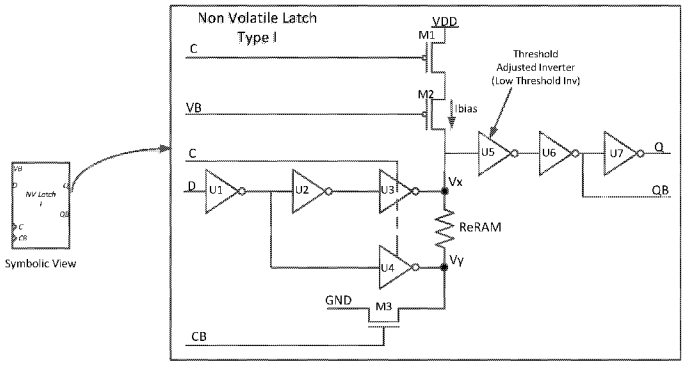

FIGURE 1

(57) Abstract: A non-volatile latch circuitry, comprising a Re RAM cell configured to store a final value of the non-volatile latch circuitry; a data selection circuitry configured to connect or disconnect a data input to a plus voltage node and a minus voltage node of the Re Ram cell depending on a clock input voltage level; a pull down transistor configured to set a first voltage level at the minus voltage node to a logically low voltage level if the data input is not connected to the plus and minus voltage nodes of the Re RAM cell; a bias circuitry configured to provide a fix bias current to set a second voltage level at the plus voltage node to a varying voltage level depending on the resistor value of the Re RAM cell if the data input is not connected to the plus voltage node; and a threshold adjusted circuitry arranged to convert an analog value of the second voltage level into a digital value and configured to generate an output signal and / or an inverted output signal.

WO 2014/184752 A1

CMOS Compatible Non-Volatile Latch and D-Flip Flop Using Resistive Switching Materials

Technical field

The invention relates to CMOS compatible non-volatile D-latch and D-flip-flop structures constructed by Resistive Switching Materials.

Background

In advanced technology nodes, as the dimensions of the devices get smaller and high speed operation of the circuits is required, the power consumption of the logical circuits becomes more crucial. To overcome this issue several techniques are realized such as voltage scaling, power and clock gating. When the power is turned down through the power gating, the computed data inside the logical circuits become volatile. Thus the storage of the data is very important in such kind of applications. Using non-volatile latches or non-volatile flip-flop structures, power gating would not cause any data loss and these non-volatile elements make the circuitry more reliable in terms of the data storage.

A Re-RAM based non-volatile flip-flop which is optimized for sub-VT operation is generally known in I. Kazi et al., "A ReRAM-based non-volatile flip-flop with sub-VT read and CMOS voltage-compatible write," IEEE NEWCAS, 2013. Sub-VT operation enables energy-efficient VLSI systems with zero leakage power states. The disadvantage of the generally known Re-Ram based non-volatile flip-flop is that non-volatile read and write operation is not performed in each clock cycle thereby requiring extra control signals to perform the write and read operation.

One aim of the present invention is to provide a solution to the above discussed disadvantage.

Summary of invention

In a first aspect the invention provides a non-volatile latch circuitry, comprising a ReRAM cell configured to store a final value of the non-volatile latch circuitry; a data selection circuitry configured to connect or disconnect a data input to a plus voltage node and a minus voltage node of the ReRam cell depending on a clock input voltage level; a pull down transistor con-

figured to set a first voltage level at the minus voltage node to a logically low voltage level if the data input is not connected to the plus and minus voltage nodes of the ReRAM cell; a bias circuitry configured to provide a fix bias current to set a second voltage level at the plus voltage node to a varying voltage level depending on the resistor value of the ReRAM cell if the data input is not connected to the plus voltage node; and a threshold adjusted circuitry arranged to convert an analog value of the second voltage level into a digital value and configured to generate an output signal and / or an inverted output signal.

In a preferred embodiment of the non-volatile latch circuitry, the data selection circuitry comprises a first inverter with a first input port and a first output port, a second inverter with a second input port and a second output port, a first tri-stated inverter with a third input port, a third output port and a first enable port, and a second tri-stated inverter with a fourth input port, a fourth output port and a second enable port. The first inverter is configured to connect the data input to the first input port, and to connect the second input port and the fourth input port to the first output port. The second inverter is further configured to connect the second output port to the third input port. The first tri-stated inverter is further configured to connect the plus voltage node to the third output port and the clock input to the first enable port. The second tri-stated inverter is further configured to connect the minus voltage node to the fourth output port, and the clock input to the second enable port.

In a further preferred embodiment of the non-volatile latch circuitry, the data selection circuitry comprises a first OR gate with a first OR gate input port, a second OR gate input port and a first OR gate output port, a first AND gate with a first AND gate input port, a second AND gate input port and a first AND gate output port, a second OR gate with a third OR gate input port, a fourth OR gate input port and a second OR gate output port. The first OR gate is configured to connect an inverted clock input to the first OR gate input port, the data input to the second OR gate input port, and a gate of a second PMOS transistor to the first OR gate output port; the first AND gate is configured to connect the clock input to the first AND gate input port, the data input to the second AND gate input port, and a gate of a second NMOS transistor to the first AND gate output port; the second OR gate is configured to connect the inverted clock input to the third OR gate input port, the inverted data input to the fourth OR gate input port, a gate of a first PMOS transistor to the second OR gate output port, and a gate of a first NMOS transistor to the second OR gate output port; the first NMOS transistor further including a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the minus voltage node of the ReRAM cell to the drain input; the first PMOS transistor further including a drain

input and a source input, and being further configured to connect a logically high voltage input to the source input, and the minus voltage node of the ReRAM cell to the drain input; the second NMOS transistor further including a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the plus voltage node of the ReRAM cell to the drain input; and the second PMOS transistor further including a drain input and a source input, being further configured to connect the logically high voltage input to the source input, and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment of the non-volatile latch circuitry, the bias circuitry comprises a first PMOS transistor and a second PMOS transistor, wherein the first PMOS transistor includes a gate input, a drain input and a source input configured to connect the clock input to the gate input, the logically high voltage to the source input, and a source input of the second PMOS transistor to the drain input; and the second PMOS transistor includes a gate input, a drain input and a source input configured to connect a bias voltage input to the gate input, the drain of the first PMOS transistor to the source, and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment of the non-volatile latch circuitry, the threshold adjusted circuitry comprises a threshold adjusted inverter, a first inverter, and a second inverter , wherein the threshold adjusted inverter includes an input port and an output port configured to connect the plus voltage node of the ReRAM cell to the input port and an input port of the first inverter to the output port; the first inverter includes an input port and an output port configured to connect the output of the threshold adjusted inverter to the input port , the inverted output signal to the output port, and an input of the second inverter to the output port; and the second inverter includes an input port and an output port configured to connect the output of the first inverter to the input port and the output signal to the output port.

In a further preferred embodiment of the non-volatile latch circuitry, this further comprises an asynchronous reset circuitry in the data selection circuitry, configured to set the first voltage node and the second voltage node of the ReRAM cell to program the ReRAM to high resistor value with reset input signal.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous reset circuitry comprises a NAND gate, an OR gate, a first tri-stated inverter, and a second tri-stated inverter, wherein the NAND gate includes a first input port, a second input port and an output port configured to connect the data input to the first input port, the reset input to the

second input port, an input port of a inverter to the output port, and an input port of the second tri-stated inverter to the output port; the OR gate includes a first input port, a second input port and an output port configured to connect the clock input to the first input port, the inverted reset input to the second input port and an enable port of the first tri-stated inverter, and an enable port of the second tri-stated inverter to the output port; the inverter includes the input port and an output port configured to connect the output port of the NAND gate to the input port and an input port of the first tri-stated inverter to the output port; the first tri-stated inverter includes the input port, an output port and the enable port configured to connect to the output port of the inverter to the input port, the plus voltage node of ReRAM cell to the output port, and the output port of the OR gate to the enable port; and the second tri-stated inverter includes the input port, an output port and the enable port configured to connect to the output port of the NAND gate to the input port, the minus voltage node of ReRAM cell to the output port and the output port of the OR gate to the enable port.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous reset circuitry comprises a first OR gate, a first AND gate, a second OR gate, a second AND gate, a third AND gate, a third OR gate, a first NMOS transistor, a first PMOS transistor, a second NMOS transistor, and a second PMOS transistor, the first OR gate including a first input port, a second input port and an output port configured to connect an inverted clock input to the first input port, the data input to the second input port, and a first input port of the second AND gate to the output port; the first AND gate including a first input port, a second input port and an output port configured to connect the clock input to the first input port, the data input to the second input port, and a first input port of the third AND gate to the output port; the second OR gate including a first input port, a second input port and an output port configured to connect the inverted clock input to the first input port, the inverted data input to the second input port, and a first input port of the third OR gate to the output port; the second AND gate including the first input port, a second input port and an output port configured to connect the output port of the first OR gate to the first input port; the reset input to the second input port, and a gate of the second PMOS transistor to the output port; the third AND gate including the first input port, a second input port and an output port configured to connect the output port of the first AND gate to the first input port, the reset input to the second input port, and a gate of the second NMOS transistor to the output port; the third OR gate including the first input port, a second input port and an output port configured to connect the output port of the second OR gate to the first input port, the inverted reset input to the second input port, a gate of the first NMOS transistor to the output port,

and a gate of the first PMOS transistor to the output port; the first NMOS transistor including the gate input, a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the minus voltage node of the ReRAM cell to the drain input; the first PMOS transistor including the gate input, a drain input and a source input, and being further configured to connect the logically high voltage input to the source input, and the minus voltage node of the ReRAM cell to the drain input; the second NMOS transistor including the gate input, a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the plus voltage node of the ReRAM cell to the drain input; and the second PMOS transistor including a gate input, a drain input and a source input, and being further configured to connect the logically high voltage input to the source input, and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment of the non-volatile latch circuitry, the bias circuitry comprises an OR gate, a first PMOS transistor, and a second PMOS transistor, the OR gate including a first input port, a second input port and an output port configured to connect the clock input to the first input port and the inverted reset input to the second input port, and a gate input of the first PMOS transistor to the output port; the first PMOS transistor including the gate input, a drain input and a source input, and being further configured to connect the logically high voltage to the source input, and a source input of the second PMOS transistor to the drain input; and the second PMOS transistor including gate input, a drain input and the source input configured to connect the bias voltage input to the gate input, the drain of the first PMOS transistor to the source, and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment the non-volatile latch circuitry, further comprises an asynchronous set circuitry in the data selection circuitry configured to set the first voltage node and the second voltage node of the ReRAM cell to program the ReRAM to low resistor value with reset input signal.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous set circuitry comprises a NOR gate, an OR gate, an inverter, a first tri-stated inverter, a second tri-stated inverter, the NOR gate including a first input port, a second input port and an output port configured to connect the data input to the first input port, the inverted set input to the second input port, an input port of the inverter to the output port, and an input port of the second tri-stated inverter to the output port; the OR gate including a first input port, a second

input port and an output port configured to connect the clock input to the first input port, the inverted set input to the second input port, and an enable port of the first tri-stated inverter and an enable port of the second tri-stated inverter to the output port; the inverter including the input port and an output port configured to connect the output port of the NOR gate to the input port and an input port of the first tri-stated inverter to the output port; the first tri-stated inverter including the input port, an output port and the enable port configured to connect to the output port of the inverter to the input port, the plus voltage node of the ReRAM cell to the output port and the output port of the OR gate to the enable port; and the second tri-stated inverter including the input port, an output port and the enable port configured to connect to the output port of the NOR gate to the input port, the minus voltage node of the ReRAM cell to the output port, and the output port of the OR gate to the enable port.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous set circuitry comprises a first OR gate, a first AND gate, a second OR gate, a third OR gate, a fourth OR gate, a second AND gate, a first NMOS transistor, a first PMOS transistor, a second NMOS transistor, and a second PMOS transistor, the first OR gate including a first input port, a second input port and an output port configured to connect an inverted clock input to the first input port, the data input to the second input port, and a first input port of the third OR gate to the output port; the first AND gate including a first input port, a second input port and an output port configured to connect the clock input to the first input port, the data input to the second input port, and a first input port of the fourth OR gate to the output port; the second OR gate including a first input port, a second input port and an output port configured to connect the inverted clock input to the first input port, the inverted data input to the second input port, and a first input port of the second AND gate to the output port; the third OR gate including the first input port, a second input port and an output port configured to connect the output port of the first OR gate to the first input port, the inverted set input to the second input port, and a gate of the second PMOS transistor to the output port; the fourth OR gate including the first input port, a second input port and an output port configured to connect the output port of the first AND gate to the first input port, the inverted set input to the second input port, and a gate of the second NMOS transistor to the output port; the second AND gate including the first input port, a second input port and an output port configured to connect the output port of the second OR gate to the first input port, the set input signal to the second input port, a gate of the first NMOS transistor to the output port, and a gate of the first PMOS transistor to the output port; the first NMOS transistor including the gate input, a drain input and a source input, being further configured to connect the

logically low voltage input to the source input and the minus voltage node of the ReRAM cell to the drain input; the first PMOS transistor including the gate input, a drain input and a source input, being further configured to connect a logically high voltage input to the source input and the minus voltage node of the ReRAM cell to the drain input; the second NMOS transistor including the gate input, a drain input and a source input, being further configured to connect the logically low voltage input to the source input and the plus voltage node of the ReRAM cell to the drain input; the second PMOS transistor including the gate input, a drain input and a source input, being further configured to connect the logically high voltage input to the source input and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment of the non-volatile latch circuitry, the bias circuitry comprises an OR gate, a first PMOS transistor, and a second PMOS transistor, the OR gate including a first input port, a second input port and an output port configured to connect the clock input to the first input port and the inverted set input to the second input port and a gate input of the first PMOS transistor to the output port; the first PMOS transistor including the gate input, a drain input and a source input, being further configured to connect the logically high voltage to the source input and a source input of the second PMOS transistor to the drain input; the second PMOS transistor including a gate input, a drain input and the source input configured to connect a bias voltage input to the gate input, the drain of the first PMOS transistor to the source and the plus voltage node of the ReRAM cell to the drain input.

In a further preferred embodiment the non-volatile latch circuitry further comprises an asynchronous force to high circuitry configured to set the output signal to logically high voltage and the inverted output signal to logically low voltage and connected to the plus voltage node of the ReRAM cell.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous force to high circuitry comprises a threshold adjusted inverter, a NOR gate, and an inverter, the threshold adjusted inverter including an input port and an output port configured to connect the plus voltage node of the ReRAM cell to the input port and a first input port of the NOR gate to the output port; the NOR gate including the first input port, a second input port and an output port configured to connect the output of the adjusted inverter to the first input port, a force to high input to the second input port, the inverted output signal to the output port, and an input port of the inverter to the output port; and the inverter including the input

port and an output port configured to connect the output of the NOR gate to the input port and the output signal to the output port.

In a further preferred embodiment the non-volatile latch circuitry further comprises an asynchronous force to low circuitry configured to set the output signal to logically low voltage and the inverted output signal to logically high voltage and connected to the plus voltage node of the ReRAM cell.

In a further preferred embodiment of the non-volatile latch circuitry, the asynchronous force to low circuitry comprises a threshold adjusted inverter, a NAND gate, and an inverter, the threshold adjusted inverter including an input port and an output port configured to connect the plus voltage node of the ReRAM cell to the input port and a first input port of the NAND gate to the output port; the NAND gate including the first input port, a second input port and an output port configured to connect the output of the adjusted inverter to the first input port, an inverted force to low input to the second input port, the inverted output signal to the output port, and an input port of the inverter to the output port; and the inverter including the input port and an output port configured to connect the output of the NAND gate to the input port and the output signal to the output port.

In a second aspect the invention provides a non-volatile rising edge D-Flip Flop, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry according to claim 1, including the data port, a clock port, a bias voltage port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the output port to an output signal and the inverted output port to an inverted output signal.

In a third aspect the invention provides a non-volatile falling edge D-Flip Flop, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the

clock port to an inverted clock input, the bias voltage port to the bias voltage input, the output port to an output signal and the inverted output port to an inverted output signal.

In a fourth aspect the invention provides a non-volatile rising edge D-Flip Flop with asynchronous reset, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the reset port to a reset input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a reset port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the reset port to the reset input, the output port to an output signal and the inverted output port to an inverted output signal.

In a fifth aspect the invention provides a non-volatile falling edge D-Flip Flop with asynchronous reset, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the reset port to a reset input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a reset port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the reset port to the reset input, the output port to an output signal and the inverted output port to an inverted output signal.

In a sixth aspect the invention provides a non-volatile rising edge D-Flip Flop with asynchronous set, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the set port to a set input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a set port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a

clock input, the bias voltage port to the bias voltage input, the set port to the set input, the output port to an output signal and the inverted output port to an inverted output signal.

In a seventh aspect the invention provides non-volatile falling edge D-Flip Flop with asynchronous set, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the set port to a set input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a set port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the set port to the set input, the output port to an output signal and the inverted output port to an inverted output signal.

In an eighth aspect the invention provides a non-volatile rising edge D-Flip Flop with force-to-high, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the force-to-high port to a force to high input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry according to claim 14, including the data port, a clock port, a bias voltage port, a force-to-high port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the force-to-high port to the force to high input, the output port to an output signal and the inverted output port to an inverted output signal.

In a ninth aspect the invention provides a non-volatile falling edge D-Flip Flop with force-to-high, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the force-to-high port to a force to high input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-high port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the

force-to-high port to the force to high input, the output port to an output signal and the inverted output port to an inverted output signal.

In a tenth aspect the invention provides a non-volatile rising edge D-Flip Flop with force-to-low, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the force-to-low port to a force to low input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-low port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the force-to-low port to the force to low input, the output port to an output signal and the inverted output port to an inverted output signal.

In an eleventh aspect the invention provides a non-volatile falling edge D-Flip Flop with force-to-low, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the force-to-low port to a force to low input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-low port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the force-to-low port to the force to low input, the output port to an output signal and the inverted output port to an inverted output signal.

In a twelveth aspect the invention provides a non-volatile rising edge D-Flip Flop, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input and the output port to an output signal.

In a thirteenth aspect the invention provides a non-volatile falling edge D-Flip Flop, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, and an output, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input and the output port to an output signal.

In a fourteenth aspect the invention provides a non-volatile rising edge D-Flip Flop with asynchronous reset, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the reset port to a reset input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a reset port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the reset port to the reset input, and the output port to an output signal.

In a fifteenth aspect the invention provides a non-volatile falling edge D-Flip Flop with asynchronous reset, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the reset port to a reset input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a reset port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the reset port to the reset input, and the output port to an output signal.

In a sixteenth aspect the invention provides a non-volatile rising edge D-Flip Flop with asynchronous set, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the set port to a set input and the output port to a data port of a second non-volatile

latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a set port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the set port to the set input, and the output port to an output signal.

In a seventeenth aspect the invention provides a non-volatile falling edge D-Flip Flop with asynchronous set, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the set port to a set input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a set port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the set port to the set input, and the output port to an output signal.

In an eighteenth aspect the invention provides a non-volatile rising edge D-Flip Flop with force-to-high, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the force-to-high port to a force to high input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-high port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the force-to-high port to the force to high input, and the output port to an output signal.

In a nineteenth aspect the invention provides a non-volatile falling edge D-Flip Flop with force-to-high, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the force-to-high port to a force to high input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-high port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock

port to an inverted clock input, the bias voltage port to the bias voltage input, the force-to-high port to the force to high input, and the output port to an output signal.

In a twentieth aspect the invention provides a non-volatile rising edge D-Flip Flop with force-to-low, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input, the clock port to an inverted clock input, the bias voltage port to a bias voltage input, the force-to-low port to a force to low input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-low port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input, the bias voltage port to the bias voltage input, the force-to-low port to the force to low input, and the output port to an output signal.

In a twenty first aspect the invention provides a non-volatile falling edge D-Flip Flop with force-to-low, comprising a first non-volatile latch circuitry, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input, the clock port to a clock input, the bias voltage port to a bias voltage input, the force-to-low port to a force to low input and the output port to a data port of a second non-volatile latch circuitry; and the second non-volatile latch circuitry, including the data port, a clock port, a bias voltage port, a force-to-low port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input, the bias voltage port to the bias voltage input, the force-to-low port to the force to low input, and the output port to an output signal.

Brief description of the figures

The invention will now be explained in more detail by describing preferred embodiments and referring to figures, wherein:

figures 1 and 2 illustrate two different implementations of non-volatile latch circuitry;

figure 3 shows the timing diagram of the operation of the latch circuitry;

figures 4 and 5 illustrate two different implementations of non-volatile latch circuitry with reset function;

figures 6 and 7 illustrate two different implementations of non-volatile latch circuitry with set function;

figures 8 and 9 illustrate two different implementations of non-volatile latch circuitry in which their outputs are forced to high with Force High (FH) input signal;

figures 10 and 11 illustrate two different implementations of non-volatile latch circuitry in which their outputs are forced to low with Force Low (FL) input signal;

figures 12, 13, 14, 15 and 16 show implementations of non-volatile D-type flip-flop with different functionalities using non-volatile latch structures described in the invention (e.g., reset, set, force to high, force to low).

Detailed description of preferred embodiments of the invention

General description of the invention

The present invention gives the method of implementing different type of CMOS compatible non-volatile D-latch and D-flip-flop (DFF) structures constructed by Resistive Switching Materials (RSM) (resistive RAM memory (ReRAM) elements). As a consequence of the non-volatility, the D-Latch and DFFs store their last state even on their next power-up (/power cycling). The working principle of the non-volatile latch and DFFs are similar to the conventional latch and DFF structures.

First example

Non-Volatile Latch Circuitry

Figure 1 illustrates a first example implementation of a non-volatile latch circuitry.

In figure 1, once a high voltage is applied to the clock "C" the data "D" is stored in a ReRAM cell and according to the polarity of the "D" input, the resistor value R of the ReRAM cell varies, e.g.,

- if the voltage level on "D" is "low" then $R = R_{high}$;
- if the voltage level on "D" is "high" then $R = R_{low}$;

where R_{high} and R_{low} denote the high resistor and low resistor value of the ReRAM cell respectively.

During the high time of the "C" input, M1 and M2 PMOS transistors are off since M1's gate is connected directly to "C" input. Therefore, "D" is propagated to "Q" output through U1, U2, U3, U5, U6 and U7 inverters. Once the clock "C" is applied "low", the data is gated by

U3 and U4 inverters and it is not transmitted to the ReRAM cell. Therefore, ReRAM resistor value and "Q" output are not affected by the transitions on "D" input. In order to keep "Q" output value that is set through "D" input during the high time of "C" input, I_{bias} current is applied to ReRAM cell through M1 and M2 PMOS transistors. In this mode, a Vy voltage node in Figure 1 is grounded by M3 transistor and a Vx voltage node has the voltage value of

$$Vx = I_{bias} \times \text{resistor value of ReRAM}$$

which results in

- $Vx_{high} = I_{bias} \times R_{high}$ and
- $Vx_{low} = I_{bias} \times R_{low}$.

Therefore, the threshold of the U5 inverter needs to be around $(Vx_{high} + Vx_{low})/2$ so that the stored value of ReRAM is transmitted to Q output correctly. Because of the use of ReRAM cell, the latch shown in this example will keep its last stored value even though the power applied to the circuitry is removed.

Figure 2 shows an other type of non-volatile latch circuitry however the operation principle is similar to the one in figure 1. The only difference is the way how Vx and Vy nodes are set according to the "D" input during the high time of "C" input. This time, Vx and Vy voltage nodes are controlled through M3, M4, M5 and M6 transistors. While the clock input is at low voltage level Vy voltage node is set to ground and the Vx is controlled through the I_{bias} current applied to the circuitry. While the clock input is at high voltage level, depending on the data input (D) voltage level either M5 or M6 transistor is turned on to set the Vx voltage node; similarly M4 or M3 transistor is turned on to set the Vy voltage node.

Figure 3 shows the timing diagram of the latch circuitry demonstrated in figure 1 and figure 2. The details of the operation are as follows:

- Assumptions:
    - R_{low} = 10 kOhm,
    - R_{high} = 100 kOhm,
    - VP = 1.2 V,

- If ReRAM voltage VR, (Vx - Vy) > 1.2V, ReRAM resistor value becomes R_{high}. If ReRAM voltage VR, (Vx – Vy) < 1.2V, ReRAM resistor value becomes R_{low}

  - I_{bias} = 5 µA,
  - Initial value of ReRAM = 100 kOhm (R_{high}),
  - the threshold voltage of U5 is around "300 mV",
  - VDD = 1.8 V +/- 10%;

- Region I → "C" is "low", "D" is not written across the ReRAM. Vy is grounded through M3 transistor and Vx is set by $I_{bias} \times R_{high}$. Using the assumption above, Vx is around 500 mV. Since Vx is greater than the threshold voltage of U5 inverter, Q output is held at logic "low".

- Region II → "C" and "D" are both at logic "high" levels and forcing Vx node to "~GND/ground" and Vy node to "~VDD/supply". The voltage drop across the resistor (VR = Vx-Vy) is now around "-VDD". The absolute value of VR is high enough to change the resistor value from R_{high} to R_{low}. With the rising edge of "C", "Q" output is changing from "low voltage level" to "high voltage level" Region III → Similar to Region I, Vx is set by $I_{bias} \times R_{low}$ and it is around 50 mV which is lower than the threshold of U5 inverter. Therefore, Q output is still at logic "high". In this region, the Q output is not affected by "high" to "low" transition on "D" input.

- Region IV → This time "C" is "high" but "D" is "low". "C" and "D" sets Vx as "~VDD" and Vy as "~GND". The voltage drop across the resistor is around "+VDD" which is sufficient to change the resistor value from R_{low} to R_{high}. Since the data is "low", Q output is now changing from "high" to "low" state.

- Region V → Same operation as Region I → $Vx = I_{bias} \times R_{high} = 500$ mV. The circuitry keeps "Q" output at logic "low" and ignores all the transitions that occur in "D" input.

- Region VI → Same operation as Region II → VR is around "–VDD" and changes the resistor value from "R_{high}" to "R_{low}". And the output "Q" is exactly at the same polarity as "D" input.

The diagram in figure 3 illustrates that the data is sampled during the high level of the clock input and holds the value during the low level the clock input as in the classical D-type latches. However, it also shows that the ReRAM cell is programmed to R_{high} or R_{low} level depending on the data (D) level. Since ReRAM cells are used as a non-volatile memory element, programming the ReRAM value ensures to store the sampled data value at each clock high level and helps to restore the data value in the next power cycles.

Second example

Non-Volatile Latch Circuitry with Asynchronous Reset Function

The operation of the latch in figure 4 and figure 5 is similar to the one in figure 1 and figure 2 with the following exception:

with asynchronous reset (RN) signal assertion (applying low voltage to RN) Vx and Vy nodes are set in a way that ReRAM resistor value is changed to "R_{high}" state which is also forcing the Q output to logic "low".

A nand gate (U12) in figure 4, forces the data input to a low voltage level. This low voltage will be transmitted across the ReRAM cell once a low voltage is applied to the reset (RN) signal.

Similarly M3, M4, M5 and M6 transistors in figure 5 are controlled through the data input (D), clock input (C) and reset input (RN). If the reset signal is asserted low Vx voltage node is set to high voltage while Vy voltage node is set to low voltage independent from the data input and clock input voltage levels. This ensures that the ReRAM resistor value is programmed to R_{high}.

Third example

Non-Volatile Latch Circuitry with Asynchronous Set Function

The operation of the latch in figure 6 and figure 7 is similar to the one in figure 1 and figure 2 with the following exception:

with asynchronous set (SN) signal assertion (applying low voltage to SN) Vx and Vy nodes are set in a way that ReRAM resistor value is changed to "R_{low}" state which is also forcing the Q output to logic "high".

A nor gate (U13) in figure 6, forces the data input to a high voltage level. Once a low voltage is applied to the set (SN) signal, this high voltage will be transmitted across the ReRAM cell.

Similarly M3, M4, M5 and M6 transistors are controlled through the data input (D), clock input (C) and set input (SN). If the set signal is asserted low, Vx voltage node is set to low voltage while Vy voltage node is set to high voltage independent from the data input and clock input voltage levels. This ensures that the ReRAM resistor value is programmed to R_{low}.

Fourth example

Non-Volatile Latch Circuitry with Asynchronous Force-to-High Function

The operation of the latch in figure 8 and figure 9 is similar to the one in figure 1 and figure 2 with the following exception:

with force high signal (FH) assertion (applying high voltage to FH) only Q output of the latch is forced to "high". The ReRAM value does not change with FH assertion. This force operation is done through U61 nor gate. The FH input signal is connected to the U61 nor gate input. Once a high voltage is applied to the FH input, U61 nor gate output is set to logic low and the output of the preceding inverter (U7), which is the Q output of the latch, is set to high.

Fifth example

Non-Volatile Latch Circuitry with Asynchronous Force-to-Low Function

The operation of the latch in figure 10 and figure 11 is similar to the one in figure 1 and figure 2 with the following exception:

with force low signal assertion (applying high voltage to FL) only Q output of the latch is forced to "low". The ReRAM value does not change with FL assertion. This force operation is done through U62 nand gate. The inverted FL input signal is connected to the U62 nand gate input. Once a high voltage is applied to the FL input, U62 nand gate output is set to logic high and the output of the preceding inverter (U7), which is the Q output of the latch, is set to low.

Sixth example

Non-Volatile Rising and Falling Edge Triggered D-Flip Flop Circuitry

In figure 12, two different rising edge triggered D-flip-flop structures (DFFs) are shown. The operational principle of DFFs is similar to that of classical rising edge triggered DFF struc-

tures: the data is transmitted to the master latch output (not illustrated in figure 12) during the low time of clock "C" input and the value is stored on the next low to high transition of C input. At this time, the stored data on the master side is transmitted to the Q output of the flip-flop which is the output of the slave latch. During the low time of the clock input, the slave latch output is kept at its previous state. Using the non-volatile latch structures that are illustrated as master and slave in figure 12, the last stored value of DFF is going to be kept at the next power-up or power-cycling.

Using the same principle, non-volatile falling edge triggered DFF can also be obtained by changing the polarity of C and CB inputs on both master and slave latches.

Seventh example

Non-Volatile Rising and Falling Edge Triggered D-Flip Flop Circuitry with Reset Function

The operation of the rising edge triggered DFF in figure 13 is similar to the one in figure 12 with the following exception:

with reset signal (RN) assertion (applying low voltage to RN) Vx and Vy nodes of both master and slave latches are set in a way that ReRAM resistor values of both master and slave latches are changed to "R_{high}" state forcing Q output of DFF to logic "low".

Using the same principle, non-volatile falling edge triggered DFF with reset function can also be obtained by changing the polarity of C and CB inputs on both master and slave latches.

Eight example

Non-Volatile Rising and Falling Edge Triggered D-Flip Flop Circuitry with Set Function

The operation of the rising edge triggered DFF in figure 14 is similar to the one in figure 12 with the following exception:

with set signal (SN) assertion (applying low voltage to SN) Vx and Vy nodes of both master and slave latches are set in a way that ReRAM resistor values of both master and slave latches are changed to "R_{low}" state forcing Q output to logic "high".

Using the same principle, non-volatile falling edge triggered DFF with set function can also be obtained by changing the polarity of C and CB inputs on both master and slave latches.

Ninth example

Non-Volatile Rising and Falling Edge Triggered D-Flip Flop Circuitry with Force-to-High Function

The operation of the rising edge triggered DFF in figure 15 is similar to the one in figure 12 with the following exception:

with force high (FH) signal assertion (applying high voltage to FH) only Q output of DFF is forced to "high". The ReRAM values of both master and slave latches do not change with FH assertion.

Using the same principle, non-volatile falling edge triggered DFF with Force-to-High function can also be obtained by changing the polarity of C and CB inputs on both master and slave latches.

Tenth example

Non-Volatile Rising and Falling Edge Triggered D-Flip Flop Circuitry with Force-to-Low Function

The operation of the rising edge triggered DFF in figure 16 is similar to the one in figure 12 with the following exception:

With force low (FL) assertion (applying high voltage to FL) only Q output of DFF is forced to "low". The ReRAM values of both master and slave latches do not change with FL assertion.

Using the same principle, non-volatile falling edge triggered DFF with Force-to-Low function can also be obtained by changing the polarity of C and CB inputs on both master and slave latches.

Claims

1. A non-volatile latch circuitry, comprising

a ReRAM cell configured to store a final value of the non-volatile latch circuitry;

a data selection circuitry (U1, U2, U3, U4) configured to connect or disconnect a data input (D) to a plus voltage node and a minus voltage node of the ReRam cell (Vx, Vy) depending on a clock input (C) voltage level;

a pull down transistor (M3) configured to set a first voltage level at the minus voltage node (Vy) to a logically low voltage level if the data input (D) is not connected to the plus and minus voltage nodes (Vx, Vy) of the ReRAM cell;

a bias circuitry (M1, M2) configured to provide a fix bias current to set a second voltage level at the plus voltage node (Vx) to a varying voltage level depending on the resistor value of the ReRAM cell if the data input (D) is not connected to the plus voltage node (Vx); and

a threshold adjusted circuitry arranged to convert an analog value of the second voltage level into a digital value and configured to generate an output signal (Q) and / or an inverted output signal (QB).

2. The non-volatile latch circuitry of claim 1, wherein the data selection circuitry comprises

a first inverter (U1) with a first input port and a first output port, a second inverter (U2) with a second input port and a second output port, a first tri-stated inverter (U3) with a third input port, a third output port and a first enable port, and a second tri-stated inverter (U4) with a fourth input port, a fourth output port and a second enable port, wherein

the first inverter (U1) is configured to connect the data input (D) to the first input port, and to connect the second input port and the fourth input port to the first output port;

the second inverter (U2) is further configured to connect the second output port to the third input port;

the first tri-stated inverter (U3) is further configured to connect the plus voltage

node (Vx) to the third output port and the clock input (C) to the first enable port; and

the second tri-stated inverter (U4) is further configured to connect the minus voltage node (Vy) to the fourth output port, and the clock input (C) to the second enable port.

3. The non-volatile latch circuitry of claim 1, wherein the data selection circuitry comprises

a first OR gate (OR1) with a first OR gate input port, a second OR gate input port and a first OR gate output port, a first AND gate (AND1) with a first AND gate input port, a second AND gate input port and a first AND gate output port, a second OR gate (OR2) with a third OR gate input port, a fourth OR gate input port and a second OR gate output port, wherein

the first OR gate (OR1) is configured to connect an inverted clock input (CB) to the first OR gate input port, the data input (D) to the second OR gate input port, and a gate of a second PMOS transistor (M6) to the first OR gate output port;

the first AND gate (AND1) is configured to connect the clock input (C) to the first AND gate input port, the data input (D) to the second AND gate input port, and a gate of a second NMOS transistor (M5) to the first AND gate output port;

the second OR gate (OR2) is configured to connect the inverted clock input (CB) to the third OR gate input port, the inverted data input (DB) to the fourth OR gate input port, a gate of a first PMOS transistor (M4) to the second OR gate output port, and a gate of a first NMOS transistor (M3) to the second OR gate output port;

the first NMOS transistor (M3) further including a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the first PMOS transistor (M4) further including a drain input and a source input, and being further configured to connect a logically high voltage input to the

source input, and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the second NMOS transistor (M5) further including a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the plus voltage node (Vx) of the ReRAM cell to the drain input; and

the second PMOS transistor (M6) further including a drain input and a source input, being further configured to connect the logically high voltage input to the source input, and the plus voltage node (Vx) of the ReRAM cell to the drain input.

4. The non-volatile latch circuitry of claim 1, wherein the bias circuitry comprises

a first PMOS transistor (M1) and a second PMOS transistor (M2), wherein

the first PMOS transistor (M1) includes a gate input, a drain input and a source input configured to connect the clock (C) input to the gate input, the logically high voltage to the source input, and a source input of the second PMOS transistor (M2) to the drain input; and

the second PMOS transistor (M2) includes a gate input, a drain input and a source input configured to connect a bias voltage input (VB) to the gate input, the drain of the first PMOS transistor (M1) to the source, and the plus voltage node (Vx) of the ReRAM cell to the drain input.

5. The non-volatile latch circuitry of claim 1, wherein the threshold adjusted circuitry comprises

a threshold adjusted inverter (U5), a first inverter (U6), and a second inverter (U7) , wherein

the threshold adjusted inverter (U5) includes an input port and an output port configured to connect the plus voltage node (Vx) of the ReRAM cell to the input port and an input port of the first inverter (U6) to the output port;

the first inverter (U6) includes an input port and an output port configured to connect the output of the threshold adjusted inverter to the input port , the inverted output signal (QB) to the output port, and an input of the second in-

verter (U7) to the output port; and

the second inverter (U7) includes an input port and an output port configured to connect the output of the first inverter to the input port and the output signal (Q) to the output port.

6. The non-volatile latch circuitry of claim 1, further comprising

an asynchronous reset circuitry (U12, U2, U3, U4) in the data selection circuitry, configured to set the first voltage node (Vx) and the second voltage node (Vy) of the ReRAM cell to program the ReRAM to high resistor value with reset (RN) input signal.

7. The non-volatile latch circuitry of claim 6, wherein the asynchronous reset circuitry comprises

a NAND gate (U12), an OR gate (OR1), a first tri-stated inverter, and a second tri-stated inverter, wherein

the NAND gate (U12) includes a first input port, a second input port and an output port configured to connect the data input (D) to the first input port, the reset input (RN) to the second input port, an input port of a inverter (U2) to the output port, and an input port of the second tri-stated inverter to the output port;

the OR gate (OR1) includes a first input port, a second input port and an output port configured to connect the clock input (C) to the first input port, the inverted reset input (RN') to the second input port and an enable port of the first tri-stated inverter, and an enable port of the second tri-stated inverter to the output port;

the inverter (U2) includes the input port and an output port configured to connect the output port of the NAND gate (U12) to the input port and an input port of the first tri-stated inverter (U3) to the output port;

the first tri-stated inverter (U3) includes the input port, an output port and the enable port configured to connect to the output port of the inverter (U2) to the input port, the plus voltage node of ReRAM cell (Vx) to the output port, and the output port of the OR gate (OR1) to the enable port; and

the second tri-stated inverter (U4) includes the input port, an output port and the enable port configured to connect to the output port of the NAND gate (U12) to the input port, the minus voltage node of ReRAM cell (Vy) to the output port and the output port of the OR gate (OR1) to the enable port.

8. The non-volatile latch circuitry of claim 6, wherein the asynchronous reset circuitry comprises

a first OR gate (OR1), a first AND gate (AND1), a second OR gate (OR2), a second AND gate (AND2), a third AND gate (AND3), a third OR gate (OR3), a first NMOS transistor (M3), a first PMOS transistor (M4), a second NMOS transistor (M5), and a second PMOS transistor (M6),

the first OR gate (OR1) including a first input port, a second input port and an output port configured to connect an inverted clock input (CB) to the first input port, the data input (D) to the second input port, and a first input port of the second AND gate (AND2) to the output port;

the first AND gate (AND1) including a first input port, a second input port and an output port configured to connect the clock input (C) to the first input port, the data input (D) to the second input port, and a first input port of the third AND gate (AND3) to the output port;

the second OR gate (OR2) including a first input port, a second input port and an output port configured to connect the inverted clock input (CB) to the first input port, the inverted data input (DB) to the second input port, and a first input port of the third OR gate (OR3) to the output port;

the second AND gate (AND2) including the first input port, a second input port and an output port configured to connect the output port of the first OR gate (OR1) to the first input port; the reset input (RN) to the second input port, and a gate of the second PMOS transistor (M6) to the output port;

the third AND gate (AND3) including the first input port, a second input port and an output port configured to connect the output port of the first AND gate (AND1) to the first input port, the reset input (RN) to the second input port, and a gate of the second NMOS transistor (M5) to the output port;

the third OR gate (OR3) including the first input port, a second input port and an

output port configured to connect the output port of the second OR gate (OR2) to the first input port, the inverted reset input (RN') to the second input port, a gate of the first NMOS transistor (M4) to the output port, and a gate of the first PMOS transistor (M3) to the output port;

the first NMOS transistor (M3) including the gate input, a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the first PMOS transistor (M4) including the gate input, a drain input and a source input, and being further configured to connect the logically high voltage input to the source input, and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the second NMOS transistor (M5) including the gate input, a drain input and a source input, and being further configured to connect the logically low voltage input to the source input, and the plus voltage node (Vx) of the ReRAM cell to the drain input; and

the second PMOS transistor (M6) including a gate input, a drain input and a source input, and being further configured to connect the logically high voltage input to the source input, and the plus voltage node (Vx) of the ReRAM cell to the drain input.

9. The non-volatile latch circuitry of claim 6, wherein the bias circuitry comprises

an OR gate (OR1), a first PMOS transistor (M1), and a second PMOS transistor (M2),

the OR gate (OR1) including a first input port, a second input port and an output port configured to connect the clock input (C) to the first input port and the inverted reset input (RN') to the second input port, and a gate input of the first PMOS transistor (M1) to the output port;

the first PMOS transistor (M1) including the gate input, a drain input and a source input, and being further configured to connect the logically high voltage to the source input, and a source input of the second PMOS transistor (M2) to the drain input; and

the second PMOS transistor (M2) including gate input, a drain input and the source input configured to connect the bias voltage input (VB) to the gate input, the drain of the first PMOS transistor (M1) to the source, and the plus voltage node (Vx) of the ReRAM cell to the drain input.

10. The non-volatile latch circuitry of claim 1, further comprising

an asynchronous set circuitry (U13, U2, U3, U4) in the data selection circuitry configured to set the first voltage node (Vx) and the second voltage node (Vy) of the ReRAM cell to program the ReRAM to low resistor value with reset (SN) input signal.

11. The non-volatile latch circuitry of claim 10, wherein the asynchronous set circuitry comprises

a NOR gate (U13), an OR gate (OR1), an inverter (U2), a first tri-stated inverter (U3), a second tri-stated inverter (U4),

the NOR gate (U13) including a first input port, a second input port and an output port configured to connect the data input (D) to the first input port, the inverted set input (SN') to the second input port, an input port of the inverter (U2) to the output port, and an input port of the second tri-stated inverter (U4) to the output port;

the OR gate (OR1) including a first input port, a second input port and an output port configured to connect the clock input (C) to the first input port, the inverted set input (SN') to the second input port, and an enable port of the first tri-stated inverter (U3) and an enable port of the second tri-stated inverter (U4) to the output port;

the inverter (U2) including the input port and an output port configured to connect the output port of the NOR gate (U13) to the input port and an input port of the first tri-stated inverter (U3) to the output port;

the first tri-stated inverter (U3) including the input port, an output port and the enable port configured to connect to the output port of the inverter (U2) to the input port, the plus voltage node of the ReRAM cell (Vx) to the output port and the output port of the OR gate (OR1) to the enable port; and

the second tri-stated inverter (U4) including the input port, an output port and the enable port configured to connect to the output port of the NOR gate (U13) to the input port, the minus voltage node of the ReRAM cell (Vy) to the output port, and the output port of the OR gate (OR1) to the enable port.

12. The non-volatile latch circuitry of claim 10, wherein the asynchronous set circuitry comprises

a first OR gate (OR1), a first AND gate (AND1), a second OR gate (OR2), a third OR gate (OR3), a fourth OR gate (OR4), a second AND gate (AND2), a first NMOS transistor (M3), a first PMOS transistor (M4), a second NMOS transistor (M5), and a second PMOS transistor (M6),

the first OR gate (OR1) including a first input port, a second input port and an output port configured to connect an inverted clock input (CB) to the first input port, the data input (D) to the second input port, and a first input port of the third OR gate (OR3) to the output port;

the first AND gate (AND1) including a first input port, a second input port and an output port configured to connect the clock input (C) to the first input port, the data input (D) to the second input port, and a first input port of the fourth OR gate (OR4) to the output port;

the second OR gate (OR2) including a first input port, a second input port and an output port configured to connect the inverted clock input (CB) to the first input port, the inverted data input (DB) to the second input port, and a first input port of the second AND gate (AND2) to the output port;

the third OR gate (OR3) including the first input port, a second input port and an output port configured to connect the output port of the first OR gate (OR1) to the first input port, the inverted set input (SN') to the second input port, and a gate of the second PMOS transistor (M6) to the output port;

the fourth OR gate (OR4) including the first input port, a second input port and an output port configured to connect the output port of the first AND gate (AND1) to the first input port, the inverted set input (SN') to the second input port, and a gate of the second NMOS transistor (M5) to the output port;

the second AND gate (AND2) including the first input port, a second input port and an output port configured to connect the output port of the second OR gate to the first input port, the set input (SN) signal to the second input port, a gate of the first NMOS transistor (M4) to the output port, and a gate of the first PMOS transistor (M3) to the output port;

the first NMOS transistor (M3) including the gate input, a drain input and a source input, being further configured to connect the logically low voltage input to the source input and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the first PMOS transistor (M4) including the gate input, a drain input and a source input, being further configured to connect a logically high voltage input to the source input and the minus voltage node (Vy) of the ReRAM cell to the drain input;

the second NMOS transistor (M5) including the gate input, a drain input and a source input, being further configured to connect the logically low voltage input to the source input and the plus voltage node (Vx) of the ReRAM cell to the drain input;

the second PMOS transistor (M6) including the gate input, a drain input and a source input, being further configured to connect the logically high voltage input to the source input and the plus voltage node (Vx) of the ReRAM cell to the drain input;

13. The non-volatile latch circuitry of claim 10, wherein the bias circuitry comprises

an OR gate (OR1), a first PMOS transistor (M1), and a second PMOS transistor (M2),

the OR gate (OR1) including a first input port, a second input port and an output port configured to connect the clock (C) input to the first input port and the inverted set input (SN') to the second input port and a gate input of the first PMOS transistor (M1) to the output port;

the first PMOS transistor (M1) including the gate input, a drain input and a source input, being further configured to connect the logically high voltage to the source input and a source input of the second PMOS transistor (M2) to the

drain input;

the second PMOS transistor (M2) including a gate input, a drain input and the source input configured to connect a bias voltage (VB) input to the gate input, the drain of the first PMOS transistor (M1) to the source and the plus voltage node (Vx) of the ReRAM cell to the drain input.

14. The non-volatile latch circuitry of any one of the claims 1,6 and 10, further comprising

an asynchronous force to high circuitry (U5, U61, U7) configured to set the output signal (Q) to logically high voltage and the inverted output signal (QB) to logically low voltage and connected to the plus voltage node of the ReRAM cell (Vx)

15. The non-volatile latch circuitry of claim 14, wherein the asynchronous force to high circuitry comprises

a threshold adjusted inverter (U5), a NOR gate (U61), and an inverter (U7),

the threshold adjusted inverter (U5) including an input port and an output port configured to connect the plus voltage node of the ReRAM cell (Vx) to the input port and a first input port of the NOR gate (U61) to the output port;

the NOR gate (U61) including the first input port, a second input port and an output port configured to connect the output of the adjusted inverter (U5) to the first input port, a force to high input (FH) to the second input port, the inverted output signal (QB) to the output port, and an input port of the inverter (U7) to the output port; and

the inverter (U7) including the input port and an output port configured to connect the output of the NOR gate (U61) to the input port and the output signal (Q) to the output port.

16. The non-volatile latch circuitry of any one of the claims 1, 6 and 10, further comprising

an asynchronous force to low circuitry (U5, U62, U7) configured to set the output signal (Q) to logically low voltage and the inverted output signal (QB) to

logically high voltage and connected to the plus voltage node of the ReRAM cell (Vx)

17. The non-volatile latch circuitry of claim 16, wherein the asynchronous force to low circuitry comprises

a threshold adjusted inverter (U5), a NAND gate (U62), and an inverter (U7),

the threshold adjusted inverter (U5) including an input port and an output port configured to connect the plus voltage node of the ReRAM cell (Vx) to the input port and a first input port of the NAND gate (U62) to the output port;

the NAND gate (U62) including the first input port, a second input port and an output port configured to connect the output of the adjusted inverter (U5) to the first input port, an inverted force to low input (FL') to the second input port, the inverted output signal (QB) to the output port, and an input port of the inverter (U7) to the output port; and

the inverter (U7) including the input port and an output port configured to connect the output of the NAND gate (U62) to the input port and the output signal (Q) to the output port.

18. A non-volatile rising edge D-Flip Flop, comprising

a first non-volatile latch circuitry according to claim 1, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 1, including the data port, a clock port, a bias voltage port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

19. A non-volatile falling edge D-Flip Flop, comprising

a first non-volatile latch circuitry according to claim 1, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 1, including the data port, a clock port, a bias voltage port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

20. A non-volatile rising edge D-Flip Flop with asynchronous reset, comprising

a first non-volatile latch circuitry according to claim 6, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the reset port to a reset input (RN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 6, including the data port, a clock port, a bias voltage port, a reset port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the reset port to the reset input (RN), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

21. A non-volatile falling edge D-Flip Flop with asynchronous reset, comprising

a first non-volatile latch circuitry according to claim 6, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the reset port to a reset input (RN) and the output port to a data port of a second non-volatile latch

circuitry; and

the second non-volatile latch circuitry according to claim 6, including the data port, a clock port, a bias voltage port, a reset port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the reset port to the reset input (RN), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

22. A non-volatile rising edge D-Flip Flop with asynchronous set, comprising

a first non-volatile latch circuitry according to claim 10, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the set port to a set input (SN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 10, including the data port, a clock port, a bias voltage port, a set port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the set port to the set input (SN), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

23. A non-volatile falling edge D-Flip Flop with asynchronous set, comprising

a first non-volatile latch circuitry according to claim 10, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the set port to a set input (SN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 10, including the data port, a clock port, a bias voltage port, a set port, an output port and an inverted

output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the set port to the set input (SN), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

24. A non-volatile rising edge D-Flip Flop with force-to-high, comprising

a first non-volatile latch circuitry according to claim 14, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the force-to-high port to a force to high input (FH) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 14, including the data port, a clock port, a bias voltage port, a force-to-high port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the force-to-high port to the force to high input (FH), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

25. A non-volatile falling edge D-Flip Flop with force-to-high, comprising

a first non-volatile latch circuitry according to claim 14, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the force-to-high port to a force to high input (FH) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 14, including the data port, a clock port, a bias voltage port, a force-to-high port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the force-to-high

port to the force to high input (FH), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

26. A non-volatile rising edge D-Flip Flop with force-to-low, comprising

a first non-volatile latch circuitry according to claim 16, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the force-to-low port to a force to low input (FL) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 16, including the data port, a clock port, a bias voltage port, a force-to-low port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the force-to-low port to the force to low input (FL), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

27. A non-volatile falling edge D-Flip Flop with force-to-low, comprising

a first non-volatile latch circuitry according to claim 16, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the force-to-low port to a force to low input (FL) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 16, including the data port, a clock port, a bias voltage port, a force-to-low port, an output port and an inverted output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the force-to-low port to the force to low input (FL), the output port to an output signal (Q) and the inverted output port to an inverted output signal (QB).

28. A non-volatile rising edge D-Flip Flop, comprising

a first non-volatile latch circuitry according to claim 1, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 1, including the data port, a clock port, a bias voltage port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB) and the output port to an output signal (Q)

29. A non-volatile falling edge D-Flip Flop, comprising

a first non-volatile latch circuitry according to claim 1, including a data port, a clock port, a bias voltage port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 1, including the data port, a clock port, a bias voltage port, and an output, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB) and the output port to an output signal (Q).

30. A non-volatile rising edge D-Flip Flop with asynchronous reset, comprising

a first non-volatile latch circuitry according to claim 6, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the reset port to a reset input (RN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 6, including the data port, a clock port, a bias voltage port, a reset port, and an output port, configured to

connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the reset port to the reset input (RN), and the output port to an output signal (Q).

31. A non-volatile falling edge D-Flip Flop with asynchronous reset, comprising

a first non-volatile latch circuitry according to claim 6, including a data port, a clock port, a bias voltage port, a reset port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the reset port to a reset input (RN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 6, including the data port, a clock port, a bias voltage port, a reset port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the reset port to the reset input (RN), and the output port to an output signal (Q).

32. A non-volatile rising edge D-Flip Flop with asynchronous set, comprising

a first non-volatile latch circuitry according to claim 10, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the set port to a set input (SN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 10, including the data port, a clock port, a bias voltage port, a set port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the set port to the set input (SN), and the output port to an output signal (Q).

33. A non-volatile falling edge D-Flip Flop with asynchronous set, comprising

a first non-volatile latch circuitry according to claim 10, including a data port, a clock port, a bias voltage port, a set port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the set port to a set input (SN) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 10, including the data port, a clock port, a bias voltage port, a set port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the set port to the set input (SN), and the output port to an output signal (Q).

34. A non-volatile rising edge D-Flip Flop with force-to-high, comprising

a first non-volatile latch circuitry according to claim 14, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the force-to-high port to a force to high input (FH) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 14, including the data port, a clock port, a bias voltage port, a force-to-high port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the force-to-high port to the force to high input (FH), and the output port to an output signal (Q).

35. A non-volatile falling edge D-Flip Flop with force-to-high, comprising

a first non-volatile latch circuitry according to claim 14, including a data port, a clock port, a bias voltage port, a force-to-high port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the force-to-high port

to a force to high input (FH) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 14, including the data port, a clock port, a bias voltage port, a force-to-high port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the force-to-high port to the force to high input (FH), and the output port to an output signal (Q)

36. A non-volatile rising edge D-Flip Flop with force-to-low, comprising

a first non-volatile latch circuitry according to claim 16, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input (D), the clock port to an inverted clock input (CB), the bias voltage port to a bias voltage input (VB), the force-to-low port to a force to low input (FL) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 16, including the data port, a clock port, a bias voltage port, a force-to-low port, and an output port, configured to connect the input port to the output of the first non-volatile latch circuitry, the clock port to a clock input (C), the bias voltage port to the bias voltage input (VB), the force-to-low port to the force to low input (FL), and the output port to an output signal (Q).

37. A non-volatile falling edge D-Flip Flop with force-to-low, comprising

a first non-volatile latch circuitry according to claim 16, including a data port, a clock port, a bias voltage port, a force-to-low port and an output port, configured to connect the input port to a data input (D), the clock port to a clock input (C), the bias voltage port to a bias voltage input (VB), the force-to-low port to a force to low input (FL) and the output port to a data port of a second non-volatile latch circuitry; and

the second non-volatile latch circuitry according to claim 16, including the data port, a clock port, a bias voltage port, a force-to-low port, and an output port, configured to connect the input port to the output of the first non-volatile

latch circuitry, the clock port to an inverted clock input (CB), the bias voltage port to the bias voltage input (VB), the force-to-low port to the force to low input (FL), and the output port to an output signal (Q).

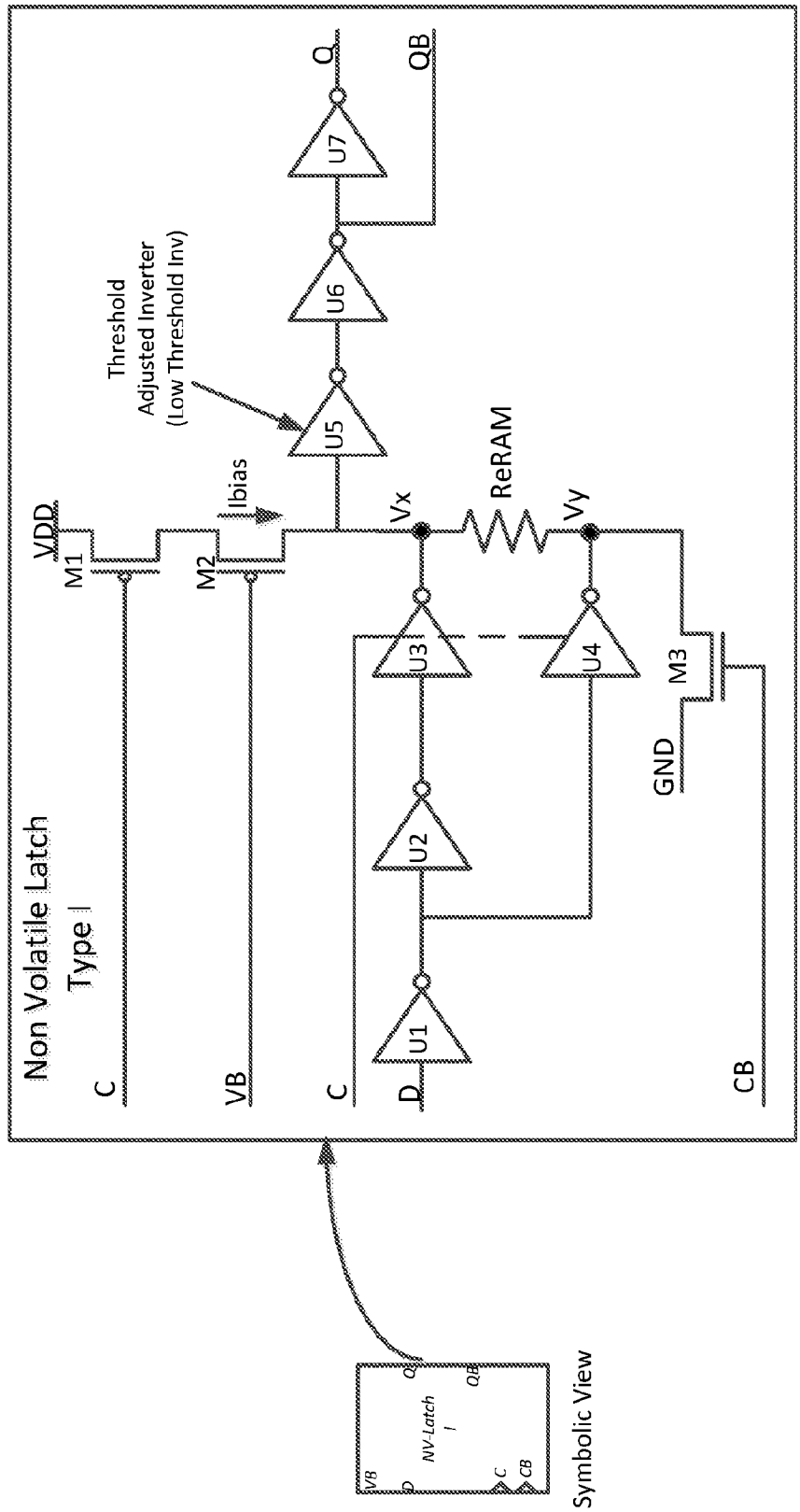
Non Volatile Latch
Type I
VDD
M1
M2
Ibias
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
Vx
ReRAM
Vy
U3
U4
U2
U1
M3
GND
C
VB
C
D
CB
NV-Latch
I
Symbolic View

FIGURE 1

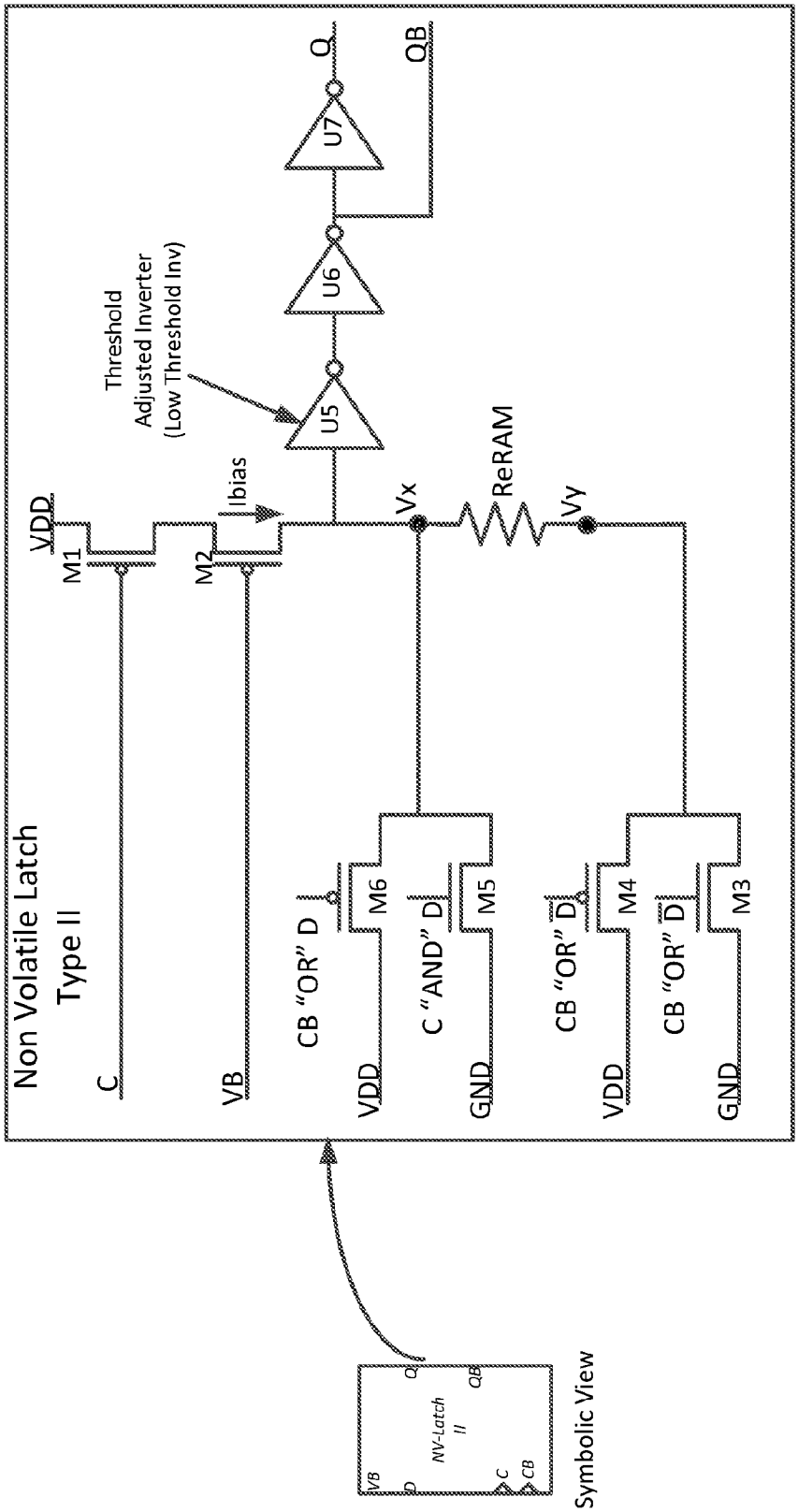
Non Volatile Latch
Type II
C
VB
CB "OR" D
C "AND" D
CB "OR" D
CB "OR" D
VDD
GND
VDD
GND
M6
M5
M4
M3
VDD
M1
M2
Ibias
Vx
ReRAM
Vy
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
NV-Latch
II
VB
D
C
CB
Q
QB
Symbolic View

FIGURE 2

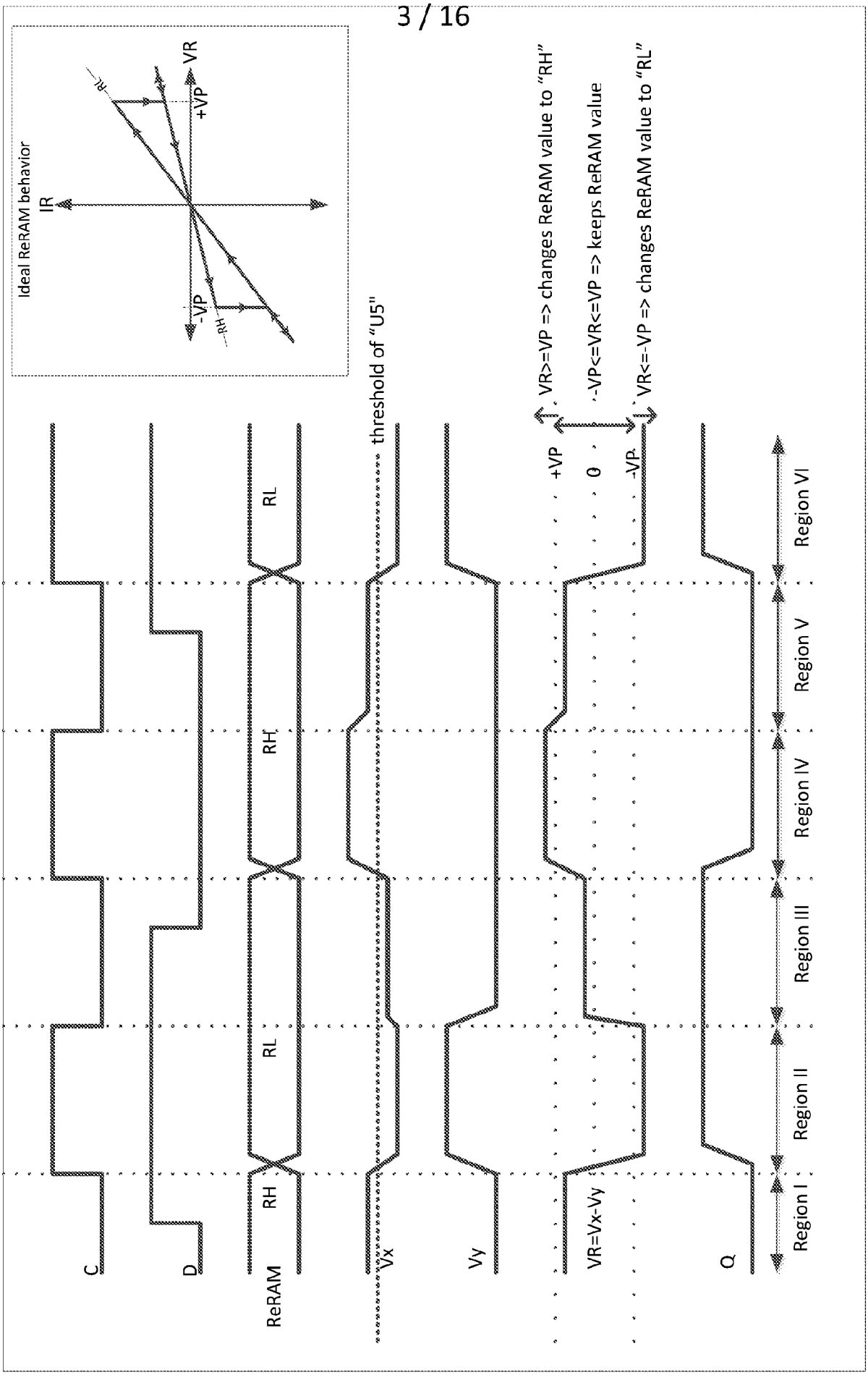
Ideal ReRAM behavior
IR
VR
+VP
-VP
RH
RL
C
D
ReRAM
RH
RL
RH
RL
Vx
threshold of "U5"
Vy
VR=Vx-Vy
+VP
0
-VP
VR>=VP => changes ReRAM value to "RH"
-VP<=VR<=VP => keeps ReRAM value
VR<=-VP => changes ReRAM value to "RL"
Q
Region I
Region II
Region III
Region IV
Region V
Region VI

FIGURE 3

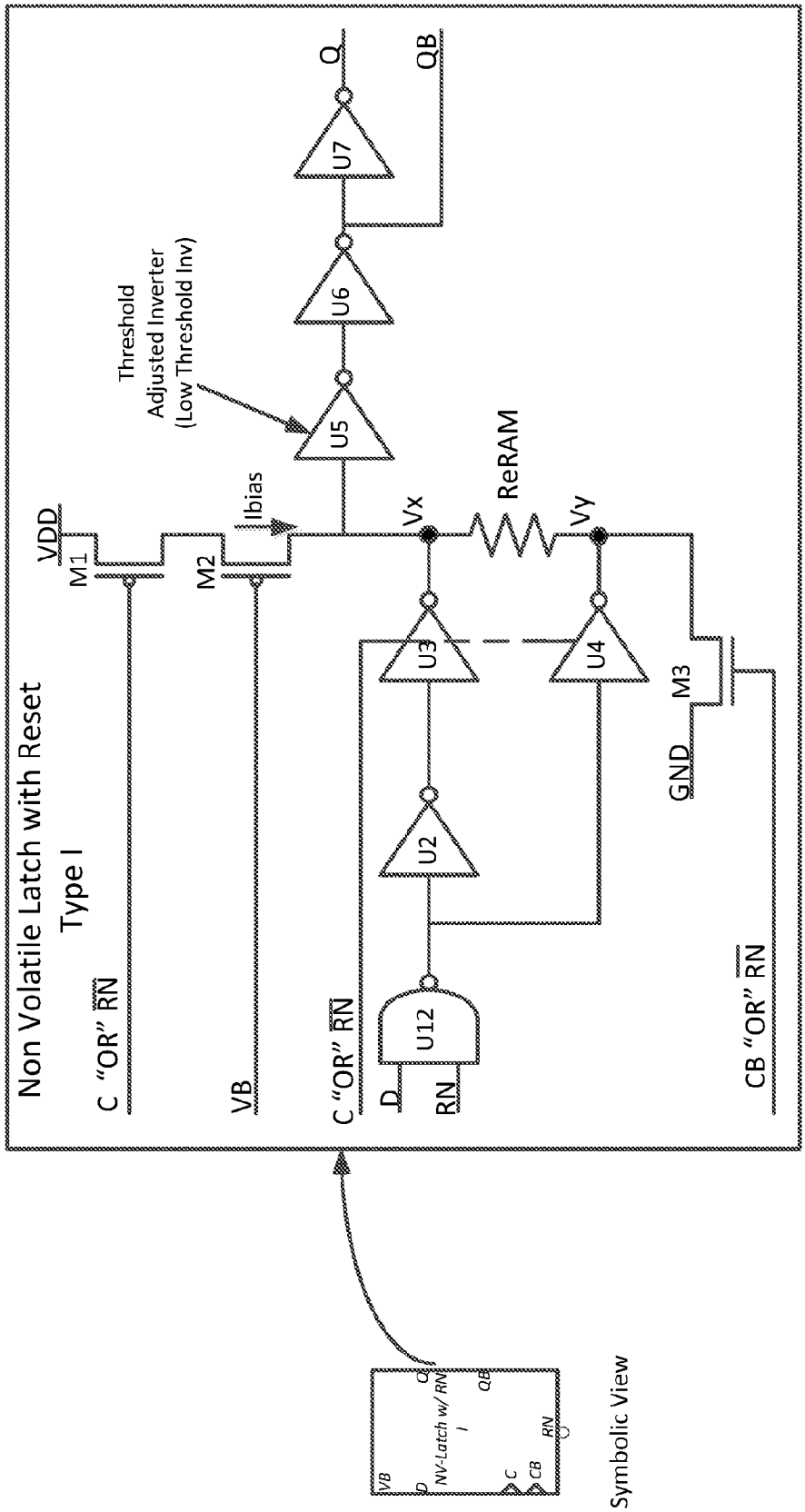
Non Volatile Latch with Reset
Type I
C "OR" RN
VB
C "OR" RN
D
RN
CB "OR" RN
VDD
M1
M2
Ibias
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
Vx
ReRAM
Vy
U3
U4
U2
U12
M3
GND
NV-Latch w/ RN
I
VB
D
C
CB
RN
Q
QB
Symbolic View

FIGURE 4

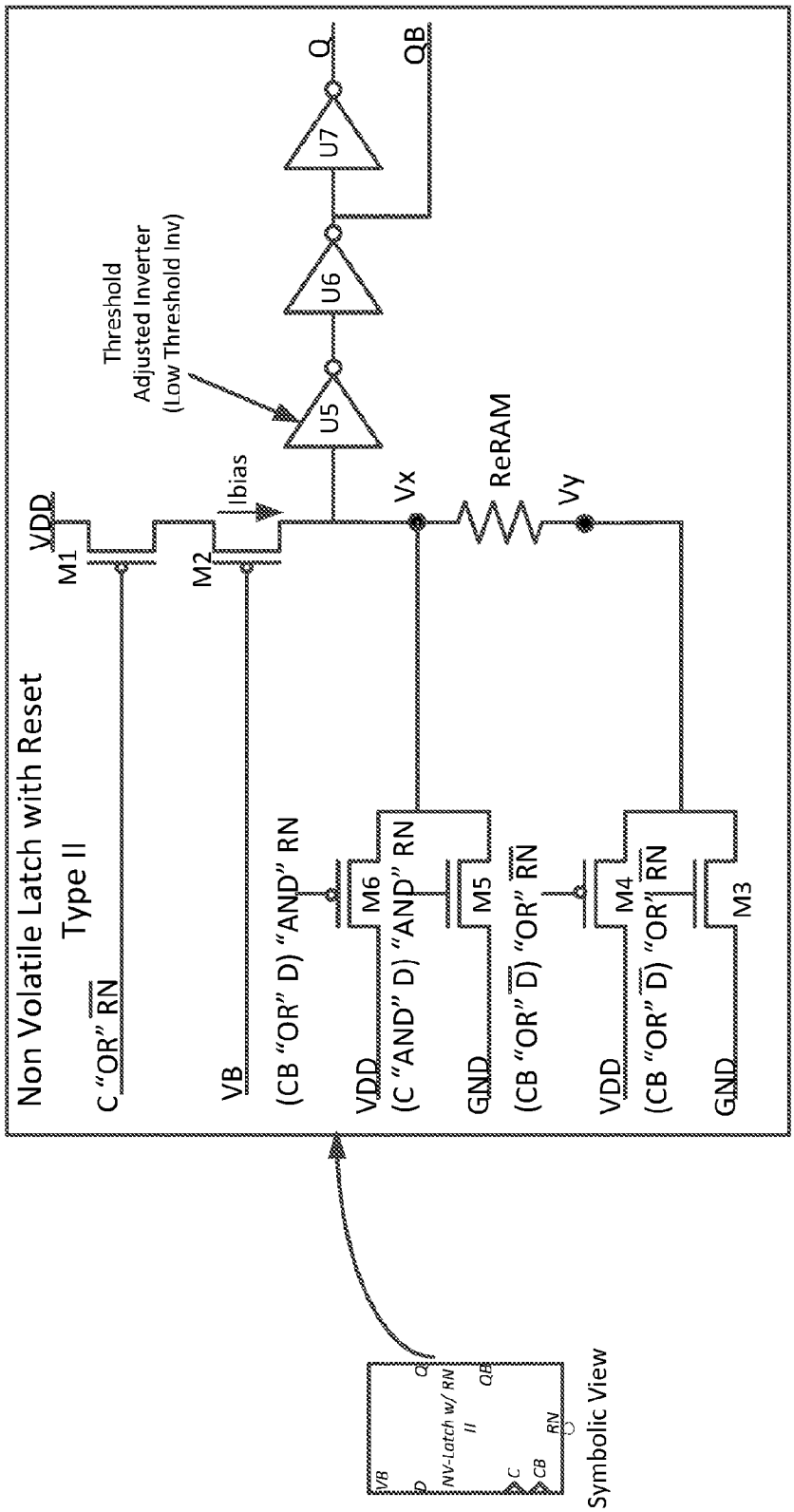
Non Volatile Latch with Reset
Type II
C "OR" RN
VB
(CB "OR" D) "AND" RN
VDD
(C "AND" D) "AND" RN
GND
(CB "OR" D) "OR" RN
VDD
(CB "OR" D) "OR" RN
GND
M1
M2
M3
M4
M5
M6
VDD
Ibias
Vx
ReRAM
Vy
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
Symbolic View
NV-Latch w/ RN
VB
D
C
CB
RN
Q
QB

FIGURE 5

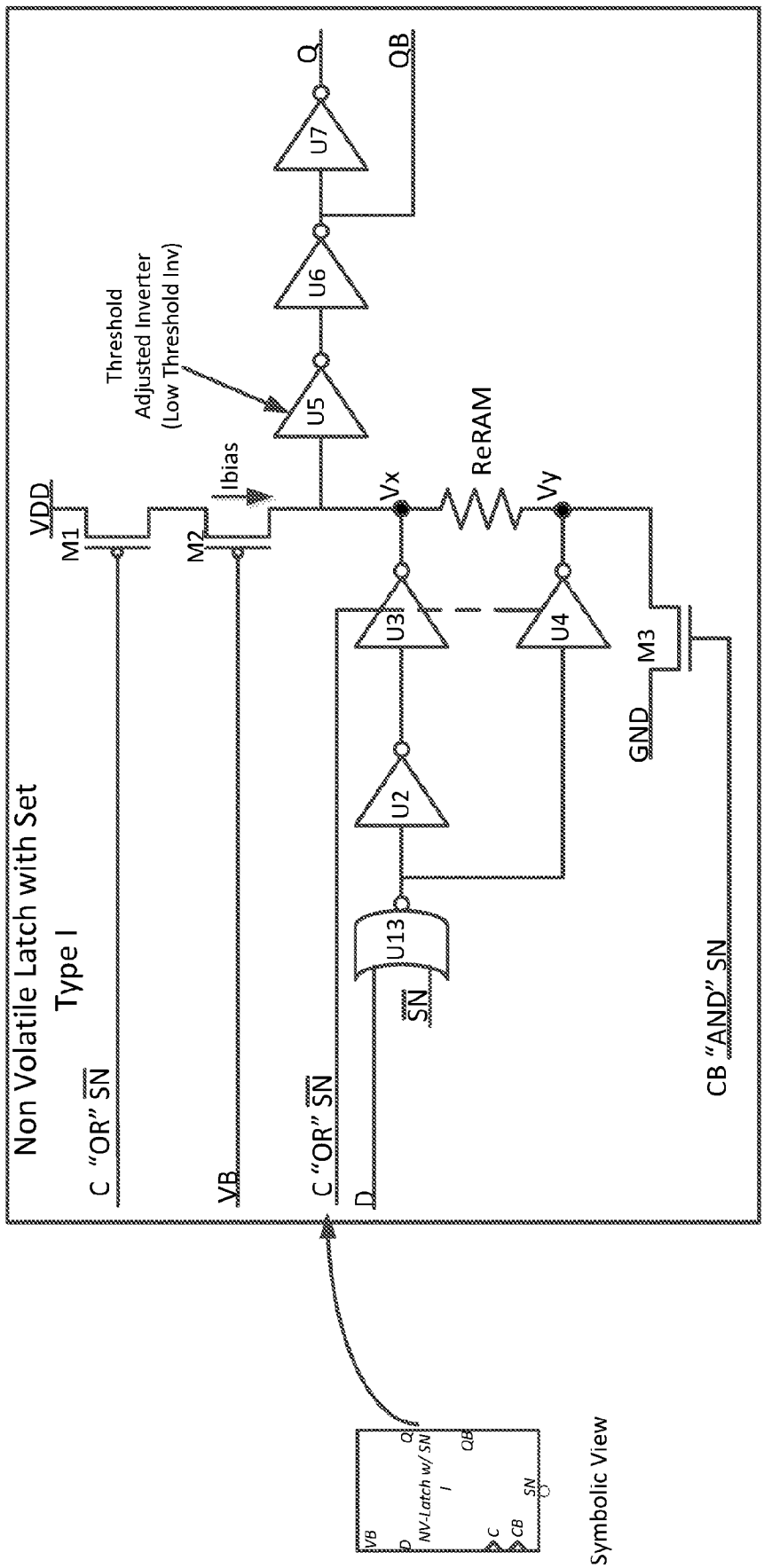
Non Volatile Latch with Set
Type I
C "OR" SN
VB
C "OR" SN
D
CB "AND" SN
VDD
M1
M2
Ibias
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
Vx
ReRAM
Vy
U3
U4
U2
U13
SN
M3
GND
NV-Latch w/ SR
Symbolic View

FIGURE 6

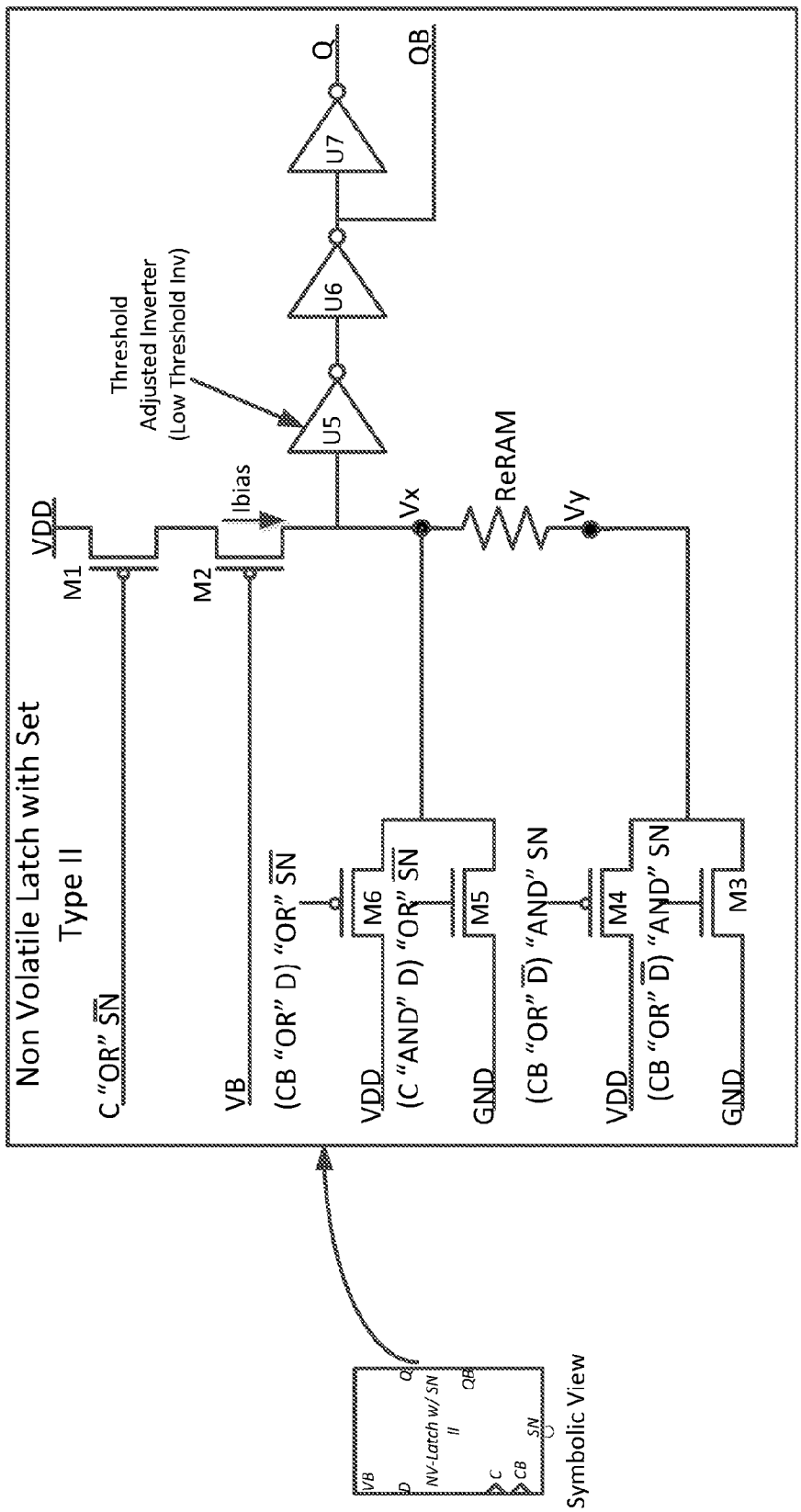
Non Volatile Latch with Set
Type II
C "OR" SN
VB
(CB "OR" D) "OR" SN
VDD
(C "AND" D) "OR" SN
GND
(CB "OR" D) "AND" SN
VDD
(CB "OR" D) "AND" SN
GND
M1
M2
M6
M5
M4
M3
Ibias
VDD
Vx
ReRAM
Vy
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U6
U7
Q
QB
Symbolic View
NV-Latch w/ SN
VB
D
C
CB
SN
Q
QB

FIGURE 7

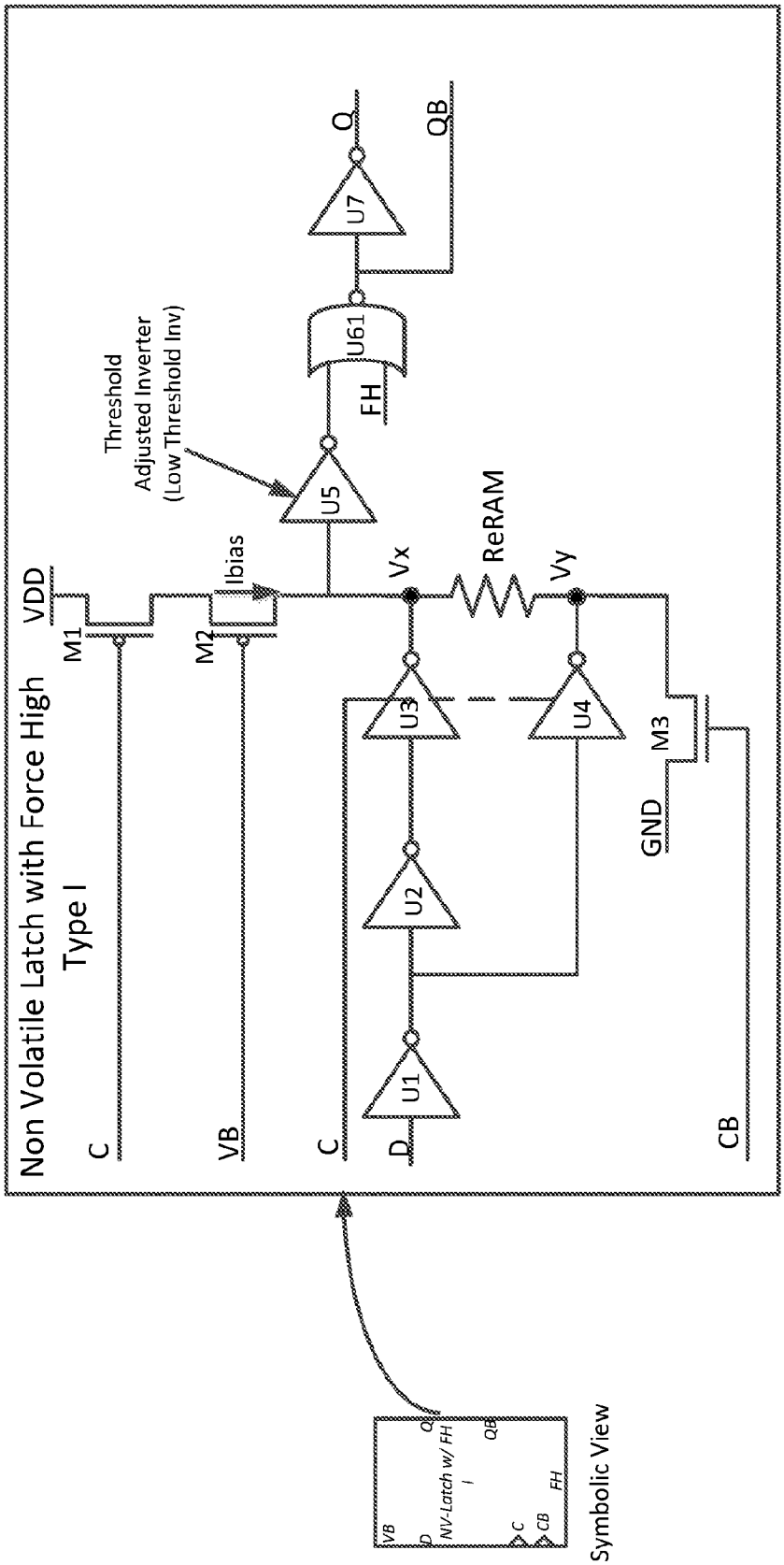
Non Volatile Latch with Force High
Type I
VDD
M1
M2
Ibias
Vx
ReRAM
Vy
U5
Threshold
Adjusted Inverter
(Low Threshold Inv)
U61
FH
U7
Q
QB
U3
U4
M3
GND
U2
U1
C
VB
C
D
CB
Symbolic View
NV-Latch w/ FH
VB
D
C
CB
FH
Q
QB

FIGURE 8

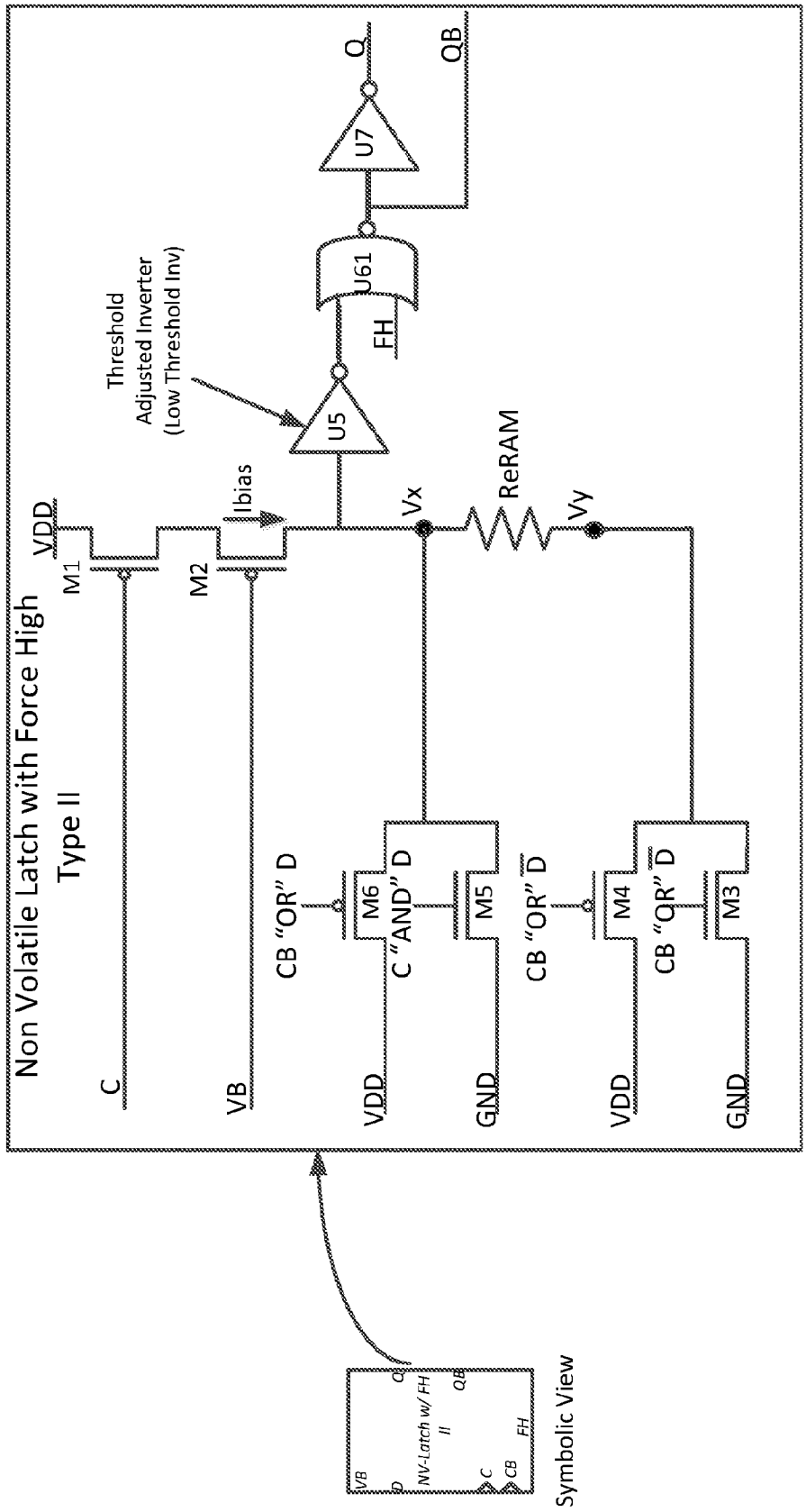
Non Volatile Latch with Force High
Type II
C
VB
VDD
M1
M2
Ibias
Vx
ReRAM
Vy
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U61
FH
U7
Q
QB
CB "OR" D
C "AND" D
M6
M5
CB "OR" $\overline{D}$
CB "QR" $\overline{D}$
M4
M3
VDD
GND
VDD
GND
Symbolic View
NV-Latch w/ FH
II
VB
D
C
CB
FH
Q
QB

FIGURE 9

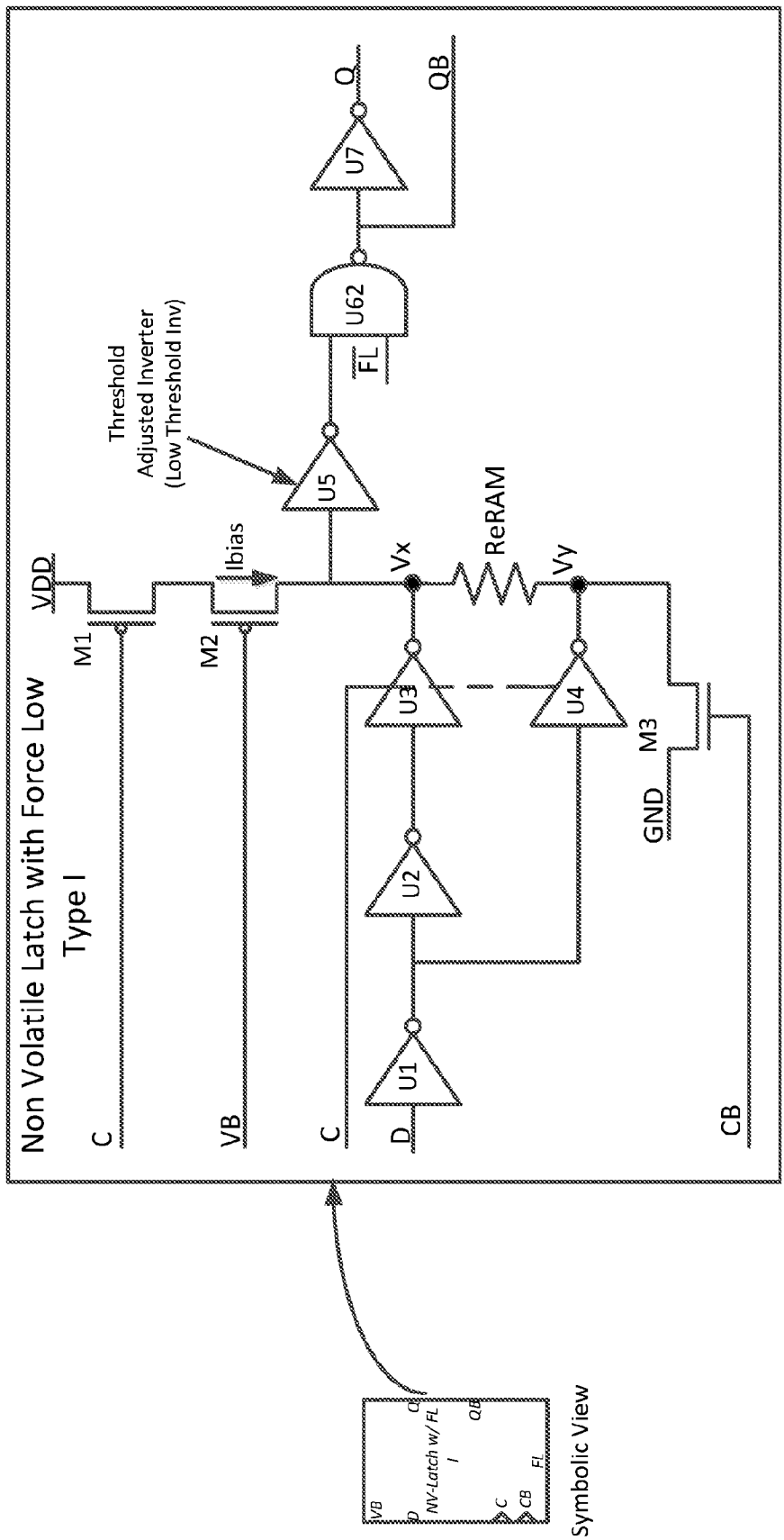
Non Volatile Latch with Force Low
Type I
VDD
M1
M2
Ibias
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U62
FL
Q
QB
U7
Vx
ReRAM
Vy
U3
U4
M3
GND
U2
U1
C
VB
C
D
CB
Symbolic View
NV-Latch w/ FL
VB
D
C
CB
FL
Q
QB

FIGURE 10

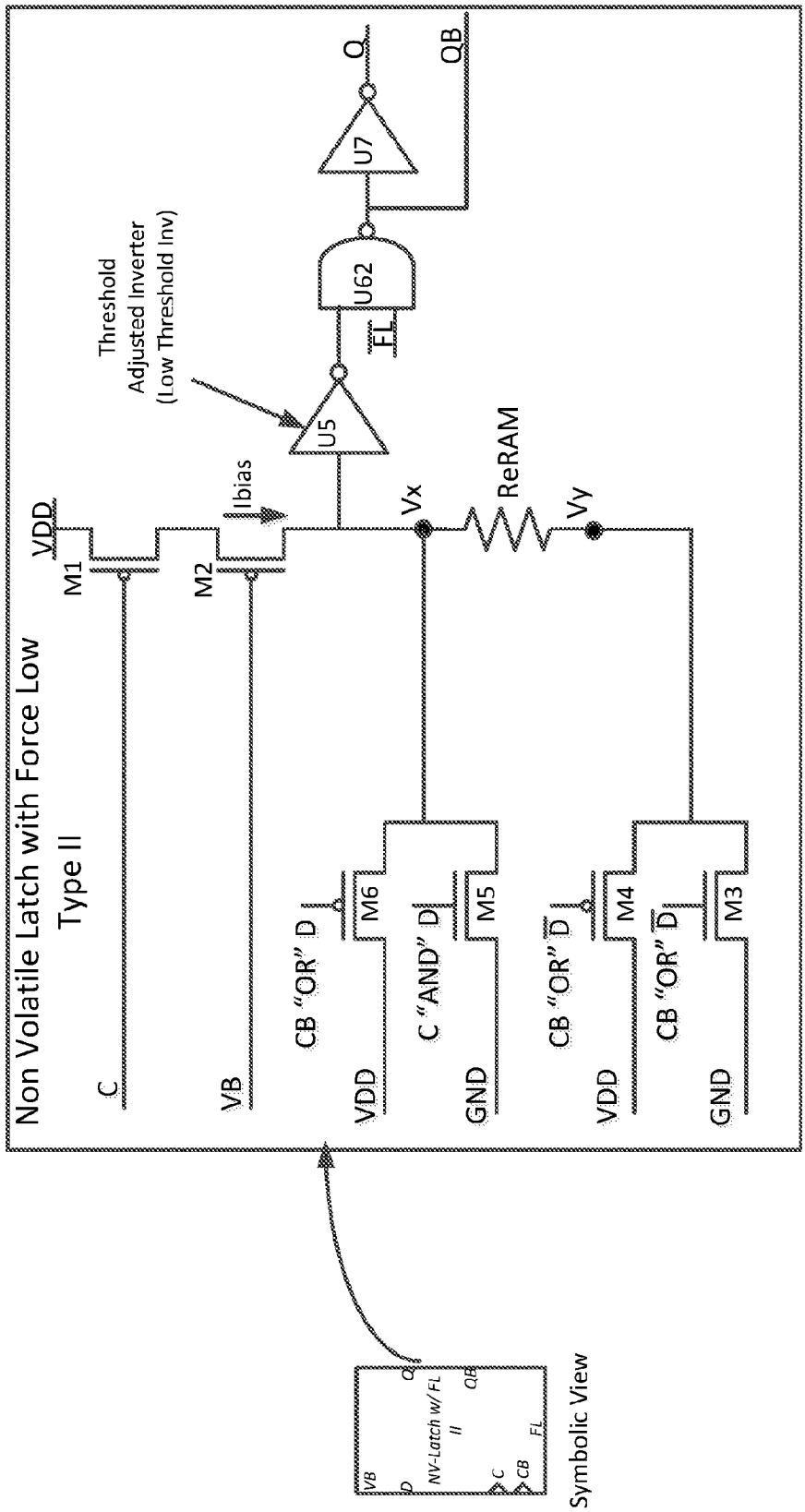
Non Volatile Latch with Force Low
Type II
VDD
M1
M2
Ibias
C
VB
Vx
ReRAM
Vy
Threshold
Adjusted Inverter
(Low Threshold Inv)
U5
U62
FL
U7
Q
QB
CB "OR" D
M6
VDD
C "AND" D
M5
GND
CB "OR" $\overline{D}$
M4
VDD
CB "OR" $\overline{D}$
M3
GND
NV-Latch w/ FL
II
VB
D
C
CB
FL
Q
QB
Symbolic View

FIGURE 11

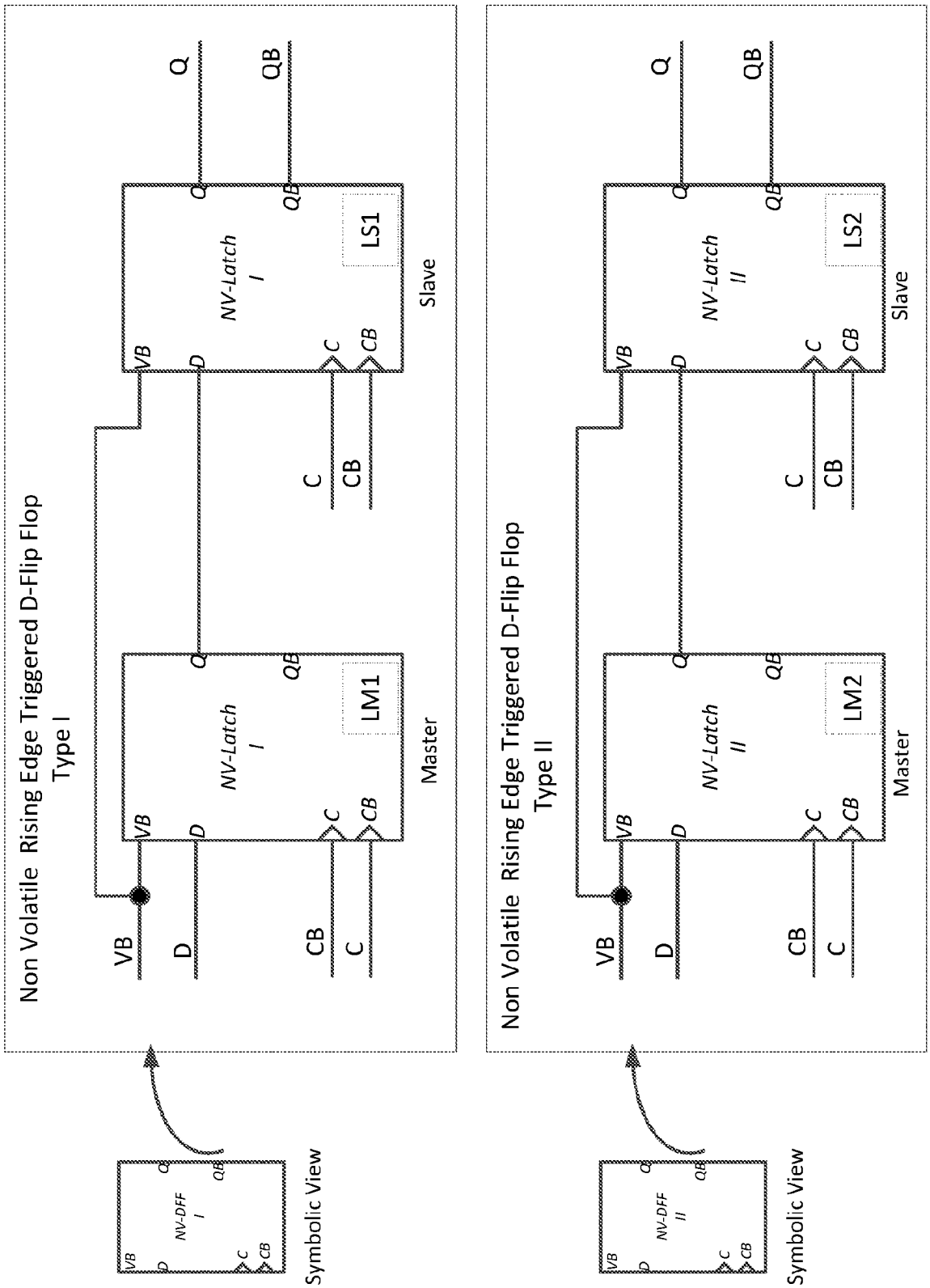
Non Volatile Rising Edge Triggered D-Flip Flop
Type I
NV-Latch
I
LM1
LS1
Master
Slave
VB
D
CB
C
Q
QB
Symbolic View
NV-DFF
I
Non Volatile Rising Edge Triggered D-Flip Flop
Type II
NV-Latch
II
LM2
LS2
NV-DFF
II

FIGURE 12

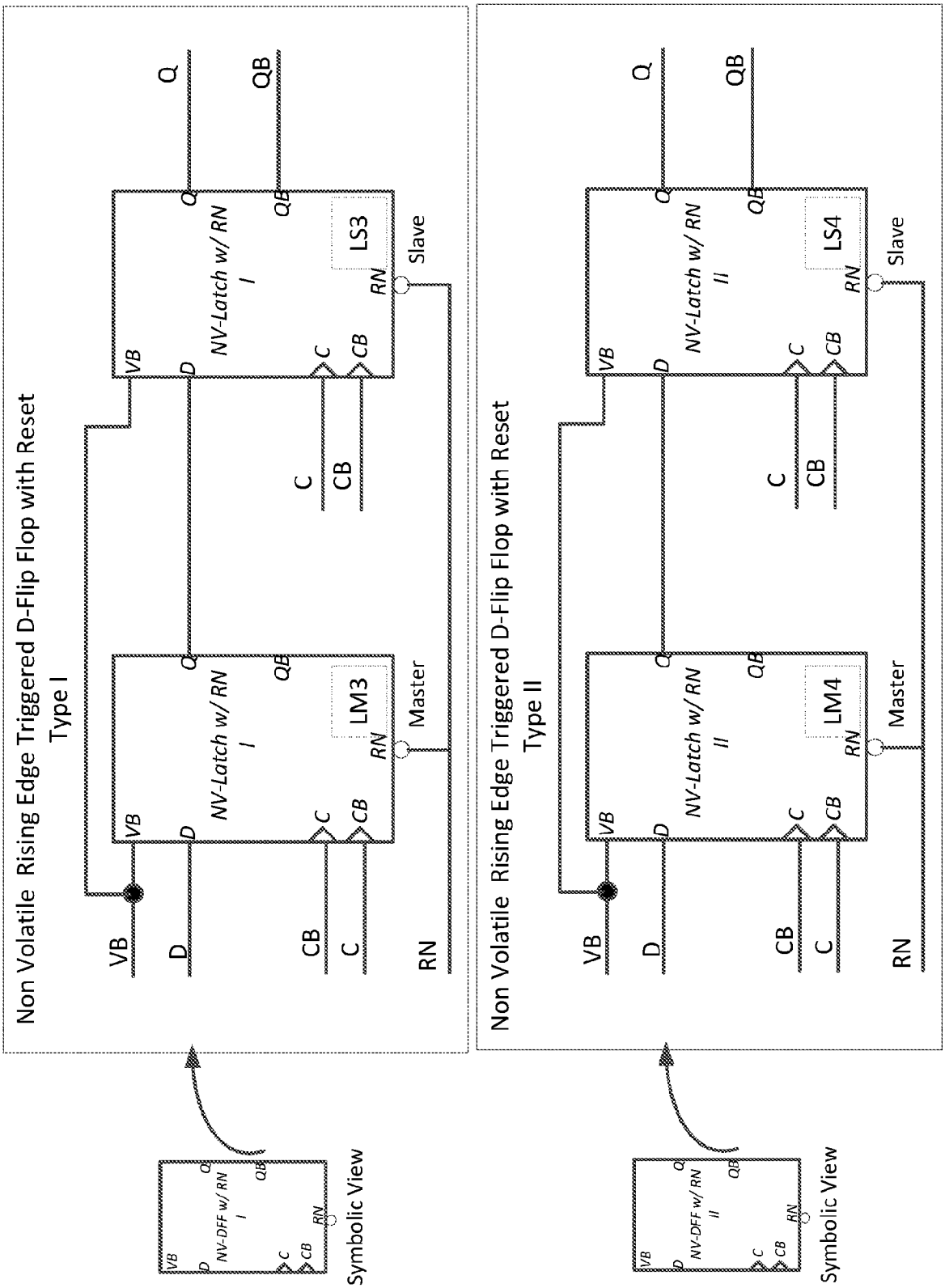
Non Volatile Rising Edge Triggered D-Flip Flop with Reset
Type I
VB
D
CB
C
RN
Q
QB
NV-Latch w/ RN
I
LM3
LS3
Master
Slave
Symbolic View
NV-DFF w/ RN
I
Non Volatile Rising Edge Triggered D-Flip Flop with Reset
Type II
NV-Latch w/ RN
II
LM4
LS4
NV-DFF w/ RN
II

FIGURE 13

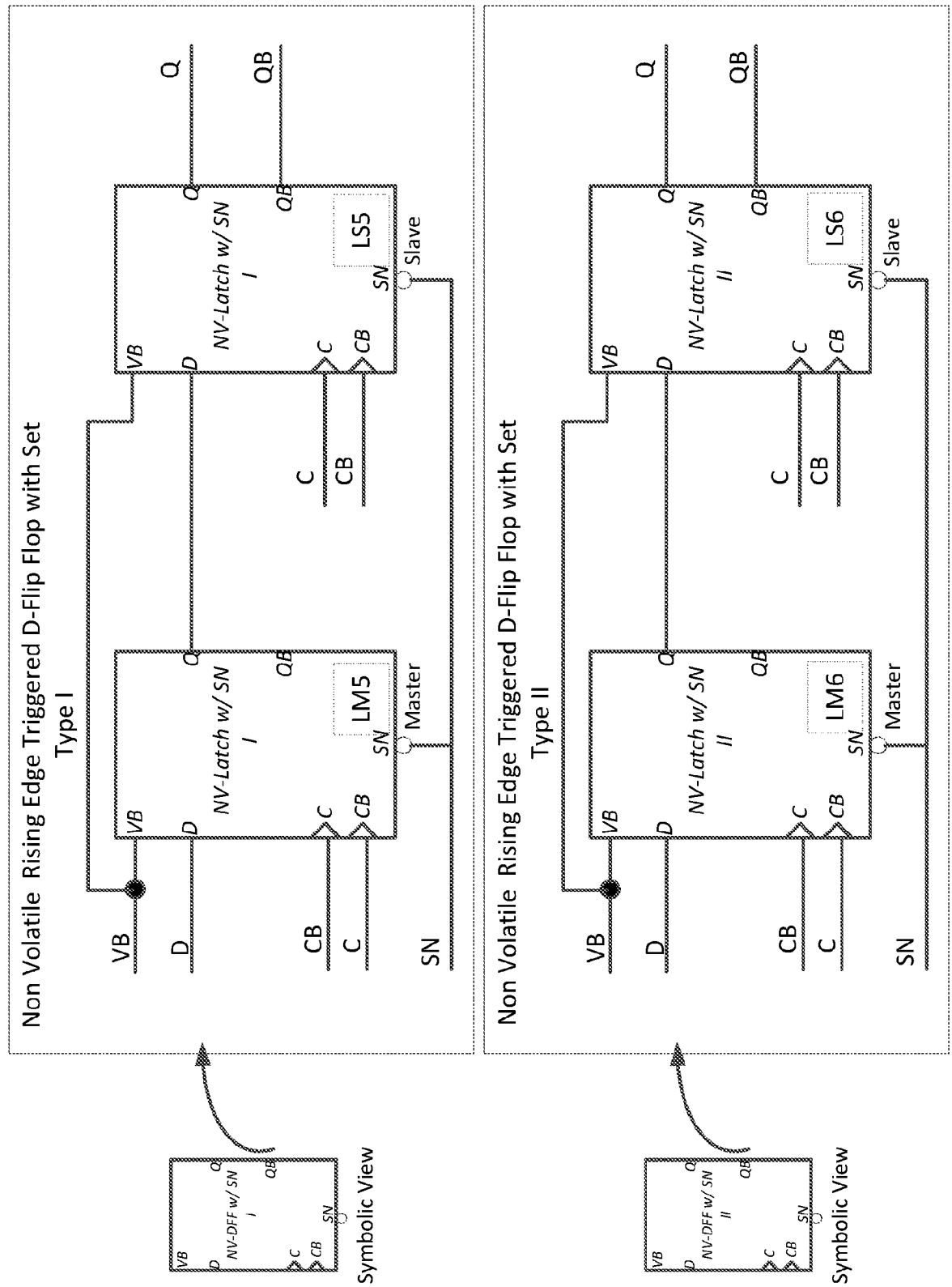
Non Volatile Rising Edge Triggered D-Flip Flop with Set
Type I
VB
D
CB
C
SN
NV-Latch w/ SN
I
LM5
Master
LS5
Slave
Q
QB
Symbolic View
NV-DFF w/ SN
I
Non Volatile Rising Edge Triggered D-Flip Flop with Set
Type II
NV-Latch w/ SN
II
LM6
LS6
NV-DFF w/ SN
II

FIGURE 14

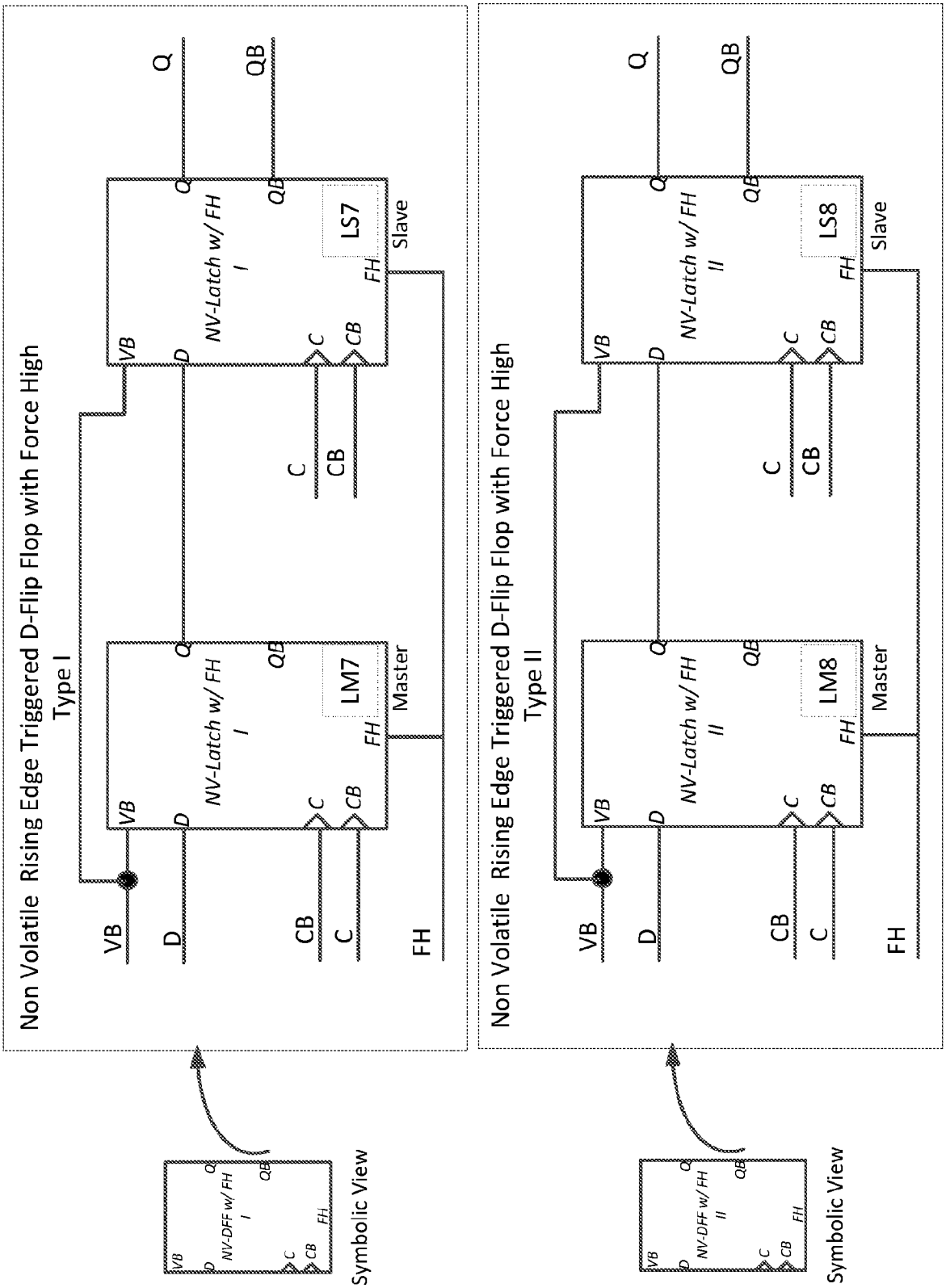
Non Volatile Rising Edge Triggered D-Flip Flop with Force High
Type I
VB
D
CB
C
FH
Q
QB
NV-Latch w/ FH
I
LM7
Master
LS7
Slave
Symbolic View
NV-DFF w/ FH
I
Non Volatile Rising Edge Triggered D-Flip Flop with Force High
Type II
NV-Latch w/ FH
II
LM8
LS8
NV-DFF w/ FH
II

FIGURE 15

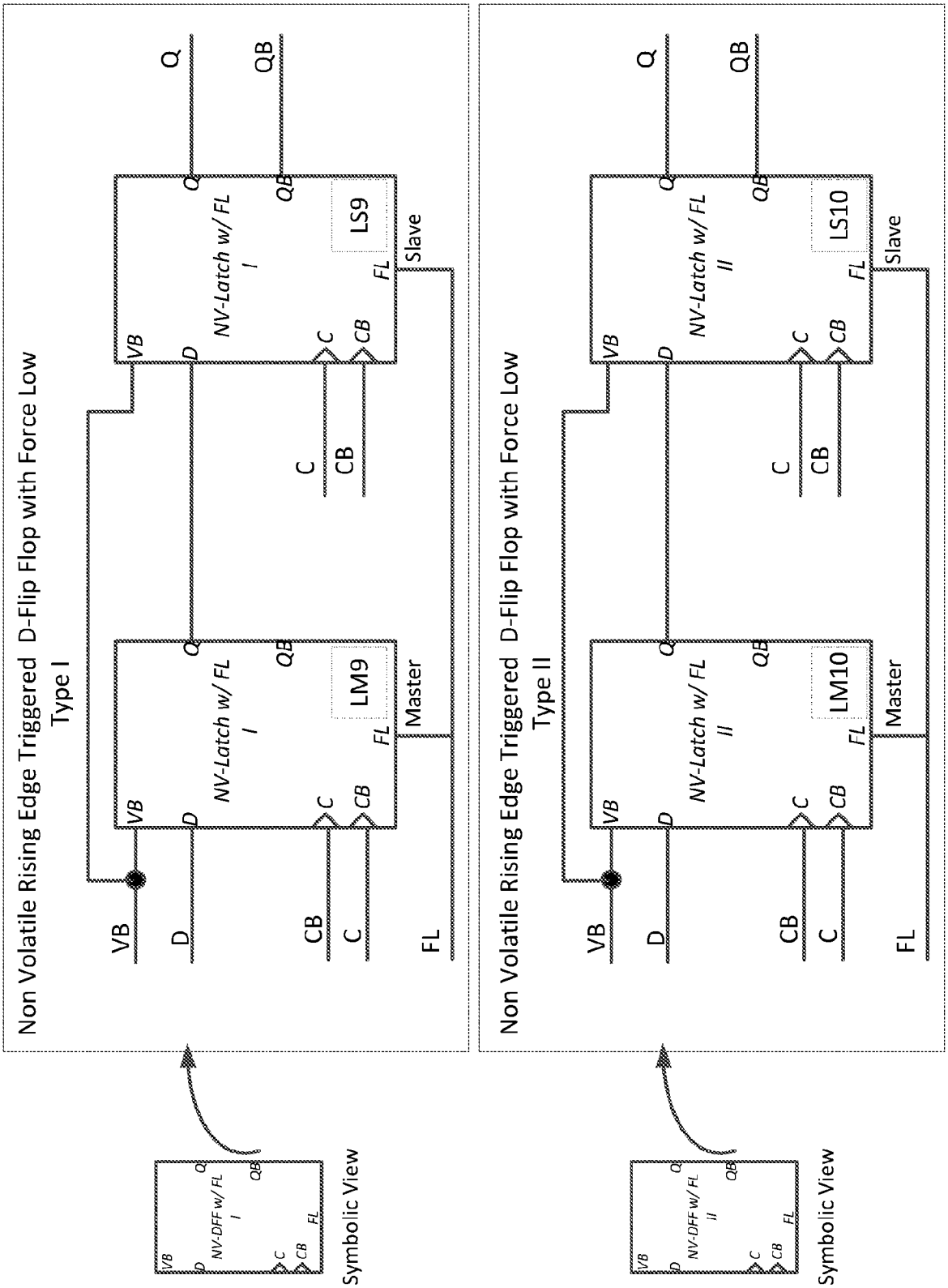
Non Volatile Rising Edge Triggered D-Flip Flop with Force Low
Type I
VB
D
CB
C
FL
NV-Latch w/ FL
I
LM9
LS9
Master
Slave
Q
QB
Symbolic View
NV-DFF w/ FL
I
Non Volatile Rising Edge Triggered D-Flip Flop with Force Low
Type II
NV-Latch w/ FL
II
LM10
LS10
NV-DFF w/ FL
II

FIGURE 16

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2014/061433

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C13/00 G11C14/00
ADD. G11C19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2010/065691 A1 (QUALCOMM INC [US]; CHUA-EOAN LEW G [US]) 10 June 2010 (2010-06-10) paragraph [0032] - paragraph [0040]; figures 3,4	1-37
A	US 2013/107606 A1 (KATOH YOSHIKAZU [JP]) 2 May 2013 (2013-05-02) paragraph [0205] - paragraph [0243]; figures 16-19	1-37

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
1 September 2014	11/09/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Colling, Pierre

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2014/061433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2010065691 A1	10-06-2010	CN 102227777 A	26-10-2011
		EP 2364497 A1	14-09-2011
		JP 5274670 B2	28-08-2013
		JP 2012510695 A	10-05-2012
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		WO 2010065691 A1	10-06-2010
US 2013107606 A1	02-05-2013	CN 102763331 A	31-10-2012
		JP 5075294 B2	21-11-2012
		US 2013107606 A1	02-05-2013
		WO 2012108151 A1	16-08-2012