(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
01 August 2019 (01.08.2019)

(10) **International Publication Number**
WO 2019/144854 A1

(51) **International Patent Classification:**
H01L 33/54 (2010.01)

(21) **International Application Number:**
PCT/CN2019/072486

(22) **International Filing Date:**
21 January 2019 (21.01.2019)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
15/879,576 25 January 2018 (25.01.2018) US

(71) **Applicants: SHENZHEN SKYWORTH-RGB ELECTRONIC CO., LTD.** [CN/CN]; 13-16 F, Block A, Skyworth Building, Shennan Road, Nanshan District, Shenzhen, Guangdong 518057 (CN). **RADIANT CHOICE LIMITED** [GB/GB]; P. O. Box 941, The Valley, Anguilla PI-2640 (AI).

(72) **Inventors: TRAN, Nguyenthe**; 1524 W Tonia Ct., Anaheim, California 92802 (US). **YOU, Jiun-pyng**; 61 Bershire Wood, Irvine, Califonia 92620 (US).

(74) **Agent: CENFO INTELLECTUAL PROPERTY AGENCY**; 201, Auto Electric Power Building, North Zone, High-Tech Industrial Park, No. 3, Songping Mountain Road, Yuehai Street, Nanshan District, Shenzhen, Guangdong 518057 (CN).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) **Title:** PACKAGE BODY AND LIGHT EMITTING DEVICE USING SAME

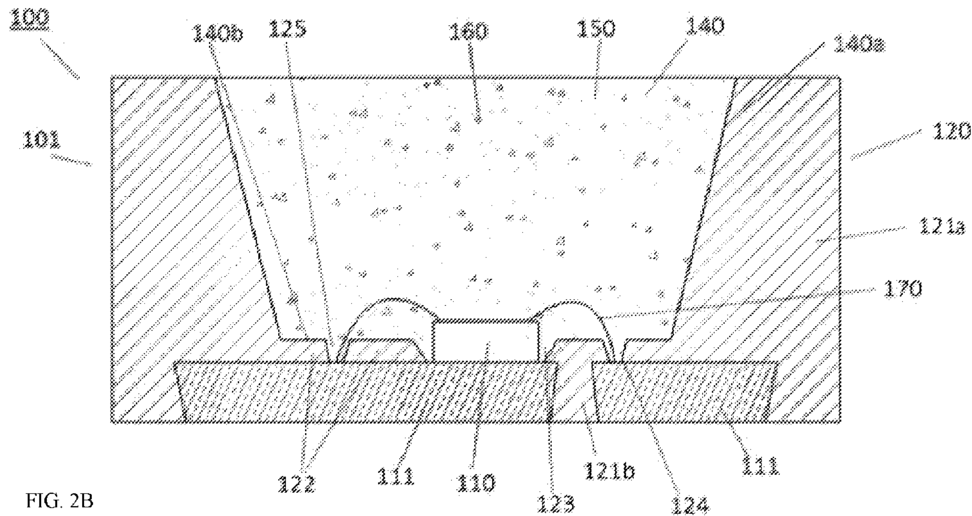
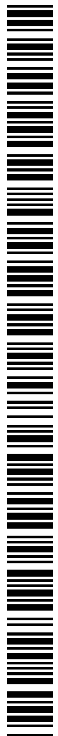


FIG. 2B

(57) **Abstract:** A package body for a semiconductor device includes a lead frame, an insulating package, and a reflective coating layer. The lead frame has a first electrode and a second electrode separated from each other. The insulating package provides a housing structure and forming a package cavity therein. The package cavity has a reflective side surface formed by the insulating package. The reflective coating layer partially covers the first electrode and the second electrode and forms a reflective bottom surface of the package cavity. Each of the first electrode and the second electrode may have an angled cut. The insulating package may be made of a binder-filler composite containing white pigments. The package body may be an all diffusive integrated reflecting surfaces (AR-IRS) package body, and may be used in an encapsulant-free semiconductor package.



WO 2019/144854 A1

[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

PACKAGE BODY AND LIGHT EMITTING DEVICE USING SAME

Description

[1] FIELD

[2] The present disclosure relates generally to liquid crystal displays, and more particularly to a package body with all diffusive integrated reflecting surfaces (AD-IRS) for a light emitting device, and a light emitting device using the AD-IRS package body.

[3] BACKGROUND

[4] The background description provided herein is for the purpose of generally presenting the context of the present disclosure. The subject matter discussed in the background of the disclosure section should not be assumed to be prior art merely as a result of its mention in the background of the disclosure section. Similarly, a problem mentioned in the background of the disclosure section or associated with the subject matter of the background of the disclosure section should not be assumed to have been previously recognized in the prior art. The subject matter in the background of the disclosure section merely represents different approaches, which in and of themselves may also be disclosures. Work of the presently named inventors, to the extent it is described in the background of the disclosure section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[5] A light emitting device (LED), sometimes also referred to as a light emitting diode, is a sort of semiconductor device that changes electricity into infrared rays or light by using the characteristics of compound semiconductors to input/ output a signal, which may be used as a light source. Typically, a LED package includes a package body, also referred to as a lead frame package, and one LED chip (or multiple LED chips) electrically connected to terminals of the package body via small metal wires such as gold wires. For example, in a semiconductor device using a conventional lead frame package, the a conventional package body may have a lead frame substrate that is typically coated with a metal such as silver, which functions as a lead frame, and a thermoplastic body that is made of thermoplastic resin and formed on and around the lead frame substrate. The thermoplastic body may form a reflecting cup, which has a bottom reflecting surface on the surface of the lead frame substrate. However, the thermoplastic resin of the thermoplastic body has little adhesion with the lead frame substrate, and the resin part of the thermoplastic body and the lead frame substrate are likely to be detached. Further, the interface between the reflecting cup of the ther-

moplastic body and the bottom reflecting surface on the lead frame substrate shows potential for gas leakage due to the low adhesion between these two materials, as disclosed in U.S. Patent No. 8,530,250. Moreover, the metal coating of the lead frame is very expensive and time consuming. The metal coating also causes long-term reliability issues such as sulfidation on silver plating which reduces the optical output. Conventional LED package also has an encapsulating layer that covers the LED chip (or LED chips) and fills the cavity of the lead frame or the chip-on-board package. The encapsulating layer usually has low thermal dissipation property that restricts heat flow.

[6] Generally, LED package design involves the simultaneous integration and balancing of many different design factors including optical, thermal, mechanical, and electrical challenges. Designing of LED package becomes more challenging to ensure the reliability of an LED package as the demand of power per package area increases. High power density per unit area could lead to material failures including delamination of integrated parts of LED package and degradation of reflectivity and optical properties of materials.

[7] Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

[8] SUMMARY

[9] It is therefore one main object of this disclosure to provide a package body for a semiconductor device, aiming to address the aforementioned deficiencies and inadequacies.

[10] In one aspect, the disclosure relates to a package body for a semiconductor device. In one embodiment, the package body includes a lead frame having a first electrode and a second electrode separated from each other; an insulating package providing a housing structure and forming a package cavity therein, where the package cavity has a reflective side surface formed by the insulating package; and a reflective coating layer partially covering the first electrode and the second electrode and forming a reflective bottom surface of the package cavity.

[11] In one embodiment, the package body is an all diffusive integrated reflecting surfaces (AR-IRS) package body.

[12] In one embodiment, the first electrode and the second electrode are separated by the insulating package.

[13] In one embodiment, each of the first electrode and the second electrode has an angled cut such that a bottom surface area of the first electrode is smaller than a top surface area of the first electrode, and a bottom surface area of the second electrode is smaller than a top surface area of the second electrode.

[14] In one embodiment, each of the first electrode and the second electrode has a vertical

cut.

[15] In one embodiment, at least one semiconductor chip is configured to be attached to the first electrode and electrically connected to the first electrode and the second electrode respectively.

[16] In one embodiment, the reflective coating layer has a first recess, a second recess and at least one chip recess formed thereon, where a portion of the lead frame is exposed through each of the at least one chip recess to provide a chip-attaching area, such that the at least one semiconductor chip is attached to the lead frame via the at least one chip recess; a portion of the first electrode is exposed through the first recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the first electrode through a first wire via the first recess; and a portion of the second electrode is exposed through the second recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the second electrode through a second wire via the second recess.

[17] In one embodiment, the at least one semiconductor chip comprises a light emitting diode (LED) chip or a laser diode (LD) chip.

[18] In one embodiment, the insulating package is made of a binder-filler composite containing white pigments.

[19] In one embodiment, the binder-filler composite is polycyclohexylenedimethylene terephthalate (PCT), polyphthalamide (PPA), a silicone resin, a silicone molding resin, an epoxy molding resin, an acrylate resin, an urethane resin, or a copolymer system thereof, and the white pigments are made of at least one pigment selected from the group consisting of TiO2, SiO2, Al2O3, BN, MgO, CaO, ZrO2, ZnO, BaO, AlN, Sb2O3, and BaSO4.

[20] In one embodiment, the white pigments are amorphous, partially crystalline, crystalline or a mixture thereof in any ratio, and the white pigments have a weight ratio from 1 to 95 percent of the binder-filler composite forming the insulating package.

[21] In one embodiment, each of the white pigments has a size from 10 nm to 10 microns.

[22] In one embodiment, the reflective coating layer is made of the same binder-filler composite forming the insulating package.

[23] In one embodiment, the reflective coating layer is made of a binder filler composite different from the binder-filler composite forming the insulating package.

[24] Another aspect of the present disclosure relates to an encapsulant-free semiconductor package, which includes: a semiconductor flip-chip; and a package body as described above, where the reflective coating layer has at least one recess formed thereon, and a portion of the first electrode and a portion of the second electrode of the lead frame are exposed through the at least one recess to provide a bonding pad area, such that the semiconductor flip-chip is attached to the first electrode and the second electrode via

the at least one recess.

[25] In one embodiment, the semiconductor flip-chip is a light emitting diode (LED) flip-chip or a laser diode (LD) flip-chip.

[26] In one embodiment, the LED flip-chip or the LD flip-chip is configured to emit a blue light, a green light, a red light or a white light.

[27] In one embodiment, the semiconductor flip-chip is coated with a thin coating of a transparent material.

[28] In one embodiment, the semiconductor flip-chip is configured to emit light in a first color, and the transparent material comprises a light conversion material to partially convert the light emitted by the semiconductor flip-chip to a second color different from the first color.

[29] A further aspect of the present disclosure relates to a method for forming a package body as described above. In certain embodiments, the method includes: providing a lead frame array; punching or etching the lead frame array to form a plurality of electrode separating gaps and a plurality of package gaps; forming the insulating package and the reflective coating layer on the lead frame array to form a semiconductor package array; and dicing or singulating the package body from the package array along the package gaps, where one of the electrode separating gaps separates the first electrode and the second electrode of the lead frame of the package body.

[30] In one embodiment, the method further includes: forming a coating on the lead frame array to cover at least exposed areas of the lead frame of the package body.

[31] In one embodiment, the insulating package and the reflective coating layer are formed by transfer molding, compressing molding or injection molding.

[32] A further aspect of the present disclosure relates to a LED device, which includes the package body as described above, and a LED chip attached to the package body.

[33] Yet a further aspect of the present disclosure relates to a package body for a semiconductor device, which includes: a substrate; a first electrode and a second electrode formed on the substrate and separated from each other; an insulating package providing a housing structure and forming a package cavity therein, where the package cavity has a reflective side surface formed by the insulating package; and a reflective coating layer forming a reflective bottom surface of the package cavity and partially covering the first electrode and the second electrode.

[34] In one embodiment, the first electrode and the second electrode are formed by a lead frame.

[35] In one embodiment, a semiconductor flip-chip is configured to be attached to the first electrode and the second electrode respectively.

[36] In one embodiment, the reflective coating layer has at least one recess formed thereon, and a portion of the first electrode and a portion of the second electrode of the

lead frame are exposed through the at least one recess to provide a bonding pad area, such that the semiconductor flip-chip is attached to the first electrode and the second electrode via the at least one recess.

[37] In one embodiment, at least one semiconductor chip is configured to be attached to the first electrode and electrically connected to the first electrode and the second electrode respectively.

[38] In one embodiment, the reflective coating layer has a first recess, a second recess and at least one chip recess formed thereon, where a portion of the lead frame is exposed through each of the at least one chip recess to provide a chip-attaching area, such that the at least one semiconductor chip is attached to the lead frame via the at least one chip recess; a portion of the first electrode is exposed through the first recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the first electrode through a first wire via the first recess; and a portion of the second electrode is exposed through the second recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the second electrode through a second wire via the second recess.

[39] According to certain embodiments of the disclosure, the package body provides highly optical and reliable reflecting surfaces at the side and bottom of the package cavity, thus improving optical output and reliability of the semiconductor package.

[40] These and other aspects of the disclosure will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be affected without departing from the spirit and scope of the novel concepts of the disclosure.

[41] BRIEF DESCRIPTION OF THE DRAWINGS

[42] To better illustrate the technical solutions that are reflected in various embodiments according to this disclosure or that are found in the prior art, the accompanying drawings intended for the description of the embodiments herein or for the prior art will now be briefly described, it is evident that the accompanying drawings listed in the following description show merely some embodiments according to this disclosure, and that those having ordinary skill in the art will be able to obtain other drawings based on the arrangements shown in these drawings without making inventive efforts, where in these drawings.

[43] FIG. 1 is a schematic cross-sectional view of a semiconductor device using a lead frame package according to one embodiment of the disclosure;

[44] FIG. 2A is a schematic top view of a semiconductor package structure according to one embodiment of the disclosure;

[45] FIG. 2B is a schematic cross-sectional view along the line A-A of the semiconductor package structure as shown in FIG. 2A.

[46] FIG. 3A is a schematic top view of a lead frame array before the semiconductor packages are made and diced according to one embodiment of the disclosure.

[47] FIG. 3B is a schematic top view of a lead frame array before the semiconductor packages are made and diced according to a different embodiment of the disclosure.

[48] FIG. 4A is a schematic view of a semiconductor package array according to one embodiment of the disclosure.

[49] FIG. 4B is a schematic view of a semiconductor package array according to a different embodiment of the disclosure.

[50] FIG. 4C is a schematic view of a semiconductor package array according to a further different embodiment of the disclosure.

[51] FIG. 4D is a schematic view of a semiconductor package array according to yet a further different embodiment of the disclosure.

[52] FIG. 5 is a flowchart of a method of forming the package body according to one embodiment of the disclosure.

[53] FIG. 6 is a schematic cross-sectional view of a chip-on-board (COB) package structure according to one embodiment of the disclosure.

[54] FIG. 7A is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to one embodiment of the disclosure.

[55] FIG. 7B is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to another embodiment of the disclosure.

[56] FIG. 7C is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to a further embodiment of the disclosure.

[57] FIG. 7D is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to yet another embodiment of the disclosure.

[58] FIG. 7E is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to yet a further embodiment of the disclosure.

[59] FIG. 7F is a schematic cross-sectional view of an encapsulant-free semiconductor package structure according to a further embodiment of the disclosure.

[60] FIG. 8 is a schematic view of a semiconductor package array for the encapsulant-free semiconductor packages according to one embodiment of the disclosure.

[61] The realization of the aim, functional characteristics, advantages of the present disclosure are further described specifically with reference to the accompanying drawings and embodiments.

[62] DETAILED DESCRIPTION

[63] The disclosure will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the disclosure are shown. This disclosure may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments

are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Like reference numerals refer to like elements throughout.

[64] The terms used in this specification generally have their ordinary meanings in the art, within the context of the disclosure, and in the specific context where each term is used. Certain terms that are used to describe the disclosure are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the disclosure. For convenience, certain terms may be highlighted, for example using italics and/or quotation marks. The use of highlighting and/or capital letters has no influence on the scope and meaning of a term; the scope and meaning of a term are the same, in the same context, whether or not it is highlighted and/or in capital letters. It will be appreciated that the same thing can be said in more than one way. Consequently, alternative language and synonyms may be used for any one or more of the terms discussed herein, nor is any special significance to be placed upon whether or not a term is elaborated or discussed herein. Synonyms for certain terms are provided. A recital of one or more synonyms does not exclude the use of other synonyms. The use of examples anywhere in this specification, including examples of any terms discussed herein, is illustrative only and in no way limits the scope and meaning of the disclosure or of any exemplified term. Likewise, the disclosure is not limited to various embodiments given in this specification.

[65] It will be understood that when an element is referred to as being “on” another element, it can be directly on the other element or intervening elements may be present therebetween. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[66] It will be understood that, although the terms first, second, third, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below can be termed a second element, component, region, layer or section without departing from the teachings of the disclosure.

[67] It will be understood that when an element is referred to as being “on”, “attached” to, “connected” to, “coupled” with, “contacting”, etc., another element, it can be directly on, attached to, connected to, coupled with or contacting the other element or intervening elements may also be present. In contrast, when an element is referred to as being, for example, “directly on”, “directly attached” to, “directly connected” to,

"directly coupled" with or "directly contacting" another element, there are no intervening elements present. It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" to another feature may have portions that overlap or underlie the adjacent feature.

[68] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising", or "includes" and/or "including" or "has" and/or "having" when used in this specification specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[69] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top", may be used herein to describe one element's relationship to another element as illustrated in the figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation shown in the figures. For example, if the device in one of the figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on the "upper" sides of the other elements. The exemplary term "lower" can, therefore, encompass both an orientation of lower and upper, depending on the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[70] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[71] As used herein, the terms "comprise" or "comprising", "include" or "including", "carry" or "carrying", "has/have" or "having", "contain" or "containing", "involve" or "involving" and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

[72] As used herein, the phrase "at least one of A, B, and C" should be construed to mean a logical (A or B or C), using a non-exclusive logical OR. It should be understood that

one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the disclosure.

[73] Typically, terms such as “about,” “approximately,” “generally,” “substantially,” and the like unless otherwise indicated mean within 20 percent, preferably within 10 percent, preferably within 5 percent, and even more preferably within 3 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term “about,” “approximately,” “generally,” or “substantially” can be inferred if not expressly stated.

[74] Embodiments of the disclosure are illustrated in detail hereinafter with reference to accompanying drawings. It should be understood that specific embodiments described herein are merely intended to explain the disclosure, but not intended to limit the disclosure. In accordance with the purposes of this disclosure, as embodied and broadly described herein, this disclosure, in certain aspects, relates to a package body and a LED device using the same.

[75] FIG. 1 shows a semiconductor device using a lead frame package according to one embodiment of the disclosure. As shown in FIG. 1, the package body has a lead frame substrate 11 that is typically coated with a lead frame 12 which is made of a metal such as silver, and a thermoplastic body 13 that is made of thermoplastic resin and formed on and around the lead frame substrate 11. The thermoplastic body 13 forms a reflecting cup 14, which is a cavity that has a bottom reflecting surface 13b on the surface of the lead frame 12. The lead frame 12 includes two separate portions which are separated by a part of the thermoplastic body 13, and each portion functions as an electrode. A semiconductor chip 10 is disposed on the lead frame 12 and electrically connected to the two electrodes respectively via metal wires. Moreover, an encapsulating layer 15 is filled in the reflecting cup 14 to encapsulate the semiconductor chip 10, and the encapsulating layer 15 may be formed of a binder-filler composite, which includes a binder material and filler particles 16. A reflecting side surface 13a is provided between the thermoplastic body 13 and the encapsulating layer 15.

[76] However, in the package body as shown in FIG. 1, the thermoplastic resin of the thermoplastic body 13 and the lead frame 12 are likely to be detached due to the little adhesion between the thermoplastic resin of the thermoplastic body 13 and the lead frame 12. Further, due to the low adhesion between the two different materials, the interface between the reflecting cup 14 of the thermoplastic body 13 and the bottom reflecting surface 13b may be potentially detached for a gas leakage. Moreover, as discussed above, the encapsulating layer 15 usually has low thermal dissipation property that restricts heat flow, thus reducing the thermal dissipation efficiency of the semiconductor device.

[77] To address the aforementioned deficiencies and inadequacies, certain aspects of the

disclosure are directed to a semiconductor device, which utilized an all diffusive integrated reflecting surfaces (AR-IRS) package body as the package body for the semiconductor device. For example, FIG. 2A is a schematic top view of a semiconductor package structure according to one embodiment of the disclosure. FIG. 2B is a schematic cross-sectional view along the line A-A of the semiconductor package structure as shown in FIG. 2A. Specifically, the semiconductor package structure as shown in FIGS. 2A and 2B is a single package structure, which may be formed by dicing a semiconductor package array. In other words, the semiconductor package structure as shown in FIGS. 2A and 2B may be formed after a singulation or dicing process.

[78] As shown in FIGS. 2A and 2B, the semiconductor device 100 includes an AD-IRS package body 101, a semiconductor chip 110 attached in the package body 101, and an optical encapsulating resin layer 150. The AD-IRS package body 101 includes a lead frame 111, an insulating package 120, and a reflective coating layer 122. The semiconductor chip 110 can be any semiconductor chip. For example, when the semiconductor device 100 is a light emitting diode (LED) device, the semiconductor chip 110 can be a LED chip. Alternatively, when the semiconductor device 100 is a laser diode (LD) device, the semiconductor chip 110 can be a LD chip. The lead frame 111 includes two electrodes (namely a first electrode and a second electrode) separated from each other, for providing electrical contacts for the semiconductor chip 110 via the gold wires 170. The insulating package 120 provides a housing structure, which forms a package cavity 140 therein, such that the optical encapsulating resin layer 150 is filled in the package cavity 140 to encapsulate the semiconductor chip 110. In certain embodiments, the package cavity 140 functions as a reflective cup, which may have different shapes. In certain embodiments, the insulating package 120 includes a lateral region 121a that forms the main support of the package body 101, and a bottom region 121b that forms between the two electrodes of the lead frame 111 to electrically insulates the two electrodes from each other. The package cavity 140 has a reflective side surface 140a formed by the lateral region 121a. Further, the reflective coating layer 122 is disposed at a horizontal region extended from the insulating package 120 that partially covers the top surface of the lead frame 111, and forms a reflective bottom surface 140b of the package cavity 140. In other words, the reflective coating layer 122 partially covers the two electrodes of the lead frame 111.

[79] In certain embodiments, the lead frame 111 may have angled cuts, with the larger cut being on the bottom side of the lead frame 111, such that the lead frame 111 (i.e., the two electrodes) can be strongly held to the insulating package 120 to avoid detaching from the insulating package 120. For example, as shown in FIG. 2B, each of the two electrodes of the lead frame 111 has an angled cut, such that a bottom surface area of

each electrode is smaller than a top surface area of each electrode, thus increase bonding of each electrode of the lead frame 111 to the insulating package 120. In certain embodiments, the lead frame 111 can have vertical cuts or angled cuts.

[80] In certain embodiments, the lead frame 111 may have vertical cuts.

[81] As discussed above, the package cavity 140 functions as a reflective cup, which can have different shapes. In certain embodiments, the package cavity 140 can be shaped as an inverted truncated cone, as shown in FIGS. 2A and 2B. In certain embodiments, the package cavity 140 can be formed in other shapes, such as an inverted truncated pyramid, an inverted truncated pyramid with round corners, a parabolic shape, or other suitable shapes.

[82] The insulating package 120 and the reflective coating layer 122 are formed to provide highly optical reflecting surfaces and reliable reflecting surfaces, including the reflective side surface 140a and the reflective bottom surface 140b, thus improving the optical output and reliability of the semiconductor device 100. In certain embodiments, the insulating package 120 may be a resin package. In certain embodiments, the reflective coating layer 122 and the insulating package 120 may be made of the same material. In this case, the reflective coating layer 122 can be essentially an extended horizontal portion of the insulating package 120, which improves the bonding and holding of the lead frame 111 to the insulating package 120 and strengthens the electrically-separating region 121b of the insulating package 120 to mechanically enhance the holding of the lead frame 111 to the insulating package 120, thus improving reliability of the semiconductor device 100. In contrast, as shown in the package body as shown in FIG. 1, the electrical-separating region of the thermoplastic body 13 (which corresponds to the electrically-separating region 121b of the insulating package 120) only contacts with the lead frame 11 at small vertical sides between the two electrodes of the lead frame 11.

[83] As shown in FIGS. 2A and 2B, the reflective coating layer 122 (i.e., the extended horizontal region of the insulating package 120) covers the lead frame 111 with a plurality of openings 123, 124 and 125 to expose the lead frame 111 for semiconductor chip attaching area and wire-bonding areas. Specifically, the openings include a chip recess 123, a first recess 125 and a second recess 124. The size of the chip recess 123 is relatively small, and large enough to expose a portion of the lead frame 111 and provide a chip-attaching area, such that the semiconductor chip 110 can be attached to the lead frame 111 via the chip recess 123. Each of the first recess 125 and the second recess 124 is formed on one of the two electrodes of the lead frame 111 such that a portion of each electrode is exposed to provide a wire-bonding area, such that the semiconductor chip 110 can be electrically connected to the two electrodes through two wires via the first recess 125 and the second recess 124, respectively. Specifically,

as shown in FIGS. 2A and 2B, the chip recess 123, the first recess 125 and the second recess 124 forms multiple exposed regions on the lead frame 111, and none of the exposed regions expose the electrode separating gap (where the bottom region 121b of the insulating package 120 is located) between two electrodes, so that mechanical bonding between the electrodes of the lead frame 111 and the insulating package 120 can be improved to avoid lead frame detachment and failure as well as leaking. The single electrode exposure of the exposed region of the chip recess 123 can enable a symmetrical shape of the exposed region 123 to prevent optical output with non-symmetrical intensity distribution that causes challenge in designing optical components in some applications such as secondary optics for backlighting in liquid crystal display. In certain embodiments, the shape of the chip recess 123 can be an inverted truncated cone to provide a rotational symmetrical shape around a vertical axis. In certain embodiments, the shape of the chip recess 123 can have a polyhedron that can be viewed as being made by cutting the reflective coating layer 122 (i.e., the extended horizontal region of the insulating package 120) by extruding a polygon vertically. In certain embodiments, the polyhedron can be tapped outwardly.

[84] As shown in FIGS. 2A and 2B, the reflective coating layer 122 includes only one chip recess 123. However, in certain embodiments, the semiconductor device 100 may include multiple semiconductor chips 110. In this case, the reflective coating layer 122 may include multiple chip recesses 123 to enable the semiconductor device 100 with multiple semiconductor chips 110.

[85] In certain embodiments, reflective coating materials may be used to enhance the reflectivity of the reflective side surface 140a and the reflective bottom surface 140b of the package cavity 140. For example, in one embodiment, the reflective coating layer 122 can be a coating layer of a high light reflectivity material that covers the entire bottom and/or top surfaces of the two electrodes of the lead frame 111. In one embodiments, the surface of the lead frame 111 at the opening 123 can be plated with a high reflectivity material. In one embodiment, the surface of the lead frame 111 can be plated with the high reflectivity material. Examples of the high reflectivity material may include, without being limited thereto, silver, metal alloy, gold, tin, tin alloy, aluminum, or a combination thereof.

[86] In certain embodiments, the insulating package 120 can be made of a binder-filler composite, which includes at least one binder and at least one filler. In comparison to the conventional silver/metal coating, the binder-filler composite coating can provide better reliability and higher reflectivity. Further, the binder-filler composite coating can also act as a passive cooling agent of the package body, so that it can prolong the lifetime of the semiconductor package. In certain embodiments, the binder can be thermosetting or thermoplastic binders, and can be polymer resins or inorganic binders. In

certain embodiments, the filler can be white pigments. In certain embodiments, the insulating package 120 can be formed by transfer molding, compression molding, or injection molding. In certain embodiments, the binder-filler composite may also include a catalyst, an additive and/or an solvent. In certain embodiments, the composition of resins can be, but not limited to, polycyclohexylenedimethylene terephthalate (PCT), polyphthalamide (PPA), silicone resin, silicone molding resin, epoxy molding resin, acrylate resin, urethane resin, or a copolymer system thereof. In certain embodiments, the white pigment fillers are made of at least one pigment selected from the group consisting of TiO2, SiO2, Al2O3, BN, MgO, CaO, ZrO2, ZnO, BaO, AlN, Sb2O3, and BaSO4. In certain embodiments, the white pigments can be amorphous, partially crystalline, crystalline or a mixture in any ratio. In certain embodiments, the composition of the white pigments in the binder-filler composite is between 1 to 95 weight percent of the total composite. In other words, the white pigments may have a weight ratio from 1 to 95 percent of the binder-filler composite. In certain embodiments, the optical reflectivity of the binder-filler composite may be at least 80% at a wavelength ranging from 350 to 1000 nm, and the filler (e.g., the white pigments) can have a size from 10 nm to 10 microns to achieve high light reflectivity.

[87] In certain embodiments, the insulating package 120 and the reflective coating layer 122 can be formed in a one-step formation, in which the reflective coating layer 122 is formed together with the electrical-separating region 121b and the main portion 121a of the insulating package 120. In this case, the insulating package 120 and the reflective coating layer 122 may be made of the same material. For example, the insulating package 120 and the reflective coating layer 122 may be made of the same binder-filler composite. Alternatively, in certain embodiments, the reflective coating layer 122 can be formed separately from other regions of the insulating package 120. For example, the reflective coating layer 122 may be formed by coating on top of the lead frame 111 before the insulating package 120 is formed. In this case, the reflective coating layer 122 and the insulating package 120 can be made of the same material, or can be made of different materials. For example, the reflective coating layer 122 can be made of a binder filler composite different from the binder-filler composite forming the insulating package 120.

[88] As shown in FIGS. 2A and 2B, the semiconductor chip 110 is electrically connected to the two electrodes through two wires via the first recess 125 and the second recess 124, respectively. Alternatively, in certain embodiments, different chip mounting structures may be adopted for the electrical connections between the semiconductor chip 110 and the two electrodes. For example, the semiconductor chip 110 may be mounted as a vertical chip, where no wire is needed for electrically connected to the one of the electrode. In this case, only two recesses (i.e., one chip-attaching area and

one wire-bonding area) may be required, and only one wire is required for electrically connecting the semiconductor chip 110 (i.e., the vertical chip) to the other electrode via the one wire-bonding area.

[89] In certain embodiments, the lead frame 111 can be formed by punching or etching a metal plate. In certain embodiments, in order to improve productivity of the semiconductor packages, the lead frame 111 can be made in an array. For example, FIG. 3A is a schematic top view of a lead frame array before the semiconductor packages are made and diced according to one embodiment of the disclosure. As shown in FIG. 3A, the lead frame array is made of a metal plate 111f, which includes an array of multiple lead frames 111 (for example, a lead frame 111 is shown in FIG. 3A by a dotted rectangle). The lead frame array includes multiple slots 111sp and 111sl thereon. The slots 111sp and 111sl are used to divide the multiple lead frames 111, and form the electrode separating gap between the two electrodes of each lead frame 111. Each of the slots 111sp, which is a vertically elongated slot, can separate a column of the lead frames 111 from each package, and enable less cutting for dicing the lead frame packages. Each of the slots 111sl, which include a vertically elongated slot and multiple horizontal slots, can enable electrically separation for the lead frames 111 in each column, and forms the electrode separating gap between the two electrodes. In other words, the slots 111sp and the horizontal slots of the slots 111sl forms the package gaps between the lead frames 111, which may enable less cutting of the lead frames 111 in the dicing or singulating process; and the vertical slot of the slots 111sl forms the electrode separating gap between the two electrodes of each lead frame 111, so that the electrically-separating region 121b of the insulating package 120 may be filled in the electrode separating gap to separate the two electrodes. FIG. 3B shows a different example of the lead frame array, where the shape of each of the slots 111sp is different. Specifically, each the slots 111sp as shown in FIG. 3B includes multiple vertically sectioned slots, instead of a single vertically elongated slot as shown in FIG. 3A.

[90] Once the lead frame array is provided, the lead frame array may be used to prepare a semiconductor package array. FIGS. 4A-4D shows different examples of the semiconductor package arrays according to certain embodiments of the disclosure. Specifically, the semiconductor package array may be made from the lead frame array as shown in either one of FIGS. 3A and 3B. Specifically, for each of the lead frame 111 on the lead frame array 111f, the insulating package 120 and the reflective coating layer 122 are formed thereon to form the package body 101. As shown in FIG. 4A, the insulating packages 120 and the reflective coating layers 122 of the package bodies 101 in the array are formed integrally, such that the insulating packages 120 of the adjacent package bodies are continuously connected with each other. In comparison, as

shown in FIG. 4B, the resin bodies 120 of the package bodies in the array can be connected in one direction (i.e., the vertical direction) and separated in another orthogonal direction (i.e., the horizontal direction) by slots 190a. In this case, the package bodies may be diced by cutting in only one direction along the horizontal lines 180 to reduce cutting time and dirt. FIG. 4C shows another embodiment, where the package bodies may be further divided by additional slots 390A and 390B to reduce the volume to be cut and thus to reduce dirt produced. FIG. 4D shows a further embodiment, which is slightly different from the embodiment as shown in FIG. 4C in that each of the slots 390A are sectioned slots instead of an elongated slot.

[91] A further aspect of the present disclosure relates to a method for forming a package body as described above. Specifically, as discussed above, the package body may be formed in an array. FIG. 5 is a flowchart of a method of forming the package body according to one embodiment of the disclosure. In certain embodiments, the method as shown in FIG. 5 may be used to form a package body according to certain embodiments of the disclosure, such as the package body 101 as shown in FIGS. 2A and 2B. It should be particularly noted that, unless otherwise stated in the present disclosure, the steps of the method or process may be arranged in a different sequential order, and are thus not limited to the sequential order as shown in FIG. 5. Further, the method may include additional steps not shown in the flowchart of FIG. 5.

[92] As shown in FIG. 5, at procedure 510, a lead frame array is provided. Specifically, the lead frame array may be made of a metal sheet. At procedure 520, the lead frame array (i.e., the metal sheet) may be punched or etched to form a plurality of electrode separating gaps and a plurality of package gaps thereon. Specifically, an example of the lead frame array is shown in either FIG. 3A or FIG. 3B, where the slots 111sp and the horizontal slots of the slots 111sl forms the package gaps between the lead frames 111, which may enable less cutting of the lead frames 111 in the dicing or singulating process; and the vertical slot of the slots 111sl forms the electrode separating gap between the two electrodes of each lead frame 111. Optionally, at procedure 530, a coating may be formed on the lead frame array to cover at least the exposed areas (i.e., the openings) of the lead frame. In certain embodiments, the coating may be formed to cover the entire surfaces of the lead frame. At procedure 540, the insulating package and the reflective coating layer are formed on the lead frame array by transfer molding, compressing molding or injection molding to form a semiconductor package array. Specifically, an example of the semiconductor package array is shown in either one of FIGS. 4A-4D. In certain embodiments, additional steps may be performed on the semiconductor package array to make semiconductor packages. The additional steps may include, without being limited thereto, die attaching, wire bonding, and encapsulation, Once the semiconductor package array is ready for cutting, at procedure 550, the

package body can be diced or singulated from the package array along the package gaps. In this case, the package body may include a part of one of the electrode separating gaps, which separates the first electrode and the second electrode of the lead frame of package body.

[93] In the embodiments as described above, the lead frame package is used as the example of the package body of the semiconductor package. However, similar to the lead frame package, the disclosure can also be used in a chip-on-board (COB) package to replace silver coating and to improve the reliability as well the performance of a COB package. FIG. 6 is a schematic cross-sectional view of a COB package structure according to one embodiment of the disclosure. As shown in FIG. 6, the COB package 200 has a similar structure to that of the package body 101 of the semiconductor package 100. Specifically, the COB package 200 includes a package body 201, which functions as a COB housing/body, a semiconductor chip 210 attached in the package body 201, and an optical encapsulating resin layer 250 encapsulating and protecting the semiconductor chip 210. The package body 201 is formed on a substrate 230. Similar to the package body of the semiconductor package 100 as shown in FIGS. 2A and 2B, the package body 201 includes a metal lead 211, an insulating package 220, and a reflective coating layer 222. The semiconductor chip 210 can be any semiconductor chip. The metal lead 211 is bonded on top of the substrate 230 and electrically insulated from the substrate 230. The metal lead 211 includes two electrodes (namely a first electrode and a second electrode) separated and insulated from each other, for providing electrical contacts for the semiconductor chip 210 via the gold wires. The insulating package 220 can be formed on top of the substrate 230 and have a package cavity 240 where the encapsulating material 250 of the COB package 200 is filled. The reflective coating layer 222 is formed on the metal lead 211, and has openings 223, 224, and 225 for semiconductor chip bonding area and wire bonding areas. Specifically, the openings include a chip recess 223, a first recess 225 and a second recess 224. In certain embodiments, the insulating package 220 can be mechanically bond to the substrate 230 through plurality of holes where the resin regions 221b are formed in to prevent detaching of the insulating package 220 from the substrate 230. In certain embodiments, when the COB package 200 includes multiple semiconductor chips 210, the reflective coating layer 222 can have multiple chip recesses 223 to enable the COB semiconductor package 200 with the multiple semiconductor chips 210.

[94] In certain embodiments, the insulating package 220 and the reflective coating layer 222 can be formed in a one-step formation, in which the reflective coating layer 222 is formed together with the electrical-separating region between the two electrodes of the metal lead 211 and the main portion 221a of the insulating package 220. In this case,

the insulating package 220 and the reflective coating layer 222 may be made of the same material. For example, the insulating package 220 and the reflective coating layer 222 may be made of the same binder-filler composite. Alternatively, in certain embodiments, the reflective coating layer 222 can be formed separately from other regions of the insulating package 220. For example, the reflective coating layer 222 may be formed by coating on top of the metal lead 211 before the insulating package 220 is formed. In this case, the reflective coating layer 222 and the insulating package 220 can be made of the same material, or can be made of different materials. For example, the reflective coating layer 222 can be made of a binder filler composite different from the binder-filler composite forming the insulating package 220.

[95] In certain embodiments, the disclosure can also be applied to other lighting structures or applications, such that the metal coating in the lighting structure can be replaced by the binder-filler composite coating. For example, a lamp using diffuse reflectors to reflect light may utilize the binder-filler composite coating structure. Other applications may include, without being limited thereto, remote phosphor applications where the light output of the device greatly depends on the reflectivity of the reflectors.

[96] In certain embodiments, the package body according to certain embodiments of the disclosure may be used in an encapsulant-free semiconductor package, which does not require the encapsulating resin layer to be filled in the package cavity of the package body. For example, FIGS. 7A-7F show multiple encapsulant-free semiconductor package structures according to certain embodiments of the disclosure.

[97] As shown in FIG. 7A, the encapsulant-free semiconductor package includes a semiconductor chip 310, which is bonded to a pair of electrodes 311a and 311b of a lead frame. Further, an insulating package is formed to include multiple regions 321a and 321b. Specifically, the lateral region 321 forms the main support of the package body, and the bottom region 321b forms between the two electrodes 311a and 311b of the lead frame to electrically insulates the two electrodes 311a and 311b from each other. The semiconductor chip 310 is located directly above the bottom region 321b of the insulating package. It should be noted that there is no encapsulating resin layer as shown in FIG. 7A, leaving the semiconductor chip 310 unprotected.

[98] FIG. 7B shows an encapsulant-free semiconductor package which is very similar to that as shown in FIG. 7A, with the only difference being that the semiconductor chip 310 as shown in FIG. 7B is protected with a thin encapsulating layer 330. The thin encapsulating layer 330 is a thin layer, which does not fill the package cavity. The thin layer can be made of an optical transparent material such as silicones or polymers. In certain embodiments, the thin layer can contain white pigments that are made of at least one selected from the group consisting of TiO2, SiO2, Al2O3, BN, MgO, CaO, ZrO2, ZnO, BaO, AlN, Sb2O3, and BaSO4. In certain embodiments, the thin layer can

contain wavelength conversion materials such as phosphor materials and/or quantum dot materials.

[99] As shown in FIG. 7C, the encapsulant-free semiconductor package includes a semiconductor chip 410, which is bonded to a pair of electrodes 411a and 411b of a lead frame. Further, an insulating package is formed to include multiple regions 421a and 421b. Specifically, the lateral region 421 forms the main support of the package body, and the bottom region 421b forms between the two electrodes 411a and 411b of the lead frame to electrically insulates the two electrodes 411a and 411b from each other. The semiconductor chip 410 is located directly above the bottom region 421b of the insulating package. Moreover, a reflective coating layer 440 is formed on the electrodes 411a and 411b of the lead frame It should be noted that there is no encapsulating resin layer as shown in FIG. 7C, leaving the semiconductor chip 410 unprotected.

[100] FIG. 7D shows an encapsulant-free semiconductor package which is very similar to that as shown in FIG. 7C, with the only difference being that the semiconductor chip 410 as shown in FIG. 7D is protected with a thin encapsulating layer 430. The thin encapsulating layer 430 is a thin layer, which does not fill the package cavity. The thin layer can be similar to the thin encapsulating layer 330 as shown in FIG. 7B.

[101] As shown in FIGS. 7C and 7D, the semiconductor chip 410 is attached to the electrodes 411a and 411b via a single recess. In certain embodiments, the encapsulant-free semiconductor package may include multiple recesses, such that multiple semiconductor chips may be provided and respectively attached to the electrodes via the multiple recesses.

[102] FIG. 7E shows an encapsulant-free semiconductor package using a COB package structure. As shown in FIG. 7E, the encapsulant-free semiconductor package includes a semiconductor flip-chip 510, which is bonded to a pair of electrodes 511a and 511b of a lead frame. The lead frame (i.e., the electrodes 511a and 511b) is formed on a substrate 560. Further, the semiconductor flip-chip 510 is protected with a thin encapsulating layer 530. The thin encapsulating layer 530 is a thin layer, which can be similar to the thin encapsulating layer 330 as shown in FIG. 7B. In certain embodiments, the semiconductor flip-chip 510 can be a LED flip-chip or a LD flip-chip, which is configured to emit a blue light, a green light, a red light or a white light.

[103] FIG. 7F shows an encapsulant-free semiconductor package, which has a lead frame package structure that is similar to the structure as shown in FIG. 2B. Specifically, the semiconductor chip 110 as shown in FIG. 7F is a wire-bonding chip, which is the same as that as shown in FIG. 2B. The structure as shown in FIG. 7F is different from the structure as shown in FIG. 2B in that a thin encapsulating layer 630 is provided to replaces for the encapsulant resin layer 150 as shown in FIG. 2B. In other words, the encapsulant resin layer 150 and the fillers 160 of the package 100 as shown in FIG. 2B

are removed and replaced by the thin encapsulating layer 630 to form the encapsulant-free semiconductor package as shown in FIG. 7F. The thin encapsulating layer 630 is a thin layer, which does not fill the package cavity, and can be similar to the thin encapsulating layer 330 as shown in FIG. 7B. In certain embodiments, the structure as shown in FIG. 7F may be used as a semiconductor emitter.

[104] In certain embodiments, by removing the encapsulant resin layer 150 that is filled within the package cavity as shown in FIG. 2B, thermal dissipation of a semiconductor package could be improved. Junction temperature and light output of an encapsulant-free semiconductor package are found to be improved (lower junction temperature and higher light output) compared to an encapsulated semiconductor package. Moreover, the encapsulant-free semiconductor package also reduces processing steps and thus enables low cost.

[105] In certain embodiments, the thin encapsulating layers 330, 430, 530 and 630 may be made of a light conversion material to partially convert the light emitted by the semiconductor flip-chip to a different color. Using the COB structure as shown in FIG. 7E as an example, the semiconductor flip-chip 510 may emit light in a first color, and the thin encapsulating layer 530 may convert the light to a different second color.

[106] For mass production, the lead frame package for the encapsulant-free semiconductor package can be made in an array, such as the array as shown in FIG. 3A or FIG. 3B. Mass production schemes as shown in FIGS. 4A-4D can be used for any one of the encapsulant-free semiconductor packages as shown in FIGS. 7A-7F. FIG. 8 is an example of the lead frame package array of mass production for encapsulant-free semiconductor package shown in FIGS. 7C-D. For example, FIG. 8 is a schematic view of a semiconductor package array for the encapsulant-free semiconductor packages according to one embodiment of the disclosure. Specifically, the semiconductor package array as shown in FIG. 8 is similar to the semiconductor package array as shown in FIG. 4D, with the difference being that the semiconductor packages as shown in FIG. 8 are encapsulant-free semiconductor packages.

[107] In certain embodiments, the semiconductor chip as used in certain embodiments of the disclosure can be any of semiconductor chips that emit or receive light, such as light emitting diodes, laser diodes, vertical-cavity-surface-emitting lasers, optical sensors/detectors, or other suitable chips.

[108] The foregoing description of the exemplary embodiments of the disclosure has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

[109] The embodiments are chosen and described in order to explain the principles of the disclosure and their practical application so as to activate others skilled in the art to

utilize the disclosure and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present disclosure pertains without departing from its spirit and scope. Accordingly, the scope of the present disclosure is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

Claims

[Claim 1] A package body for a semiconductor device, comprising:
a lead frame having a first electrode and a second electrode separated from each other;
an insulating package providing a housing structure and forming a package cavity therein, wherein the package cavity has a reflective side surface formed by the insulating package; and
a reflective coating layer partially covering the first electrode and the second electrode and forming a reflective bottom surface of the package cavity.

[Claim 2] The package body according to claim 1, being an all diffusive integrated reflecting surfaces (AR-IRS) package body.

[Claim 3] The package body according to claim 1, wherein the first electrode and the second electrode are separated by the insulating package.

[Claim 4] The package body according to claim 1, wherein each of the first electrode and the second electrode has an angled cut such that a bottom surface area of the first electrode is smaller than a top surface area of the first electrode, and a bottom surface area of the second electrode is smaller than a top surface area of the second electrode.

[Claim 5] The package body according to claim 1, wherein each of the first electrode and the second electrode has a vertical cut.

[Claim 6] The package body according to claim 1, wherein at least one semiconductor chip is configured to be attached to the first electrode and electrically connected to the first electrode and the second electrode respectively.

[Claim 7] The package body according to claim 6, wherein the reflective coating layer has a first recess, a second recess and at least one chip recess formed thereon, wherein:
a portion of the lead frame is exposed through each of the at least one chip recess to provide a chip-attaching area, such that the at least one semiconductor chip is attached to the lead frame via the at least one chip recess;
a portion of the first electrode is exposed through the first recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the first electrode through a first wire via the first recess; and
a portion of the second electrode is exposed through the second recess

to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the second electrode through a second wire via the second recess.

[Claim 8] The package body according to claim 6, wherein the at least one semiconductor chip comprises a light emitting diode (LED) chip or a laser diode (LD) chip.

[Claim 9] The package body according to claim 1, wherein the insulating package is made of a binder-filler composite containing white pigments.

[Claim 10] The package body according to claim 9, wherein the binder-filler composite is polycyclohexylenedimethylene terephthalate (PCT), polyphthalamide (PPA), a silicone resin, a silicone molding resin, an epoxy molding resin, an acrylate resin, an urethane resin, or a copolymer system thereof, and the white pigments are made of at least one pigment selected from the group consisting of TiO_2, SiO_2, Al_2O_3, BN, MgO, CaO, ZrO_2, ZnO, BaO, AlN, Sb_2O_3, and $BaSO_4$.

[Claim 11] The package body according to claim 10, wherein the white pigments are amorphous, partially crystalline, crystalline or a mixture thereof in any ratio, and the white pigments have a weight ratio from 1 to 95 percent of the binder-filler composite forming the insulating package.

[Claim 12] The package body according to claim 10, wherein each of the white pigments has a size from 10 nm to 10 microns.

[Claim 13] The package body according to claim 9, wherein the reflective coating layer is made of the same binder-filler composite forming the insulating package.

[Claim 14] The package body according to claim 9, wherein the reflective coating layer is made of a binder filler composite different from the binder-filler composite forming the insulating package.

[Claim 15] An encapsulant-free semiconductor package, comprising:
a semiconductor flip-chip; and
a package body according to claim 1, wherein the reflective coating layer has at least one recess formed thereon, and a portion of the first electrode and a portion of the second electrode of the lead frame are exposed through the at least one recess to provide a bonding pad area, such that the semiconductor flip-chip is attached to the first electrode and the second electrode via the at least one recess.

[Claim 16] The encapsulant-free semiconductor package according to claim 15, wherein the semiconductor flip-chip is a light emitting diode (LED) flip-chip or a laser diode (LD) flip-chip.

[Claim 17] The encapsulant-free semiconductor package according to claim 16, wherein the LED flip-chip or the LD flip-chip is configured to emit a blue light, a green light, a red light or a white light.

[Claim 18] The encapsulant-free semiconductor package according to claim 15, wherein the semiconductor flip-chip is coated with a thin coating of a transparent material.

[Claim 19] The encapsulant-free semiconductor package according to claim 18, wherein the semiconductor flip-chip is configured to emit light in a first color, and the transparent material comprises a light conversion material to partially convert the light emitted by the semiconductor flip-chip to a second color different from the first color.

[Claim 20] A method for forming a package body according to claim 1, comprising:
providing a lead frame array;
punching or etching the lead frame array to form a plurality of electrode separating gaps and a plurality of package gaps;
forming the insulating package and the reflective coating layer on the lead frame array to form a semiconductor package array; and
dicing or singulating the package body from the package array along the package gaps,
wherein one of the electrode separating gaps separates the first electrode and the second electrode of the lead frame of the package body.

[Claim 21] The method according to claim 20, further comprising:
forming a coating on the lead frame array to cover at least exposed areas of the lead frame of the package body.

[Claim 22] The method according to claim 20, wherein the insulating package and the reflective coating layer are formed by transfer molding, compressing molding or injection molding.

[Claim 23] A light emitting diode (LED) device, comprising:
the package body according to claim 1; and
a LED chip attached to the package body.

[Claim 24] A package body for a semiconductor device, comprising:
a substrate;
a first electrode and a second electrode formed on the substrate and separated from each other;
an insulating package providing a housing structure and forming a package cavity therein, wherein the package cavity has a reflective side

surface formed by the insulating package; and
a reflective coating layer forming a reflective bottom surface of the package cavity and partially covering the first electrode and the second electrode.

[Claim 25] The package body according to claim 24, wherein the first electrode and the second electrode are formed by a lead frame.

[Claim 26] The package body according to claim 24, wherein a semiconductor flip-chip is configured to be attached to the first electrode and the second electrode respectively.

[Claim 27] The package body according to claim 26, wherein the reflective coating layer has at least one recess formed thereon, and a portion of the first electrode and a portion of the second electrode of the lead frame are exposed through the at least one recess to provide a bonding pad area, such that the semiconductor flip-chip is attached to the first electrode and the second electrode via the at least one recess.

[Claim 28] The package body according to claim 24, wherein at least one semiconductor chip is configured to be attached to the first electrode and electrically connected to the first electrode and the second electrode respectively.

[Claim 29] The package body according to claim 28, wherein the reflective coating layer has a first recess, a second recess and at least one chip recess formed thereon, wherein:
a portion of the lead frame is exposed through each of the at least one chip recess to provide a chip-attaching area, such that the at least one semiconductor chip is attached to the lead frame via the at least one chip recess;
a portion of the first electrode is exposed through the first recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the first electrode through a first wire via the first recess; and
a portion of the second electrode is exposed through the second recess to provide a wire-bonding area, such that each of the at least one semiconductor chip is electrically connected to the second electrode through a second wire via the second recess.

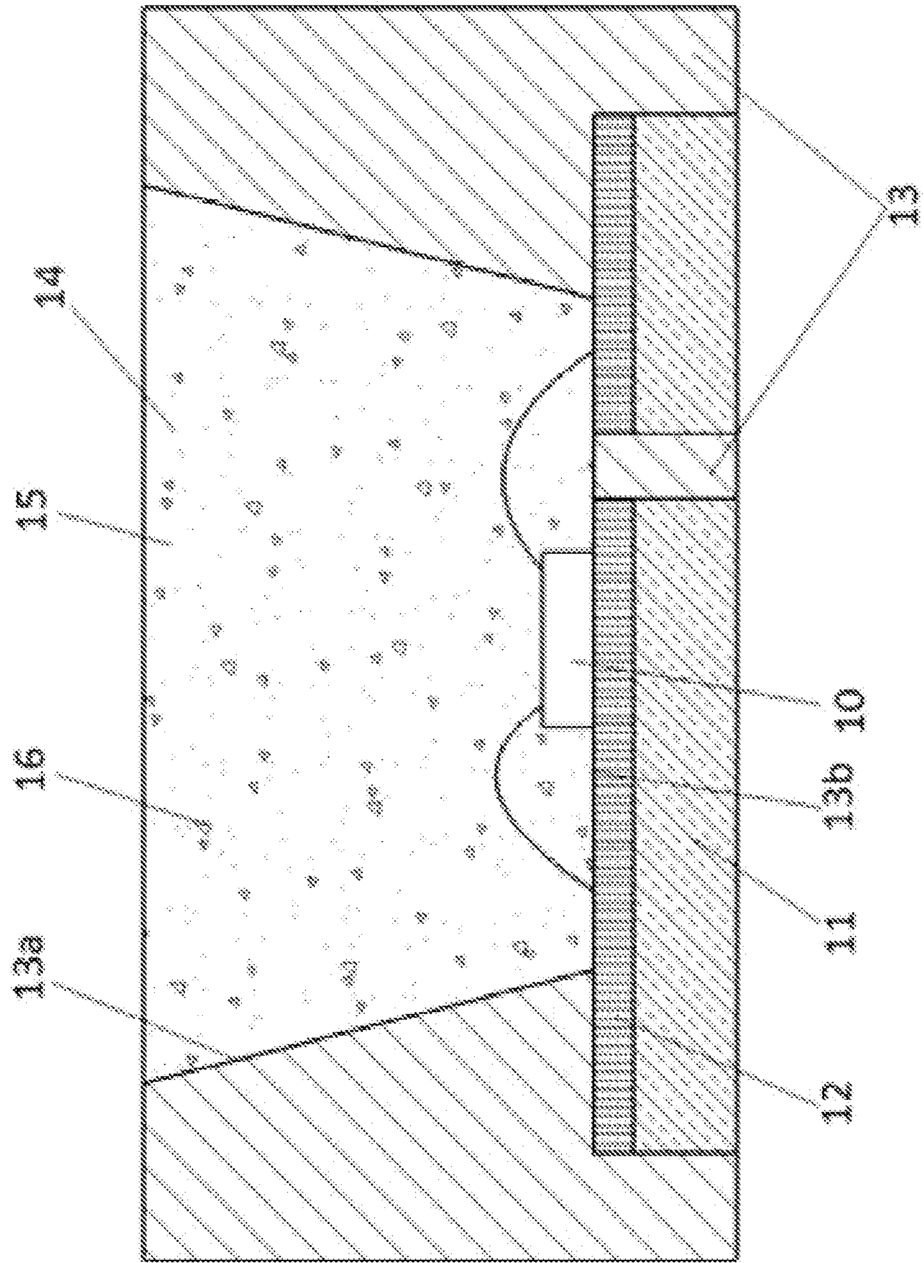


FIG. 1

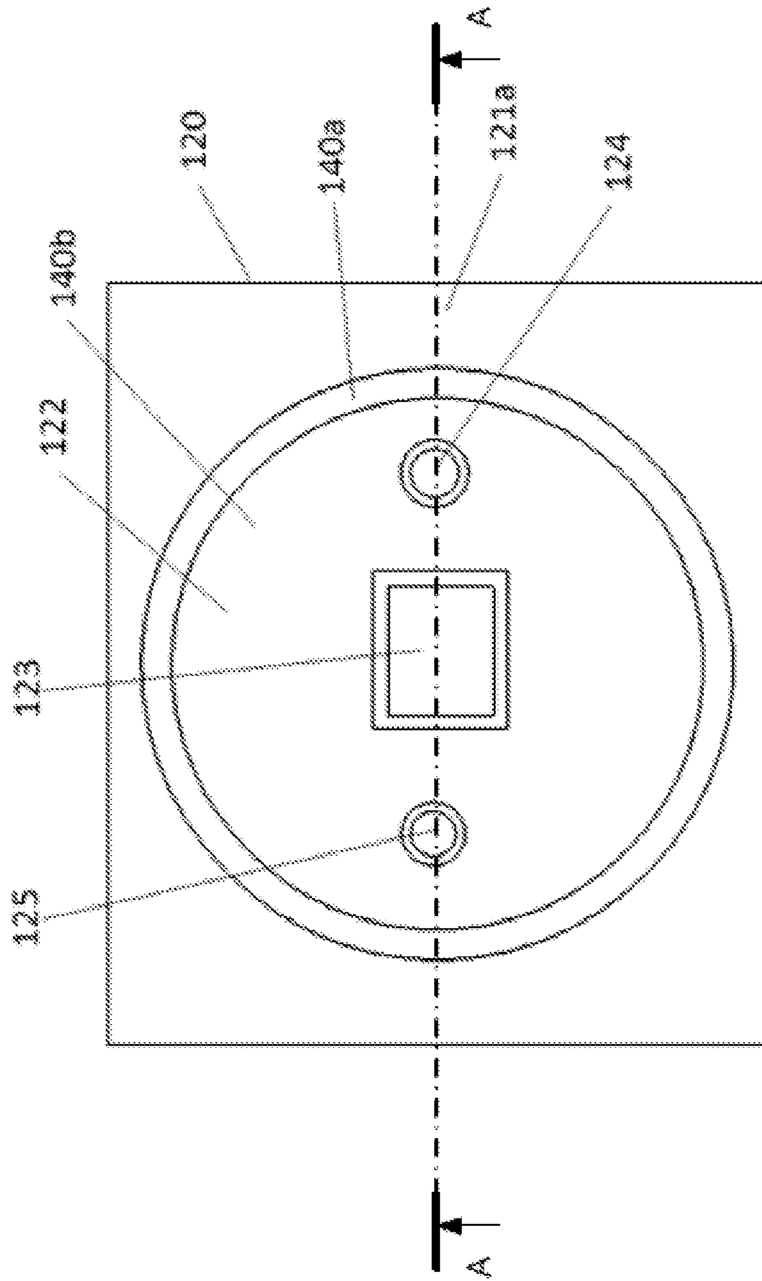


FIG. 2A

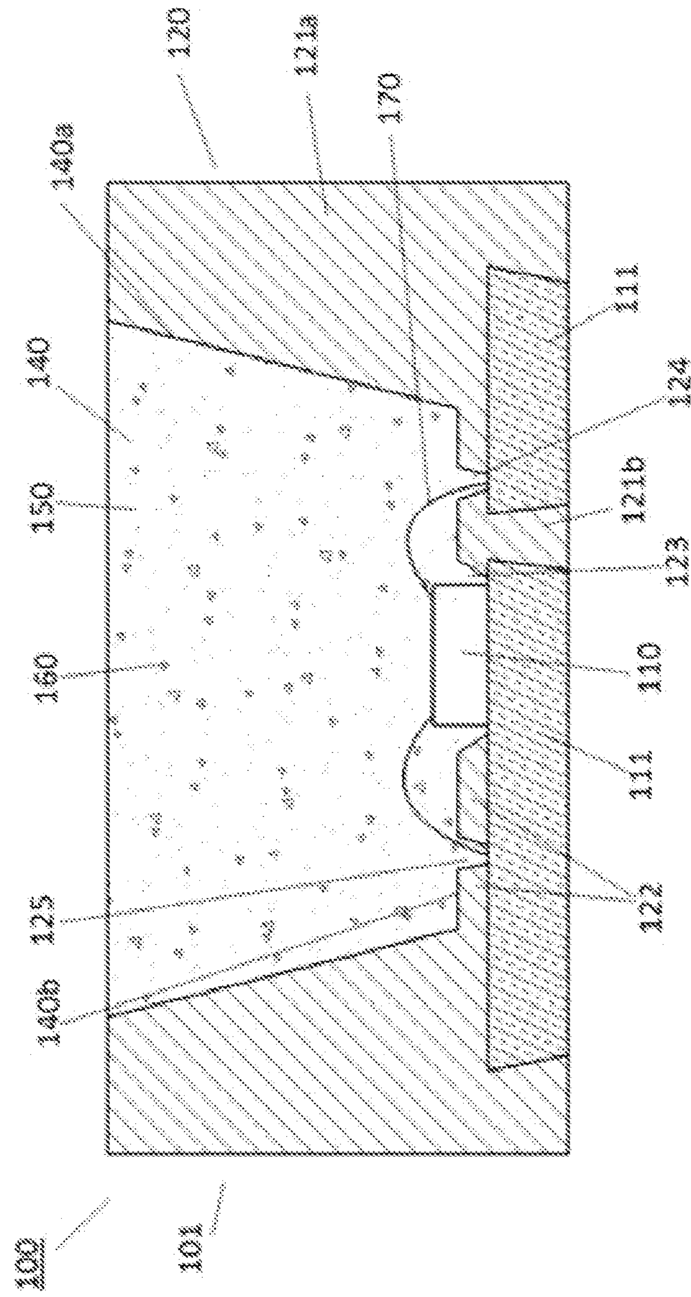


FIG. 2B

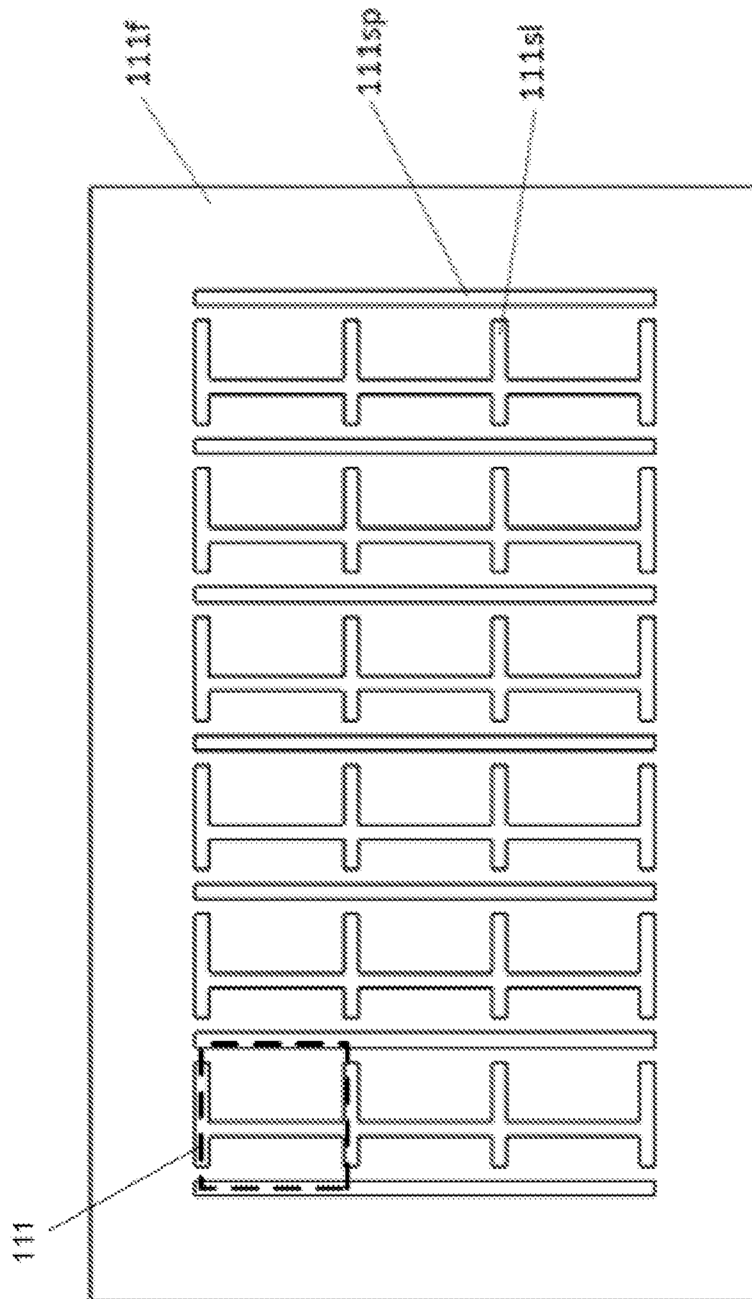


FIG. 3A

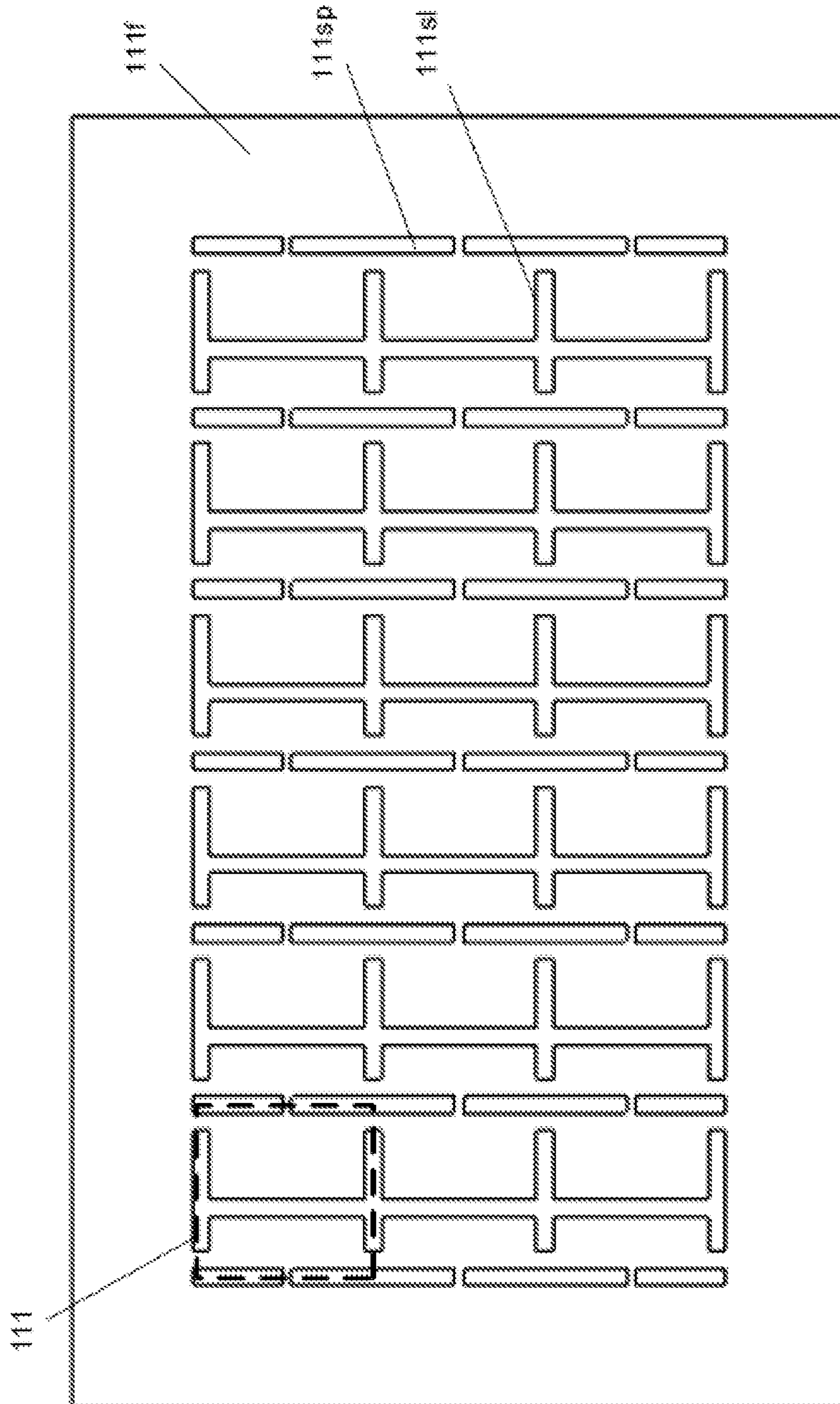


FIG. 3B

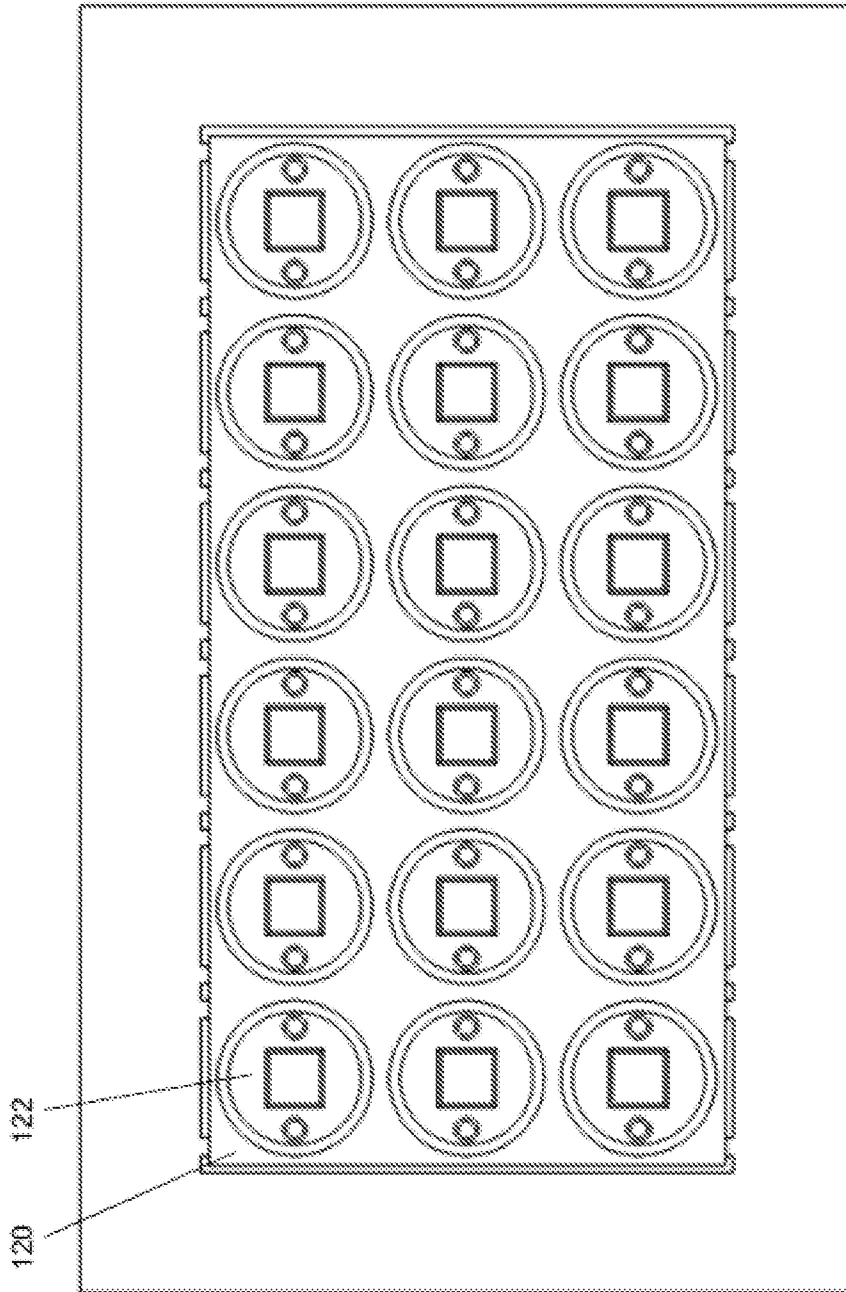


FIG. 4A

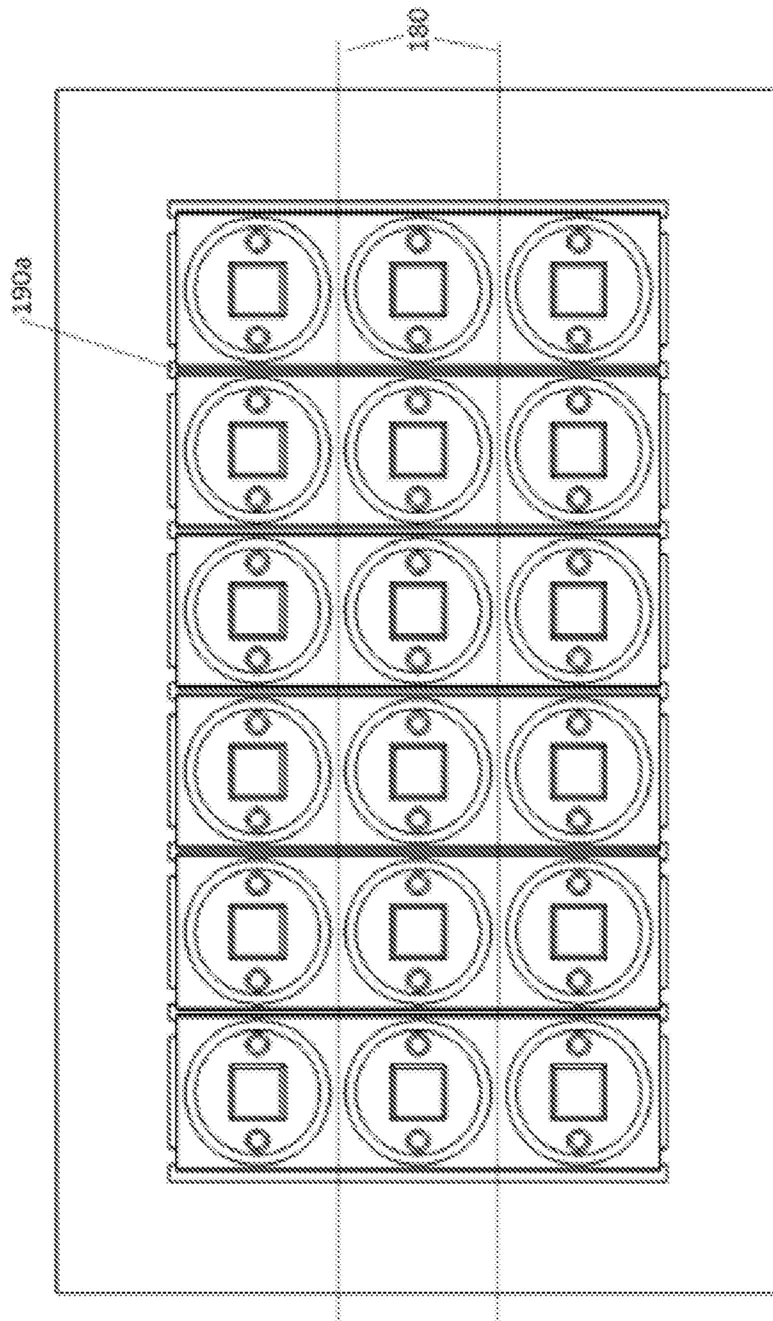


FIG. 4B

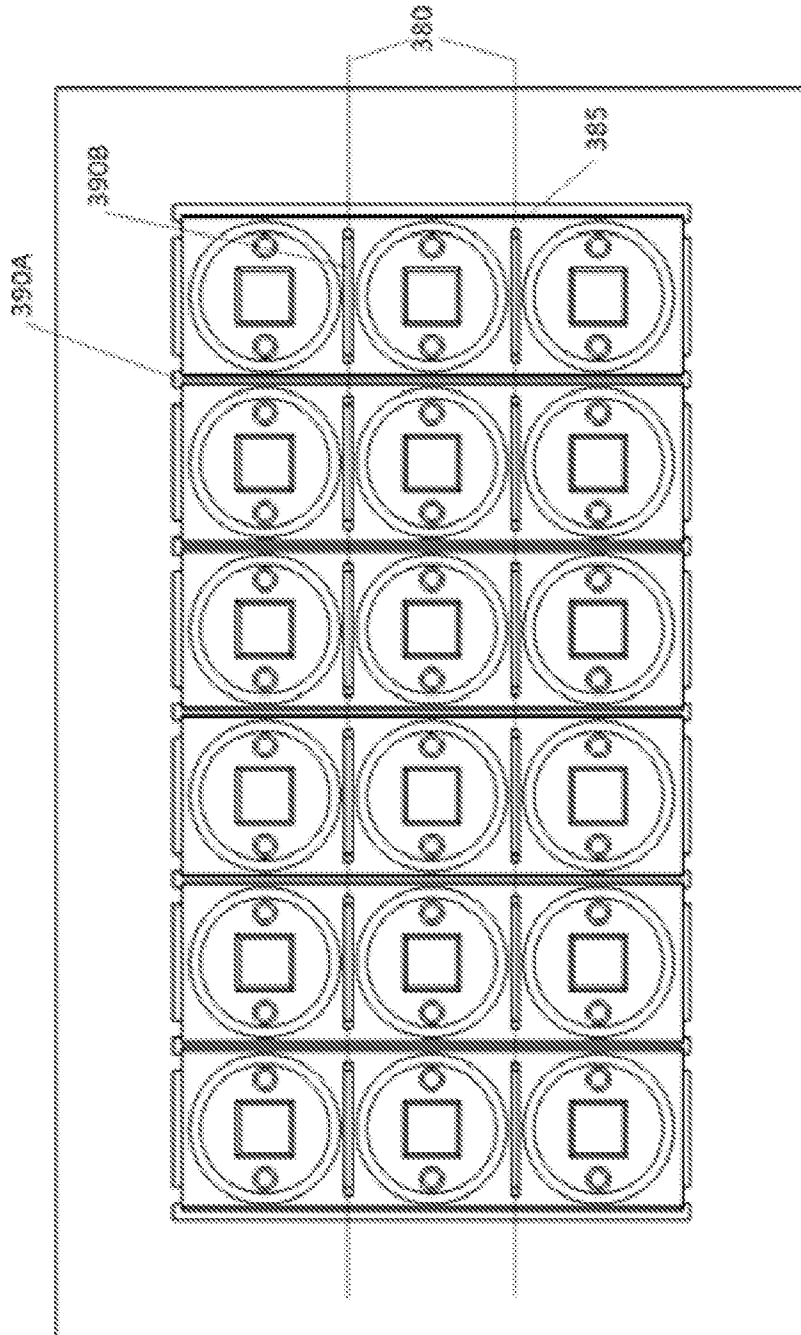


FIG. 4C

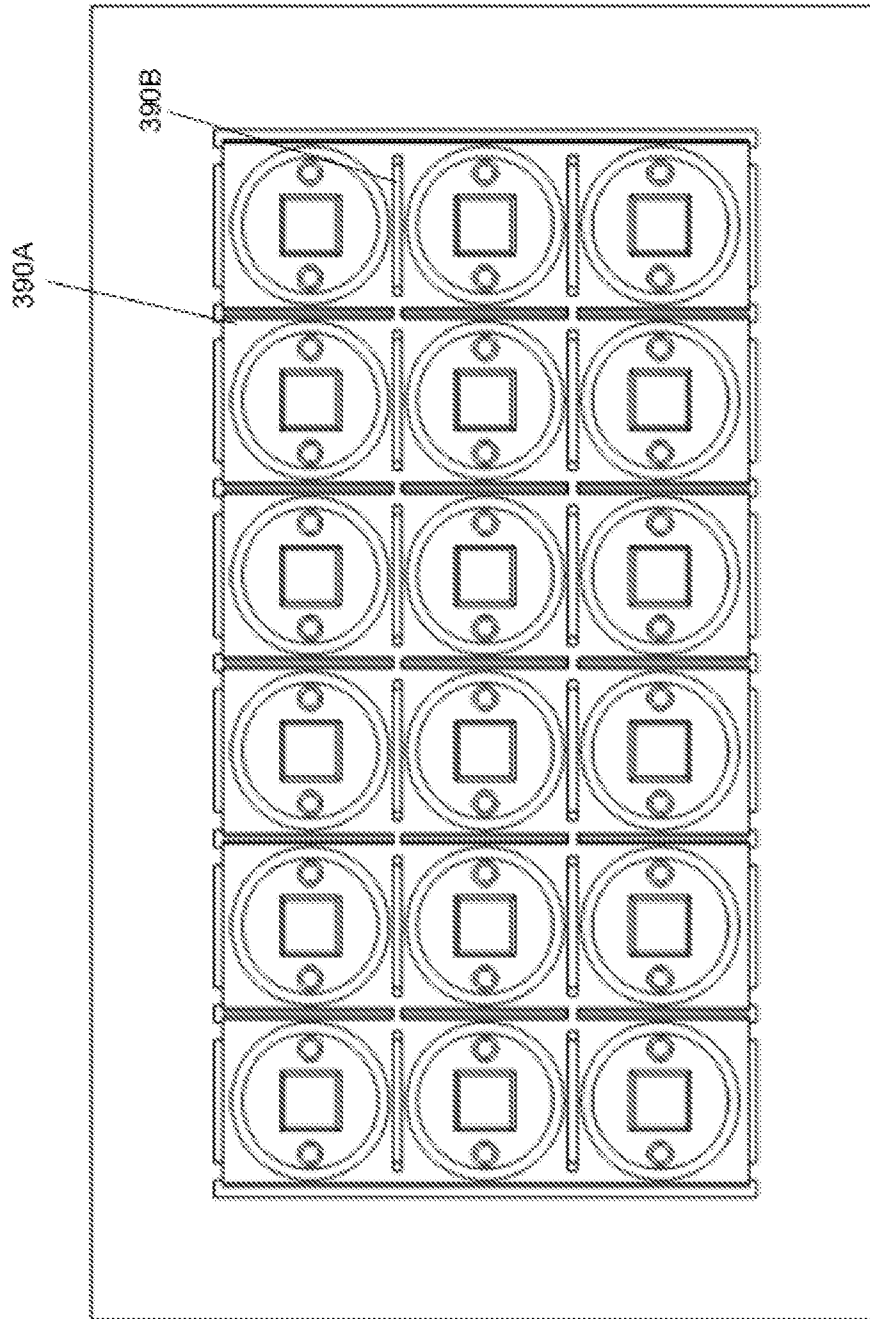


FIG. 4D

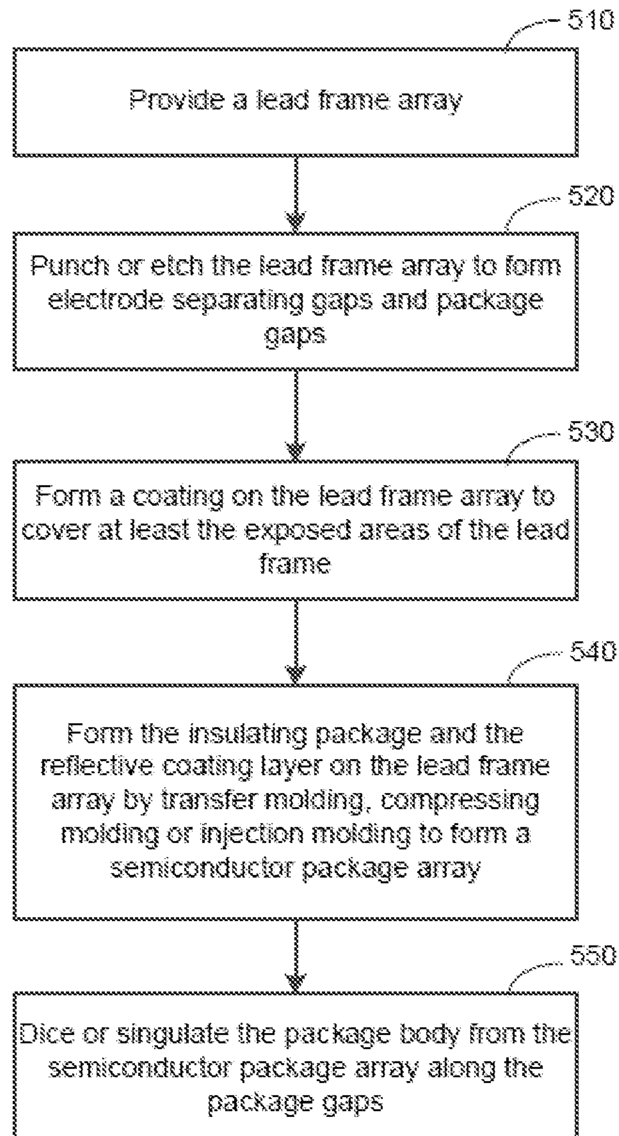


FIG. 5

200

201

220

221a

221b

240

224

222

223

211

210

250

222

225

230

FIG. 6

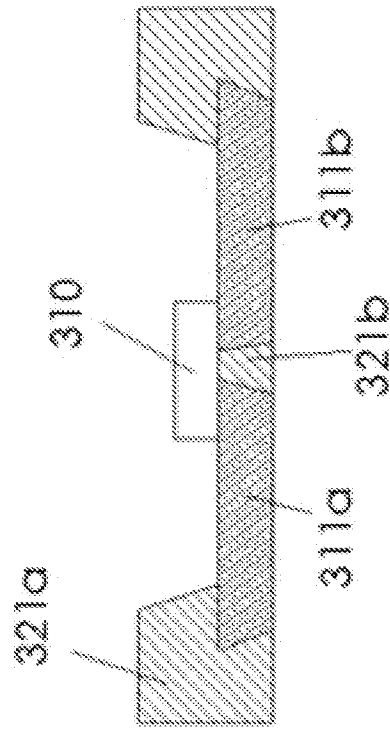


FIG. 7A

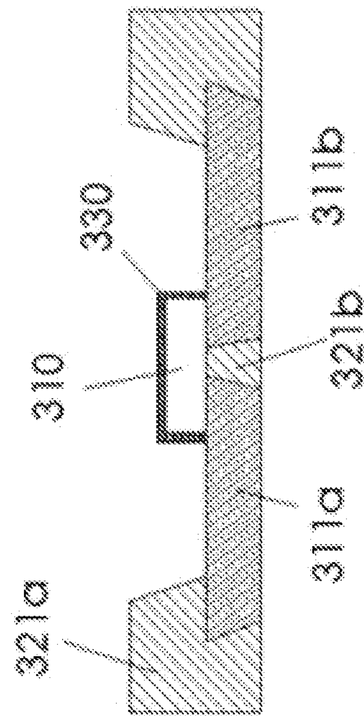


FIG. 7B

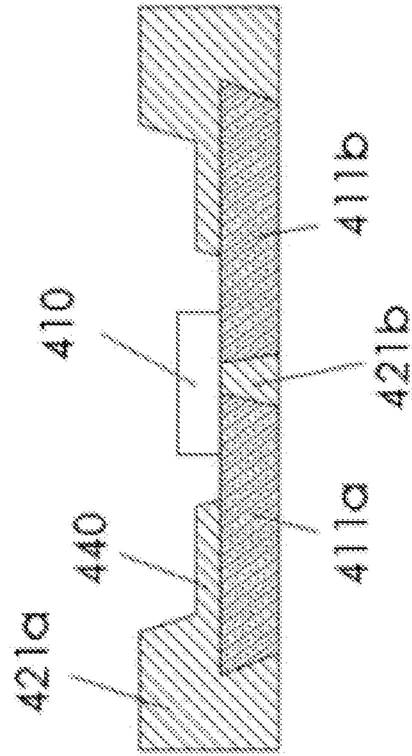


FIG. 7C

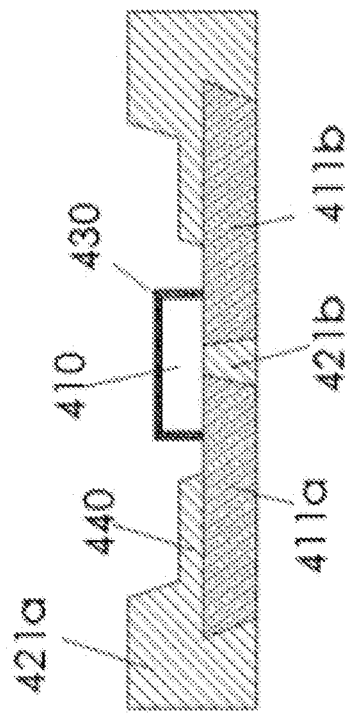


FIG. 7D

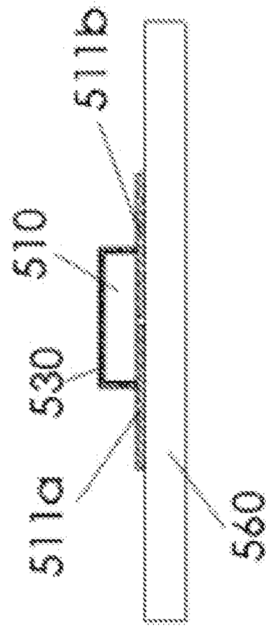


FIG. 7E

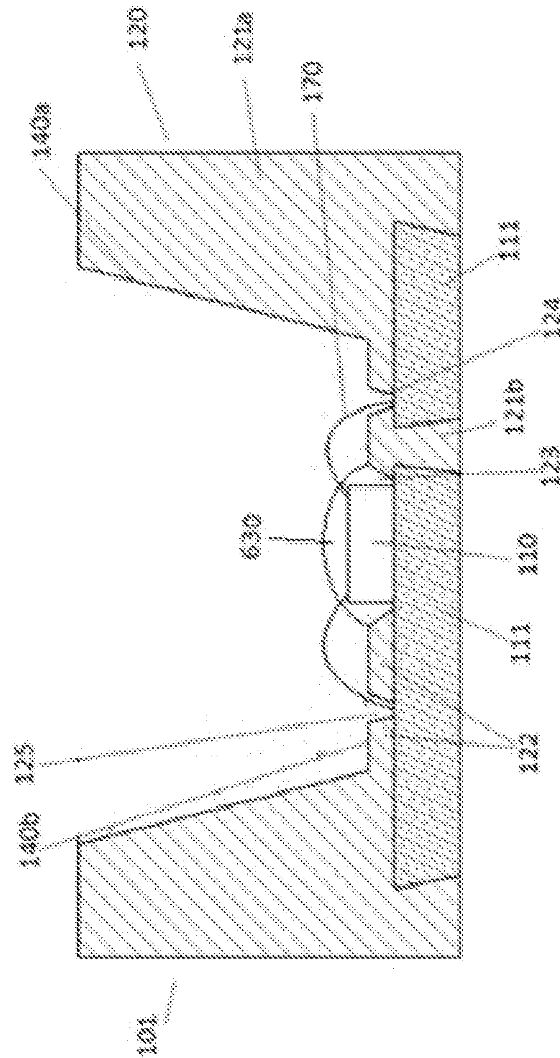


FIG. 7F

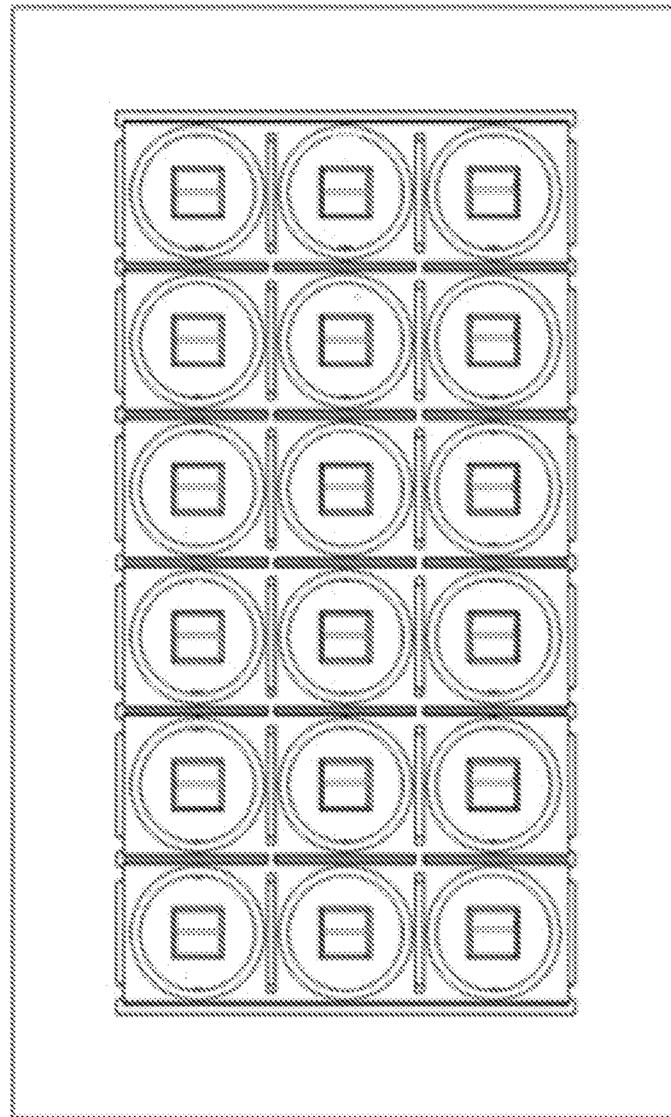


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/072486

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/54(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI;CNABS;CNTXT;VEN: package, insulat???, reflect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 105702841 A (JIUZUNCHENG NETWORK TECH SHENZHEN CO LTD) 22 June 2016 (2016-06-22) description paragraphs 0049-0067 and figures 1-7	1-29
Y	CN 104247057 A (LG INNOTEK CO LTD) 24 December 2014 (2014-12-24) description paragraphs 0024-0069 and figures 1-2	1-29
Y	JP 2011249768 A (MITSUBISHI CHEM CORP) 08 December 2011 (2011-12-08) figure 3 and relative description	1-29
A	CN 102299132 A (MATSUSHITA ELECTRIC IND CO LTD) 28 December 2011 (2011-12-28) description paragraphs 0043-0054 and figures 1A-2D	1-29
A	CN 101382242 A (TOSHIBA LIGHTING & TECHNOLOGY) 11 March 2009 (2009-03-11) figure 1 and relative description	1-29
A	CN 102089576 A (OSRAM GMBH) 08 June 2011 (2011-06-08) description paragraph 0009	1-29
A	CN 102460746 A (SHARP KK) 16 May 2012 (2012-05-16) description paragraph 0085 and figure 2	1-29

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 April 2019	**28 April 2019**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**DUAN,Keyu**
Facsimile No. **(86-10)62019451**	Telephone No. **86-010-62089909**

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9310062 B2 (TOYODA GOSEI KK) 12 April 2016 (2016-04-12) the whole document	1-29
A	US 2010295082 A1 (SAMSUNG ELECTRO MECH) 25 November 2010 (2010-11-25) the whole document	1-29

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	105702841	A	22 June 2016	CN	105702841	B	19 June 2018
CN	104247057	A	24 December 2014	US	9293672	B2	22 March 2016
				EP	2820685	A1	07 January 2015
				WO	2013129820	A1	06 September 2013
				JP	6148261	B2	14 June 2017
				JP	2015513800	A	14 May 2015
				US	2015014731	A1	15 January 2015
				KR	20130098048	A	04 September 2013
				EP	2820685	A4	30 September 2015
				TW	201347240	A	16 November 2013
				TW	I606616	B	21 November 2017
JP	2011249768	A	08 December 2011		None		
CN	102299132	A	28 December 2011	CN	102299132	B	26 March 2014
				US	2012001311	A1	05 January 2012
				JP	2012028744	A	09 February 2012
CN	101382242	A	11 March 2009	US	2009067172	A1	12 March 2009
				EP	2034234	B1	07 December 2011
				CN	101382242	B	28 March 2012
				US	2010195329	A1	05 August 2010
				JP	4894688	B2	14 March 2012
				US	7722213	B2	25 May 2010
				US	8042973	B2	25 October 2011
				JP	2009064637	A	26 March 2009
				CN	101915386	A	15 December 2010
				EP	2034234	A1	11 March 2009
				US	8047687	B2	01 November 2011
				US	8079736	B2	20 December 2011
				US	2010195327	A1	05 August 2010
				US	2010195328	A1	05 August 2010
CN	102089576	A	08 June 2011	DE	102008031987	A1	15 April 2010
				US	2011090671	A1	21 April 2011
				EP	2307793	B1	31 August 2016
				CA	2726857	A1	14 January 2010
				EP	2307793	A1	13 April 2011
				WO	2010003626	A1	14 January 2010
				US	8480252	B2	09 July 2013
				KR	101182094	B1	19 September 2012
				KR	20110014217	A	10 February 2011
CN	102460746	A	16 May 2012	WO	2010146904	A1	23 December 2010
				US	2012081614	A1	05 April 2012
US	9310062	B2	12 April 2016	US	2014028173	A1	30 January 2014
				JP	2014041993	A	06 March 2014
US	2010295082	A1	25 November 2010	US	7888689	B2	15 February 2011
				US	7985975	B2	26 July 2011
				JP	2007311786	A	29 November 2007
				KR	100735432	B1	27 June 2007
				US	2007267637	A1	22 November 2007
				JP	5200301	B2	05 June 2013