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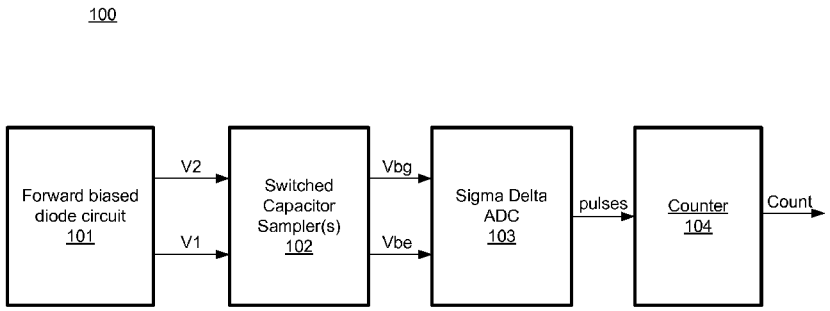


Fig. 1

(57) Abstract: Described is an apparatus of a thermal sensor and/or bandgap reference circuit which is independent of an operational amplifier. The apparatus comprises: a forward biased diode circuit having one or more diodes; a first switch-capacitor sampler coupled to the forward biased diode circuit, the first switch-capacitor sampler to provide a reference voltage which is proportional to absolute temperature; and a second switch-capacitor sampler coupled to the forward biased diode circuit.

DIGITAL SWITCH-CAPACITOR BASED BANDGAP REFERENCE AND THERMAL SENSOR

BACKGROUND

[0001] A bandgap reference generator is used to generate a constant bandgap reference voltage. This constant bandgap reference voltage may be temperature independent and can be used for different applications. For example, the constant bandgap reference voltage may be used in digital-to-analog converters (DACs), phase locked loops (PLLs), linear voltage regulators (VRs), DC-DC converters, RF (radio-frequency) circuits, thermal sensors, etc.

[0002] Bandgap reference generators are typically analog circuits that require certain voltage headroom for proper operation. Digital circuits, however, are being operated on lower power supplies every process generation to save power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0004] **Fig. 1** illustrates a high level architecture of a switch-capacitor based bandgap reference and thermal sensor, according to one embodiment of the disclosure.

[0005] **Fig. 2** is an open loop dual diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure.

[0006] **Fig. 3** is an open loop single diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure.

[0007] **Fig. 4** is an open loop single switch-capacitor single diode based digital thermal sensor, according to another embodiment of the disclosure.

[0008] **Fig. 5** is a closed loop switch-capacitor based bandgap reference generator, according to one embodiment of the disclosure.

[0009] **Fig. 6** is a processor with bandgap reference generator and digital thermal sensor, according to one embodiment of the disclosure.

[0010] **Fig. 7** is a circuit illustrating rotating switches in a forward biased diode circuit for dynamic matching in a single diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure.

[0011] **Fig. 8** is a smart device or a computer system or an SoC (system-on-chip) with the bandgap reference architecture, according to one embodiment of the disclosure.

DETAILED DESCRIPTION

[0012] The embodiments describe a digital switch-capacitor based bandgap reference and thermal sensor. In one embodiment, digital switch-capacitor based bandgap reference and thermal sensor comprises a sigma-delta based analog-to-digital converter (ADC) coupled to a one or more switch-capacitor based samplers and forward biased diode circuits. Typical ADCs, which may be used in thermal sensor circuits, require the use of a fixed voltage reference i.e., a reference independent of temperature and power supply level. An example of such voltage reference is a bandgap voltage reference. Bandgap reference generators to generate bandgap voltage reference use an additional regulator and unity gain buffer, which are both area and power consuming circuits, to provide the continuous time bandgap reference input. The embodiments use a switch-capacitor based bandgap reference instead of continuous time bandgap reference. In one embodiment, use of unity gain amplifier is eliminated by using inverter(s) based switching capacitors to generate switch-capacitor based bandgap reference.

[0013] One technical effect of using a switch-capacitor based bandgap reference instead of continuous time bandgap reference is that circuit area is reduced (e.g., by 70%) over traditional bandgap reference generators and thermal sensors. In one embodiment, a single diode is used to generate bandgap reference and thermal sensor. In such an embodiment, additional area is reduced. The embodiments discussed here can properly operate at low power supplies (e.g., 0.9V). In one embodiment, the switch-capacitor based bandgap reference and thermal sensor is independent of a startup circuit which is used for traditional bandgap circuits. The absence of the startup circuit further reduces area and power of the embodiments. The embodiments also provide a built-in offset cancellation apparatus without the need of separate offset cancellation circuits, which further reduces power consumption and area. The embodiments, being largely digital design, are scalable over process nodes. The embodiments can also be reconfigured to execute different mathematical functions. The above technical effects are exemplary technical effects, and are not limiting effects.

[0014] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0015] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such

indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0016] Throughout the specification, and in the claims, the term "connected" means a direct electrical connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0017] The term “scaling” generally refers to converting a design (schematic and layout) from one process technology to another process technology. The term “scaling” generally also refers to downsizing layout and devices within the same technology node. The term “scaling” may also refer to adjusting (e.g., slow down) of a signal frequency relative to another parameter, for example, power supply level. The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 20% of a target value.

[0018] Unless otherwise specified the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0019] For purposes of the embodiments, the transistors are metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors also include Tri-Gate and FinFet transistors, Gate All Around Cylindrical Transistors or other devices implementing transistor functionality like carbon nano tubes or spintronic devices. Source and drain terminals may be identical terminals and are interchangeably used herein. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure. The term “MN” indicates an n-type transistor (e.g., NMOS, NPN BJT, etc.) and the term “MP” indicates a p-type transistor (e.g., PMOS, PNP BJT, etc.).

[0020] **Fig. 1** illustrates a high level architecture 100 of a switch-capacitor based bandgap reference and thermal sensor, according to one embodiment. In one embodiment, architecture 100 comprises forward biased diode circuit 101, switch-capacitor based sampler(s) 102 the

sampler is the circuit that samples the diode voltage (Vbe) and converts the diode voltages to a reference signal (Vbg), sigma-delta ADC 103, and counter 104. In one embodiment, for generating a bandgap reference voltage, sigma-delta ADC 103 and counter 104 may not be used.

[0021] In one embodiment, forward biased diode circuit 101 comprises one or more diodes and current source(s). In one embodiment, forward biased diode circuit 101 comprises a first branch having a first current source and a single diode (i.e., high current density diode); a second branch having a second current source and a diode with multiple instances; and a third branch having a third current source to provide reference current. In one embodiment, forward biased diode circuit 101 is independent of any startup circuit. In various embodiments, the one or more diodes may be implemented as actual PN junction diodes, as the base-emitter junction of a bipolar transistor (BJT), parasitic BJT of a CMOS transistor, or as another component with an exponential I(V) characteristic. The generic term "diode" here refers to these circuit elements. In some embodiments, a "string" of several diodes or base-emitter junctions may be formed in series, instead of a single diode or transistor.

[0022] In one embodiment, switch-capacitor sampler 102 samples voltage nodes V1 and V2 of forward biased diode circuit 101 to generate non-continuous time reference Vbg and Vbe i.e., switching voltages. In one embodiment, switch-capacitor sampler 102 is independent of any unity gain operational amplifier. In one embodiment, switch-capacitor sampler 102 operates with at least two clock signals of different phases such that in one phase internal node(s) of switch-capacitor sampler 102 is pre-charged and in another phase internal node(s) of switch-capacitor sampler 102 transfers change.

[0023] In one embodiment, switch-capacitor sampler 102 includes a first switch-capacitor sampler (discussed with reference to **Figs. 2-5**) coupled to forward biased diode circuit 101 to provide a reference voltage Vbg which is independent of temperature (reference). In one embodiment, first switch-capacitor sampler is a dual input switch-capacitor sampler. For example, first switch-capacitor samples voltage nodes from two different branches of forward biased diode circuit 101 to generate bandgap based reference. In one embodiment, switch-capacitor sampler 102 includes a second switch-capacitor sampler (discussed with reference to **Figs. 2-5**) coupled to forward biased diode circuit 101 to provide diode voltage Vbe (i.e., base-emitter voltage of a PN junction). In one embodiment, second switch-capacitor sampler is a single input switch-capacitor sampler.

[0024] In one embodiment, switch-capacitor outputs Vbg (i.e., reference) and Vbe (i.e., signal) are input to sigma-delta ADC 103. In one embodiment, sigma-delta ADC 103 is a single bit sigma-delta ADC. In other embodiments, multiple bit sigma-delta ADC may be used. In one embodiment, output of sigma-delta ADC 103 are pulses (or pulse train) in sampling clock

frequency, where the number of pulses over a given time interval is equal to the ratio between signal (i.e., Vbe) to the reference (i.e., Vbg). In one embodiment, counter 104 receives pulses from sigma-delta ADC 103 and outputs a count of the pulses. In one embodiment, the count indicates the temperature sensed by the one or more diodes of forward biased diode circuit 101.

[0025] **Fig. 2** is architecture 200 of an open loop dual diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 2** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. In one embodiment, architecture 200 comprises forward biased diode circuit 201 (e.g., 101), first switch-capacitor sampler 202a (e.g., part of 102), second switch-capacitor sampler 202b (e.g., part of 102), and sigma-delta modulator 203 (e.g., 103).

[0026] In one embodiment, forward biased diode circuit 201 comprises a first branch having p-type transistor(s) MP1 coupled in series with diode D1. In one embodiment, diode D1 is a single diode (i.e., high current density diode). In one embodiment, gate terminal of MP1 is coupled to node nR which provides a bias voltage using third branch having diode-connected MP3 and reference current circuit Iref.

[0027] In one embodiment, forward biased diode circuit 201 comprises a second branch having p-type transistor(s) MP2 coupled in series with diode D2, where diode D2 is 'N' times larger than diode D1, and where 'N' is an integer greater than one. For example, diode D2 is formed by coupling in parallel 'N' diodes D1. In one embodiment, the current through diode D2 is 'N' times the current through diode D1. In one embodiment, gate terminal of MP2 is coupled to node nR which provides a bias voltage using a third branch having diode-connected MP3 and reference current circuit Iref.

[0028] In one embodiment, source terminals of transistors MP1, MP2, and MP3 are coupled to power supply Vcc. In one embodiment, drain terminal of MP1 is coupled to diode D1. In one embodiment, drain terminal of MP2 is coupled to diode D2. In one embodiment, gate and drain terminals of MP3 are coupled to node nR which is biased by current source Iref. In one embodiment, forward biased diode circuit 201 comprises a switch S1a controllable by clock signal Φ_1. In one embodiment, switch S1a is operable to couple node n1 (i.e., drain terminal of MP1) to node n2 (i.e., drain terminal of MP2) when switch S1a is closed. In one embodiment, switch S1a is formed from a single transistor pass-gate (e.g., p-type or n-type pass gate) or a dual transistor transmission gate (e.g., n-type and p-type transistors coupled in parallel and controllable by Φ_1 and its inverse).

[0029] In one embodiment, first switch-capacitor sampler 202a comprises a first switch S1 controllable by Φ_2, where Φ_2 is inverse of Φ_1, and where switch S1 is operable to couple

nodes n2 and n3 when switch S1 is closed. In one embodiment, first switch-capacitor sampler 202a comprises a second switch S2 controllable by Φ_1, where switch S2 is operable to couple nodes n1 and n4. In one embodiment, first switch-capacitor sampler 202a comprises capacitor C1 coupled to nodes n4 and n5. In one embodiment, first switch-capacitor sampler 202a comprises third switch S3 controllable by Φ_2, where third switch S3 is operable to couple node n4 to ground (i.e., Vss). Here, Φ_2 is a clock signal which is 90 degrees out of phase compared to phase of phase of Φ_1 (i.e., Φ_2 is inverted version of clock signal Φ_1).

[0030] In one embodiment, first switch-capacitor sampler 202a comprises another capacitor coupled to nodes n3 and n5, where the other capacitor is A*C1, and where 'A' is a constant to compensate for Vbe1. In one embodiment, first switch-capacitor sampler 202a comprises a second capacitor C2 coupled to nodes n5 and n6. The relationship in capacitor sizes of capacitors C1 and C2 may depend on desired output voltage level. In one embodiment, the gain of the first switch-capacitor sampler 202a is C1/C2.

[0031] In one embodiment, first switch-capacitor sampler 202a comprises fourth switch S4 controllable by Φ_1, where switch S4 is operable to couple nodes n6 and ground. In one embodiment, first switch-capacitor sampler 202a comprises fifth switch S5 controllable by Φ_2, where switch S5 is operable to couple nodes n6 and Vbg, and where Vbg provides non-continuous bandgap reference to signal-delta ADC 103. In one embodiment, first switch-capacitor sampler 202a comprises sixth switch S6 controllable by Φ_1, where switch S6 is operable to couple nodes n5 and Vbg. In one embodiment, first switch-capacitor sampler 202a comprises a first inverter inv1 with its input coupled to node n5 and output coupled to Vbg. In one embodiment, no operational amplifier is used in first switch-capacitor sampler 202a.

[0032] In one embodiment, second switch-capacitor sampler 202b comprises a seventh switch S7 controllable by Φ_2, where switch S7 is operable to couple nodes n1 and n7. In one embodiment, second switch-capacitor sampler 202b comprises a first capacitor C1 coupled to nodes n7 and n8. In one embodiment, second switch-capacitor sampler 202b comprises eighth switch S8 controllable by Φ_1, where switch S8 is operable to couple nodes n7 and ground. In one embodiment, second switch-capacitor sampler 202b comprises second capacitor C2 coupled to nodes n8 and n9. In one embodiment, second switch-capacitor sampler 202b comprises a ninth switch S9 controllable by Φ_2, where switch S9 is operable to couple nodes n9 and ground.

[0033] In one embodiment, second switch-capacitor sampler 202b comprises tenth switch S10 controllable by Φ_1, where switch S10 is operable to couple nodes n9 to Vbe. In one embodiment, second switch-capacitor sampler 202b comprises eleventh switch S11 controllable by Φ_2, where switch S11 is operable to couple nodes n8 and Vbe. In one embodiment, second switch-capacitor sampler 202b comprises a second inverter inv2 with its input coupled to node

n8 and output coupled to Vbe. In one embodiment, no operational amplifier is used in second switch-capacitor sampler 202b.

[0034] Assuming switch S7 is closed i.e., node n1 is coupled to node n7, second switch-capacitor sampler 202b operates as follows. In phase 1 (i.e., Φ_2 causes switch S9 to close while Φ_1 causes switches S8, S9, and S11 to remain open), voltage across first capacitor C1 of second switch-capacitor sampler 202b is Vin-Vtrip, where Vin is voltage on node n7 and Vtrip is voltage on node n8 which represents tripping voltage of inverter inv2. In phase 1, voltage across second capacitor C2 is equal to Vtrip because node n6 is coupled to ground. Phase 1 is the pre-charge phase in which capacitors C1 and C2 are pre-charged. In one embodiment, phase 2 is the pre-charge phase, and phase 1 is the charge transfer phase i.e., Φ_1 switches are closed in phase 1 and Φ_2 switches are close in phase 2.

[0035] In phase 2 (i.e., Φ_2 causes switch S9 to open while Φ_1 causes switches S8, S9, and S11 to close), charge from capacitors C1 and C2 are transferred. In this embodiment, charge contained in capacitor C2 is QC2=Vin*C1 + Vtrip*C2, where Vin is voltage on node n7 and Vtrip is voltage on node n8 which represents tripping voltage of inverter inv2. In phase 1, node n7 is grounded. Vout (i.e., voltage on node Vbe) is given as (C1/C2)*Vin i.e., sampled Vbe provided to sigma-delta modulator 203 depends on voltage on node n1 (i.e., Vbe1) and ratio of capacitors C1 and C2. In one embodiment, the offset cancellation is performed by charging C2 to Vtrip level and keeping voltage on node n8 at Vtrip level where the two cancel each other from the node Vbe.

[0036] Operation of first switch-capacitor sampler 202a is similar to the operation of second switch-capacitor sampler 202b. Following the same logic of pre-charge phase (i.e., phase 1) and charge transfer phase (i.e., phase 2), output Vbg of first switch-capacitor sampler 202a is equal to (C2/C1)*(A*(V1-V2) + V1), where V1 is the voltage on node n2 when switch S1a is open, and where V2 is the voltage on node n1. The voltage on node n1 is Vbe1 (i.e., voltage between base and emitter of D1) while V1-V2 is a PTAT voltage. In one embodiment, first switch-capacitor sampler 202a samples a differential component (i.e., V1-V2) and adds a single ended component (i.e., V1).

[0037] In one embodiment, sigma-delta ADC 203 samples Vbe in phase 1 and Vbg in phase 2 cycle i.e., in phase 1 Vbe sample is set to charge transfer (when the output is valid) while Vbg is in pre-charge state and, in the following half cycle Vbe is in pre-charge state and Vbg is in charge transfer state. In one embodiment, temperature is computed by comparing Vbe with Vbg (which is a reference).

[0038] For example, number of pulses from sigma-delta ADC 203 is measured when temperature is set to -10°C and when temperature is set to 110°C, and a linear (or substantially

linear) relationship of Vbe at -10°C and 110°C is established. In one embodiment, 'A' is calibrated so Vbg voltage is substantially constant over temperature. In one embodiment, counter 104 measures the number of pulses from sigma-delta ADC 203. The number of pulses indicates a ratio of measured signal Vbe to reference Vbg. This ratio is substantially constant with temperature and is used to determine temperature sensed by the diodes D1 and D2.

[0039] In one embodiment, sigma-delta ADC 103 exhibits a strong PSRR (power supply rejection ratio) compared to the PSRR of the sampler(s) 102. In one embodiment, PSRR of sigma-delta ADC 103 can be further improved by adding dithering mechanisms.

[0040] **Fig. 3** is architecture 300 of an open loop single diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 3** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Architecture 300 is similar to architecture 200. So as not to obscure the embodiments, differences between architectures 300 and 200 are discussed. Functionally, both architectures 300 and 200 provide the ability to sense temperature.

[0041] In one embodiment, architecture 300 comprises forward biased diode circuit 301 (e.g., 101) which uses a single branch diode D1 i.e., diode is only in the first branch. As discussed with reference to **Fig. 2**, diode D1 is a high current density diode. In one embodiment, diode D1 is a single diode. In this embodiment, forward biased diode circuit 301 does not have 'N' number of diodes in the second branch. In one embodiment, third branch of architecture 300 is similar to the third branch of architecture 200.

[0042] In one embodiment, architecture 300 comprises a first switch-capacitor sampler 302a (e.g., 102). Compared to first switch-capacitor sampler 202, first switch-capacitor sampler 302 does not have first switch S1. In this embodiment, capacitor with capacitance A*C1 is coupled between nodes n5 and n1. The other components of first switch-capacitor sampler 302a are similar to components of first switch-capacitor sampler 202a.

[0043] In one embodiment, architecture 300 consumes less power and area than architecture 200 because forward biased diode circuit 301 is smaller in size than forward biased diode circuit 201 (which includes N times more diode D1s) and because first switch-capacitor sampler 302a has fewer samplers than first switch-capacitor sampler 202a. In one embodiment, the high current flows through the diode only at phase 1. In one embodiment, architecture 300 comprises a second switch-capacitor sampler 302b (e.g., 102) which is similar to second switch-capacitor sampler 202b.

[0044] In one embodiment, each sampler (i.e., sampler 302a and 302b) of architecture 300 samples the same diode branch in each phase. Here, each current source (i.e., MP1 and

MP2) has a different current. In one embodiment, current density through diode D1 is changed in each cycle (of Φ1) by changing the current source for diode D1. In one embodiment, current density through diode D1 is changed by switching the number of MP2 (X(N-1)) branches coupled to diode D1, where 'X' represent a transistor (part of MP2), and where 'N' is an integer representing number of 'X' transistor being coupled in parallel.

[0045] **Fig. 4** is architecture 400 of an open loop single switch single diode based digital thermal sensor, according to another embodiment. It is pointed out that those elements of **Fig. 4** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Architecture 400 is similar to architectures 200 and 300. So as not to obscure the embodiments, differences between architectures 400 and 200/300 are discussed. Functionally, both architectures 400 and 200/300 provide the ability to sense temperature.

[0046] In one embodiment, architecture 400 comprises a forward biased diode circuit 401 (e.g., 101) which is similar to forward biased diode circuit 301. In this embodiment, second switch-capacitor sampler (like 202b, or 303b) is not used, and so further area and power are reduced compared to the embodiments of **Fig. 2** and **Fig. 3**. Referring back to **Fig. 4**, architecture 400 comprises a dual input switch-capacitor sampler 402a which is similar to first switch-capacitor sampler 202a. In this embodiment, first switch S1 of dual input switch-capacitor sampler 402a is controllable by Φ'_1 instead of Φ_1, where Φ'_1 is a clock signal derived by dividing Φ_1 clock signal by two.

[0047] In one embodiment, output of dual input switch-capacitor sampler 402a is not directly provided as Vbg to sigma-delta ADC 203, but voltage of node n7 (output of dual input switch-capacitor sampler 402a) is sampled by switches S100 and S200 to generate Vbg and Vbe for sigma-delta ADC 203. In one embodiment, architecture 400 comprises switch S100 which is controllable by a signal which is generated by performing logical AND operation of clock signals Φ_2 and Φ'_1. In one embodiment, switch S100 is operable to couple node n7 to node Vbg. In one embodiment, architecture 400 comprises capacitor C3 coupled to node Vbg and ground.

[0048] In one embodiment, architecture 400 comprises switch S200 which is controllable by a signal which is generated by performing logical AND operation of clock signals Φ_2 and Φ'_2, where Φ'_2 is derived from Φ_2 by dividing Φ_2 by two. In one embodiment, switch S200 is operable to couple node n7 to node Vbe. In one embodiment, architecture 400 comprises capacitor C4 coupled to node Vbe and ground. Unlike the embodiment of **Fig. 2** and **Fig. 3**, sigma-delta ADC 203 of architecture 400 operates using a clock signal having a frequency for switching which is half as slow as the clock signal used to operate sigma-delta ADC 203 of **Fig. 2** and **Fig. 3**. In one embodiment, sigma-delta ADC 203 of architecture 400 operates using a

clock signal having a frequency for switching which is twice as fast as the frequency of clock signal used to operate sigma-delta ADC 203 of **Fig. 2** and **Fig. 3**.

[0049] In one embodiment, sampler 402a changes its sampling designation each half cycle. For example, when switch S1 is open (i.e., the diode D1 branch is not coupled to node n4 through switch S1, sampler 402a provides Vbe to sigma-delta ADC 203 via switch S200. In one embodiment, when switch S1 is closed (i.e., the diode D1 branch is coupled to node n4, sampler 402a provides Vbg to sigma-delta ADC 203 via switch S100. In one embodiment, voltage of Vbe and Vbg are retained by capacitors C4 and C3 respectively. In one embodiment, voltages on capacitors C4 and C3 are updated alternatively, and so Vbe and Vbg are updated alternatively.

[0050] **Fig. 5** is architecture 500 of a closed loop switch-capacitor based bandgap reference generator, according to one embodiment. It is pointed out that those elements of **Fig. 5** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Architecture 500 is similar to architecture 400. So as not to obscure the embodiments, differences between architectures 500 and 400 are discussed. Architecture is a closed loop system (unlike architecture 400) and is used to provide bandgap reference and Vbe for thermal sensing. In one embodiment, the closed loop configuration of architecture 400 can be applied to all embodiments, where instead of an independent current source the reference voltage controls the diode current.

[0051] In one embodiment, architecture 500 comprises a forward biased diode circuit 501 (e.g., 101) which is similar to forward biased diode circuit 401 of architecture 400. In one embodiment, architecture 500 comprises a switch-capacitor sampler 502a which is similar to first switch-capacitor sampler 402a. In this embodiment, n-type transistor MN1 replaces Iref of **Fig. 4**. Here, source terminal of MN1 is coupled to ground, drain terminal of MN1 is coupled to node nR, and gate terminal is coupled to node Vbg. In this embodiment, closed loop (i.e., feedback loop) is formed by feeding back Vbg to control MN1. In one embodiment, the feedback loop of architecture 500 acts as an error amplifier with a negative feedback keeping the difference between the PTAT and Vbe substantially fixed.

[0052] **Fig. 6** is architecture 600 with processor with bandgap reference generator and digital thermal sensor, according to one embodiment. It is pointed out that those elements of **Fig. 6** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0053] In one embodiment, architecture 600 comprises processor 601, thermal sensor 602, and bandgap reference circuit 603. In one embodiment, thermal sensor 602 resides outside

processor 601 and is used to sense temperature external to processor 601. In such an embodiment, thermal sensor 602 provides the temperature "temp" to processor 601 for further processing. In one embodiment, bandgap reference circuit 603 is used to provide a bandgap reference Vbg to processor 601. In one embodiment, thermal sensor 602 is implemented according to any one of embodiments of **Figs. 1-4** and **Figs. 7-8**. In one embodiment, bandgap reference circuit 603 is implemented according to embodiment of **Fig. 5**.

[0054] In one embodiment, processor 601 comprises thermal sensor 604 to measure on-die temperature of processor 601. In one embodiment, thermal sensor 604 is implemented according to any one of embodiments of **Figs. 1-4** and **Figs. 7-8**. In one embodiment, processor 601 comprises bandgap reference circuit 605 to provide bandgap reference another circuit of processor 601. In one embodiment, bandgap reference circuit 605 is implemented according to embodiment of **Fig. 5**.

[0055] In one embodiment, processor 601 comprises a remote thermal sensor 606 with remote diodes 607. In this embodiment, diode D1 and/or diode D2 of forward biased diode circuit (according to embodiments of **Figs. 1-4** and **Figs. 7-8**) are remotely positioned relative to the location of thermal sensor 606. The rest of the thermal sensor 606 is according to any one of embodiments of **Figs. 1-4** and **Figs. 7-8**. For example, diode D1 and/or diode D2 may be placed in hot spots of processor 601 without having to place the entire thermal sensor in those hot spots. In one embodiment, processor 601 comprises a power control unit PCU (not shown) to process temperature readings from external and internal thermal sensors to manage power consumption (i.e., performance) of processor 601.

[0056] **Fig. 7** is a circuit 700 illustrating rotating switches in a forward biased diode circuit for dynamic matching in a single diode switch-capacitor based digital thermal sensor, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0057] The embodiment of **Fig. 7** may be applicable to other embodiments explained here with single diode forward biased diode circuits (e.g., **Figs. 3-5**). In one embodiment, circuit 700 comprises a decoder 701, counter 702, logic gate 703, rotating switch based forward biased diode circuit 704. In one embodiment, counter 702 is an up or down counter which counts up or down every clock cycle CLKIN. In one embodiment, output of counter 702 is converted into an 'N' bit output OUT[1:N] by decoder 701. In one embodiment, decoder 701 is a thermometer decoder. However, the embodiments are not limited to thermometer decoder. Other decoding schemes may also be used in the embodiments.

[0058] In one embodiment, logic gate 703 (e.g., OR logic gate) generates control signal CONT[1:N] to dynamically rotate switches sc1-scN, where 'N' is an integer greater than 1. In one embodiment, logic gate 703 performs an OR function between output of decoder 701 and first phase of clock i.e., Φ_1. In one embodiment, by continuously turning on and off the switches sc1-scN, while keeping current thought diode D1 constant, inaccuracies in the thermal sensor measurement or bandgap reference are averaged.

[0059] In one embodiment, during the first phase of clock Φ_1, all the switches are closed and the current through the diode D1 is high (resulting in node n1 having voltage V1). In one embodiment, during Φ_2 only one switch is open leading to low current density (resulting in node n1 having voltage V2). In this embodiment, the remaining switches are open. The switch which is closed during Φ_2 changes each cycle according to the decoder output OUT[1:N], and therefore mitigating random variations between the different devices MPX, where 'X' is an integer ranging from 1 to N+1 (where 'N' is also an integer).

[0060] In one embodiment, forward biased diode circuit 704 (which here is shown without diode D1 for simplicity sake) comprises N+1 current sources, were 'N' is an integer greater than 1. In one embodiment, drain terminals of MP1-MPN are coupled to switches sc1-scN respectively. In one embodiment, other end of switches is coupled to node n1 which is then coupled to diode D1. In one embodiment, gate terminals of MN1-MP(N+1) is coupled to node nR. In one embodiment, switches sc1-scN are controlled by CONT[1:N] signal. In one embodiment, switches sc1-scN are implemented as p-type transistors, n-type transistors, or combination of both.

[0061] **Fig. 8** is a smart device or a computer system or an SoC (system-on-chip) with the bandgap reference architecture, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 8** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0062] **Fig. 8** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In one embodiment, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0063] In one embodiment, computing device 1600 includes a first processor 1610 with the bandgap reference and thermal sensor architecture described with reference to embodiments discussed. Other blocks of the computing device 1600 may also include apparatus of with

bandgap reference and thermal sensor architecture described with reference to embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant or a wearable device.

[0064] In one embodiment, processor 1610 (and/or processor 1690) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. Processor 1690 may be optional. While the embodiment shows two processors, a single or more than two processors may be used. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0065] In one embodiment, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0066] Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0067] I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems,

video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0068] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0069] In one embodiment, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0070] In one embodiment, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0071] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0072] Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0073] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0074] Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[0075] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0076] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the

same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0077] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0078] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. For example, other memory architectures e.g., Dynamic RAM (DRAM) may use the embodiments discussed. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0079] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0080] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0081] For example, in one embodiment, an apparatus independent of an operational amplifier is provided. The apparatus comprises: a forward biased diode circuit having one or more diodes; a first switch-capacitor sampler coupled to the forward biased diode circuit, the

first switch-capacitor sampler to provide a reference voltage which is proportional to absolute temperature; and a second switch-capacitor sampler coupled to the forward biased diode circuit.

[0082] In one embodiment, the first switch-capacitor sampler is a dual input switch-capacitor sampler. In one embodiment, the second switch-capacitor sampler is a single input switch-capacitor sampler. In one embodiment, the apparatus comprises a sigma-delta analog-to-digital converter coupled to the first and second switch-capacitor samplers. In one embodiment, the sigma-delta analog-to-digital converter to receive the reference voltage from the first switch-capacitor sampler and a diode voltage from the second switch-capacitor sampler.

[0083] In one embodiment, the apparatus further comprises a counter to count a number of pulses output from the sigma-delta analog-to-digital converter. In one embodiment, the forward biased diode circuit comprises: a first branch having a first current source and a single diode. In one embodiment, the forward biased diode circuit comprises: a second branch having a second current source and a diode with multiple instances; and a third branch having a third current source to provide reference current.

[0084] In one embodiment, the first switch-capacitor sampler has a first input coupled to the second branch, and a second input coupled to the first branch. In one embodiment, the second switch-capacitor sampler has an input coupled to the first branch. In one embodiment, the first switch-capacitor sampler has a first input coupled to the first branch, and a second input coupled to the first branch. In one embodiment, the one or more diodes are positioned remotely from other devices of the forward biased diode circuit.

[0085] In another example, a system comprises: a memory; a processor, coupled to the memory, the processor including a thermal sensor according to apparatus discussed above; and a wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit. In one embodiment, the display unit is a touch screen.

[0086] In another example, an apparatus to generate a bandgap reference is provided. The apparatus comprises: a forward biased diode circuit having one or more diodes; and a dual input switch-capacitor sampler coupled to the forward biased diode circuit, the dual input switch-capacitor sampler to provide a bandgap voltage reference which is used as a feedback to control reference current through the forward biased diode. In one embodiment, the forward biased diode circuit includes a switch coupled to two sets of current sources, and coupled to a single diode. In one embodiment, the forward biased diode circuit includes an n-type transistor controllable by the bandgap voltage reference.

[0087] In another example, a system comprises: a memory; a processor, coupled to the memory, the processor including a bandgap reference circuit according to the apparatus

discussed above; and a wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit. In one embodiment, the display unit is a touch screen.

[0088] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

I claim:

1. An apparatus independent of an operational amplifier, the apparatus comprising:

a forward biased diode circuit having one or more diodes;

a first switch-capacitor sampler coupled to the forward biased diode circuit, the first switch-capacitor sampler to provide a reference voltage which is proportional to absolute temperature; and

a second switch-capacitor sampler coupled to the forward biased diode circuit.

2. The apparatus of claim 1, wherein the first switch-capacitor sampler is a dual input switch-capacitor sampler.

3. The apparatus of claim 1, wherein the second switch-capacitor sampler is a single input switch-capacitor sampler.

4. The apparatus of claim 1 further comprises a sigma-delta analog-to-digital converter coupled to the first and second switch-capacitor samplers.

5. The apparatus of claim 4, wherein the sigma-delta analog-to-digital converter to receive the reference voltage from the first switch-capacitor sampler and a diode voltage from the second switch-capacitor sampler.

6. The apparatus of claim 4 further comprises a counter to count a number of pulses output from the sigma-delta analog-to-digital converter.

7. The apparatus of claim 1, wherein the forward biased diode circuit comprises:

a first branch having a first current source and a single diode.

8. The apparatus of claim 7, wherein the forward biased diode circuit comprises:

a second branch having a second current source and a diode with multiple instances; and

a third branch having a third current source to provide reference current.

9. The apparatus of claim 8, wherein the first switch-capacitor sampler has a first input coupled to the second branch, and a second input coupled to the first branch.

10. The apparatus of claim 7, wherein the second switch-capacitor sampler has an input coupled to the first branch.

11. The apparatus of claim 7, wherein the first switch-capacitor sampler has a first input coupled to the first branch, and a second input coupled to the first branch.

12. The apparatus of claim 1, wherein the one or more diodes are positioned remotely from other devices of the forward biased diode circuit.

13. An apparatus comprising:

a forward biased diode circuit having one or more diodes; and

a dual input switch-capacitor sampler coupled to the forward biased diode circuit, the dual input switch-capacitor sampler to provide a bandgap voltage reference which is used as a feedback to control reference current through the forward biased diode.

14. The apparatus of claim 13, wherein forward biased diode circuit includes a switch coupled to two sets of current sources, and coupled to a single diode.

15. The apparatus of claim 13, wherein forward biased diode circuit includes an n-type transistor controllable by the bandgap voltage reference.

16. A system comprising:

a memory;

a processor, coupled to the memory, the processor including a thermal sensor which comprises an apparatus according to any one of apparatus claims 1 to 12; and

a wireless interface for allowing the processor to communicate with another device.

17. The system of claim 16 further comprises a display unit.

18. The system of claim 17, wherein the display unit is a touch screen.

19. A system comprising:

a memory;

a processor, coupled to the memory, the processor including a bandgap reference circuit which comprises an apparatus according to any one of apparatus claims 13 to 15; and

a wireless interface for allowing the processor to communicate with another device.

20. The system of claim 19 further comprises a display unit.

21. The system of claim 20, wherein the display unit is a touch screen.

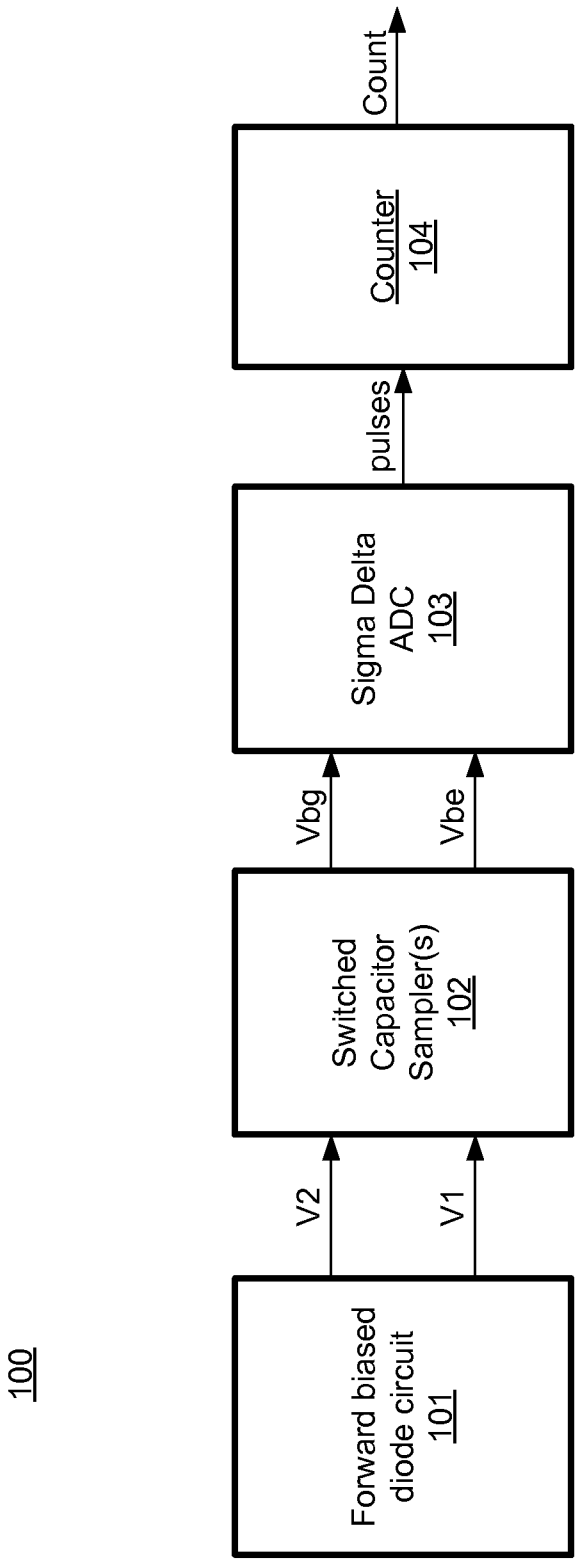

100
Forward biased diode circuit 101
V2
V1
Switched Capacitor Sampler(s) 102
Vbg
Vbe
Sigma Delta ADC 103
pulses
Counter 104
Count

Fig. 1

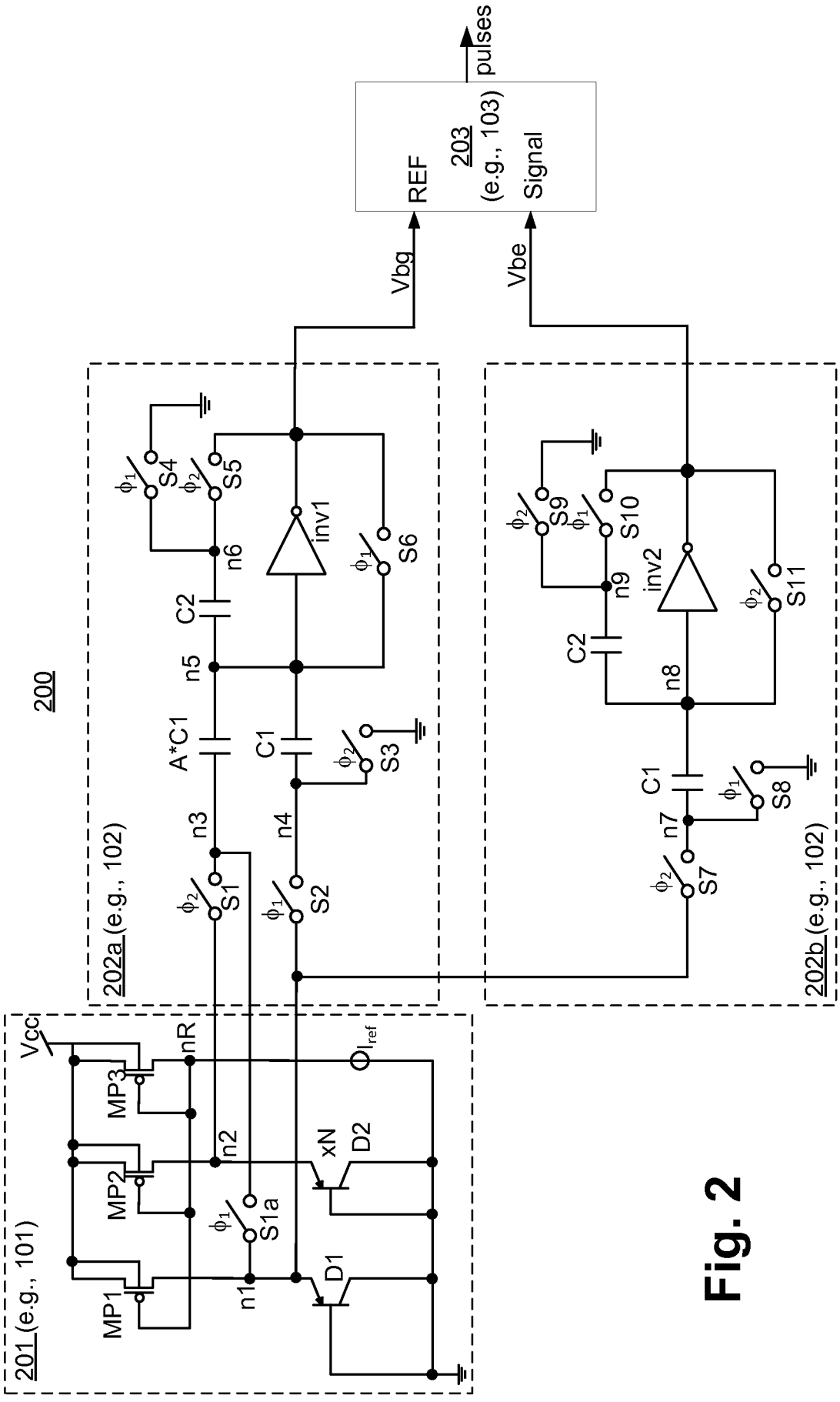

200
201 (e.g., 101)
202a (e.g., 102)
202b (e.g., 102)
203 (e.g., 103)
Vcc
nR
MP1
MP2
MP3
n1
n2
S1a
D1
xN
D2
Iref
Vbg
Vbe
REF
Signal
pulses
inv1
inv2
n3
n4
n5
n6
n7
n8
n9
A*C1
C1
C2
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11

Fig. 2

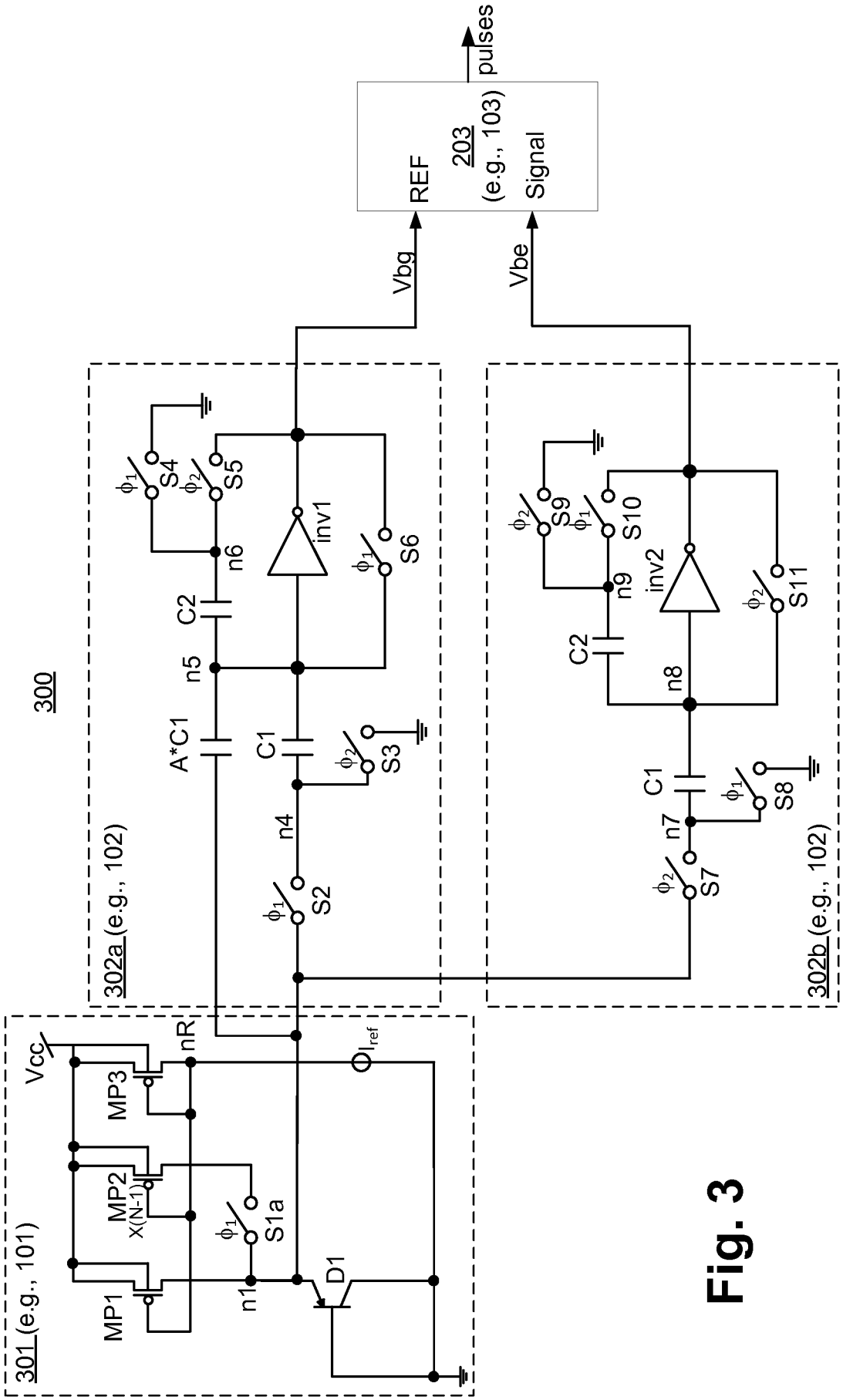

300
301 (e.g., 101)
Vcc
MP3
MP2
x(N-1)
MP1
nR
n1
S1a
D1
I_{ref}
302a (e.g., 102)
A*C1
C1
C2
n4
n5
n6
S2
S3
S4
S5
S6
inv1
302b (e.g., 102)
C1
C2
n7
n8
n9
S7
S8
S9
S10
S11
inv2
Vbg
Vbe
203
(e.g., 103)
REF
Signal
pulses

Fig. 3

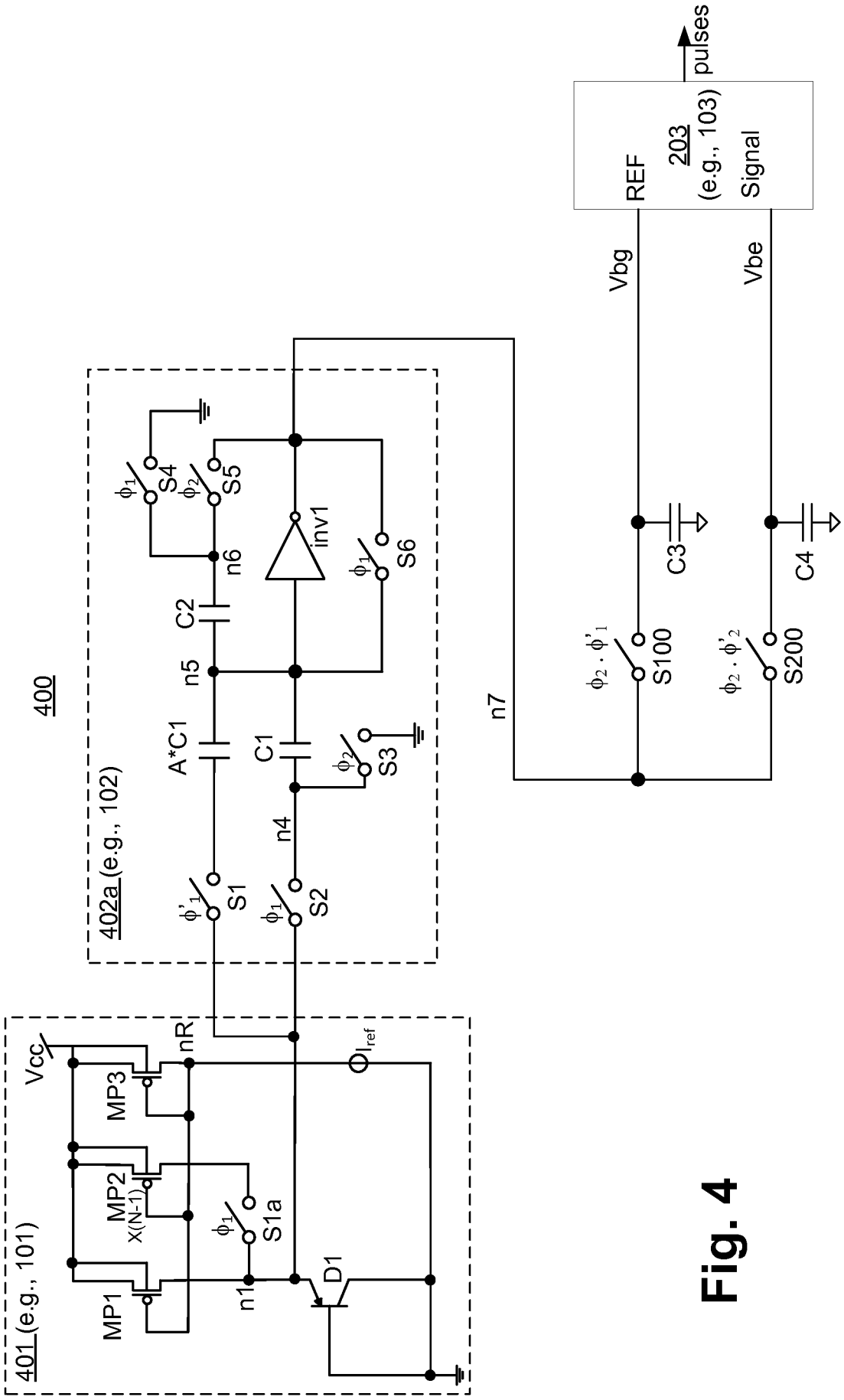

400
401 (e.g., 101)
Vcc
MP3
MP2
x(N-1)
MP1
nR
n1
S1a
D1
Iref
402a (e.g., 102)
S1
S2
S3
S4
S5
S6
A*C1
C1
C2
n4
n5
n6
inv1
n7
203
(e.g., 103)
REF
Signal
pulses
Vbg
Vbe
C3
C4
S100
S200

Fig. 4

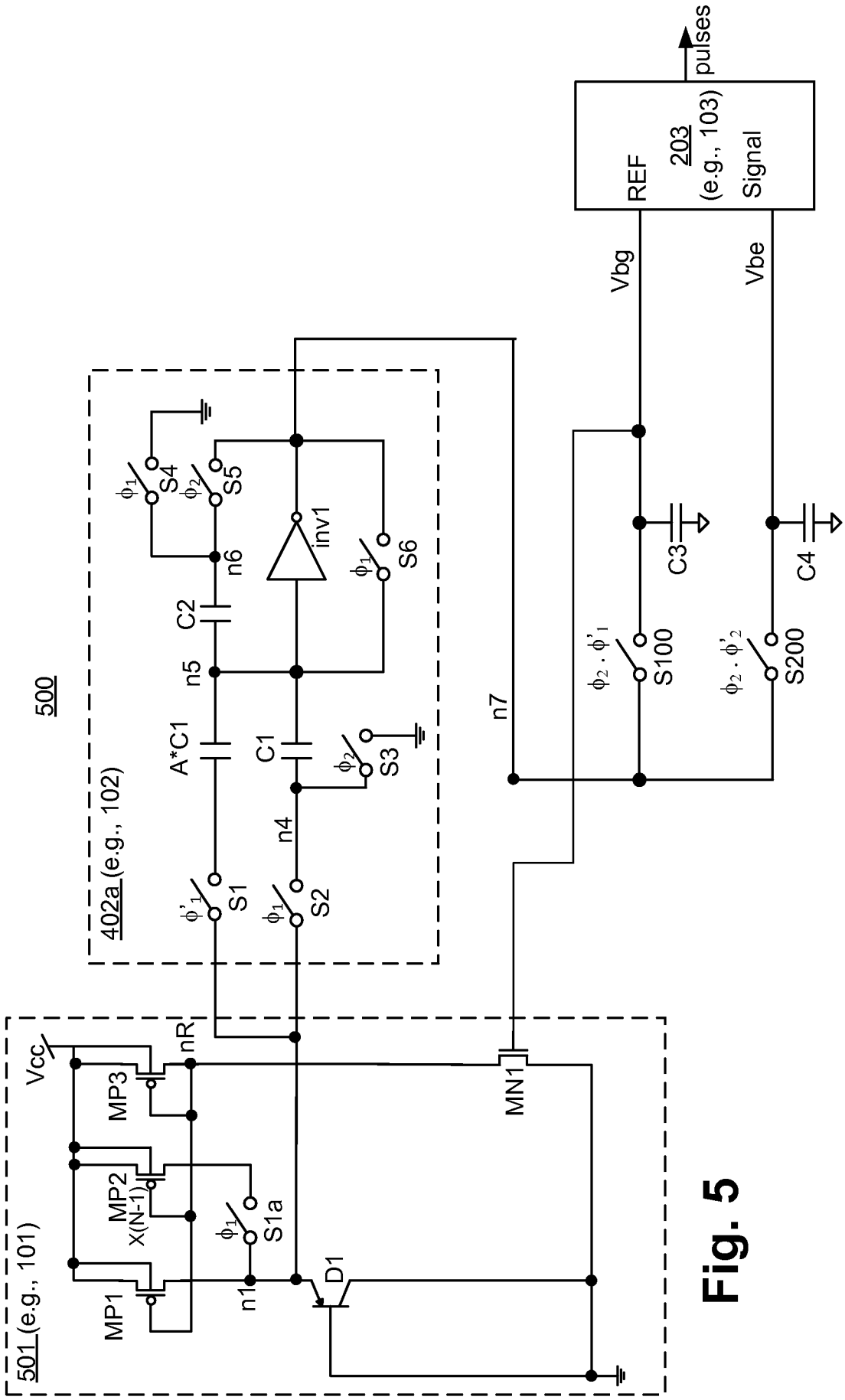

pulses
203 (e.g., 103)
REF
Signal
Vbg
Vbe
500
402a (e.g., 102)
501 (e.g., 101)
Vcc
nR
MP3
MP2 X(N-1)
MP1
S1a
n1
D1
MN1
n7
n6
n5
n4
A*C1
C1
C2
C3
C4
inv1
S1
S2
S3
S4
S5
S6
S100
S200

Fig. 5

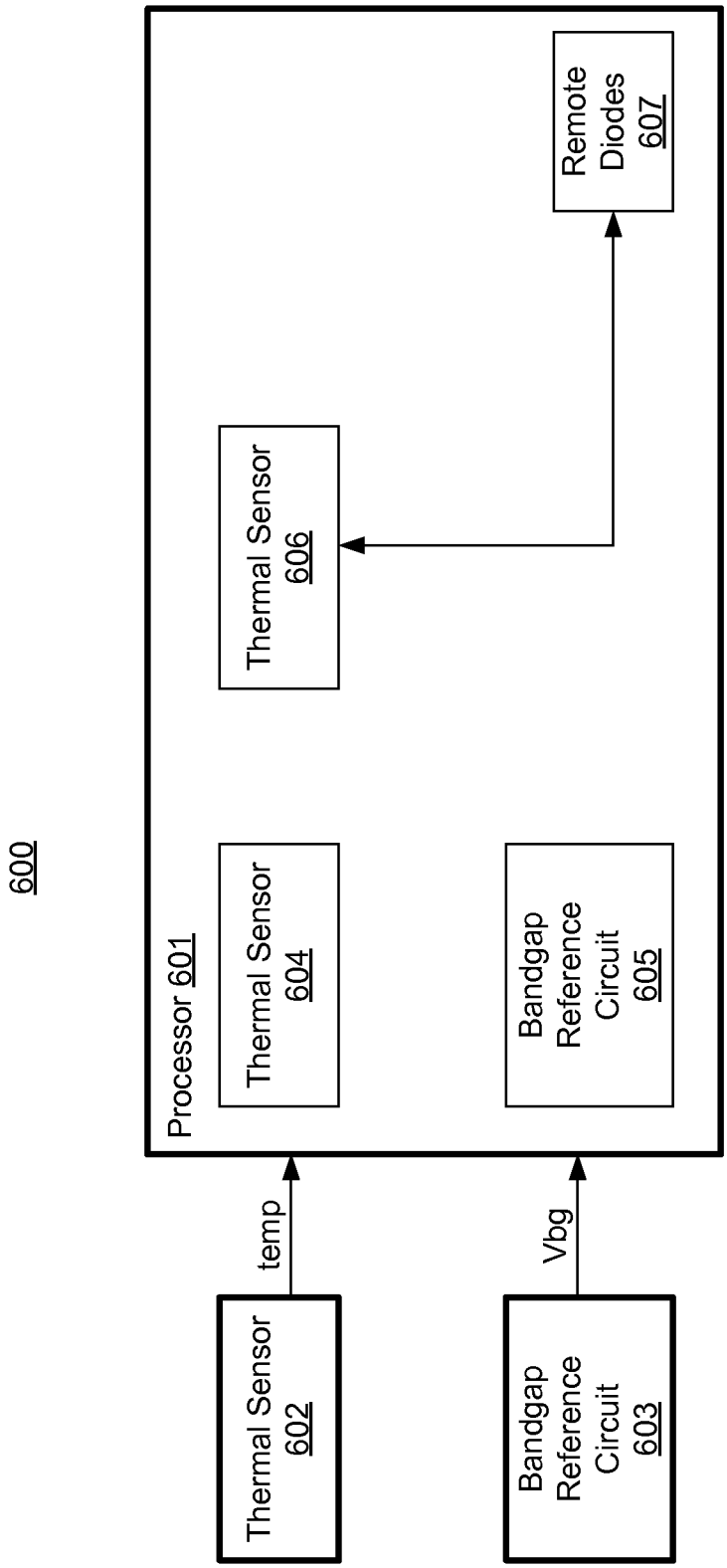

600
Processor 601
Thermal Sensor 604
Bandgap Reference Circuit 605
Thermal Sensor 606
Remote Diodes 607
temp
Vbg
Thermal Sensor 602
Bandgap Reference Circuit 603

Fig. 6

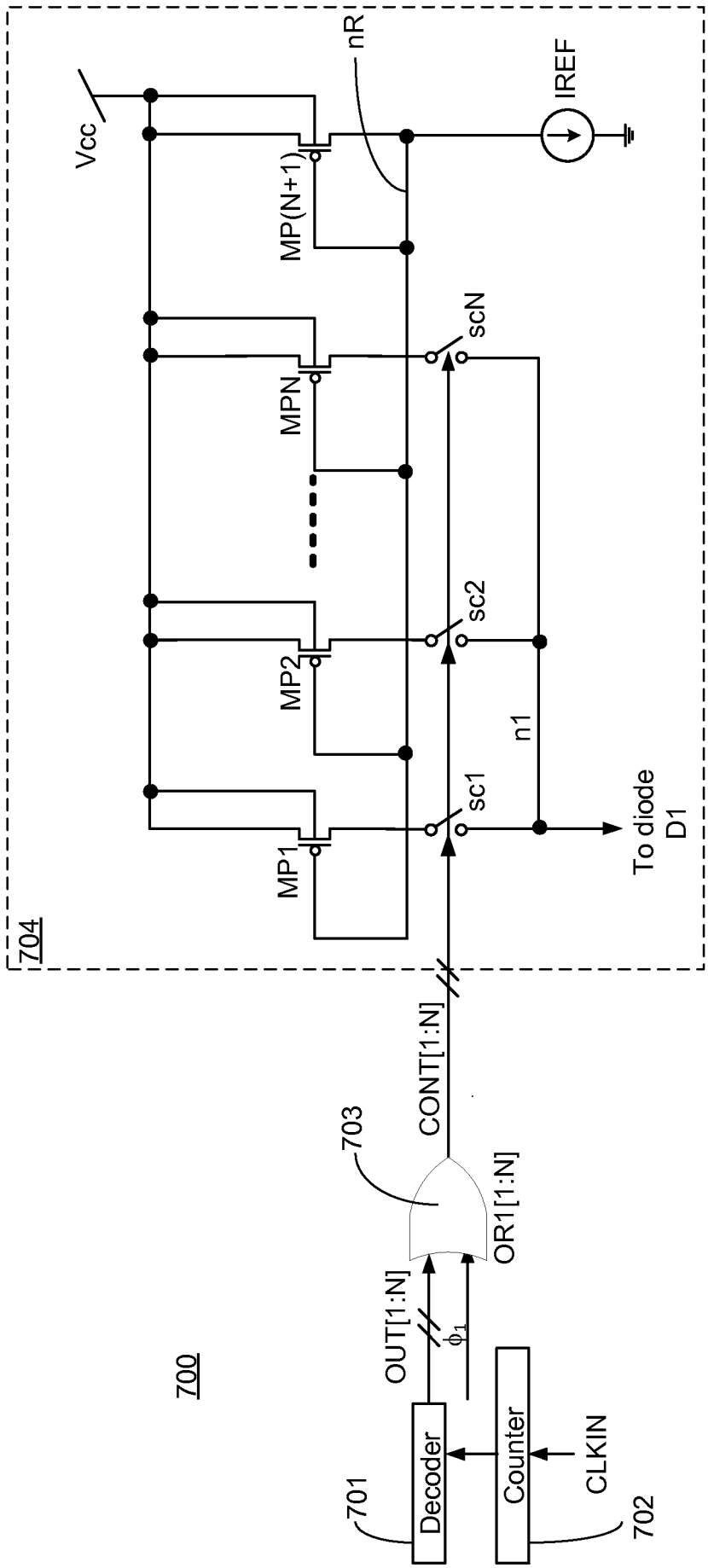

700
701
Decoder
OUT[1:N]
ϕ_1
Counter
CLKIN
702
703
OR1[1:N]
CONT[1:N]
704
Vcc
nR
IREF
MP(N+1)
scN
MPN
sc2
MP2
n1
sc1
MP1
To diode
D1

Fig. 7

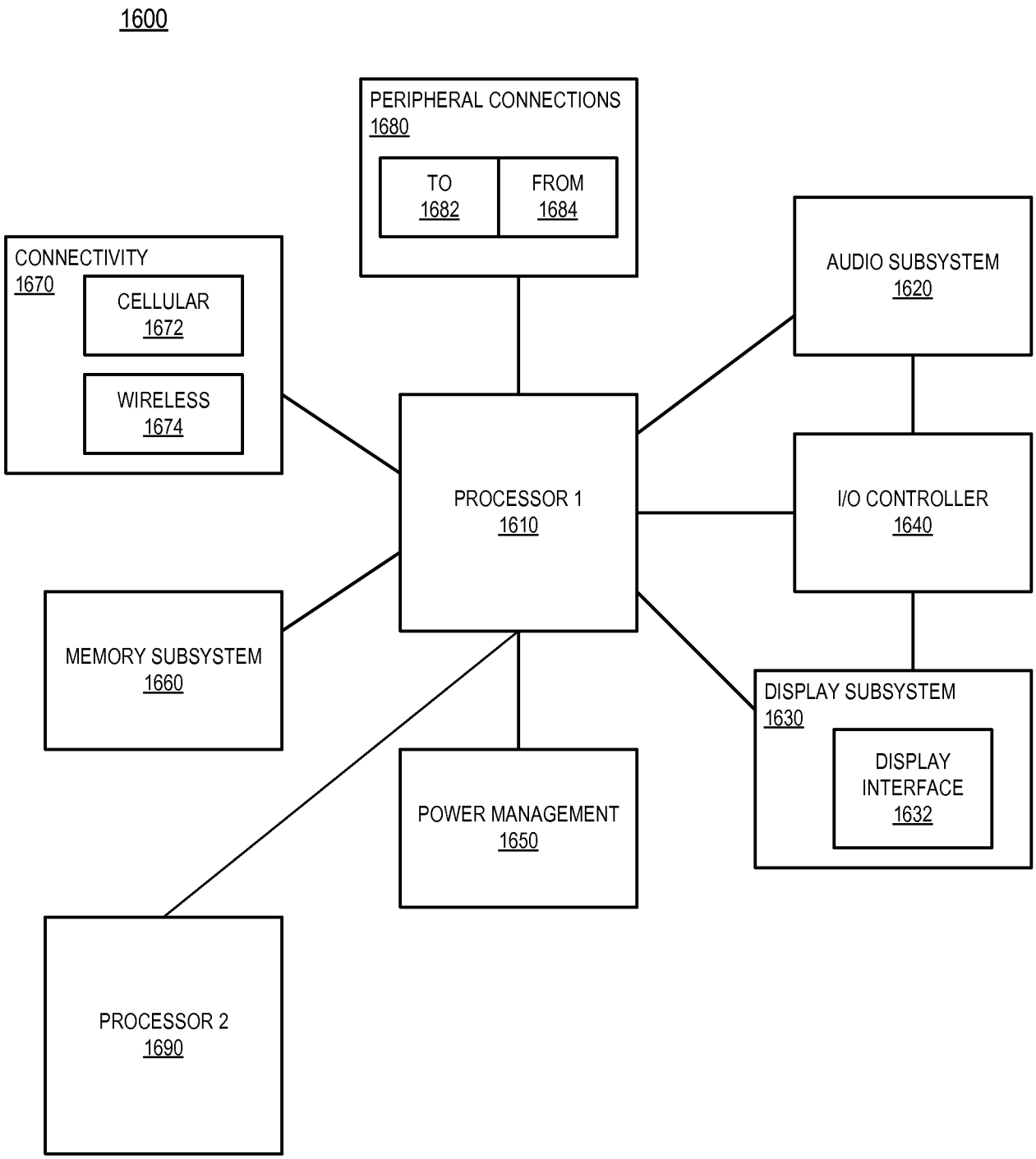

1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1620
PROCESSOR 1
1610
I/O CONTROLLER
1640
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650
PROCESSOR 2
1690

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2013/062222

A. CLASSIFICATION OF SUBJECT MATTER

G01K 7/01 *(2006.01)*
G05F 3/30 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01K 7/00, 7/01, G05F 3/00, 3/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0120930 A1 (GRIGORI TEMKINE et al) 16.05.2013, abstract, pages 2-4, fig.1, 2	1-21
A	US 2013/0241526 A1 (PANASONIC CORPORATION) 19.09.2013, pages 3-5, fig.2, 3	1-21
A	RU 2493592 C1 (OBSCHESTVO S OGRANICHENNOI OTVETSTVENNOSTYU "NAUCHNO PROIZVODSTVENNOE PREDPRIYATIE ROBIC") 20.09.2013, pages 6-7, fig.1	1-21

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search	Date of mailing of the international search report
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