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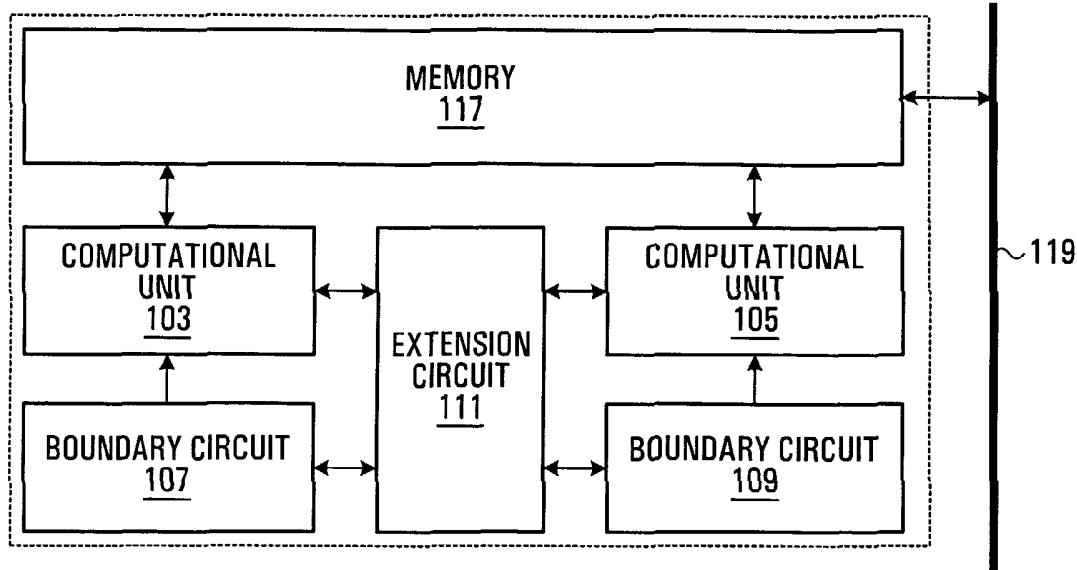
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(54) Title: APPARATUS FOR VARIABLE WORD LENGTH COMPUTING IN AN ARRAY PROCESSOR



(57) Abstract: A computational unit comprises a processor having a plurality of processing elements, each having an arithmetic logic unit, and a controller for controlling the processor elements. The processor can provide a respective bit of a multiple bit word to each of the processor elements and enables signals to be transmitted between the arithmetic logic units to enable the units to perform a parallel operation on the bits of the multiple bit word. Extension circuitry is provided for selectively coupling one or more computational units together to combine their parallel processing capability.



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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	EP 0 973 100 A (SONY CORP) 19 January 2000 (2000-01-19) the whole document ---	1,2,7 3-6,8-27
A	EP 0 463 721 A (GENNUM CORP) 2 January 1992 (1992-01-02) the whole document ---	1,2,7 3-6,8-27
A	US 5 797 027 A (KAJIURA HIROYUKI) 18 August 1998 (1998-08-18) the whole document ---	1-27
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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