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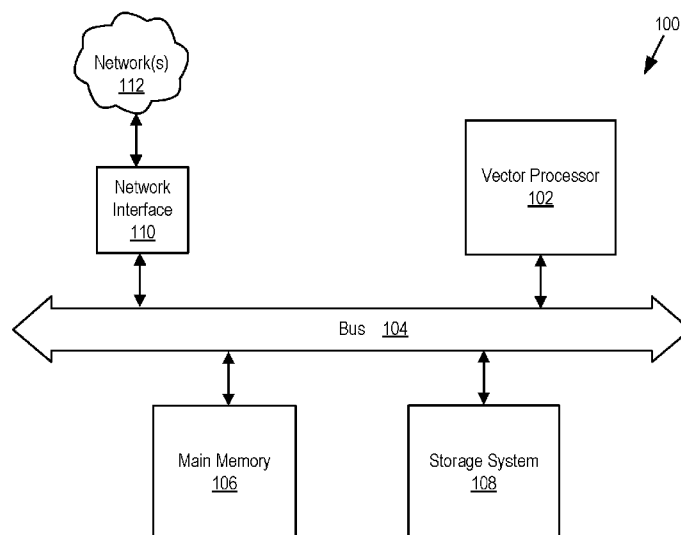


FIG. 1

(57) Abstract: Disclosed herein are vector index registers for storing or loading indexes of true and/or false results of conditional operations in vector processors. Each of the vector index registers store multiple addresses for accessing multiple positions in operand vectors in various types of operations.



## CONDITIONAL OPERATIONS IN A VECTOR PROCESSOR

### RELATED APPLICATION

**[0001]** The present application claims priority to U.S. Pat. App. Ser. No. 16/417,508, filed May 20, 2019 and entitled "CONDITIONAL OPERATIONS IN A VECTOR PROCESSOR," the entire disclosure of which is hereby incorporated herein by reference.

### FIELD OF THE TECHNOLOGY

**[0002]** In general, at least some embodiments disclosed herein relate to vector processors. Also, at least some embodiments disclosed herein relate to registers in vector processors that store addresses for accessing vectors.

### BACKGROUND

**[0003]** A vector processor can be or include a central processing unit (CPU) that implements an instruction set containing instructions that operate on arrays of data of commonly referred to as vectors. This is different from a scalar processor, wherein instructions operate on single data items. Vector processors can greatly improve performance on certain workloads over scalar processor, notably numerical simulation and similar tasks. Vector processors appeared in the early 1970s and where a large part of supercomputing design through the 1970s into the 1990s. The rapid fall in the price-to-performance ratio of more conventional microprocessor designs, such as scalar processor designs, as led to less development and manufacturing of vector processors.

**[0004]** In general, conventional CPUs (e.g., scalar based CPUs) are able to manipulate a few pieces of data at a time, at most. For instance, such CPUs have an instruction that essentially provide adding A to B and store the result in C. The data for A, B and C is usually pointed to by passing in an address to a memory location that holds the data. Decoding this address and getting the data out of the memory takes some time, during which the CPU can sit idle waiting for the requested data to show up.

**[0005]** To reduce the amount of time consumed by these steps, more

contemporary CPUs use a technique known as instruction pipelining in which the instructions pass through several sub-units in turn. The first sub-unit reads the address and decodes it, the next fetches the values at those addresses, and the next does the math itself. With pipelining, the CPU starts decoding the next instruction even before the first has left the CPU, similar to an assembly line. This way, the address decoder, and other mentioned parts are simultaneously and constantly in use. Because of the pipelining, any instruction takes the same amount of time to complete.

**[0006]** Vector processors improve on pipelining by, instead of pipelining merely the instructions, such processors also pipeline the data itself. Thus, instead of constantly having to decode instructions and then fetch the data needed to complete the instructions, the vector processor reads a single instruction from memory. This allows for reduced decoding time and reduced power consumption (e.g., one decode with vector processors instead of multiple decodes).

**[0007]** Vector processors as well as other types of processors, such as the commonly used scalar processors, include index registers for modifying operand addresses during the run of a program or operation. Often indexes are used and beneficial for doing vector or array operations. The contents of an index register can be added to or subtracted from an immediate address to form an effective address of the actual data or operand. Commonly, instructions can test the index register and, if the test fails, the instructions can reset the start of the loop. Some instruction sets allow multiple index registers to be used.

**[0008]** In general, it is known to use scalar registers for indexing. In other words, it is known to use scalar index registers. However, there are many limitations associated with using a scalar register for indexing. And, some of these limitations can curb the performance of a processor using the index register. For example, to access multiple positions of an operand vector, a scalar index register needs to be incremented and each incrementation needs to be separately loaded by the processor to be used for accessing the operand vector.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** The present disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure.

**[0010]** FIG. 1 illustrates example parts of an example computing device 100, in accordance with some embodiments of the present disclosure.

**[0011]** FIG. 2 illustrates example parts of an example computing device 200, in accordance with some embodiments of the present disclosure.

**[0012]** FIG. 3 illustrates an example system 300 including a vector index register 302, in accordance with some embodiments of the present disclosure.

**[0013]** FIG. 4 illustrates an example system 400 including vector index registers 402a, 402b, and 402c, in accordance with some embodiments of the present disclosure.

**[0014]** FIG. 5 illustrates an example system 500 including a vector index register 502 and a vector first register 503, in accordance with some embodiments of the present disclosure.

**[0015]** FIG. 6 illustrates example operations of method 600 for accessing elements of an operand vector, in accordance with some embodiments of the present disclosure.

**[0016]** FIG. 7 illustrates example operations of method 700 for compressing elements of an operand vector, in accordance with some embodiments of the present disclosure.

**[0017]** FIG. 8 illustrates an example system 800 including a vector index register 802 being used for compressing elements of an input operand vector stored in an input OVR 804, in accordance with some embodiments of the present disclosure.

**[0018]** FIG. 9 illustrates example operations of method 900 for expanding elements of an operand vector, such as elements of a compressed operand vector, in accordance with some embodiments of the present disclosure.

**[0019]** FIG. 10 illustrates example operations of method 1000 related to operations on multiple compressed vectors, in accordance with some embodiments of the present disclosure.

**[0020]** FIG. 11 illustrates example operations of method 1100 for building indexing vectors for storing in vector indexing registers for TRUE and FALSE results (e.g., "0" and "1" results) of a comparison (VIR\_TRUE and VIR\_FALSE), in accordance with some embodiments of the present disclosure.

**[0021]** FIG. 12 illustrates an example system 1200 for building indexing vectors for storing in VIR\_TRUE 1202a and VIR\_FALSE 1202b, in accordance with some embodiments of the present disclosure.

**[0022]** FIG. 13 illustrates example operations of method 1300 for building a combined indexing vector for storing in a combined vector indexing register for TRUE and FALSE results of a comparison (VIR\_combined), in accordance with some embodiments of the present disclosure.

**[0023]** FIG. 14 illustrates an example system 1400 for building a combined indexing vector for storing in VIR\_combined 1402, in accordance with some embodiments of the present disclosure.

**[0024]** FIG. 15 illustrates an example system 1500 including a VIR\_TRUE 1502a and a VIR\_FALSE 1502b, in accordance with some embodiments of the present disclosure.

**[0025]** FIG. 16 illustrates example operations of method 1600 for compressing elements of an operand vector according to a VIR\_TRUE, in accordance with some embodiments of the present disclosure.

**[0026]** FIG. 17 illustrates an example system 1700 including a VIR\_TRUE 1702a being used for compressing elements of an input operand vector stored in an input OVR 1704, in accordance with some embodiments of the present disclosure.

**[0027]** FIGS. 18 and 19 each illustrates example operations for building indexing vectors for storing in vector indexing registers for TRUE and FALSE results (e.g., “0” and “1” results) of a conditional test operation (VIR\_TRUE and VIR\_FALSE), in accordance with some embodiments of the present disclosure.

**[0028]** FIG. 20 illustrates an example system 2000 for building indexing vectors for storing in VIR\_TRUE 2002a and VIR\_FALSE 2002b, in accordance with some embodiments of the present disclosure.

**[0029]** FIGS. 21 and 22 illustrates example operations of method 2100 for running operations on elements of operand vectors according to a VIR\_TRUE and a VIR\_FALSE (or TRUE and FALSE sections of a VIR\_COMBINED), in accordance with some embodiments of the present disclosure.

**[0030]** FIG. 23 illustrates an example system 2200 including VIR\_TRUE and VIR\_FALSE being used for running first and second operations on elements of input operand vectors stored in input operand vector registers, in accordance with some embodiments of the present disclosure.

**[0031]** FIG. 24 illustrates an example system 2300 including TRUE and FALSE sections of a VIR\_COMBINED being used for running first and second operations on elements of input operand vectors stored in input operand vector registers, in

accordance with some embodiments of the present disclosure.

**[0032]** FIG. 25 illustrates an example system 2400 including VIR\_TRUE and VIR\_FALSE being used for running first and second operations, in parallel, on elements of input operand vectors stored in input operand vector registers, in accordance with some embodiments of the present disclosure.

### DETAILED DESCRIPTION

**[0033]** In general, at least some embodiments disclosed herein relate to vector processors. Also, at least some embodiments disclosed herein relate to registers in vector processors that store addresses for accessing vectors. And, at least some of the embodiments disclosed herein are vector index registers in vector processors that each store multiple addresses for accessing multiple positions in vectors.

**[0034]** It is known to use a scalar index register in a vector processor to reference multiple positions of vectors by changing the value stored in the scalar index register during a vector operation. However, by using a vector indexing register for indexing multiple positions of one or more operand vectors, the scalar index register can be replaced and at least the continual changing of values in the scalar index register during a vector operation can be avoided. This is just one example of a technical solution to a technical problem described herein.

**[0035]** A scalar or single-entry register can store an index  $i$  that allows the operation on a vector register to start at element  $i$ , or the operation can start at element zero. The subsequent parts of the operation access elements  $0+1$  or  $i+1$  at each increment. On a side note, using a single-entry register that stores an index  $i$  can be used for vector first operations and indexing, which is also disclosed herein to some extent.

**[0036]** However, there are many limitations associated with using a scalar register or single-entry vector for indexing. And, some of these limitations can curb the performance of a vector processor using the index register. For example, to access multiple positions of an operand vector, a scalar or single-entry index register needs to be incremented and each incrementation needs to be separately loaded by the vector processor to be used for accessing the operand vector.

**[0037]** By using a vector indexing register for indexing a plurality of positions of one or more operand vectors, the scalar index register can be replaced and at least the continual changing of the scalar index register during a vector operation can be

avoided

**[0038]** In general, the embodiments disclosed herein provide specific technical solutions to at least the technical problems mentioned in the background section and other parts of the application as well as other technical problems not described herein but recognized by those of skill in the art.

**[0039]** In some embodiments, a vector index register (VIR) can store address components for vector operations that use selective indexing. This is somewhat analogous to vector first processing or indexing. For example, using selective indexing, a VIR can store address parts  $i_1, i_2, \dots, i_n$ . This allows the operations on a vector register to move through elements  $i_1, i_2, \dots, i_n$  of an input vector, instead of  $i, i+1, i+2, \dots, i+n$  of the input vector. For example, using selective indexing, a VIR can store non-sequential address parts  $i_1, i_3, \dots, i_8$ . This allows the operations on a vector register to move through non-sequential elements of an input vector.

**[0040]** The uses of a VIR are many. For example, a VIR can be used to implement a vector compress or expand function more efficiently. For example, when a vector comparison operation generates an index vector of selected elements, the selected components can be loaded in the VIR that can be used for addressing in the generation of the compressed vector. The elements in the VIR (or the elements in  $VMX(i)$ ) are address components for accessing non-continuous elements in vector  $V(i)$ . Instead of accessing  $V(i)$  through a single-entry index vector, where  $i = i + 1$  for each iteration, the vector processor can sequentially access  $V(VMX(i))$ , where  $i = i + 1$  for each iteration. Also, this way the components are only loaded once from the VIR for use by the vector processor. If a single-entry index vector is used, such as a vector first register is used, the element in the input vector is addressed by a counter that starts with the value in the single-entry index vector. To use the single-entry index register, each address is loaded sequentially from the index register. Again, with a VIR, each address or address component stored in the VIR is loaded at the same time only once. This creates a significant performance boost for the vector processor using a VIR.

**[0041]** In some embodiments, a counter (e.g., counter register) can drive the VIR. Also, a multiplexor, such as an N:1 multiplexor (i.e., multiple input single output multiplexor), can be used to selectively switch between outputs of the counter, to generate the output to access a certain position of the operand register for each vector

iteration, or the index coming out of VIR to access a certain position of the operand register for each iteration of the counter.

**[0042]** The aforesaid features and other features disclosed herein can be useful in conditional operations. For example, instead of generating the vector mask register for conditional operations on a vector, one of the circuits disclosed herein can generate one or more index vectors. Then, using the index vector(s), branches of a vector mask register can be evaluated via the corresponding VIR(s) respectively. The VIR(s) speed up the processing by the vector processor because the vector mask does not need to be generated or be iterated through, and the components of the mask do not need to be separately loaded per iteration.

**[0043]** Such functionality can also be useful for vector expand operations and/or merging the results of vector operations into a vector register. For example, a VIR can be used for indexing in operation  $B(\text{VMX}(i)) = A(i)$ , wherein “ $B(\text{VMX}(i))$ ” is expand compressed vector  $A$ . Also, a VIR can be used for indexing in operation  $B(\text{VMX}(i)) = A(i) + a$ , in which “ $B(\text{VMX}(i))$ ” is expand compressed vector  $A$  and a scalar value “ $a$ ” is added to expanded vector  $A$ . Also, a VIR can be used for indexing in operation  $B(\text{VMX}(i)) = \text{function}(A(\text{VMX}(i)), C(\text{VMX}(i)))$ , in which the processor preforms an operation on vectors  $A$  and  $C$  for elements selected through the VIR labeled “ $\text{VMX}$ ”. This is an example of conditional processing and can be used for nested conditional processing as well.

**[0044]** The index values or addressing components stored in a VIR (e.g., [2, 4, 5, 8] for accessing elements within an operand vector register (OVR) can be converted to memory addresses (e.g., the base address plus increments for each memory unit). Thus, the outputs described herein, such as the outputs from the multiplexors described herein can be converted to memory addresses for accessing vectors in main memory directly, in a way similar to accessing operand vector registers (OVRs).

**[0045]** FIG. 1 illustrates example parts of an example computing device 100, in accordance with some embodiments of the present disclosure. The device 100 can be communicatively coupled to one or more networks 112, as shown. The device 100 includes a vector processor 102 that is in accordance with some embodiments of the present disclosure. The device 100 also includes at least a bus 104, a main memory 106, a data storage system 108, and a network interface 110. The bus 104 communicatively couples the vector processor 102, the main memory 106, the data storage system 108, and the network interface 110. The device 100 includes a



computer system that includes at least vector processor 102, main memory 106 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), static random access memory (SRAM), etc.), and data storage system 108, which communicate with each other via bus 104 (which can include multiple buses).

**[0046]** To put it another way, FIG. 1 is a block diagram of an example device 100 having a computer system in which embodiments of the present disclosure can operate. In some embodiments, the computer system can include a set of instructions, for causing a machine to perform any one or more of the methodologies discussed herein, when executed. In such embodiments, the machine can be connected (e.g., networked via network interface 110) to other machines in a LAN, an intranet, an extranet, and/or the Internet (e.g., network(s) 112). The machine can operate in the capacity of a server or a client machine in client-server network environment, as a peer machine in a peer-to-peer (or distributed) network environment (such as the peer-to-peer networks described herein), or as a server or a client machine in a cloud computing infrastructure or environment.

**[0047]** Vector processor 102 represents one or more vector processors that are in accordance with some embodiments of the present disclosure. The vector processor 102 can include a microprocessor, a central processing unit, or the like. More particularly, the vector processor 102 can include a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, or a processor implementing other instruction sets, or processors implementing a combination of instruction sets, as long as the processor uses: vector instructions, vector registers, a vector first and multi-lane configuration. The vector processor 102 can also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), graphics processing unit (GPU), network processor, or the like. The vector processor 102 can be configured to execute instructions for performing the operations and steps discussed herein. The vector processor 102 can further include a network interface device such as network interface 110 to communicate over one or more communications network (such as network(s) 112).

**[0048]** The data storage system 108 can include a machine-readable storage medium (also known as a computer-readable medium) on which is stored one or more

sets of instructions or software and can embody at least some aspects of one or more of the methodologies or functions described herein. The data storage system 108 can include non-volatile storage. The instructions can also reside, completely or at least partially, within the main memory 106 and/or within the vector processor 102 during execution thereof by the computer system, the main memory 106 and the vector processor 102 also can constitute a machine-readable storage media. While the memory, vector processor, and data storage parts are shown in the example embodiment to each be a single part, each part should be taken to include a single part or multiple parts that can store the instructions and perform their respective operations. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present disclosure. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, optical media, and magnetic media.

**[0049]** FIG. 2 illustrates example parts of an example computing device 200, in accordance with some embodiments of the present disclosure. As shown, computing device 200 includes vector processor 102 as well as bus 104 and main memory 106 (e.g., see FIG. 1). Computing device 200 can also be or include computing device 100.

**[0050]** As shown in FIG. 2, vector processor 102 includes vector registers 202, scalar registers 204, bus 206, arithmetic logic units 208 (ALUs 208), and vector load-store unit 210. Other embodiments of the computing device 200 can include the scalar registers 204 being external to the vector processor 102 or in a separate unit of the vector processor from a unit in the vector processor having the vector registers 202. The bus 206 communicatively couples vector registers 202, scalar registers 204, arithmetic logic units (ALUs) 208, and vector load-store unit 210, and such components can communicate with each other via bus 206 (which can include multiple buses). Vector registers 202 include multiple vector registers. And, ALUs 208 include multiple ALUs--e.g., arithmetic logic unit (ALU) 0, ALU 1, and ALU N.

**[0051]** Vector processor 102 includes at least one vector index register. Vector processor 102 can be or include one or more central processing units (CPUs) that implement instructions that operate on one-dimensional arrays of data called vectors.

**[0052]** Vector registers 202 in the vector processor 102 can include operand vector

registers (i.e., input vector registers), result vector registers (i.e., output vector registers), and vector index registers that store values used for accessing elements in operand vector registers and/or result vector registers. The values in the accessed elements of operand vector registers and/or result vector registers can be used as input for ALUs such as one or more of the ALUs 208.

**[0053]** In general, the vector processor 102 can include index registers that can include scalar index registers and vector index registers such as the vector index registers illustrated in FIGS. 3, 4, and 5.

**[0054]** The scalar registers 204 of the vector processor 102 can include scalar index registers as well as operand scalar registers (i.e., input scalar registers) and result scalar registers (i.e., output scalar registers). At least some of the scalar registers can provide indexing and control values for many different types of operations on scalars and vectors. Also, scalar registers can also provide numerical values used by the vector instructions. For example, a vector provided by a vector register can be multiplied by a scalar provided by a scalar register.

**[0055]** At least some of the scalar registers 204 and the vector registers 202 can be connected to respective ALUs of the ALUs 208. An ALU of ALUs 208 can include a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. In the vector processor 102, an ALU of the ALUs 208 can be connected to input vector registers and in some instances output vector registers if the output vector register is providing feedback in an operation. In such instances the output vector register is both an input and output vector.

**[0056]** Also, the scalar registers 204 can include programable scalar registers. A programable scalar register can be used so that a vector provided by a vector register (e.g., one of the vector registers 202) can be operated on by a scalar provided by and programmed into one of the programable scalar registers. For example, one of the operations can include a vector multiplied by a scalar value (e.g., vector  $A(i)$  X scalar  $p$ ).

**[0057]** The bus 206 depicted can be configured to communicatively couple the vector load-store unit 210, the vector registers 202, the scalar registers 204, and the arithmetic logic units 208. The bus 206 can include a 2:1 multiplexor, 3:1 multiplexor, or a N:1 multiplexor configured to receive inputs from vector index registers and to output an address or address component for access of an operand vector. (e.g., see FIGS. 3, 4, and 5).

**[0058]** Vector load-store unit 210 includes circuitry for executing load and store instructions, generating addresses of load and store vector operations and loading data from memory or storing it back to memory from the registers of the vector processor 102. Vector load-store unit 210 can perform many of the operations described herein including many of the operations of methods 600, 700, 900, and 1000 in FIGS. 6-10.

**[0059]** Each of the computing devices described herein can be a machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while a single machine is illustrated for each of the illustrated computing devices of FIGS. 1 and 2, the term "machine" shall also be taken to include any collection of machines that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies or operations discussed herein. And, each of the illustrated computing devices can each include at least a bus and/or motherboard, one or more controllers (such as one or more CPUs), a main memory that can include temporary data storage, at least one type of network interface, a storage system that can include permanent data storage, and/or any combination thereof.

**[0060]** Before the discussion of the systems 300, 400, and 500 depicted in FIGS. 3, 4, and 5, it is important to understand that elements in a vector register can be addressed using at least an index coming out of a vector index register (VIR) or another type of register such as a counter register. In general, when a counter register is used, the counter adds 1 to itself for each iteration or step in a DO or FOR loop that generates the address for the next iteration or step. The VIR does not have to be driven by a counter, but it can be useful to have the VIR driven by a counter. A common counter can do both of driving the VIR and can provide a separate input to a receiving multiplexor that outputs an address component for use in accessing an operand vector in a vector operation.

**[0061]** For example, a VIR can store a vector VMX, where  $VMX(i)$ , and  $i = 0, 1, \dots, n-1$ . A simple example of an application of use of the VIR would be a compress operation such as  $B(i) = A(VMX(i))$ . Also, when another vector register stores a vector A, its elements are  $A(i)$ , where  $i = 0, 1, 2, \dots, n$ . In a regular mode (such as when the counter output is selected for use by a multiplexor), the processor can do  $A + a$ , where "a" is a scaler from the counter via the multiplexor. The result is stored in an output vector register B, where  $B(i) = A(i) + a$ , and where  $i = 0, 1, \dots, n-1$ . In the mode using

the VIR (e.g., an alternative selection control of the multiplexor), the processor can do  $A(\text{VMX}) + a$  by using the addresses generated from the output of the VIR. Thus, the output vector register has  $B$ , where  $B(i) = A(\text{VMX}(i)) + a$ , and where  $i=0, 1, \dots, n-1$ . Also, for example, the vector processor can be configured to operate on two vectors, e.g.,  $B(i) = \text{function}(A(\text{VMX}(i)), C(\text{VMX}(i)))$ , where the "function" is implemented via an ALU.

**[0062]** FIG. 3 illustrates an example system 300 including a vector index register 302, in accordance with some embodiments of the present disclosure.

**[0063]** The system 300 can be a part of vector processor 102 (e.g., see FIG. 1 or 2) or multiple vector processors. System 300 includes the vector index register 302 (VIR 302), a counter register 304, a 2:1 multiplexor 306, and a select register 308 connected to the multiplexor. The VIR 302 can be one of the vector registers 202 shown in FIG. 2. The counter register 304 and the select register 308 can be registers of the scalar registers 204. The 2:1 multiplexor 306 can be a part of the bus 206 shown in FIG. 2 or the bus 104 shown in FIG. 1.

**[0064]** The system 300 can be part of a vector processor that includes an arithmetic logic unit (ALU) of a plurality of arithmetic logic units (ALUs). The vector processor can also include an operand vector register (OVR) of a plurality of operand vector registers. The OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU.

**[0065]** The VIR 302 can be configured to store a plurality of address components corresponding to a plurality of positions in the OVR. Each address component can be addable to an effective address for accessing a corresponding position in the OVR. Each position of the OVR can include an element of the operand vector to be operated upon by the ALU.

**[0066]** In some embodiments, an example OVR can be 64 bits in length. If an operand is less than 64 bits (for example a 32-bit integer) that operand can be right justified. In such an example, the indexing techniques described herein are similarly applied. For example, the OVR can include padding in its elements to accommodate different data types.

**[0067]** As shown, the counter register 304 is part of the system 300. The counter register 304 can also be a part of the vector processor having the system 300. The counter register 304 can be configured to store a count 310. The count 310 can be addable to an effective address for accessing the OVR or the count can be used by

the vector processor for iterating on the plurality of address components stored in the VIR 302.

**[0068]** As shown, the 2:1 multiplexor 306 is part of the system 300. The 2:1 multiplexor 306 can also be a part of the vector processor having the system 300. The 2:1 multiplexor 306 can be configured to receive, as inputs, the count 310 from the counter register 304 and an output 312 from the VIR 302. The output 312 from the VIR 302 can include one of the plurality of address components of the VIR corresponding to the count 310. The 2:1 multiplexor 306 can also be configured to receive, as a selection input, a mode value 314. The mode value 314 can be or include a value for selection of the count 310 or a value for selection of the output 312 from the VIR 302. The 2:1 multiplexor 306 can also be configured to select either the count 310 or the output 312 from the VIR 302 according to the received mode value 314. The 2:1 multiplexor 306 can also be configured to output and communicate, via a bus (such as one of the buses of FIG. 1 or 2), a selection output 316 that is one of the selected count or the selected output from the VIR. The selection output 316 can be communicated to a requester accessing the OVR for the ALU. The requester can be a vector load-store unit of the vector processor (e.g., see vector load-store unit 210 shown in FIG. 2), or a vector load-store unit of another vector processor.

**[0069]** When the requester is a vector load-store unit it can be configured to generate effective addresses of load and store operations of the vector processor. The vector load-store unit can also be configured to, for each address component of the VIR, add the address component of the VIR to an effective address for accessing a corresponding position in the OVR.

**[0070]** FIG. 4 illustrates an example system 400 including vector index registers 402a, 402b, and 402c, in accordance with some embodiments of the present disclosure.

**[0071]** The system 400 can be a part of vector processor 102 (e.g., see FIG. 1 or 2) or multiple vector processors. System 400 includes multiple vector index registers including the vector index registers 402a, 402b, and 402c (VIRs 402a, 402b, and 402c). The system 400 also includes a counter register 404, a N:1 multiplexor 406, and a select register 408 connected to the multiplexor. The VIRs 402a, 402b, and 402c can be vector registers of the vector registers 202 shown in FIG. 2. The counter register 404 and the select register 408 can be registers of the scalar registers 204. The N:1 multiplexor 406 can be a part of the bus 206 shown in FIG. 2 or the bus 104

shown in FIG. 1. The N:1 multiplexor 406 is a multiplexor that can receive at least four inputs as shown. But, in some embodiments, the multiplexor 406 can receive much more than four inputs. The N:1 multiplexor 406 outputs one output which can be an address component used for accessing an operand vector register (OVR).

**[0072]** The system 400 can be part of a vector processor that includes an ALU ALUs. The vector processor can also include an OVR of OVRs. The OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU.

**[0073]** The VIRs 402a, 402b, and 402c each can be configured to store a plurality of address components corresponding to a plurality of positions in the OVR or three separate OVRs, for example. In an example with multiple OVRs there can be a separate multiplexor for each OVR. Also, in an example with multiple OVRs there can be a separate addressing system, such as system 300, for each OVR. Each address component of the multiple VIRs (e.g., VIRs 402a, 402b, and 402c) can be addable to an effective address for accessing a corresponding position in the OVR or multiple OVRs. Each position of the OVR(s) can include an element of the operand vector to be operated upon by the ALU.

**[0074]** As shown, the counter register 404 is part of the system 400. The counter register 404 can also be a part of the vector processor having the system 400. The counter register 404 can be configured to store a count 410. The count 410 can be addable to an effective address for accessing one or more OVRs or the count can be used by the vector processor for iterating on the plurality of address components stored in multiple VIRs (e.g., VIRs 402a, 402b, and 402c).

**[0075]** As shown, the N:1 multiplexor 406 is part of the system 400. The N:1 multiplexor 406 can also be a part of the vector processor having the system 400. The N:1 multiplexor 406 can be configured to receive, as inputs, the count 410 from the counter register 404 and outputs (e.g., outputs 412a, 412b, and 412c) from multiple VIRs (e.g., VIRs 402a, 402b, and 402c). Outputs 412a, 412b, and 412c from the VIRs 402a, 402b, and 402c each can include one of the plurality of address components of the respective VIR corresponding to the count 410. The N:1 multiplexor 406 can also be configured to receive, as a selection input, a mode value 414. The mode value 414 can be or include a value for selection of the count 410 or a value for selection of the outputs 412a, 412b, and 412c from the VIRs 402a, 402b, and 402c, for example. The N:1 multiplexor 406 can also be configured to select either the count 410 or the outputs

412a, 412b, and 412c from the VIRs 402a, 402b, and 402c according to the received mode value 414. The N:1 multiplexor 406 can also be configured to output and communicate, via a bus (such as one of the buses of FIG. 1 or 2), a selection output 416 that is one of the selected count or the selected output from the VIRs. The selection output 416 can be communicated to a requester accessing the OVR or multiple OVRs for the ALU or multiple ALUs. The requester can be a vector load-store unit of the vector processor (e.g., see vector load-store unit 210 shown in FIG. 2), or a vector load-store unit of another vector processor. When the requester is a vector load-store unit it can be configured to generate effective addresses of load and store operations of the vector processor. The vector load-store unit can also be configured to, for each address component of the VIRs, add the address component to an effective address for accessing a corresponding position in the OVR(s).

**[0076]** In some embodiments, a vector processor having multiple VIRs can include a counter configured to store a count and the count is addable to an effective address for accessing the OVR or wherein the count is for iterating on each respective plurality of address components stored in the VIRs. In such examples, the processor can also include a N:1 multiplexor configured to receive, as inputs, the count from the counter and respective outputs from the VIRs. Each output from a given VIR of the VIRs can include one of a plurality of address components of the given VIR corresponding to the count. The multiplexor can also be configured to receive, as a selection input, a mode value. The mode value can be a value for selection of the count or a value for selection of one of the respective outputs from the VIRs. The multiplexor can also be configured to select either the count or one of the respective outputs from the VIRs according to the received mode value. The multiplexor can also be configured to communicate the selected count or selected one of the respective outputs from the VIRs to a requester (e.g., such as vector load-store unit of the vector processor) accessing the OVR for the ALU.

**[0077]** FIG. 5 illustrates an example system 500 including a vector index register 502, in accordance with some embodiments of the present disclosure.

**[0078]** The system 500 can be a part of vector processor 102 (e.g., see FIG. 1 or 2) or multiple vector processors. System 500 includes the vector index register 502 (VIR 502), a counter register 504, a 3:1 multiplexor 506, and a select register 508 connected to the multiplexor. System 500 also includes the vector first register 503 connected to the multiplexor 506. The VIR 502 can be one of the vector registers 502



shown in FIG. 2. The counter register 504, the select register 508, and the vector first register 503 (VFR 503) can be registers of the scalar registers 204. The 3:1 multiplexor 506 can be a part of the bus 206 shown in FIG. 2 or the bus 104 shown in FIG. 1.

**[0079]** The system 500 can be part of a vector processor that includes an arithmetic logic unit (ALU) of a plurality of arithmetic logic units (ALUs). The vector processor can also include an operand vector register (OVR) of a plurality of operand vector registers. The OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU. The VIR 502 can be configured to store a plurality of address components corresponding to a plurality of positions in the OVR. Each address component can be addable to an effective address for accessing a corresponding position in the OVR. Each position of the OVR can include an element of the operand vector to be operated upon by the ALU.

**[0080]** The VFR 503 can be configured to store a single address component 511. The single address component 511 is an address component that directs initial access of the OVR at an initial position of the OVR based on the single address component 511 such that the initial position accessed is not the first position of the OVR. For example, if the VFR 503 stores the scalar “3”, then a fourth position of the OVR is initially accessed during a vector operation of the OVR. This is instead of starting access of the OVR at the first position of the OVR (e.g., OVR(0)).

**[0081]** As shown, the counter register 504 is part of the system 500. The counter register 504 can also be a part of the vector processor having the system 500. The counter register 504 can be configured to store a count 510. The count 510 can be addable to an effective address for accessing the OVR or the count can be used by the vector processor for iterating on the plurality of address components stored in the VIR 502. Also, the count 510 can be used by the vector processor for incrementing the single address component 511 of the VFR 503 or as shown, it can be added to the single address component 511 and the summation of the count 510 and the single address component 511 is vector first address component 513.

**[0082]** As shown, the 3:1 multiplexor 506 is part of the system 500. The 3:1 multiplexor 506 can also be a part of the vector processor having the system 500. The 3:1 multiplexor 506 can be configured to receive, as inputs, the count 510 from the counter register 504 and an output 512 from the VIR 502 as well as the vector first address component 513 of the summation of the output of the VFR 503 and the

counter 504. The output 512 from the VIR 502 can include one of the plurality of address components of the VIR corresponding to the count 510. The 3:1 multiplexor 506 can also be configured to receive, as a selection input, a mode value 514. The mode value 514 can be or include a value for selection of the count 510 or a value for selection of the output 512 from the VIR 502 or a value for selection of the vector first address component 513 of the summation of the output of the VFR 503 and the counter 504. The 3:1 multiplexor 506 can also be configured to select either the count 510 or the output 512 from the VIR 502 or the vector first address component 513 according to the received mode value 514. The 3:1 multiplexor 506 can also be configured to output and communicate, via a bus (such as one of the buses of FIG. 1 or 2), a selection output 516 that is one of the selected count or the selected output from the VIR or the vector first address component 513. The selection output 516 can be communicated to a requester accessing the OVR for the ALU. The requester can be a vector load-store unit of the vector processor (e.g., see vector load-store unit 210 shown in FIG. 2), or a vector load-store unit of another vector processor. When the requester is a vector load-store unit it can be configured to generate effective addresses of load and store operations of the vector processor. The vector load-store unit can also be configured to, for each address component of the VIR, add the address component of the VIR to an effective address for accessing a corresponding position in the OVR.

**[0083]** In some embodiments, a vector processor having at least one VIR can also include at least one VFR as well as at least one respective counter connected to the VIR and the VFR. The counter can be configured to store a count. The count can be addable to an effective address for accessing the OVR. The count can be for incrementing the vector first address component, or the count is for iterating on the plurality of address components stored in the VIR. The vector processor can also include a 3:1 multiplexor configured to receive, as inputs, the count from the counter, an output from the VFR, and an output from the VIR. The output from the VIR can include one of the plurality of address components of the VIR corresponding to the count, and the vector first address component can correspond to the count too. The multiplexor can be configured to receive, as a selection input, a mode value. The mode value can be a value for selection of the count, a value for selection of the output from the VFR, or a value for selection of the output from the VIR. The multiplexor can be configured to select either the count, the output from the VFR, or the output from

the VIR according to the received mode value, and to communicate the selected count, the selected output from the VFR, or the selected output from the VIR to a requester (e.g., such as vector load-store unit of the vector processor) accessing the OVR for the ALU.

**[0084]** Not shown in FIGS. 3-5, the systems can include respective vector length registers for each VIR of the VIRs. Each respective vector length register can be configured to store a length of a vector stored in a corresponding VIR. For example, the system 300 can include a vector length register (VLR) configured to store a length of a vector stored in the VIR. The VLRS can be useful in some operations leveraging the use of VIRs for address generation in vector operations.

**[0085]** In some embodiments, the result of the summation of the output of a counter and the output of an alternative address candidate can be multiplexed with the output of a VIR and/or the counter (e.g., see the vector first address component 513 in FIG. 5, which is the summation of the output of the counter 504 and the single address component 511 stored in the VFR 503). Alternatively, the alternative address candidate (e.g., the address component stored in VFR 503) can be used to set the initial value of a counter. The counter set by the alternative address candidate, in the alternative embodiment, is a separate counter from a counter driving a VIR.

**[0086]** In some embodiments, a vector processor having one of the systems 300, 400, or 500 can further include a vector load-store unit configured to generate effective addresses of load and store operations of the vector processor. The vector load-store unit can also be configured to, for each address component of a VIR, add the address component of the VIR to an effective address for accessing a corresponding position in an OVR. The effective address and the values in the VLR can be used by some vector operations to enhance the performance of the operations.

**[0087]** In some embodiments, a vector load-store unit connected to one of the systems 300, 400, or 500 is configured to load an operand vector stored in the OVR as well as load a scalar stored in a scalar register. Such a vector load-store unit can also be configured to compare elements of the loaded operand vector with the loaded scalar as well as store, in the VIR, positions of the elements of the loaded operand vector according to the comparison. For example, the vector load-store unit can also be configured to store position of the elements that match a scalar, store position of the elements that are greater than the scalar, or store position of the elements that are greater than or equal to the scalar. Also, for example, vector load-store unit can be

configured to store the positions of the elements that are even, and not store those that are odd, or vice versa.

**[0088]** The vector load-store unit connected to one of the systems 300, 400, or 500 can also be configured to load, from the VIR, the stored positions of the elements of the loaded operand vector. And, the vector load-store unit can be configured to iterate a vector operation over the elements of the loaded operand vector according to the loaded positions stored in the VIR.

**[0089]** In some embodiments, the vector operation is a compress operation configured to store the elements of the loaded operand vector into an output OVR that correspond to the loaded positions stored in the VIR.

**[0090]** In some embodiments, the vector load-store unit can be configured to load the stored elements from the output OVR, and then iterate a second vector operation over the stored elements from the output OVR according to the loaded positions stored in the VIR. The second vector operation can be an expand operation configured to store the elements from the output OVR into a second output OVR at positions of the second output OVR according to the loaded positions stored in the VIR. The expand operation can also be further configured to store a scalar into the second output OVR at other positions of the second output OVR.

**[0091]** In some embodiments, the vector load-store unit can be configured to iterate a second compress operation over elements of a second loaded operand vector according to loaded positions stored in a second VIR. In such embodiments, the vector load-store unit can be configured to store the elements of the second loaded operand vector into a second output OVR that correspond to the loaded positions stored in the second VIR. And, the vector load-store unit can be configured to perform one or more vector operations using the elements from the first output OVR and the second output OVR.

**[0092]** In some embodiments, vector load-store unit can be configured to perform one or more vector operations using the elements from the first output OVR and/or the second output OVR and elements of a third operand vector stored in a third OVR that is sequentially accessed and was not generated by indexing of a VIR. The results of the operation(s) can be stored in a fourth OVR sequentially.

**[0093]** As mentioned the systems 300, 400, and 500 can be a part of one or more vector processors. The systems 300, 400, and 500 can also be sub-systems of a greater system of one or more vector processors.

**[0094]** For example, the systems 300, 400, and 500 can be included in another system or connected to another system of one or more vector processors. Such a system may also not be a part of a vector processor.

**[0095]** Disclosed herein is also a system that can include an ALU of a plurality of ALUs. The system can also include an OVR of a plurality of operand vector registers (OVRs). The OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU. The system can also include a VIR of a plurality of vector index registers (VIRs). The VIR can be configured to store a plurality of address components corresponding to a plurality of positions in the OVR. Each address component can be addable to an effective address for accessing a corresponding position in the OVR. And, each position of the OVR can include an element of the operand vector to be operated upon by the ALU.

**[0096]** The system can also include a counter (or a counter register). The counter can be configured to store a count. The count is at least addable to an effective address for accessing the OVR or for iterating on the plurality of address components stored in the VIR.

**[0097]** The system can also include a N:1 multiplexor. In other words, the system, can include a multiplexor with multiple inputs and one output. The N:1 multiplexor can be configured to receive, as inputs, at least the count from the counter and an output from the VIR. The output from the VIR can include one of the plurality of address components of the VIR corresponding to the count. The N:1 multiplexor can also be configured to receive, as a selection input, a mode value, the mode value being at least a value for selection of the count or a value for selection of the output from the VIR. The N:1 multiplexor can also be configured to select at least either the count or the output from the VIR according to the received mode value. The N:1 multiplexor can also be configured to output and communicate the selection to a vector load-store unit accessing the OVR for the ALU.

**[0098]** In some embodiments, the count can also be for incrementing an address component of a scalar index register for accessing the OVR. In such examples, the N:1 multiplexor can be further configured to receive, as inputs, at least the count from the counter, an output from the VIR, and an output from the scalar index register. The N:1 multiplexor can also be further configured to receive, as a selection input, a mode value, the mode value being at least a value for selection of the count, a value for selection of the output from the VIR, or a value for selection of the output from the

scalar index register. The N:1 multiplexor can also be further configured to select at least either the count, the output from the VIR, or the output from the scalar index register, according to the received mode value.

**[0099]** In some embodiments, the scalar index register can be a vector first register (VFR). The VFR can be configured to store a vector first address component. The vector first address component can be an address component that directs initial access of the OVR at an initial position of the OVR based on the vector first address component such that the initial position accessed is not the first position of the OVR. The VFR can be used to access an OVR initially at any position of the OVR based on the value stored in the VFR.

**[00100]** In some embodiments, the count can also be for iterating on a plurality of address components stored in a second VIR of the VIRs. In such examples, the N:1 multiplexor can be configured to receive, as inputs, at least the count from the counter, an output from the VIR, and an output from the second VIR. Also, the N:1 multiplexor can be configured to receive, as a selection input, a mode value, the mode value being at least a value for selection of the count, a value for selection of the output from the VIR, or a value for selection of the output from the second VIR. And, the N:1 multiplexor can be configured to select at least either the count, the output from the VIR, or the output from the second VIR, according to the received mode value.

**[00101]** FIGS. 6-10 illustrate example operations, in accordance with some embodiments of the present disclosure. In some embodiments, a vector load-store unit, such as vector load-store unit 210, can perform or facilitate, solely or in combination with other parts of the vector processor, many or all of the operations illustrated in FIGS. 6-10. In some embodiments, storing, loading, determinations, incrementations, and changes to values describe herein can be performed by a vector load-store unit of the vector processor according to instructions stored in the vector load-store unit. In some other embodiments, other parts of the vector processor can perform or facilitate the operations illustrated in FIGS. 6-10 as well as other operations described herein.

**[00102]** In general, the systems described herein can implement many functions including vector compress and expand functions. For example, in a list of address components stored in a VIR, such as VMX, the elements of a given vector A can be compressed into a new vector by reading the elements  $A(\text{VMX}(i))$  out of the vector A and store into the output vector B(i). Thus, vector A is compressed into B by  $B(i) =$

$A(\text{VMX}(i))$ , for  $i=0, 1, \dots n$ . Similarly, the expand can be done in reverse (e.g.,  $B(\text{VMX}(i)) = A(i)$ ). Further, one or more VIRs can allow the vector processor to perform sparse operations directly, with or without compress and/or expand. For example, a VIR can implement indexing in  $B(i) = \text{function}(A(\text{VMX}(i)), C(\text{VMX}(i)))$ , which can be a sparse operation with compress. Also, a VIR can implement indexing in  $B(\text{VMX}(i)) = \text{function}(A(\text{VMX}(i)), C(\text{VMX}(i)))$ , which can be a sparse operation without compress. Also, a VIR can implement indexing in  $B(\text{VMX}(i)) = \text{function}(A(i), C(i))$ , which can be an operation on compressed vectors with expand.

**[00103]** FIG. 6 illustrates example operations of method 600 for accessing elements of an operand vector for one or more vector operations, in accordance with some embodiments of the present disclosure.

**[00104]** In FIG. 6, the method 600 begins at step 602, with storing, in an operand vector register (OVR) of a plurality of operand vector registers (OVRs) in a vector processor, elements of an operand vector to be used as input for a vector operation of an arithmetic logic unit (ALU) of a plurality of arithmetic logic units (ALUs) in the vector processor. The storing of the elements of the operand vector in the OVR can occur any time before it is used as input for the vector operation of the ALU. For example, the step 602 can occur after step 618.

**[00105]** At step 604, the method 600 continues with storing, in a vector index register (VIR) of a plurality of vector index registers (VIRs) in the vector processor, a plurality of address components corresponding to a plurality of positions in the OVR.

**[00106]** At step 606, the method 600 continues with iterating on the plurality of address components stored in the VIR according to a count (such as a count stored in a counter register), to provide an output. Subsequently the vector load-store unit adds an output from the VIR to the effective address for accessing the OVR. The output from the VIR can include one of the plurality of address components of the VIR corresponding to the count. A single iteration over the plurality of address components stored in the VIR according to the count can occur each time the vector load-store unit requests an output from the VIR for adding the output of the VIR to the effective address for accessing the OVR. This can occur repeatedly until the VIR has been iterated through for an operation on the OVR.

**[00107]** At step 608, the method 600 continues with receiving, by a N:1 multiplexor of the vector processor, at least the count from the counter and an output from the VIR, wherein the output from the VIR can include one of the plurality of address

components of the VIR corresponding to the count.

**[00108]** At step 610, the method 600 continues with receiving, by the N:1 multiplexor, a selection input including a mode value, the mode value being at least a value for selection of the count or a value for selection of the output from the VIR.

**[00109]** At step 612, the method 600 continues with selecting, by the N:1 multiplexor, at least either the count or the output from the VIR according to the received mode value.

**[00110]** At step 614, communicating the selection to a vector load-store unit of the vector processor accessing the OVR for the ALU.

**[00111]** At step 616, the method 600 continues with adding a count stored in a counter to an effective address for accessing the OVR.

**[00112]** At step 618, the method 600 continues with adding an address component of the VIR to an effective address for accessing a corresponding position in the OVR. Each position of the OVR can include an element of the operand vector to be operated upon by the ALU.

**[00113]** At step 620, the method 600 continues with accessing the OVR for the ALU, by the vector load-store unit, according to the effective address generated at step 616 or 618.

**[00114]** FIG. 7 illustrates example operations of method 700 for compressing elements of an operand vector, in accordance with some embodiments of the present disclosure. In FIG. 7, the method 700 begins at step 702, with loading, by a vector load-store unit, an input operand vector stored in an input OVR.

**[00115]** At step 704, the method 700 continues with loading, by the vector load-store unit, the count stored in a counter register.

**[00116]** At step 706, the method 700 continues with loading from a VIR, by the vector load-store unit, a stored position of an element of the loaded input operand vector according to the count.

**[00117]** At step 708, the method 700 continues with running a vector compress operation over the elements of the loaded input operand vector according to the loaded position from the VIR. Step 708 includes step 710 that includes the method 700 continuing with storing the element of the loaded input operand vector into an output OVR that corresponds to the loaded position from the VIR.

**[00118]** At step 712, the method 700 continues with comparing the count to a value representing the vector length of the VIR (i.e., VL) such that the vector compress



operation can be iterated over the input OVR for each of the positions stored in the VIR. When the count equals the vector length of the VIR, then the method 700 ends. When the count is less than the vector length of the VIR, then the method 700 continues with incrementing the count at 714 and then returning to step 704 (loading the count stored in a counter register) which is followed by steps 706 (loading from a VIR, by the vector load-store unit, a stored position of an element of the loaded input operand vector according to the count) and 708 (running the vector compress operation over the elements of the loaded input operand vector according to the loaded position from the VIR). This way the vector compress operation is iterated over the input OVR for each of the positions stored in the VIR.

**[00119]** FIG. 8 illustrates an example system 800 including a vector index register 802 (VIR 802) being used for compressing elements of an input operand vector stored in an input OVR 804, in accordance with some embodiments of the present disclosure. Example system 800 is one example of a system that can implement at least method 700.

**[00120]** In FIG. 8, the VIR 802 stores a list of positions of the input OVR 804 (e.g., “2” as the input OVR’s first element, and “4” as the input OVR’s second element”). In this illustrated example, it is shown that the vector processor runs for two cycles or iterations of a vector compress operation. At the first iteration, counter 806 outputs the count of “0” which is the value stored in the counter at the first cycle. In the first cycle, VIR 802 is shown outputting “2”. The multiplexor 808 selects between the address component (“0”) as specified by the counter 806 in a normal mode operation or the address component (“2”) as specified by the VIR 802 in a VIR mode of operation (or a compress mode of operation in this specific example). When the VIR (or compress mode) is selected by the multiplexor 808 in the first cycle the output of “2” from the VIR 802 is the address component used for accessing the input OVR 804. As a result, the input OVR 804 is accessed for an output of element “C” at position “2” of the input OVR. The output OVR 810 is addressed directly through the count stored in the counter 806. Since the count of the counter 806 is “0” in the first cycle, the output ORV 810 stores “C” as its first element. In the next iteration or cycle, the output ORV 810 stores “E” as a second element at position “1” of the output OVR. In this example with two cycles show, the input OVR 804 having elements of {A, B, C, D, E} is compressed into the output OVR 810 having elements of {C, E}.

**[00121]** Also, in reference to FIG. 8, if the address signals for the input/output

vectors are reversed, {C, E} can be expanded into a second output OVR having element of {x, x, C, x, E} where x is the existing values before the compress operation or a scalar value selected from a scalar register (e.g., see FIG. 9 which is an example method expanding a compressed vector with a scalar value from a scalar register).

**[00122]** Further, if a value from a VFR is added to the count of the counter, the summation can be used so that the first iteration of an operation on the input OVR occurs at another position of the input OVR instead of the first position of the input OVR (e.g., the first position of input OVR 804 is labeled "0"). E.g., see FIG. 5. Alternatively, the VFR can be used to provide an input for the count register so that the initial value of the count register at the beginning of a vector operation is the value stored in the VFR. Such options allow for vector first processing.

**[00123]** FIG. 9 illustrates example operations of method 900 for expanding elements of an operand vector, such as elements of a compressed operand vector, in accordance with some embodiments of the present disclosure.

**[00124]** As shown in FIG. 9, the method 900 can begin with method 700, which concludes with an output of a compressed operand vector stored in the output OVR. Next, the method 900 continues at step 902, with loading, by the vector load-store unit, the stored elements from the output OVR. The stored elements being elements of a compressed vector.

**[00125]** At step 904, the method 900 continues with iterating a second vector operation over the stored elements from the output OVR according to the loaded positions stored in the VIR. The second operation is a vector expand operation. In other words, the second vector operation, being a vector expand operation, expands the compressed vector stored in the output OVR.

**[00126]** At step 906, the method 900 continues with storing, according to the expand operation, the elements from the output OVR into a second output OVR at positions of the second output OVR according to the loaded positions stored in the VIR.

**[00127]** At step 908, the method 900 continues with storing, according to the expand operation, a scalar into the second output OVR at other positions of the second output OVR. The final output of the expand operation after step 908 is an expanded vector with the elements from the compressed vector and one or more instances of the scalar value at other positions of the expanded vector. The positioning of the elements from the compressed vector in the expanded vector correspond to the loaded positions or address components stored in the VIR.

**[00128]** FIG. 10 illustrates example operations of method 1000 related to operations on multiple compressed vectors, in accordance with some embodiments of the present disclosure.

**[00129]** As shown in FIG. 10, the method 1000 can begin with method 700, which concludes with an output of a compressed operand vector stored in the output OVR. Also, analogous operations to method 700 are performed on a second operand vector. For example, at step 1002, the method 1000 continues with iterating a second compress operation over elements of a second loaded operand vector according to loaded positions stored in a second VIR.

**[00130]** At step 1004, the method 1000 continues with storing the elements of the second loaded operand vector into a second output OVR that correspond to the loaded positions stored in the second VIR.

**[00131]** At step 1006, the method 1000 continues with performing one or more vector operations using the elements from the first output OVR and the second output OVR. The one or more vector operations are using the elements from two compressed vectors, which are the elements from first output OVR and the second output OVR.

**[00132]** As mentioned herein, at least some of the embodiments disclosed herein are vector index registers in vector processors that each store multiple addresses for accessing multiple positions in vectors. Further, at least some of the embodiments disclosed herein are vector index registers for TRUE and/or FALSE results of one or more comparisons (such as numerical comparisons) that each store multiple addresses for accessing multiple positions in operand vectors.

**[00133]** Also, as mentioned herein, it is known to use a scalar index register in a vector processor to reference multiple positions of vectors by changing the value stored in the scalar index register during a vector operation. However, by using a vector indexing register (VIR), such as a VIR for TRUE results or a VIR for FALSE results, for indexing multiple positions of one or more operand vectors, the scalar index register can be replaced and at least the continual changing of values in the scalar index register during a vector operation using TRUE and/or FALSE results can be avoided.

**[00134]** As mentioned herein, there are many limitations associated with using a scalar register or single-entry vector for indexing a vector. And, some of these limitations can curb the performance of a vector processor using the scalar index

register. By using a vector indexing register, such as a VIR for TRUE results or a VIR for FALSE results, for indexing a plurality of positions of one or more operand vectors used in vector comparison operations or other types of operations, the scalar index register can be replaced and at least the continual changing of the scalar index register during a vector operation can be avoided.

**[00135]** In some embodiments, when a vector of TRUE and FALSE elements is computed (e.g., the contents of vector mask,  $V_m$ ), a system or circuit can generate an index vector to compliment or replace the vector. The index vector can be for TRUE results or FALSE results or a combination thereof, and these type of index vectors can be stored in respective vector index registers, VIR\_TRUE, VIR\_FALSE, and VIR\_COMBINED. The VIR\_COMBINED is a single VIR that includes a TRUE section and a FALSE section.

**[00136]** A VIR\_TRUE, VIR\_FALSE, and/or VIR\_COMBINED can include the elements in a vector mask ( $V_m$ ) or a corresponding OVR. A  $V_m$  is a vector that stores the TRUE and FALSE results of a comparison on a vector (such as a numerical comparison on a vector). The  $V_m$  can be used for conditional operations and compress and expand operations. A vector register for the  $V_m$  can be replaced by the VIR\_TRUE, VIR\_FALSE, and/or VIR\_COMBINED. And, the VIR\_TRUE, VIR\_FALSE, and/or VIR\_COMBINED can increase the performance of a vector processor in replacing a  $V_m$  when the vector processor performs vector operations.

**[00137]** For example, a counter can be used to track the number of TRUE elements in the computing of  $V_m$ , starting with zero. When the  $i$ th TRUE element is identified as the result of the  $j$ th element of  $V_m$ , the index  $j$  is saved into the  $i$ th element of vector  $V_{mxT}$  (and store in VIR\_TRUE). Similarly, a counter can be used to track the FALSE results and save the indices of the FALSE results in a vector  $V_{mxF}$  (and store in VIR\_FALSE). The sum of the vector lengths of  $V_{mxT}$  and  $V_{mxF}$  is equal to the vector length of  $V_m$ . The vector process can use  $V_i$  as the vector where  $i$ th element has the value  $I$  to generate  $V_{mxT}$  and  $V_{mxF}$ , wherein  $V_{mxT} = \text{compress}(V_i, V_m)$  and  $V_{mxF} = \text{compress}(V_i, !V_m)$ .

**[00138]** The compressed index or address vector  $V_{mxT}$  and/or  $V_{mxF}$  stored or loaded in VIR\_TRUE or VIR\_FALSE, can be used in conditional operations and/or for compress and expand operations (such as the compress and expand operations described herein). With the capability to access a vector with compressed index or address vectors, such operations can run directly on the vectors without having to

generate the compressed vector on an intermediate vector register such as a register for iterating through Vm.

**[00139]** As mentioned herein, the uses of a VIR, such as a VIR\_TRUE or VIR\_FALSE, are many. For example, a VIR\_TRUE or a VIR\_FALSE can be used to implement a vector compress or expand function more efficiently.

**[00140]** FIG. 11 illustrates example operations of method 1100 for building indexing vectors for storing in vector indexing registers for TRUE and FALSE results (e.g., “1” or “0” results) of a comparison (VIR\_TRUE and VIR\_FALSE), in accordance with some embodiments of the present disclosure.

**[00141]** The method 1100 begins at step 1102 with loading, by a vector load-store unit of a vector processor, an operand vector stored in an operand vector register (OVR).

**[00142]** At step 1104, the method 1100 continues with loading, by the vector load-store unit, a scalar stored in a scalar register of the vector processor.

**[00143]** At step 1106, the method 1100 continues with comparing, by the vector processor, an element of the loaded operand vector with the loaded scalar according to a count stored in a counter. The counter can be another scalar register and a part of the vector processor. Also, in some embodiments, the method 1100 can continue with comparing, by the vector processor, an element of the loaded operand vector with another operand vector according to a count stored in a counter. In some embodiments, for the comparison, the element of the loaded operand vector is accessed by the vector processor according to a first count in a first counter, and the element of the other loaded operand vector is accessed by the vector processor according to a second count in a second counter. The comparison can be a numerical comparison.

**[00144]** At step 1108, the method 1100 continues with identifying whether the result of the comparison of step 1106 is TRUE or FALSE (e.g., “1” or “0”). If the result of the comparison of step 1106 is TRUE, then the method 1100 continues at step 1110a with storing, in a vector index register for TRUE results of the comparison (VIR\_TRUE), a position of the element of the loaded operand vector according to the count (such as according to the count via a TRUE count stored in a TRUE counter—e.g., see TRUE counter 1216a depicted in FIG. 12). If the result of the comparison of step 1106 is FALSE, then the method 1100 continues at step 1110b with storing, in a vector index register for FALSE results of the comparison (VIR\_FALSE), a position

of the element of the loaded operand vector according to the count (such as according to the count via a FALSE count stored in a FALSE counter—e.g., see FALSE counter 1216b depicted in FIG. 12).

**[00145]** At step 1112, the method 1100 continues with identifying whether the count equals the vector length (VL) of the operand vector stored in the OVR. In some embodiments, the method 1100 can continue with identifying whether the VL of the OVR equals the result of adding the VL of the VIR\_TRUE and the VL of the VIR\_FALSE, which can be another way to identify whether the count equals the VL of the operand vector stored in the OVR. These example alternative ways of identifying whether the count equals the VL of the OVR can show that all the elements of the OVR are compared. If the count is less than the VL, then the method continues at step 1114 with incrementing the count. By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_TRUE or the VIR\_FALSE. In other words, the method 1100 continues the storing of positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_TRUE or the VIR\_FALSE.

**[00146]** At step 1112, if the count is equal to the VL, then the method 1100 has completed the building of indexing vectors for storing in VIR\_TRUE and VIR\_FALSE. The count cannot be greater than the VL because the operation of building the indexing vectors is complete upon the count being equal to the VL. When new indexing vectors are to be built, the count is reset and a VL register storing the scalar value of the VL can be reset as well. The vector processor can initially determine the vector length of an OVR and then store the length in the VL register before performing method 1100.

**[00147]** Upon completion of the building of indexing vectors which are stored in VIR\_TRUE and VIR\_FALSE, the method 1100 continues, at step 1116, with loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by the vector load-store unit, stored positions of the elements of the loaded operand vector. And, at step 1118, the method 1100 continues with iterating one or more vector operations over the elements of the loaded operand vector according to the loaded positions.

**[00148]** FIG. 12 illustrates an example system 1200 for building indexing vectors for

storing in VIR\_TRUE 1202a and VIR\_FALSE 1202b, in accordance with some embodiments of the present disclosure. The system 1200 can implement many of the operations and aspects of method 1100 and the system 1200 can be a part of one or more vector processors.

**[00149]** The system 1200 includes the VIR\_TRUE 1202a and VIR\_FALSE 1202b, such as the VIR\_TRUE and VIR\_FALSE described in the description of method 1100. The system also includes an OVR 1204, such as the OVR described in the description of method 1100.

**[00150]** The system 1200 also includes a scalar register (SR) 1206, such as the scalar register described in the description of method 1100. In some embodiments, the scalar register can be replaced with another OVR addressed in a same way as the OVR 1204.

**[00151]** The system also includes a counter 1208, which can be partially implemented by a counter register and can be the counter described in the description of the method 1100.

**[00152]** The system 1200 also includes a comparator 1210 that can perform a comparison of the value stored in the SR 1206 and a value stored in an element of the OVR 1204. The comparator 1210 can perform comparisons such as  $OVR(i) < SR$ ,  $OVR(i) = SR$ ,  $OVR(i) > SR$ ,  $OVR(i) \leq SR$ , or  $OVR(i) \geq SR$ . The comparator 1210 compares two numbers at a time or per cycle. At each iteration  $i$  (which also represents address or address component  $i$ ), the counter 1208 provides address  $i$  for accessing the OVR 1204 for the comparison with the scalar value from SR 1206 by the comparator 1210. In short, the output of OVR 1204 at iteration or address  $i$  is compared with the value from the scalar register 1206. The comparator 1210 generates a single output, which is either TRUE or FALSE (e.g., "1" or "0").

**[00153]** The comparator 1210 can be configured to perform the comparison at step 1106 of method 1100. In other words, the comparator 1210 can be configured to compare an element of a loaded operand vector with a loaded scalar according to a count stored in a counter register. The comparator 1210 can also be configured to perform the identification of a TRUE or FALSE result at step 1108. In other words, the comparator 1210 can be configured to identify whether the result of the comparison of step 1106 is TRUE or FALSE. The comparator 1210 can be configured to output a TRUE or FALSE result, such as a "1" for a TRUE result or a "0" for a FALSE result. The output of the comparator 1210 is inputted into a respective write enable for each

of the VIR\_TRUE 1202a and the VIR\_FALSE 1202b.

**[00154]** The output from the comparator 1210 can be communicated directly to the write enable 1212a for the VIR\_TRUE 1202a. The output from the comparator 1210 can be communicated indirectly to the write enable 1212b for the VIR\_FALSE 1202b, via an inverter 1214. The inverter 1214 is configured to invert the output of comparator 1210 before it reaches the write enable 1212b for the VIR\_FALSE 1202b. For example, if the output of the comparator 1210 is TRUE (e.g., "1"), then when it is inputted into the inverter 1214 the inverter inverts the value to FALSE (e.g., "0") and outputs FALSE.

**[00155]** The system 1200 also includes a separate TRUE counter 1216a for the VIR\_TRUE 1202a and a separate FALSE counter 1216b for the VIR\_FALSE 1202b. The output of the comparator 1210 drives the two counters, counters 1216a and 1216b. The counters 1216a and 1216b are separate from the counter 1208 that provides the address for the OVR 1204. Output of TRUE counter 1216a is used as the address for accessing VIR\_TRUE 1202a. Output of FALSE counter 1216b is used as the address for accessing VIR\_FALSE 1202b.

**[00156]** For example, when the output of the comparator 1210 is TRUE, the output triggers write enable 1212a to write the current position from the OVR 1204 into the VIR\_TRUE 1202a. When the output of the comparator 1210 is FALSE, the output triggers write enable 1212b to write the current position from the OVR 1204 into the VIR\_FALSE 1202b. This functionality is provided via the circuit including the inverter 1214 and the two write enables 1212a and 1212b.

**[00157]** The output of counter 1208 is used as the address or address component to be written into VIR\_TRUE 1202a at an address specified by the TRUE counter 1216a. This occurs when the output of the comparator 1210 is TRUE. The value stored in counter TRUE 1216a is increased by one for each triggering TRUE output from the comparator 1210. The output of counter 1208 is used as the address or address component to be written into VIR\_FALSE 1202b at an address specified by the FALSE counter 1216b. This occurs when the output of the comparator 1210 is FALSE. The value stored in FALSE counter 1216b is increased by one for each triggering FALSE output from the comparator 1210. This overall functionality of selecting where to store the addresses of the OVR components is provided by the circuit including the comparator 1210, the write enables 1212a and 1212b, the inverter 1214, and the TRUE and FALSE counters 1216a and 1216b.



**[00158]** The VIR\_TRUE 1202a and the VIR\_FALSE 1202b each are an output register of the system 1200. The VIR\_TRUE 1202a has three inputs. The first input is from write enable 1212a. For example, the input of TRUE from this first input allows writing into the VIR\_TRUE 1202a and FALSE disallows writing into the register. The second input is from the TRUE counter 1216a, which is for the address of accessing VIR\_TRUE 1202a. The third input is from the counter 1208 and this input includes the data written into the VIR\_TRUE 1202a at the address of the register provided by the TRUE counter 1216a (or the second input).

**[00159]** The system 1200 can be a part of a vector processor that includes a vector load-store unit. The vector load-store unit can load data stored in the registers of the system 1200 to main memory as well as store data from main memory to the registers of the system, and vice versa (load data stored in memory to the registers of system 1200 as well as store data from registers of the system to memory).

**[00160]** The system 1200 is also shown to include a scalar register for vector length, vector length register 1224 (VLR 1224). VLR 1224 is configured to store the vector length (VL) of the OVR 1204. A vector processor can load the VL into memory from VLR 1224 to identify whether the count from counter 1208 equals the VL of the operand vector stored in the OVR 1204. This is one way for example to implement step 1112 of method 1100 in FIG. 11. If the count is less than the VL, then the count in the counter 1208 continues to increment per clock cycle or another trigger or iteration (e.g., see step 1114). By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the OVR 1204 according to the count until the positions of the elements of the OVR are stored in the VIR\_TRUE 1202a or the VIR\_FALSE 1202b. In other words, the system 1200 can continue with the storing of positions of elements of the OVR 1204 according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_TRUE 1202a or the VIR\_FALSE 1202a. This is one of the ways that the system 1200 can implement operations of the method 1100.

**[00161]** If the count is equal to the VL, then the vector processor using system 1200 has completed the building of indexing vectors for storing in VIR\_TRUE 1202a and VIR\_FALSE 1202b. The count cannot be greater than the VL because the operation of building the indexing vectors is complete upon the count being equal to the VL. When new indexing vectors are to be built, the count is reset in counter 1208 and VL is determined and stored in VLR 1224. The vector processor can initially determine

the vector length of an OVR (e.g., the OVR 1204) and then store it in the VLR 1224 before performing method 1100.

**[00162]** Upon completion of the building of indexing vectors which are stored in VIR\_TRUE 1202a and VIR\_FALSE 1202b, the vector processor can continue with loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by a vector load-store unit of the processor, stored positions of the elements of the OVR 1204. And, the vector processor can also continue with iterating one or more vector operations over the elements of the OVR 1204 according to the loaded positions in the VIR\_TRUE 1202a and/or VIR\_FALSE 1202b.

**[00163]** An alternative to system 1200 is illustrated in FIG. 14 in which both the VIR\_TRUE and the VIR\_FALSE are essentially combined into one vector index register with the TRUE addresses of the OVR stored from the top down and the FALSE addresses of the OVR stored from the bottom up of the register. In such an alternative, counter for addressing the TRUE portion of the combined VIR starts with address "zero" and adds one for each TRUE input into the combined register. The FALSE counter starts with "N-1" for the address to access the combined VIR and the counter reduces by one for each FALSE input into the combined register. A multiplexor, as shown in FIG. 14 can be used to choose from either the counter for TRUE inputs or the counter for FALSE inputs. With each cycle, the VIR is enabled once for write because the input is either to the TRUE section (e.g., addresses 0, 1, 2, ..., count + 1, wherein count begins with "0"), or the FALSE section of the VIR (e.g., addresses N-1, N-2, N-3, ..., VIR\_length – count+1, wherein count begins with "0"); and thus, the index is generated from either the top down or the bottom up.

**[00164]** FIG. 13 illustrates example operations of method 1300 for building a combined indexing vector for storing in a combined vector indexing register for TRUE and FALSE results (e.g., "1" or "0" results) of a comparison (VIR\_combined), in accordance with some embodiments of the present disclosure.

**[00165]** The method 1300 begins at step 1302 with loading, by a vector load-store unit of a vector processor, an operand vector stored in an OVR.

**[00166]** At step 1304, the method 1300 continues with loading, by the vector load-store unit, a scalar stored in a scalar register of the vector processor.

**[00167]** At step 1306, the method 1300 continues with comparing, by the vector processor, an element of the loaded operand vector with the loaded scalar according to a count stored in a counter. The counter can be another scalar register and a part

of the vector processor. Also, in some embodiments, the method 1300 can continue with comparing, by the vector processor, an element of the loaded operand vector with another operand vector according to a count stored in a counter. In some embodiments, for the comparison, the element of the loaded operand vector is accessed by the vector processor according to a first count in a first counter, and the element of the other loaded operand vector is accessed by the vector processor according to a second count in a second counter. The comparison can be a numerical comparison.

**[00168]** At step 1308, the method 1300 continues with identifying whether the result of the comparison of step 1306 is TRUE or FALSE (e.g., “1” or “0”). If the result of the comparison of step 1306 is TRUE, then the method 1100 continues at step 1310a with storing, at the top-most unfilled position in VIR\_combined, position of the element of the loaded operand vector according to the count (such as according to the count via a TRUE count stored in a TRUE counter—e.g., see TRUE counter 1416a depicted in FIG. 14). If the result of the comparison of step 1306 is FALSE, then the method 1300 continues at step 1310b with storing, at the bottom-most unfilled position in VIR\_combined, position of the element of the loaded operand vector according to the count (such as according to the count via a FALSE count stored in a FALSE counter—e.g., see FALSE counter 1416b depicted in FIG. 14).

**[00169]** At step 1312, the method 1300 continues with identifying whether the count equals the vector length (VL) of the operand vector stored in the OVR. In some embodiments, the method 1300 can continue with identifying whether the VL of the OVR equals the result of adding the VL of the TRUE section of the VIR\_COMBINED and the FALSE section of the VIR\_COMBINED, which can be another way to identify whether the count equals the VL of the operand vector stored in the OVR. These example alternative ways of identifying whether the count equals the VL of the OVR can show that all the elements of the OVR are compared. If the count is less than the VL, then the method continues at step 1314 with incrementing the count. By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_combined. In other words, the method 1300 continues the storing of positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the

VIR\_combined.

**[00170]** At step 1312, if the count is equal to the VL, then the method 1300 has completed the building of the indexing vector for storing in VIR\_combined. The count cannot be greater than the VL because the operation of building the indexing vectors is complete upon the count being equal to the VL. When new indexing vectors are to be built, the count is reset and a VL register storing the scalar value of the VL can be reset as well. The vector processor can initially determine the vector length of an OVR and then store the length in the VL register before performing method 1300.

**[00171]** Upon completion of the building of the indexing vector which are stored in VIR\_combined, the method 1300 continues, at step 1316, with loading from the VIR\_combined, by the vector load-store unit, stored positions of the elements of the loaded operand vector. And, at step 1318, the method 1300 continues with iterating one or more vector operations over the elements of the loaded operand vector according to the loaded positions.

**[00172]** FIG. 14 illustrates an example system 1400 for building a combined indexing vector for storing in VIR\_combined 1402, in accordance with some embodiments of the present disclosure.

**[00173]** The system 1400 includes the VIR\_combined 1402, such as VIR\_combined 1402 described in the description of method 1300. The system also includes an OVR 1404, such as the OVR described in the description of method 1400.

**[00174]** The system 1400 also includes a scalar register (SR) 1406, such as the scalar register described in the description of method 1300. In some embodiments, the scalar register can be replaced with another OVR addressed in a same way as the OVR 1404.

**[00175]** The system also includes a counter 1408, which can be partially implemented by a counter register and can be the counter described in the description of the method 1300.

**[00176]** The system 1400 also includes a comparator 1410 that can perform a comparison of the value stored in the SR 1406 and a value stored in an element of the OVR 1404. The comparator 1410 can perform comparisons such as  $OVR(i) < SR$ ,  $OVR(i) = SR$ ,  $OVR(i) > SR$ ,  $OVR(i) \leq SR$ , or  $OVR(i) \geq SR$ . The comparator 1410 compares two numbers at a time or per cycle. At each iteration  $i$  (which also represents address or address component  $i$ ), the counter 1408 provides address  $i$  for accessing the OVR 1404 for the comparison with the scalar value from SR 1406 by

the comparator 1410. In short, the output of OVR 1404 at iteration or address *i* is compared with the value from the scalar register 1406. The comparator 1410 generates a single output, which is either TRUE or FALSE.

**[00177]** The comparator 1410 can be configured to perform the comparison at step 1306 of method 1300. In other words, the comparator 1410 can be configured to compare an element of a loaded operand vector with a loaded scalar according to a count stored in a counter register. The comparator 1410 can also be configured to perform the identification of a TRUE or FALSE result at step 1308. In other words, the comparator 1410 can be configured to identify whether the result of the comparison of step 1306 is TRUE or FALSE. The comparator 1410 can be configured to output a TRUE or FALSE result, such as a "1" for a TRUE result or a "0" for a FALSE result. The output of the comparator 1410 is inputted into one of the respective write enables for TRUE and FALSE sections of the VIR\_COMBINED 1402.

**[00178]** The system 1400 also includes a separate TRUE counter 1416a for the addressing of the TRUE section of VIR\_COMBINED 1402 and a separate FALSE counter 1416b for the addressing of the FALSE section of the VIR\_COMBINED. The output of the comparator 1410 drives the two counters, counters 1416a and 1416b. The counters 1416a and 1416b are separate from the counter 1408 that provides the address for the OVR 1404. Output of counter TRUE 1416a is used as the address for accessing VIR\_COMBINED 1402 from the top down. Output of FALSE counter 1416b is used as the address for accessing VIR\_COMBINED 1402 as well, but from the bottom up. Further explanation of how the counters address the VIR\_COMBINED 1402 is discussed below.

**[00179]** The output of counter 1408 is used as the address or address component to be written into the TRUE section at an address specified by the TRUE counter 1416a. This occurs when the output of the comparator 1410 is TRUE. The value stored in TRUE counter 1416a is increased by one for each triggering TRUE output from the comparator 1410. The output of counter 1408 is used as the address or address component to be written into the FALSE section at an address specified by the FALSE counter 1416b. This occurs when the output of the comparator 1410 is FALSE. The value stored in FALSE counter 1416b is decreased by one for each triggering FALSE output from the comparator 1410. This overall functionality of selecting where to store the addresses of the OVR components is provided by the circuit including the comparator 1410, the TRUE and FALSE counters 1416a and

1416b and the multiplexor 1420. The output from the comparator 1410 controls the multiplexor 1420 via a select register 1422.

**[00180]** The multiplexor 1420 controls which counter output of the counters 1416a and 1416b is received by the VIR\_COMBINED 1402. The control is via the selection of either counter 1416a or 1416b and the selection is controlled via a mode value stored in the select register 1422. The select register 1422 receives the mode value from the output of the comparator 1410. With each cycle, the VIR\_COMBINED 1402 is enabled once for write because the input is to the TRUE section of the VIR (e.g., addresses 0, 1, 2, ..., count + 1, wherein count begins with "0"), or the FALSE section of the VIR (e.g., addresses N-1, N-2, N-3, ..., VIR\_length - count+1, wherein count begins with "0"); and thus, the index is generated from either the top down or the bottom up. In the example shown in FIG. 14, the TRUE counter 1416a starts with "0" and increments by "1" with each cycle. In this example, the FALSE counter 1416b starts with a scalar value representing the length of the VIR\_COMBINED 1402 (i.e., N-1) and decrements by "1" with each cycle. For example, in FIG. 14, the comparison by the comparator 1410 is  $SR < OVR(i)$ , and thus, "2", the value at address "0" of the OVR 1404, is TRUE and therefore address "0" of the OVR is stored at address "0" of the VIR\_COMBINED 1402 (or the top of the VIR). And, "5", the value at address "1" of the OVR 1404, is FALSE and therefore address "1" of the OVR is stored at address "N-1" of the VIR\_COMBINED 1402 (or the bottom of the VIR). And, "3", the value at address "2" of the OVR 1404, is TRUE and therefore address "2" of the OVR is stored at address "1" of the VIR\_COMBINED 1402 (or the top-most position of the VIR not filled). And, "6", the value at address "3" of the OVR 1404, is FALSE and therefore address "3" of the OVR is stored at address "N-2" of the VIR\_COMBINED 1042 (or the bottom-most position of the VIR not filled).

**[00181]** The TRUE section and the FALSE section each are part of the output register of the system 1400. The VIR\_COMBINED 1402 has at least two inputs. The first input is from the counter 1416a or 1416b, which is for the address of accessing VIR\_COMBINED 1402. The second input is from the counter 1408 and this input includes the data written into the VIR\_COMBINED 1402 at the address of the register provided by the counter 1416a or 1416b.

**[00182]** The system 1400 can be a part of a vector processor that includes a vector load-store unit. The vector load-store unit can load data stored in the registers of the system 1400 to main memory as well as store data from main memory to the registers

of the system, and vice versa (load data stored in memory to the registers of system 1400 as well as store data from registers of the system to memory).

**[00183]** The system 1400 is also shown to include a scalar register for vector length, vector length register 1424 (VLR 1424). VLR 1424 is configured to store the vector length (VL) of the OVR 1404. A vector processor can load the VL into memory from VLR 1424 to identify whether the count from counter 1408 equals the VL of the operand vector stored in the OVR 1404. This is one way for example to implement step 1312 of method 1300 in FIG. 13. If the count is less than the VL, then the count in the counter 1408 continues to increment per clock cycle or another trigger or iteration (e.g., see step 1314). By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the OVR 1404 according to the count until the positions of the elements of the OVR are stored in the TRUE section or the FALSE section of the VIR\_COMBINED 1402. In other words, the system 1400 can continue with the storing of positions of elements of the OVR 1404 according to the count until the positions of the elements of the loaded operand vector are stored in the TRUE section or the FALSE section of the VIR\_COMBINED 1402. This is one of the ways that the system 1400 can implement operations of the method 1300.

**[00184]** If the count is equal to the VL, then the vector processor using system 1400 has completed the building of indexing vectors for storing in the TRUE section or the FALSE section of the VIR\_COMBINED 1402. The count cannot be greater than the VL because the operation of building the indexing vectors is complete upon the count being equal to the VL. When new indexing vectors are to be built, the count is reset in counter 1408 and VL is determined and stored in VLR 1424. The vector processor can initially determine the vector length of an OVR (e.g., OVR 1404) and then store it in the VLR 1424 before performing method 1300.

**[00185]** Upon completion of the building of indexing vectors which are stored in VIR\_COMBINED 1402, the vector processor can continue with loading from the VIR\_COMBINED, by a vector load-store unit of the processor, stored positions of the elements of the OVR 1404. And, the vector processor can also continue with iterating one or more vector operations over the elements of the OVR 1404 according to the loaded positions in the VIR\_COMBINED 1402.

**[00186]** FIG. 15 illustrates an example system 1500 including a VIR\_TRUE 1502a and a VIR\_FALSE 1502b, in accordance with some embodiments of the present

disclosure. For the purposes of this disclosure it is to be understood that a system similar to system 1500 can include multiple VIR\_TRUEs and multiple VIR\_FALSEs. For example, an embodiment similar to system 1500 with two VIR\_TRUEs and two VIR\_FALSEs can include a 5:1 multiplexor with four inputs to receive the two VIR\_TRUEs and two VIR\_FALSEs and an input to receive the input from the counter (e.g., counter similar to counter 1504). In some embodiments, the amount of VIR\_TRUEs equals the amount of VIR\_FALSEs in such systems.

**[00187]** The system 1500 can be a part of vector processor 102 (e.g., see FIG. 1 or 2) or multiple vector processors. System 1500 includes the vector index registers VIR\_TRUE 1502a and VIR\_FALSE 1502b, a counter register 1504, a 2:1 multiplexor 1506, and a select register 1508 connected to the multiplexor. The VIR\_TRUE 1502a and VIR\_FALSE 1502b can be registers of the vector registers 202 shown in FIG. 2. The counter register 1504 and the select register 1508 can be registers of the scalar registers 204. The 2:1 multiplexor 1506 can be a part of the bus 206 shown in FIG. 2 or the bus 104 shown in FIG. 1.

**[00188]** VIR\_TRUE 1502a is a vector index register for TRUE results of a comparison, and is configured to store a plurality of address components corresponding to a plurality of positions in an OVR that produce TRUE results when used in a comparison. For example, see VIR\_TRUE 1202a, which can be part of system 1500.

**[00189]** VIR\_FALSE 1502b is a vector index register for FALSE results of a comparison, and is configured to store a plurality of address components corresponding to a plurality of positions in an OVR that produce FALSE results when used in a comparison. For example, see VIR\_FALSE 1202b, which can be part of system 1500.

**[00190]** Each address component can be addable to an effective address for accessing a corresponding position in the OVR. Each position of the OVR can include an element of the operand vector to be operated upon by the ALU. For example, the system 1500 can be part of a vector processor that includes an arithmetic logic unit (ALU) of a plurality of arithmetic logic units (ALUs). The vector processor can also include an operand vector register (OVR) of a plurality of operand vector registers. The OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU.

**[00191]** As shown, the counter register 1504 is part of the system 1500. The



counter register 1504 can also be a part of the vector processor having the system 1500. The counter register 1504 can be configured to store a count 1510. The count 1510 can be addable to an effective address for accessing the OVR or the count can be used by the vector processor for iterating on the plurality of address components stored in the VIR 1502.

**[00192]** As shown, the 3:1 multiplexor 1506 is part of the system 1500. The 3:1 multiplexor 1506 can also be a part of the vector processor having the system 1500. The 3:1 multiplexor 1506 can be configured to receive, as inputs, the count 1510 from the counter register 1504 and respective outputs 1512a and 1512b from the VIRs 1502a and 1502b. The outputs 1512a and 1512b from the VIRs 1502a and 1502b can include one of the plurality of address components of the VIRs corresponding to the count 1510. The 3:1 multiplexor 1506 can also be configured to receive, as a selection input, a mode value 1514. The mode value 1514 can be or include a value for selection of the count 1510 or a value for selection of one of the outputs 1512a or 1512b from the VIRs 1502a and 1502b. The 3:1 multiplexor 1506 can also be configured to select either the count 1510 or one of the outputs 1512a or 1512b from the VIRs 1502a and 1502b according to the received mode value 1514. The 3:1 multiplexor 1506 can also be configured to output and communicate, via a bus (such as one of the buses of FIG. 1 or 2), a selection output 1516 that is the selected count or one of the selected outputs from the VIRs. The selection output 1516 can be communicated to a requester accessing the OVR for the ALU. The requester can be a vector load-store unit of the vector processor (e.g., see vector load-store unit 210 shown in FIG. 2), or a vector load-store unit of another vector processor.

**[00193]** FIG. 16 illustrates example operations of method 1600 for compressing elements of an operand vector according to a VIR\_TRUE (e.g., see VIR\_TRUE 1202a or 1502a), in accordance with some embodiments of the present disclosure. Alternatively, the example operations of method 1600 for compressing elements of an operand vector can be according to a VIR\_FALSE (e.g., see VIR\_FALSE 1202b or 1502b) or a TRUE or FALSE section of a VIR\_COMBINED (e.g., see VIR\_COMBINED 1402), in accordance with some embodiments of the present disclosure.

**[00194]** In FIG. 16, the method 1600 begins at step 1602, with loading, by a vector load-store unit, an input operand vector stored in an input OVR. At step 1604, the method 1600 continues with loading, by the vector load-store unit, the count stored in a counter register. At step 1606, the method 1600 continues with loading from a

VIR\_TRUE, by the vector load-store unit, a stored position of an element of the loaded input operand vector according to the count. At step 1608, the method 1600 continues with running a vector compress operation over the elements of the loaded input operand vector according to the loaded position from the VIR\_TRUE. Step 1608 includes step 1610 that includes the method 1600 continuing with storing the element of the loaded input operand vector into an output OVR that corresponds to the loaded position from the VIR\_TRUE. At step 1612, the method 1600 continues with comparing the count to a value representing the vector length of the VIR\_TRUE (i.e., VL) such that the vector compress operation can be iterated over the input OVR for each of the positions stored in the VIR\_TRUE. When the count equals the vector length of the VIR\_TRUE, then the method 1600 ends. When the count is less than the vector length of the VIR\_TRUE, then the method 1600 continues with incrementing the count at 1614 and then returning to step 1604 (loading the count stored in a counter register) which is followed by steps 1606 (loading from a VIR\_TRUE, by the vector load-store unit, a stored position of an element of the loaded input operand vector according to the count) and 1608 (running the vector compress operation over the elements of the loaded input operand vector according to the loaded position from the VIR\_TRUE). This way the vector compress operation is iterated over the input OVR for each of the positions stored in the VIR\_TRUE.

**[00195]** FIG. 17 illustrates an example system 1700 including a VIR\_TRUE 1702a (which can be similar to VIR\_TRUE 1202a or 1502a) being used for compressing elements of an input operand vector stored in an input OVR 1704, in accordance with some embodiments of the present disclosure. Alternatively, the example system 1700 can be used to compress elements of an operand vector according to a VIR\_FALSE 1702b (which can be similar to VIR\_FALSE 1202b or 1502b), in accordance with some embodiments of the present disclosure. Also, the example system 1700 can be used to compress elements of an operand vector according to a TRUE or FALSE section of a VIR\_COMBINED (e.g., see VIR\_COMBINED 1402), in accordance with some embodiments of the present disclosure.

**[00196]** Example system 1700 is one example of a system that can implement at least method 1600.

**[00197]** In FIG. 17, the VIR\_TRUE 1702a stores a list of positions of the input OVR 1704 (e.g., “2” as the input OVR’s first element, and “4” as the input OVR’s second element”). In this illustrated example, it is shown that the vector processor runs for

two cycles or iterations of a vector compress operation. At the first iteration, counter 1706 outputs the count of "0" which is the value stored in the counter at the first cycle. In the first cycle, VIR\_TRUE 1702a is shown outputting "2". The multiplexor 1708 selects between the address component ("0") as specified by the counter 1706 in a normal mode operation or the address component ("2") as specified by the VIR\_TRUE 1702a in a VIR\_TRUE mode of operation (or a compress mode of operation based on contents of the VIR\_TRUE 1702a in this specific example). When the VIR\_TRUE (or VIR\_TRUE compress mode) is selected by the multiplexor 1708 in the first cycle the output of "2" from the VIR\_TRUE 1702a is the address component used for accessing the input OVR 1704. As a result, the input OVR 1704 is accessed for an output of element "C" at position "2" of the input OVR. The output OVR 1710 is addressed directly through the count stored in the counter 1706. Since the count of the counter 1706 is "0" in the first cycle, the output ORV 1710 stores "C" as its first element. In the next iteration or cycle, the output ORV 1710 stores "E" as a second element at position "1" of the output OVR. In this example with two cycles show, the input OVR 1704 having elements of {A, B, C, D, E} is compressed into the output OVR 1710 having elements of {C, E}.

**[00198]** Also, in reference to FIG. 17, if the address signals for the input/output vectors are reversed, {C, E} can be expanded into a second output OVR having element of {x, x, C, x, E} where x is the existing values before the compress operation or a scalar value selected from a scalar register (e.g., see FIG. 9 which is an example method expanding a compressed vector with a scalar value from a scalar register).

**[00199]** Further, if a value from a VFR is added to the count of the counter, the summation can be used so that the first iteration of an operation on the input OVR occurs at another position of the input OVR instead of the first position of the input OVR (e.g., the first position of input OVR 1704 is labeled "0"). E.g., see FIG. 5. Alternatively, the VIR\_TRUE 1702a can be used to provide an input for the count register so that the initial value of the count register at the beginning of a vector operation is the value stored in the VIR\_TRUE 1702a. Such options allow for vector first processing. It is to be understood, the for different types of operations the VIR\_FALSE 1702b could be used instead of VIR\_TRUE 1702a. For example, a compress operation could be based on the index in VIR\_FALSE 1702b instead of VIR\_TRUE 1702a. Also, a VIR\_COMBINED can replace VIR\_FALSE 1702b and VIR\_FALSE 1702b in the system 1700.

**[00200]** As mentioned herein, at least some of the embodiments disclosed herein are vector index registers in vector processors that each store multiple addresses (also known as indexes) for accessing multiple positions in vectors in vector registers. Further, at least some of the embodiments disclosed herein are vector index registers for TRUE and/or FALSE results of one or more conditional test operations (such as numerical comparisons) that each store multiple addresses for accessing multiple positions in operand vectors (VIR\_TRUE and VIR\_FALSE). Also, at least some embodiments described herein are directed to conditional operations in a vector processor having vector index registers VIR\_TRUE and VIR\_FALSE. Further, disclosed herein are processes of using VIR\_TRUE and VIR\_FALSE for more efficiently or faster process vector conditional operations in a vector processor.

**[00201]** The technologies disclosed herein can at least provide support for basic or complex conditional operations. For example, the technologies can support the following basic conditional operation; if (  $A(i) > B(i)$  )  $A(i) = A(i) + B(i)$  else  $A(i) = A(i) - B(i)$ . In such a basic conditional operation a single set of VIRs, VIR\_TRUE and VIR\_FALSE, can be used to perform the same operation more efficiently via the vector processor running  $A(\text{VIR\_TRUE}(j)) = A(\text{VIR\_TRUE}(j)) + B(\text{VIR\_TRUE}(j))$  and  $A(\text{VIR\_FALSE}(k)) = A(\text{VIR\_FALSE}(k)) - B(\text{VIR\_FALSE}(k))$ . Also, disclosed herein are systems that can support efficient implementations of conditional operations in a vector processor, such as conditional operations including, for example, if ( 'test condition' )  $A(i) = A(i) + B(i)$  else  $A(i) = A(i) - B(i)$  using a pair of VIR\_TRUE and VIR\_FALSE.

**[00202]** The results of the test condition can also be used to set the indices in the two vector index registers, VIR\_TRUE and VIR\_FALSE.

**[00203]** The test condition can be simple (e.g., " $A(i) > 0$ ", or " $A(i) > B(i)$ ", or " $A(i) > C(i)$ "). The test condition can also be more complex (e.g., " $(A(i) > 0 \text{ and } A(i) > B(i))$  or " $(A(i) > C(i))$ "). Thus, whether the test condition is simple or complex, a single set of VIR\_TRUE and VIR\_FALSE can be used to handle the two or more branches of operations selected via a conditional test operation ( e.g., two branches of operations including: then " $A(i) = A(i) + B(i)$ " else " $A(i) = A(i) - B(i)$ " ).

**[00204]** It is to be understood for the purposes of this disclosure that a conditional test in general does not have to be testing ">". The test condition can be other types of numerical tests and/or Boolean operations.

**[00205]** In some embodiments, when there are complex tests and/or Boolean

operations, it can be advantageous to use a Vm register to track the vector True and False values so that different TRUE and FALSE vectors can be combined to generate the final testing results. It can be complicated to translate complex Boolean operations into corresponding index operations such as VIR\_TRUE and VIR\_FALSE, so using a Vm as an intermediate indexing vector can be useful in some embodiments.

**[00206]** Some example embodiments can include a system that includes a vector processor, a plurality of operand vector registers (OVRs), a vector load-store unit, and at least two vector index registers such as VIR\_TRUE and VIR\_FALSE. The vector processor can be configured to perform a conditional test operation on elements of a first loaded operand vector and a second loaded operand vector according to a count stored in a counter register of the vector processor.

**[00207]** The OVRs can include a first operand vector register (OVR) of the vector processor configured to store a first operand vector, and a second OVR of the vector processor configured to store a second operand vector.

**[00208]** The vector load-store unit of the vector processor can be configured to load a first operand vector stored in the first OVR and load a second operand vector stored in the second OVR. In such an example, the vector processor can be configured to perform a conditional test operation on each element of the first and the second operand vectors according to a count stored in a counter register. Also, in such an example, the conditional test operations can provide a vector of test results.

**[00209]** The vector load-store unit of the vector processor can also be configured to store, in a first vector index register for each TRUE result of TRUE results of the conditional test operation (VIR\_TRUE), a position of the TRUE result in the vector of test results. And, the vector load-store unit of the vector processor can also be configured to store, in a second vector index register for each FALSE result of FALSE results of the conditional test operation (VIR\_FALSE), a position of the FALSE result in the vector of test results. In such an example, the vector processor can be configured to perform a first vector operation on first elements in the first and the second operand vectors, the first elements identified by positions stored in the first vector index register (VIR\_TRUE). The vector processor can also be configured to perform a second vector operation on second elements in the first and the second operand vectors, the second elements identified by positions stored in the second vector index register (VIR\_FALSE). In some embodiments, the vector processor uses instructions (e.g., user level programmable instructions) that use the registers to

perform the vector operations described herein.

**[00210]** In some embodiments of the example system, the first operand vector is a first input operand vector and the second operand vector is a second input operand vector. And, in such embodiments, the vector load-store unit can be configured to load a second count from a second counter register, as well as load, from the VIR\_TRUE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count. In such embodiments, the vector processor can be configured to run a first operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_TRUE. Also, the vector load-store unit can be configured to store the result of the first operation into an output OVR at a position that corresponds to the loaded position from the VIR\_TRUE. Further, the vector processor can be configured to continue to run the first operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_TRUE and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE, until the second count equals the length of the VIR\_TRUE, wherein the count is incremented per loaded position from the VIR\_TRUE. And, the vector processor can be configured to reset the second count when the second count equals the length of the VIR\_TRUE.

**[00211]** In some embodiments of the last-mentioned example system, subsequent to resetting the second count by the vector processor, the vector load-store unit can be configured to load, from the VIR\_FALSE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count. Also, the vector processor can be configured to run a second operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_FALSE. Further, the vector processor can be configured to continue to run the second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE, until the second count equals the length of the VIR\_FALSE. The count can be incremented per loaded position from the VIR\_FALSE. In some examples, the first operation can include addition and the second operation can include subtraction.

**[00212]** Alternatively, in some embodiments, the VIR\_TRUE and the VIR\_FALSE

are part of one combined vector index register (VIR\_combined). In such alternative embodiments, the vector load-store unit can be configured to store, at a top-most unfilled position in the VIR\_combined for each TRUE result of the TRUE results of the conditional test operation, a position of the TRUE result in the vector of test results. Also, the vector load-store unit can be configured to store, at a bottom-most unfilled position in the VIR\_combined for each FALSE result of the FALSE results of the conditional test operation, a position of the FALSE result in the vector of test results.

**[00213]** In some embodiments described herein, a vector processor can include an arithmetic logic unit (ALU) of a plurality of arithmetic logic units in addition to OVRs, a vector load-store unit, and VIRs such as VIR\_TRUE and VIR\_FALSE. In such embodiments, the OVRs can include a first OVR and a second OVR. Each OVR can be configured to store elements of an operand vector to be used as input for a vector operation of the ALU. Also, the vector processor can be configured to perform a conditional test operation on each element of the first OVR and the second OVR according to a count stored in a counter register. The conditional test operations can provide a vector of test results in this example as well.

**[00214]** In such embodiments, the first vector index register (VIR\_TRUE) can be configured to store, for each TRUE result of a conditional test operation, a position of the TRUE result in the vector of test results. And, the second vector index register (VIR\_FALSE) can be configured to store, for each FALSE result of the conditional test operation, a position of the FALSE result in the vector of test results. Each of the positions can be addable to an effective address for accessing a corresponding position in the OVR, and each of the corresponding positions of the OVR can include an element of the operand vector to be operated upon by the ALU. Also, in such embodiments, the first operand vector can be a first input operand vector and the second operand vector can be a second input operand vector; and the vector processor can be configured to, such as through a vector load-store unit: load a second count from a second counter register; load, from the VIR\_TRUE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and load, from the VIR\_FALSE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count.

**[00215]** Furthermore, in such embodiments and others, the vector processor can be configured to, in parallel, run a first operation over respective elements of the loaded

first and second input operand vectors according to loaded positions from the VIR\_TRUE and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE. Also, the vector processor can be configured to, in parallel, run a second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE. And, for example, the first operation can include addition and the second operation can include subtraction.

**[00216]** Also, in some embodiments, the vector processor can be configured to, in parallel, run a first operation over respective elements of loaded first and second input operand vectors for a VIR\_TRUE according to loaded positions from the VIR\_TRUE and to store the results of the first operation into an output OVR for the VIR\_TRUE. And, in such embodiments, the vector processor can be configured to, in parallel, run a second operation over respective elements of the loaded first and second input operand vectors for a VIR\_FALSE according to loaded positions from the VIR\_FALSE and to store the results of the second operation into an output OVR for the VIR\_FALSE. FIG. 18 illustrates example operations of method 1800 for building indexing vectors for storing in vector indexing registers for TRUE and FALSE results (e.g., "0" and "1" results) of a conditional test operation (VIR\_TRUE and VIR\_FALSE), in accordance with some embodiments of the present disclosure.

**[00217]** The method 1800 begins at step 1102 with loading, by a vector load-store unit of a vector processor, one or more operand vectors. Each operand vector is stored in a respective operand vector register (OVR).

**[00218]** At step 1804, the method 1800 continues with performing, by the vector processor, a conditional test operation on an element of at least one of the loaded one or more operand vectors according to a count stored in a counter. Also, in some embodiments, the conditional test operation can be performed with a scalar from a scalar register and an element of at least one of the loaded one or more operand vectors according to a count stored in a counter. The counter can be a scalar register and a part of the vector processor. In some embodiments, the method 1800 at step 1804 includes comparing, by the vector processor, respective elements of two different loaded operand vectors according to a count stored in a counter (e.g., see method 1900 in FIG. 19). In some embodiments, for the conditional test operation, the



element of a first loaded operand vector is accessed by the vector processor according to a first count in a first counter, and the element of a second loaded operand vector is accessed by the vector processor according to a second count in a second counter.

**[00219]** At step 1806, the method 1800 continues with identifying, by the vector processor, whether the result of the conditional test operation is a TRUE result. To put it another way, at step 1806, the method 1800 continues with identifying whether the result of the conditional test operation of step 1804 is TRUE or FALSE (e.g., Boolean “1” or “0”). If the result of the operation at step 1804 is TRUE, then the method 1800 continues at step 1808 with storing, in a vector index register for TRUE results of the conditional test operation (VIR\_TRUE), the position of the element(s) of the loaded operand vector(s) according to the count (such as according to the count via a TRUE count stored in a TRUE counter—e.g., see TRUE counter 2016a depicted in FIG. 20). If the result of the test operation of step 1804 is FALSE, then the method 1800 continues at step 1810 with storing, in a vector index register for FALSE results of the comparison (VIR\_FALSE), the position of the element(s) of the loaded operand vector(s) according to the count (such as according to the count via a FALSE count stored in a FALSE counter—e.g., see FALSE counter 2016b depicted in FIG. 20).

**[00220]** At step 1812, the method 1800 continues with identifying whether the count equals the vector length (VL) of at least one of the operand vector(s). In some embodiments, the method 1800 can continue with identifying whether the VL of an OVR, accessed by the conditional test operation, equals the result of adding the VL of the VIR\_TRUE and the VL of the VIR\_FALSE, which can be another way to identify whether the count equals the VL of the operand vector stored in the OVR. These example alternative ways of identifying whether the count equals the VL of at least one of the operand vector(s) can show that all the elements of an OVR accessed by the test operation are used in the conditional test operation. If the count is less than the VL, then the method continues at step 1814 with incrementing the count. By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_TRUE or the VIR\_FALSE. In other words, the method 1800 continues the storing of positions of elements of the loaded operand vector according to the count until the positions of the elements of the loaded operand vector are stored in the VIR\_TRUE or the VIR\_FALSE.

**[00221]** At step 1812, if the count is equal to the VL, then the method 1800 has completed the building of indexing vectors for storing in VIR\_TRUE and VIR\_FALSE. Upon completion of the building of indexing vectors which are stored in VIR\_TRUE and VIR\_FALSE, the method 1800 continues, at step 1816, with loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by the vector load-store unit, stored positions of the elements of the loaded operand vector(s). And, at step 1818, the method 1100 continues with iterating one or more vector operations over the elements of the loaded operand vector(s) according to the loaded positions stored in the VIR\_TRUE and/or VIR\_FALSE. In some embodiments, the number of iterations for step 1818 is equal to the VL (as shown in step 1812). In such embodiments, two respective registers can be loaded with the new vector lengths for VIR\_TRUE and VIR\_FALSE (e.g., VL\_VIR\_TRUE and VL\_VIR\_FALSE). In other words, one VL register for the number of entries stored in VIR\_TRUE and one register for the number of entries stored in VIR\_FALSE. In such embodiments, respective VL registers can be loaded with vector lengths of the OVRs as well. Thus, in such embodiments, at step 1818, when the method 1100 continues with iterating one or more vector operations over the elements of the loaded operand vector(s) according to the loaded positions stored in the VIR\_TRUE and/or VIR\_FALSE, the vector processor can determine the number of iterations on the OVR(s) and/or the VIRs according to their respective VL values in respective VL registers.

**[00222]** To put it another way, methods disclosed herein can include loading, by a vector load-store unit of a vector processor, one or more operand vectors, each vector of the one or more operand vectors being stored in a respective operand vector register. Such methods can also include performing, by the vector processor, a conditional test operation on each element of at least one of the loaded one or more operand vectors according to a count stored in a counter register, the conditional test operations providing a vector of test results. The method can also include storing, in a first vector index register for each TRUE result of TRUE results of the conditional test operation (VIR\_TRUE), a position of the TRUE result in the vector of test results, as well as storing, in a second vector index register for each FALSE result of FALSE results of the conditional test operation (VIR\_FALSE), a position of the FALSE result in the vector of test results. The methods can include performing a one or more vector operations on first elements and/or second elements in the one or more operand vectors. The first elements identified by positions stored in the first vector index

register (VIR\_TRUE). The second elements identified by positions stored in the second vector index register (VIR\_FALSE).

**[00223]** In some embodiments, the methods can include performing a first vector operation on first elements in the one or more operand vectors, the first elements identified by positions stored in the first vector index register (VIR\_TRUE). Such methods can also include performing a second vector operation on second elements in the one or more operand vectors, the second elements identified by positions stored in the second vector index register (VIR\_FALSE).

**[00224]** FIG. 19 illustrates example operations of another more specific method 1900 for building indexing vectors for storing in vector indexing registers for TRUE and FALSE results (e.g., "0" and "1" Boolean results) of a conditional test operation (VIR\_TRUE and VIR\_FALSE), in accordance with some embodiments of the present disclosure. Method 1900 is similar to method 1800, except it differs from method 1900 in that the one or more operand vectors in method 1800 are a first operand vector and a second operand vector in method 1900.

**[00225]** The method 1900 begins at step 1902 with loading, by a vector load-store unit, a first operand vector ( e.g.,  $A(i)$  ) stored in a first OVR. At step 1904, the method 1900 continues with loading, by the vector load-store unit, a second operand vector ( e.g.,  $B(i)$  ) stored in a second OVR.

**[00226]** At step 1906, the method 1900 continues with performing a conditional test operation, by the vector processor, on an element of the loaded first operand vector and an element of the loaded second operand vector according to a count stored in a counter ( e.g.,  $A(i) > B(i)$  ). The counter can be a scalar register and a part of the vector processor. In some embodiments, for the conditional test operation, the element of a first loaded operand vector is accessed by the vector processor according to a first count in a first counter, and the element of a second loaded operand vector is accessed by the vector processor according to a second count in a second counter.

**[00227]** At step 1908, the method 1900 continues with identifying, by the vector processor, whether the result of the conditional test operation is a TRUE result. To put it another way, at step 1908, the method 1800 continues with identifying whether the result of the conditional test operation of step 1906 is TRUE or FALSE (e.g., "1" or "0"). If the result of the operation at step 1906 is TRUE, then the method 1900 continues at step 1910a with storing, in a vector index register for TRUE results of the conditional test operation (VIR\_TRUE), the position of the elements of the loaded first

and second operand vectors according to the count (such as according to the count via a TRUE count stored in a TRUE counter—e.g., see TRUE counter 2016a depicted in FIG. 20). If the result of the test operation of step 1906 is FALSE, then the method 1900 continues at step 1910b with storing, in a vector index register for FALSE results of the comparison (VIR\_FALSE), the position of the elements of the loaded first and second operand vectors according to the count (such as according to the count via a FALSE count stored in a FALSE counter—e.g., see FALSE counter 2016b depicted in FIG. 20). Also, in some embodiments, respective VL registers for VIR\_TRUE and VIR\_FALSE are incremented by one at steps 1910a and 1910b.

**[00228]** At step 1912, the method 1900 continues with identifying whether the count equals the vector length (VL) of at least one of the operand vectors. In some embodiments, for method 1900, the VL is the same for all the operand vectors in the OVRs. In some embodiments, the method 1900 can continue with identifying whether the VL of an OVR, accessed by the conditional test operation, equals the result of adding the VL of the VIR\_TRUE and the VL of the VIR\_FALSE, which can be another way to identify whether the count equals the VL of the operand vector stored in the OVR. If the count is less than the VL, then the method continues at step 1914 with incrementing the count. By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the loaded operand vectors according to the count until the positions of the elements of the loaded operand vectors are stored in the VIR\_TRUE or the VIR\_FALSE.

**[00229]** At step 1912, if the count is equal to the VL, then the method 1900 has completed the building of indexing vectors for storing in VIR\_TRUE and VIR\_FALSE.

**[00230]** Upon completion of the building of indexing vectors which are stored in VIR\_TRUE and VIR\_FALSE, the method 1900 continues, at step 1916, with loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by the vector load-store unit, stored positions of the elements of the loaded first and second operand vectors. And, at steps 1918 and 1920, the method 1900 continues with iterating one or more vector operations over the elements of the loaded first and second operand vectors according to the loaded positions stored in the VIR\_TRUE and/or VIR\_FALSE. For example, the method can continue with the vector processor running  $A(\text{VIR\_TRUE}(j)) = A(\text{VIR\_TRUE}(j)) + B(\text{VIR\_TRUE}(j))$  and  $A(\text{VIR\_FALSE}(k)) = A(\text{VIR\_FALSE}(k)) - B(\text{VIR\_FALSE}(k))$ . Also, for example, at step 1918, the method 1900 continues with iterating one or more vector operations over the elements of the

loaded first and second operand vectors according to the loaded positions stored in the VIR\_TRUE. And, for example, at step 1920, the method 1900 continues with iterating one or more vector operations over the elements of the loaded first and second operand vectors according to the loaded positions stored in the VIR\_FALSE.

**[00231]** To put it another way, methods disclosed herein can include loading a first operand vector stored in a first operand vector register (OVR) and loading a second operand vector stored in a second OVR. The methods can also include performing the conditional test operation on each element of the loaded first OVR and the loaded second OVR according to a count stored in a counter register. The methods also can include storing of positions of elements of the loaded first and second operand vectors according to the count until the positions of the elements of the loaded first and second operand vectors are stored in the VIR\_TRUE or the VIR\_FALSE. Further, the methods can include loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by the vector load-store unit, stored positions of the elements of the loaded first and second operand vectors. The methods also can include iterating one or more vector operations over the elements of the loaded first and second operand vectors according to the loaded positions.

**[00232]** FIG. 20 illustrates an example system 2000 for building indexing vectors for storing in VIR\_TRUE 2002a and VIR\_FALSE 2002b, in accordance with some embodiments of the present disclosure. The system 2000 can implement many of the operations and aspects of methods 1800 and 1900 and the system 2000 can be a part of one or more vector processors. The system 1200 includes the VIR\_TRUE 2002a and VIR\_FALSE 2002b. The system also includes a first OVR 2004 and a second OVR 2006, such as OVRs mentioned in the description of method 1900.

**[00233]** The system 2000 also includes a counter 2008, which can be partially implemented by a counter register and can be the counter described in the description of the methods 1800 and 1900.

**[00234]** The system 2000 also includes conditional test operation 2010 that can perform a conditional test operation, such as a comparison of the values stored in the first and second OVRs 2004 and 2006.

**[00235]** The conditional test operation 2010 can perform many different types of conditional test operations such as many different types of comparisons of the OVRs 2004 and 2006 or one or more of the OVRs compared to a scalar, e.g.,  $1^{\text{st}} \text{ OVR } (i) < 2^{\text{nd}} \text{ OVR } (i)$ ,  $1^{\text{st}} \text{ OVR } (i) = 2^{\text{nd}} \text{ OVR } (i)$ ,  $1^{\text{st}} \text{ OVR } (i) > 2^{\text{nd}} \text{ OVR } (i)$ ,  $1^{\text{st}} \text{ OVR } (i) \leq 2^{\text{nd}} \text{ OVR } (i)$

(i),  $1^{\text{st}} \text{ OVR } (i) \geq 2^{\text{nd}} \text{ OVR } (i)$ ,  $1^{\text{st}} \text{ OVR } (i) < \text{a scalar value}$ ,  $1^{\text{st}} \text{ OVR } (i) = \text{a scalar value}$ ,  $1^{\text{st}} \text{ OVR } (i) > \text{a scalar value}$ ,  $1^{\text{st}} \text{ OVR } (i) \leq \text{a scalar value}$ , or  $1^{\text{st}} \text{ OVR } (i) \geq \text{a scalar value}$ , etc.

**[00236]** The conditional test operation 2010 can run against elements of two vectors having a similar address (e.g., a similar index or iteration i) one test or comparison at a time or per cycle. At each iteration i (which also represents address or address component i), the counter 2008 provides address i for accessing the OVRs 2004 and 2006 for the conditional test operation 2010. In some examples, the elements/outputs of OVRs 2004 and 2006 at iteration or address i are compared to each other or with a value from another register such as a scalar register. The conditional test operation 2010 generates a single output, which is either TRUE or FALSE (e.g., “1” or “0”).

**[00237]** The conditional test operation 2010 can be configured to perform the test operation at step 1804 of method 1800 or step 1906 of method 1900. In other words, the conditional test operation 2010 can be configured to run on elements of the loaded operand vectors according to a count stored in a counter register such counter 2008. The conditional test operation 2010 can also be configured to perform the identification of a TRUE or FALSE result at step 1806 or step 1908. In other words, the conditional test operation 2010 can be configured to identify whether the result of the conditional test operation is TRUE or FALSE. The conditional test operation 2010 can be configured to output a TRUE or FALSE result, such as a “1” for a TRUE result or a “0” for a FALSE result. The output of the conditional test operation 2010 is inputted into a respective write enable for each of the VIR\_TRUE 2002a and the VIR\_FALSE 2002b.

**[00238]** The output from the conditional test operation 2010 can be communicated directly to the write enable 2012a for the VIR\_TRUE 2002a. The output from the conditional test operation 2010 can be communicated indirectly to the write enable 2012b for the VIR\_FALSE 2002b, via an inverter 2014. The inverter 2014 is configured to invert the output of conditional test operation 2010 before it reaches the write enable 2012b for the VIR\_FALSE 2002b. For example, if the output of the conditional test operation 2010 is TRUE (e.g., “1”), then when it is inputted into the inverter 2014 the inverter inverts the value to FALSE (e.g., “0”) and outputs FALSE.

**[00239]** The system 2000 also includes a separate TRUE counter 2016a for the VIR\_TRUE 2002a and a separate FALSE counter 2016b for the VIR\_FALSE 2002b. The output of the comparator 2010 drives the two counters, counters 2016a and

2016b. The counters 2016a and 2016b are separate from the counter 2008 that provides the address *i* for the OVRs 2004 and 2006. Output of TRUE counter 2016a is used as the address for accessing VIR\_TRUE 2002a. Output of FALSE counter 2016b is used as the address for accessing VIR\_FALSE 2002b. For example, when the output of the conditional test operation 2010 is TRUE, the output triggers write enable 2012a to write the current position of the OVRs 2004 and 2006 into the VIR\_TRUE 2002a. When the output of the comparator 2010 is FALSE, the output triggers write enable 2012b to write the current position from the OVRs 2004 and 2006 into the VIR\_FALSE 2002b. This functionality is provided via the circuit including the inverter 2014 and the two write enables 2012a and 2012b.

**[00240]** The output of counter 2008 is used as the address or address component (or index) to be written into VIR\_TRUE 2002a at an address specified by the TRUE counter 2016a. This occurs when the output of the test operation 2010 is TRUE. The value stored in counter TRUE 2016a is increased by one for each triggering TRUE output from the test operation 2010. The output of counter 2008 is used as the address or address component to be written into VIR\_FALSE 2002b at an address specified by the FALSE counter 2016b. This occurs when the output of the test operation 2010 is FALSE. The value stored in FALSE counter 2016b is increased by one for each triggering FALSE output from the test operation 2010. This overall functionality of selecting where to store the addresses of the OVR components is provided by the circuit including the test operation 2010, the write enables 2012a and 2012b, the inverter 2014, and the TRUE and FALSE counters 2016a and 2016b.

**[00241]** The VIR\_TRUE 2002a and the VIR\_FALSE 2002b each are an output register of the system 2000 similar to the output registers 1202a and 1202b in the system 1200 depicted in FIG. 12. The system 2000 somewhat similar to the system 1200 can be a part of a vector processor that includes a vector load-store unit.

**[00242]** The system 2000 is also shown to include a scalar register for vector length, vector length register 2024 (VLR 2024). VLR 2024 is configured to store the vector length (VL) of the OVRs 2004 and 2006. A vector processor can load the VL into memory from VLR 2024 to identify whether the count from counter 2008 equals the VL of the respective operand vectors stored in the OVRs 2004 and 2006. In other words, one value is in a register for the VL of the operand vectors in OVRs 2004 and 2006. This is one way for example to implement step 1812 of method 1800 in FIG. 18 or step 1912 of method 1900 in FIG. 19. If the count is less than the VL, then the

count in the counter 2008 continues to increment per clock cycle or another trigger or iteration (e.g., see step 1814 or 1914). By incrementing the count until the count equals the VL, the vector processor can continue with storing positions of elements of the OVRs 2004 and 2006 according to the count until the positions of the elements of the OVRs are stored in the VIR\_TRUE 2002a or the VIR\_FALSE 2002b. In other words, the system 2000 can continue with the storing of positions of elements of the OVRs according to the count until the positions of the elements of the loaded operand vectors are stored in the VIR\_TRUE 1202a or the VIR\_FALSE 1202a. This is one of the ways that the system 2000 can implement operations of the method 1800 or the method 1900.

**[00243]** If the count is equal to the VL, then the vector processor using system 2000 has completed the building of indexing vectors for storing in VIR\_TRUE 2002a and VIR\_FALSE 2002b. The count cannot be greater than the VL because the operation of building the indexing vectors is complete upon the count being equal to the VL. When new indexing vectors are to be built, the count is reset in counter 2008 and VL is determined and stored in VLR 2024. The vector processor can initially determine the vector length of an OVR (e.g., the lengths of the OVRs 2004 and 2006) and then store the lengths (which is one length) in the VLR 2024 before performing method 1800 or 1900.

**[00244]** FIGS. 21 and 22 illustrates example operations of method 2100 for running operations on elements of operand vectors according to a VIR\_TRUE and a VIR\_FALSE (e.g., see VIR\_TRUE 2202a and VIR\_FALSE 2202b depicted in FIG. 23), in accordance with some embodiments of the present disclosure.

**[00245]** Alternatively, the example operations of method 2100 for running operations on elements of operand vectors can be according to a TRUE and FALSE sections of a VIR\_COMBINED (e.g., see VIR\_COMBINED 2302 depicted in FIGS. 24), in accordance with some embodiments of the present disclosure. In such examples, the count is not reset during the running of the operations on the operand vectors.

**[00246]** Also, the example operations of method 2100 for running operations on elements of operand vectors can be according to a VIR\_TRUE and a VIR\_FALSE that are accessed in parallel in that, for example, both occurrences of position *i* in VIR\_TRUE and VIR\_FALSE are accessed in the same clock cycle or iteration (e.g., see VIR\_TRUE 2402a and VIR\_FALSE 2402b depicted in FIG. 25), in accordance with some embodiments of the present disclosure. In such examples, vector lengths



of VIR\_TRUE and VIR\_FALSE, VL\_VIR\_TRUE and VL\_VIR\_FALSE, are not compared to the count and the count is not reset during the running of the operations on the operand vectors. Also, in such examples and others, step 2116 can occur per clock cycle or iteration of the operations. And, in such examples, where the VIRs are accessed in parallel, steps 2106-2112 and steps 2120-2126 can be performed in parallel as well.

**[00247]** In FIG. 21, the method 2100 begins at step 2102, with loading, by a vector load-store unit, a first input operand vector stored in a first input OVR. At step 2104, the method 2100 continues with loading, by the vector load-store unit, a second input operand vector stored in a second input OVR. At step 2106, the method 2100 continues with loading, by the vector load-store unit, a count stored in a counter register. At step 2108, the method 2100 continues with loading from a VIR\_TRUE (or a TRUE section of a VIR\_COMBINED), by the vector load-store unit, a stored position of respective elements of the loaded first and second input operand vectors according to the count.

**[00248]** At step 2110, the method 2100 continues with running a first operation (e.g., addition) over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_TRUE (or the TRUE section of the VIR\_COMBINED). Step 2110 includes step 2112 that includes the method 2100 continuing with storing the result of the first operation (e.g., result from an ALU) into an output OVR at a position that corresponds to the loaded position from the VIR\_TRUE (or the TRUE section of the VIR\_COMBINED).

**[00249]** At step 2114, the method 2100 continues with comparing the count to a value representing the vector length of the VIR\_TRUE (or the TRUE section of VIR\_COMBINED), i.e., VL\_VIR\_TRUE, such that the first operation can be iterated over the loaded first and second input operand vectors stored in the input operand vector registers for each of the positions stored in the VIR\_TRUE (or the TRUE section of VIR\_COMBINED). When the count equals the vector length of the VIR\_TRUE, then the method 2100 continues with resetting the count in the count register, at step 2118.

**[00250]** It is to be understood that the VL\_VIR\_TRUE and the VL\_VIR\_FALSE are preloaded with the vector lengths of VIR\_TRUE and VIR\_FALSE before the method 2100 is initiated. In some embodiments, the VL\_VIR\_TRUE and the VL\_VIR\_FALSE are loaded with the lengths of the vectors in VIR\_TRUE and the VIR\_FALSE while

VIR\_TRUE and VIR\_FALSE are loaded with vector index elements (e.g., see steps 1808, 1810, 1910a, and 1910b).

**[00251]** When the count is less than the vector length, at step 2114, the method 2100 continues with incrementing the count at 2116 and then returning to step 2106 (loading the count stored in a counter register) which is followed by steps 2108 (loading from the VIR\_TRUE (or the TRUE section of the VIR\_COMBINED), by the vector load-store unit, a stored position of respective elements of the loaded input operand vectors according to the count) and 2110 (running the first operation over the elements of the loaded input operand vectors according to the loaded position from the VIR\_TRUE (or the TRUE section of the VIR\_COMBINED) ). This way the first operation is iterated over the input OVRs for each of the positions stored in the VIR\_TRUE (or the TRUE section of the VIR\_COMBINED).

**[00252]** As mentioned, at step 2118, when the count equals the vector length of the VIR\_TRUE, then the method 2100 continues with resetting the count in the count register. However, when VIR\_COMBINED is used, the resetting of the count does not occur because the initial position of the FALSE section of the VIR\_COMBINED is the first position after the last position of the TRUE section of the VIR\_COMBINED (which is not position "0").

**[00253]** Subsequently, at step 2120, the method 2100 continues with loading, by the vector load-store unit, the count stored in the counter register. In examples using VIR\_TRUE and VIR\_FALSE, the value of the count at the first iteration of step 2120 is "0". In examples using VIR\_COMBINED, the value of the count at the first iteration of step 2120 is the value representative of the first position of the FALSE section of the VIR\_COMBINED.

**[00254]** At step 2122, the method 2100 continues with loading from a VIR\_FALSE (or a FALSE section of a VIR\_COMBINED), by the vector load-store unit, a stored position of respective elements of the loaded first and second input operand vectors according to the count.

**[00255]** At step 2124, the method 2100 continues with running a second operation (e.g., subtraction) over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_FALSE (or the FALSE section of the VIR\_COMBINED). Step 2124 includes step 2126 that includes the method 2100 continuing with storing the result of the second operation (e.g., result from an ALU) into an output OVR at a position that corresponds to the loaded position

from the VIR\_FALSE (or the FALSE section of the VIR\_COMBINED).

**[00256]** At step 2128, the method 2100 continues with comparing the count to a value representing the vector length of the VIR\_FALSE (or the FALSE section of VIR\_COMBINED), i.e., VL\_VIR\_FALSE, such that the first operation can be iterated over the loaded first and second input operand vectors stored in the input operand vector registers for each of the positions stored in the VIR\_FALSE (or the FALSE section of VIR\_COMBINED). When the count equals the vector length of the VIR\_FALSE, then the method 2100 ends.

**[00257]** It is to be understood that the VL\_VIR\_TRUE and the VL\_VIR\_FALSE are preloaded with the vector lengths of VIR\_TRUE and VIR\_FALSE before the method 2100 is initiated. In some embodiments, the VL\_VIR\_TRUE and the VL\_VIR\_FALSE are loaded with the lengths of the vectors in VIR\_TRUE and the VIR\_FALSE while VIR\_TRUE and VIR\_FALSE are loaded with vector index elements (e.g., see steps 1808, 1810, 1910a, and 1910b).

**[00258]** When the count is less than the vector length, at step 2128, the method 2100 continues with incrementing the count at 2130 and then returning to step 2120 (loading the count stored in a counter register) which is followed by steps 2122 (loading from the VIR\_FALSE (or the FALSE section of the VIR\_COMBINED), by the vector load-store unit, a stored position of respective elements of the loaded input operand vectors according to the count) and 2124 (running the second operation over the elements of the loaded input operand vectors according to the loaded position from the VIR\_FALSE (or the FALSE section of the VIR\_COMBINED) ). This way the second operation is iterated over the input OVRs for each of the positions stored in the VIR\_FALSE (or the FALSE section of the VIR\_COMBINED).

**[00259]** In some embodiments, upon the addresses of input OVRs being stored in VIR\_TRUE and VIR\_FALSE (or TRUE and FALSE sections of VIR\_COMBINED), the methods can include loading a second count from a second counter register (wherein a first count from a first count register was used for storing the addresses in the VIR(s)). The methods can also include loading, from the VIR\_TRUE (or TRUE section), a stored position of respective elements of the loaded first and second input operand vectors according to the second count. The methods can also include running a first operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_TRUE (or TRUE section).

**[00260]** The methods can also include storing the result of the first operation into an output OVR at a position that corresponds to the loaded position from the VIR\_TRUE (or TRUE section). The methods can also include continuing to run the first operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_TRUE (or TRUE section) and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE (or TRUE section), until the second count equals the length of the VIR\_TRUE (or TRUE section), wherein the count is incremented per loaded position from the VIR\_TRUE (or TRUE section).

**[00261]** The methods can also include resetting the second count when the second count equals the length of the VIR\_TRUE (or TRUE section); and subsequent to resetting the second count, loading, from the VIR\_FALSE (or FALSE section), a stored position of respective elements of the loaded first and second input operand vectors according to the second count.

**[00262]** The methods can also include running a second operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_FALSE (or FALSE section). The methods can also include continuing to run the second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE (or FALSE section) and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE (or FALSE section), until the second count equals the length of the VIR\_FALSE (or FALSE section), wherein the count is incremented per loaded position from the VIR\_FALSE (or FALSE section).

**[00263]** In the methods described herein the first operation can include addition, subtraction, multiplication, division, or any other type of operation that can be performed by one or more ALUs. and the second operation can include a different operation from the first operation that can be performed by one or more ALUs.

**[00264]** FIG. 23 illustrates an example system 2200 including VIR\_TRUE 2202a and VIR\_FALSE 2202b being used for running first and second operations on elements of input operand vectors stored in input operand vector registers 2204a and 2204b, in accordance with some embodiments of the present disclosure. Example system 2200 is one example of a system that can implement at least method 2100.

**[00265]** In FIG. 23, the VIR\_TRUE 2202a stores a list of positions of the input OVRs

2204a and 2204b. For example, "1" is stored in position "0" of VIR\_TRUE 2022a, which can be used as an address for accessing position "1" in both input OVRs 2204a and 2204b. Also, the VIR\_FALSE 2202b stores a list of positions of the input OVRs 2204a and 2204b. For example, "0" and "2" are stored in positions "0" and "1" of VIR\_TRUE 2022a respectively, which can be used as addresses for accessing positions "0" and "2" in both input OVRs 2204a and 2204b.

**[00266]** In this illustrated example of FIG. 23, it is shown that the vector processor runs for at least two iterations of a subtraction operation and for at least one iteration of an addition operation. At the first iteration of the at least two cycles of the subtraction operation, counter 2206 outputs the count of "0" which is the value stored in the counter at the first cycle during a subtraction mode. In the first cycle of the subtraction mode, VIR\_FALSE 2202b is shown outputting selected address "0" from position "0" of the VIR\_FALSE. At the first iteration of the at least one cycle of the addition operation, counter 2206 outputs the count of "0" as well, which is the value stored in the counter at the first cycle during an addition mode. In the first cycle of the addition mode, VIR\_TRUE 2202a is shown outputting selected address "1" from position "0" of the VIR\_TRUE.

**[00267]** The multiplexor 2208 selects between the address component ("0") as specified by the counter 2206 in a NORMAL mode operation or the address component ("1") as stored in position "0" of the VIR\_TRUE 2202a in a TRUE mode of operation or the address component ("0") as stored in position "0" of the VIR\_FALSE 2202b in a FALSE mode of operation. In the next cycle or iteration, when the address component specified by the counter 2206 is "1", then multiplexor 2208 selects between the address component ("1") as specified by the counter in the NORMAL mode operation or the address component ("5") as stored in position "1" of the VIR\_TRUE 2202a in the TRUE mode of operation or the address component ("2") as stored in position "1" of the VIR\_FALSE 2202b in the FALSE mode of operation; and, so on. In other words, the multiplexor 2208 selects between the outputs of counter 2206, VIR\_TRUE 2202a, and VIR\_FALSE 2202b. And, the outputs provided by VIR\_TRUE 2202a and VIR\_FALSE 2202b are according to the count of the counter 2206. In method 2100, the multiplexor 2208 can implement a switching from the TRUE mode to the FALSE mode upon the reset of the counter at step 2118. The counter 2206 is reset when the count equals the vector length of either the VIR\_TRUE or the VIR\_FALSE (e.g., see VL\_VIR\_TRUE 2212a and VL\_VIR\_FALSE 2212b). This

switching allows for the loop of steps 2106-2116 to switch to the loop of steps 2120-2130.

**[00268]** It is to be understood that selections described herein can be according to programmer visible instructions and/or can be a hardwired circuit that is doing some a high level semantic operation.

**[00269]** When the TRUE mode is selected by the multiplexor 2208, in the first cycle, the output of "1" from the VIR\_TRUE 2202a is the address component used for accessing the input OVRs 2204a and 2204b. As a result, the input OVRs 2204a and 2204b are accessed for respective outputs of element "30" at position "1" of the input OVR 2204a and element "25" at position "1" of input OVR 2204b. The output OVR 2210 (or the third OVR) is addressed as well at position "1". The position "1" is outputted by the multiplexor 2208 which has been selected for TRUE mode in this example. Also, in the TRUE mode the ALU 2214 performs an addition operation for this example of FIG. 23. The addition operation is according to the first opcode 2216a which is selected by the multiplexor 2218 in the TRUE mode. Specifically, as shown, the elements of input OVRs 2204a and 2204b at position "1" (elements "30" and "25") are inputted into the ALU 2214. The ALU 2214 adds the elements of position "1" of OVRs 2204a and 2204b and outputs the result of the addition operation. The output of the addition operation is stored then at position "1" of the output OVR 2210 as element "55" ( $A(1) + B(1) = C(1)$  or  $30 + 25 = 55$ ).

**[00270]** When the FALSE mode is selected by the multiplexor 2208, in the first cycle, the output of "0" from the VIR\_FALSE 2202a is the address component used for accessing the input OVRs 2204a and 2204b. As a result, the input OVRs 2204a and 2204b are accessed for respective outputs of element "10" at position "0" of the input OVR 2204a and element "20" at position "0" of input OVR 2204b. The output OVR 2210 (or the third OVR) is addressed as well at position "0". The position "0" is outputted by the multiplexor 2208 which has been selected for FALSE mode in this example. Also, in the FALSE mode the ALU 2214 performs subtraction operation for this example of FIG. 23. The subtraction operation is according to the second opcode 2216b which is selected by the multiplexor 2218 in the FALSE mode. Specifically, as shown, the elements of input OVRs 2204a and 2204b at position "0" (elements "10" and "20") are inputted into the ALU 2214. The ALU 2214 subtracts the element of position "0" of OVR 2204b from the element of position "0" of OVR 2204a, and outputs the result of the subtraction operation. The output of the subtraction operation is

stored then at position “0” of the output OVR 2210 as element “-10” (  $A(0) - B(0) = C(0)$  or  $10 - 20 = -10$  ).

**[00271]** It is to be understood that the addition and subtraction operations illustrated in FIG. 23 are merely examples and that various operations can be performed on OVRs 2204a and 2204b according to the addressing by the VIRs 2202a and 2202b. Thus, the first opcode 2216a can be an opcode for any arithmetic operation of an ALU, and the second opcode 2216b can be an opcode for any arithmetic operation of an ALU as well.

**[00272]** As mentioned, the system 2200 can implement method 2100. For example, with the loading, by a vector load-store unit of a vector processor, one or more operand vectors (at steps 2102 and 2104), each vector of the one or more operand vectors can be stored in OVRs 2204a and 2204b. With the loading, by the vector load-store unit, of the count stored in a counter register, the count can be stored in counter 2206. With the loading, by the vector load-store unit of a vector processor, of the stored positions from VIRs (at steps 2108 and 2122), the positions can be store in VIRs 2202a and 2202b. The running of the first and the second operations in steps 2110 and 2124 can be implemented by a combination of the OVRs, the VIRs, the multiplexors, and the ALU depicted in FIG. 23. The storage of the results of the operations (at steps 2112 and 2126) can occur at the output OVR 2210. And, the loops in the method 2100 can be controlled according to at least the lengths stored in the registers 2212a and 2212b.

**[00273]** FIG. 24 illustrates an example system 2300 including TRUE and FALSE sections of a VIR\_COMBINED 2302 being used for running first and second operations on elements of input operand vectors stored in input operand vector registers 2304a and 2304b, in accordance with some embodiments of the present disclosure. Example system 2300 is one example of a system that can implement method 2100 for the most part.

**[00274]** Address components stored the VIR\_COMBINED 2302 are stored in either the TRUE section (e.g., addresses 0, 1, 2, ..., L-1, wherein L is the vector length of the TRUE section), or the FALSE section of the VIR (e.g., addresses N-1, N-2, N-3, ..., N-M, wherein N is the length of the index vector stored in the VIR and M is the vector length of the FALSE section). The index in TRUE section is generated and stored in the VIR\_COMBINED 2302 from the top down and the index in the FALSE section is generated and stored in the VIR from the bottom up, or vice versa depending

on the embodiment.

**[00275]** In FIG. 24, the TRUE section of the VIR\_COMBINED 2302 stores a list of positions of the input OVRs 2304a and 2304b. For example, the output position "1" is stored in position "0" of the TRUE section, which can be used as an address for accessing position "1" in both input OVRs 2304a and 2304b. Also, the FALSE section of the VIR\_COMBINED 2302 stores a list of positions of the input OVRs 2304a and 2304b. For example, "0" and "2" are stored in positions "N-1" and "N-2" of the FALSE section respectively (wherein N is the length of the vector index stored in the VIR\_COMBINED). The output positions of the FALSE section can be used as addresses for accessing positions "0" and "2" in both input OVRs 2304a and 2304b.

**[00276]** In this illustrated example of FIG. 24, it is shown that the vector processor runs for at least three cycles of an addition operation and for at least three cycles of a subtraction operation. At the first iteration of the at least three cycles of the addition operation, counter 2306 outputs the count of "0", which is the value stored in the counter at the first cycle during an addition mode. As shown, the addition mode is provided by "mode 2" shown in FIG. 24. "Mode 1" shown in FIG. 24 provides the mode of selecting either a NORMAL mode of operation or VIR\_COMBINED mode of operation. In the first cycle of the addition mode, the TRUE section is shown outputting selected address "1" from position "0" of the TRUE section. At the first iteration of the at least three cycles of the subtraction operation, counter 2306 outputs the count of "N-M" which is the value stored in the counter at the first cycle during a subtraction mode. In the first cycle of the subtraction mode, the FALSE section is shown outputting selected address "X" from position "N-M" of the FALSE section. In the second to the last cycle of the subtraction mode, the FALSE section is shown outputting selected address "2" from position "N-2" of the FALSE section. In the last cycle of the subtraction mode, the FALSE section is shown outputting selected address "0" from position "N-1" of the FALSE section.

**[00277]** The multiplexor 2308 selects between the address component ("0") as specified by the counter 2306 in a NORMAL mode operation or the address component ("1") as stored in position "0" of the TRUE section in a TRUE mode of operation. In the next cycle or iteration, when the address component specified by the counter 2306 is "1", then multiplexor 2308 selects between the address component ("1") as specified by the counter in the NORMAL mode operation or the address component ("5") as stored in position "1" of the TRUE section in the TRUE mode of



operation; and, so on. Upon the counter 2306 having a value of “N-M” the mode of operation can switch from the TRUE mode to the FALSE mode. The evaluation of determining the counter having the value “N-M” can be implanted using the register VL\_VIR\_FALSE 2312b. At some point after the count being “N-M”, when the count eventually reaches “N-1”, the multiplexor 2308 selects between the address component (“N-1”) as specified by the counter in the NORMAL mode of operation or the address component (“0”) as stored in position “N-1” of the FALSE section in the FALSE mode of operation.

**[00278]** Multiplexor 2308 selects between the outputs of counter 2306 and the VIR\_COMBINED 2302. And, the outputs provided the TRUE and FALSE sections are according to the count of the counter 2306. In method 2100, the multiplexor 2308 does not implement a switching from the TRUE mode to the FALSE mode upon a reset of the counter at step 2118. In this way, the multiplexor 2208 and 2308 function differently. In method 2100, the multiplexor 2318 dictates the mode of operation of the system 2300. The counter does not reset, but when the count reaches the value of “N-M”, the mode of operation can change in the system 2300 (e.g., “Mode 2” can change). The counter 2306 has the value “L-1” when the last position of the TRUE section is accessed, wherein L is the length of the TRUE section. L can be stored in VL\_VIR\_TRUE 2312a. The counter 2306 has the value “N-M” when the first position of the FALSE section is accessed, wherein M is the length of the FALSE section and N is the total length of the index vector. M can be stored in VL\_VIR\_FALSE 2312b. The switching from the loop of steps 2106-2116 to the loop of steps 2120-2130 can occur through the selected “Mode 2” depicted in FIG. 24. And, the switching can occur when the count equals the length of the TRUE section. However, unlike method 2100, there is no reset of the count because position “N-M” is the first position of the FALSE section and not position “0”.

**[00279]** When the TRUE mode is selected by the multiplexor 2318, in the first cycle, the output of “1” from the TRUE section is the address component used for accessing the input OVRs 2304a and 2304b. As a result, the input OVRs 2304a and 2304b are accessed for respective outputs of element “30” at position “1” of the input OVR 2304a and element “25” at position “1” of input OVR 2304b. The output OVR 2310 (or the third OVR) is addressed as well at position “1”. The position “1” is outputted by the multiplexor 2308 which has been selected for COMBINED\_VIR mode in this example. In the TRUE mode provided by “Mode 2”, the ALU 2314 performs an addition operation

for this example of FIG. 24. The addition operation is according to the first opcode 2316a which is selected by the multiplexor 2318 in the TRUE mode. Specifically, as shown, the elements of input OVRs 2304a and 2304b at position "1" (elements "30" and "25") are inputted into the ALU 2314. The ALU 2314 adds the elements of position "1" of OVRs 2304a and 2304b and outputs the result of the addition operation. The output of the addition operation is stored then at position "1" of the output OVR 2310 as element "55" ( $A(1) + B(1) = C(1)$  or  $30 + 25 = 55$ ).

**[00280]** When the FALSE mode is selected by the multiplexor 2318, in the cycle of "N-M", the output of "X" from the FALSE section is the address component used for accessing the input OVRs 2304a and 2304b. Such a process continues until the cycle of "N-1" occurs, for example. As a result, of the "N-1" cycle in the FALSE mode, the input OVRs 2304a and 2304b are accessed for respective outputs of element "10" at position "0" of the input OVR 2304a and element "20" at position "0" of input OVR 2304b. The output OVR 2310 (or the third OVR) is addressed as well at position "0". The position "0" is outputted by the multiplexor 2308 which has been selected for COMBINED\_VIR mode in this example. Also, in the FALSE mode the ALU 2314 performs subtraction operation for this example of FIG. 24. The subtraction operation is according to the second opcode 2316b which is selected by the multiplexor 2318 in the FALSE mode. Specifically, as shown, the elements of input OVRs 2304a and 2304b at position "0" (elements "10" and "20") are inputted into the ALU 2314. The ALU 2314 subtracts the element of position "0" of OVR 2304b from the element of position "0" of OVR 2304a, and outputs the result of the subtraction operation. The output of the subtraction operation is stored then at position "0" of the output OVR 2310 as element "-10" ( $A(0) - B(0) = C(0)$  or  $10 - 20 = -10$ ).

**[00281]** It is to be understood that the addition and subtraction operations illustrated in FIG. 24 are merely examples and that various operations can be performed on OVRs 2304a and 2304b according to the addressing by the VIRs 2302a and 2302b. Thus, the first opcode 2316a can be an opcode for any arithmetic operation of an ALU, and the second opcode 2316b can be an opcode for any arithmetic operation of an ALU as well.

**[00282]** As mentioned, the system 2300 can implement method 2100 for the most part. For example, with the loading, by a vector load-store unit of a vector processor, one or more operand vectors (at steps 2102 and 2104), each vector of the one or more operand vectors can be stored in OVRs 2304a and 2304b. With the loading, by the

vector load-store unit, of the count stored in a counter register, the count can be stored in counter 2306. With the loading, by the vector load-store unit of a vector processor, of the stored positions from VIRs (at steps 2108 and 2122), the positions can be store in the TRUE and FALSE sections of the VIR\_COMBINED. The running of the first and the second operations in steps 2110 and 2124 can be implemented by a combination of the OVRs, the VIR\_COMBINED, the multiplexors, and the ALU depicted in FIG. 24. The storage of the results of the operations (at steps 2112 and 2126) can occur at the output OVR 2310. And, the loops in the method 2100 can be controlled according to at least the lengths stored in the registers 2312a and 2312b.

**[00283]** FIG. 25 illustrates an example system 2400 including VIR\_TRUE 2402a and VIR\_FALSE 2402b being used for running first and second operations, in parallel, on elements of input operand vectors stored in input operand vector registers 2404a and 2404b, in accordance with some embodiments of the present disclosure. Example system 2400 is one example of a system that can implement at least method 2100 for the most part.

**[00284]** Running the first and second operations in parallel includes accessing VIR\_TRUE and a VIR\_FALSE in parallel. Accessing VIR\_TRUE and a VIR\_FALSE in parallel includes, for example, both occurrences of position *i* in VIR\_TRUE and VIR\_FALSE are accessed in the same clock cycle or iteration. In such examples, vector lengths of VIR\_TRUE and VIR\_FALSE, VL\_VIR\_TRUE and VL\_VIR\_FALSE, are not compared to the count (as shown in FIGS. 21 and 22) and the count is not reset during the running of the operations on the operand vectors (as shown in FIG. 21). However, step 2116 of method 2100 can occur per clock cycle or iteration of the operations when the VIRs are accessed in parallel. And, in such examples, where the VIRs are accessed in parallel, steps 2106-2112 and steps 2120-2126 can be performed in parallel as well.

**[00285]** In FIG. 25, the VIR\_TRUE 2402a stores a list of positions of the input OVRs 2404a and 2404b. For example, "1" is stored in position "0" of VIR\_TRUE 2022a, which can be used as an address for accessing position "1" in both input OVRs 2404a and 2404b. Also, the VIR\_FALSE 2402b stores a list of positions of the input OVRs 2404a and 2404b. For example, "0" and "2" are stored in positions "0" and "1" of VIR\_TRUE 2022a respectively, which can be used as addresses for accessing positions "0" and "2" in both input OVRs 2404a and 2404b.

**[00286]** In this illustrated example of FIG. 25, it is shown that the vector processor

runs for at least two cycles of a subtraction operation and for at least one cycle of an addition operation. At the first iteration of the at least two cycles of the subtraction operation, counter 2406 outputs the count of “0” which is the value stored in the counter at the first cycle during a subtraction mode. In the first cycle of the subtraction mode, VIR\_FALSE 2402b is shown outputting selected address “0” from position “0” of the VIR\_FALSE. At the first iteration of the at least one cycle of the addition operation, counter 2406 outputs the count of “0” as well, which is the value stored in the counter at the first cycle during an addition mode. In the first cycle of the addition mode, VIR\_TRUE 2402a is shown outputting selected address “1” from position “0” of the VIR\_TRUE.

**[00287]** In FIG. 25, there are no multiplexors for selecting a NORMAL or a VIR mode or for selecting a TRUE or FALSE mode. Multiplexors are not needed since the access of the VIRs 2402a and 2402b and the operations on the OVRs 2404a and 2404b are in parallel using separate ALUs 2414a and 2414b for operations addressed by the TRUE\_VIR 2402a and operations addressed by the FALSE\_VIR 2402b, respectively.

**[00288]** To put it another way, the TRUE mode and the FALSE mode run in all clock cycles of the operations of FIG. 25. Thus, the TRUE mode and the FALSE mode can run in parallel to each other.

**[00289]** One example way to implement operations in parallel is to use dual access registers in the system running the parallel operations. In FIG. 25, to implement running the first and second operations in parallel, the OVRs (e.g., OVRs 2404a, 2404b, and 2410) are dual access OVRs. Dual-access vector registers (e.g., OVRs 2404a, 2404b, and 2410) each have two address lines and two input/output (I/O) lines. For example, the output OVR 2410 has an address line I/O<sub>1</sub> which directs the addressing of I/O line I/O<sub>7</sub>; and, address line I/O<sub>2</sub> directs the addressing of I/O line I/O<sub>8</sub>. In other words, the data retrieved from address line connected to VIR\_T 2402a directs addressing of output from the first ALU 2414a and the data retrieved from the address line connected to VIR\_F 2402a directs addressing of output from the second ALU 2414b.

**[00290]** In the first cycle for the TRUE mode, the output of “1” from the VIR\_TRUE 2402a is the address component used for accessing the input OVRs 2404a and 2404b. As a result, the input OVRs 2404a and 2404b are accessed for respective outputs of element “30” at position “1” of the input OVR 2404a and element “25” at

position "1" of input OVR 2404b. The output OVR 2410 (or the third OVR) is addressed as well at position "1". The position "1" is outputted by the VIR\_TRUE 2402a directly in this example without passing through a multiplexor. The ALU 2414a performs an addition operation for this example of FIG. 24. Specifically, as shown, the elements of input OVRs 2404a and 2404b at position "1" (elements "30" and "25") are inputted into the ALU 2414a. The ALU 2414a adds the elements of position "1" of OVRs 2404a and 2404b and outputs the result of the addition operation. The output of the addition operation is stored then at position "1" of the output OVR 2410 as element "55" ( $A(1) + B(1) = C(1)$  or  $30 + 25 = 55$ ).

**[00291]** In the first cycle for the FALSE mode, the output of "0" from the VIR\_FALSE 2402B is the address component used for accessing the input OVRs 2404a and 2404b. As a result, the input OVRs 2404a and 2404b are accessed for respective outputs of element "10" at position "0" of the input OVR 2404a and element "20" at position "0" of input OVR 2404b. The output OVR 2410 (or the third OVR) is addressed as well at position "0". The position "0" is outputted by the VIR\_FALSE 2402b directly in this example without passing through a multiplexor. The ALU 2414B performs a subtraction operation for this example of FIG. 24. Specifically, as shown, the elements of input OVRs 2404a and 2404b at position "0" (elements "10" and "20") are inputted into the ALU 2414b. The ALU 2414b subtracts the element of position "0" of OVR 2404b from the element of position "0" of OVR 2404a, and outputs the result of the subtraction operation. The output of the subtraction operation is stored then at position "0" of the output OVR 2410 as element "-10" ( $A(0) - B(0) = C(0)$  or  $10 - 20 = -10$ ).

**[00292]** It is to be understood that the addition and subtraction operations illustrated in FIG. 25 are merely examples and that various operations can be performed on OVRs 2404a and 2404b according to the addressing by the VIRs 2402a and 2402b. Thus, the ALU 2414a can perform any arithmetic operation of an ALU, and the ALU 2414b can perform any arithmetic operation of an ALU as well.

**[00293]** As mentioned, the system 2400 can implement method 2100 for the most part. For example, with the loading, by a vector load-store unit of a vector processor, one or more operand vectors (at steps 2102 and 2104), each vector of the one or more operand vectors can be stored in OVRs 2404a and 2404b. With the loading, by the vector load-store unit, of the count stored in a counter register, the count can be stored in counter 2406. With the loading, by the vector load-store unit of a vector processor,

of the stored positions from VIRs (at steps 2108 and 2122), the positions can be store in VIRs 2402a and 2402b. The running of the first and the second operations in steps 2110 and 2124 can be implemented by a combination of the OVRs, the VIRs, and the ALUs depicted in FIG. 25. The storage of the results of the operations (at steps 2112 and 2126) can occur at the output OVR 2410. And, the loops in the method 2100 can be controlled according to at least the lengths stored in the registers 2412a and 2412b that can store the vector lengths of VIR\_TRUE 2402A and VIR\_FALSE 2402b, respectively.

**[00294]** The methods 600, 700, 900, 1000, 1100, 1300, 1600, 1800, 1900, and 2100 include just some of the many operations that can be implemented by the vector processors and systems described herein.

**[00295]** Some portions of the preceding detailed descriptions have been presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the ways used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to be a self-consistent sequence of operations leading to a desired result. The operations are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

**[00296]** It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. The present disclosure can refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage systems.

**[00297]** The present disclosure also relates to an apparatus for performing the operations herein. This apparatus can be specially constructed for the intended purposes, or it can include a computer selectively activated or reconfigured by a

computer program stored in the computer. Such a computer program can be stored in a computer readable storage medium, such as, but not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, each coupled to a computer system bus.

**[00298]** The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various systems can be used with programs in accordance with the teachings herein, or it can prove convenient to construct a more specialized apparatus to perform the method. The structure for a variety of these systems will appear as set forth in the description below. In addition, the present disclosure is not described with reference to any particular programming language. It will be appreciated that a variety of programming languages can be used to implement the teachings of the disclosure as described herein.

**[00299]** The present disclosure can be partially provided as a computer program product, or software, that can include a machine-readable medium having stored thereon instructions, which can be used to program a computer system (or other electronic devices) to perform a process according to the present disclosure. A machine-readable medium includes any mechanism for storing information in a form readable by a machine (e.g., a computer). In some embodiments, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium such as a read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory components, etc.

**[00300]** In the foregoing specification, embodiments of the disclosure have been described with reference to specific example embodiments thereof. It will be evident that various modifications can be made thereto without departing from the broader spirit and scope of embodiments of the disclosure as set forth in the following claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

## CLAIMS

What is claimed is:

1. A method, comprising:
  - loading, by a vector load-store unit of a vector processor, one or more operand vectors, each vector of the one or more operand vectors being stored in a respective operand vector register;
  - performing, by the vector processor, a conditional test operation on each element of at least one of the loaded one or more operand vectors according to a count stored in a counter register, the conditional test operations providing a vector of test results;
  - storing, in a first vector index register for each TRUE result of TRUE results of the conditional test operation (VIR\_TRUE), a position of the TRUE result in the vector of test results;
  - storing, in a second vector index register for each FALSE result of FALSE results of the conditional test operation (VIR\_FALSE), a position of the FALSE result in the vector of test results;
  - performing a first vector operation on first elements in the one or more operand vectors, the first elements identified by positions stored in the first vector index register (VIR\_TRUE); and
  - performing a second vector operation on second elements in the one or more operand vectors, the second elements identified by positions stored in the second vector index register (VIR\_FALSE).
  
2. The method of claim 1,
  - wherein the loading of the one or more operand vectors comprises:
    - loading a first operand vector stored in a first operand vector register (OVR); and
    - loading a second operand vector stored in a second OVR;
  - wherein the performing the conditional test operation on each element of at least one of the loaded one or more operand vectors comprises performing the conditional test operation on each element of the loaded first OVR and the loaded second OVR according to a count stored in a counter register; and



wherein the storing of the positions of the TRUE results and the FALSE results in the vector of test results comprises storing of positions of elements of the loaded first and second operand vectors according to the count until the positions of the elements of the loaded first and second operand vectors are stored in the VIR\_TRUE or the VIR\_FALSE.

3. The method of claim 2, further comprising:  
loading from at least one of the VIR\_TRUE, or the VIR\_FALSE, or a combination thereof, by the vector load-store unit, stored positions of the elements of the loaded first and second operand vectors; and  
iterating one or more vector operations over the elements of the loaded first and second operand vectors according to the loaded positions
4. The method of claim 2, wherein the first operand vector is a first input operand vector and the second operand vector is a second input operand vector, and wherein the method further comprises:  
loading a second count from a second counter register;  
loading, from the VIR\_TRUE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and  
running a first operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_TRUE.
5. The method of claim 4, further comprising storing the result of the first operation into an output OVR at a position that corresponds to the loaded position from the VIR\_TRUE.
6. The method of claim 5, further comprising:  
continuing to run the first operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_TRUE and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE, until the second count equals the length

- of the VIR\_TRUE, wherein the count is incremented per loaded position from the VIR\_TRUE; and  
resetting the second count when the second count equals the length of the VIR\_TRUE.
7. The method of claim 6, further comprising:  
subsequent to resetting the second count, loading, from the VIR\_FALSE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and  
running a second operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_FALSE.
  8. The method of claim 7, further comprising:  
continuing to run the second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE, until the second count equals the length of the VIR\_FALSE, wherein the count is incremented per loaded position from the VIR\_FALSE.
  9. The method of claim 8, wherein the first operation comprises addition and the second operation comprises subtraction.
  10. A system, comprising:  
a vector processor, configured to perform a conditional test operation on elements of a first loaded operand vector and a second loaded operand vector according to a count stored in a counter register of the vector processor;  
a first operand vector register (OVR) of the vector processor configured to store a first operand vector;  
a second OVR of the vector processor configured to store a second operand vector; and

a vector load-store unit of the vector processor, configured to:

load a first operand vector stored in the first OVR;

load a second operand vector stored in the second OVR, the vector processor also being configured to perform a conditional test operation on each element of the first and the second operand vectors according to a count stored in a counter register, the conditional test operations providing a vector of test results;

store, in a first vector index register for each TRUE result of TRUE results of the conditional test operation (VIR\_TRUE), a position of the TRUE result in the vector of test results; and

store, in a second vector index register for each FALSE result of FALSE results of the conditional test operation (VIR\_FALSE), a position of the FALSE result in the vector of test results, the vector processor also being configured to:

perform a first vector operation on first elements in the first and the second operand vectors, the first elements identified by positions stored in the first vector index register (VIR\_TRUE); and

perform a second vector operation on second elements in the first and the second operand vectors, the second elements identified by positions stored in the second vector index register (VIR\_FALSE).

11. The system of claim 10,  
wherein the first operand vector is a first input operand vector and the second operand vector is a second input operand vector;  
wherein the vector load-store unit is configured to:  
load a second count from a second counter register; and  
load, from the VIR\_TRUE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and  
wherein the vector processor is configured to run a first operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_TRUE.

12. The system of claim 11, wherein the vector load-store unit is configured to store the result of the first operation into an output OVR at a position that corresponds to the loaded position from the VIR\_TRUE.
13. The system of claim 12, wherein the vector processor is configured to:  
continue to run the first operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_TRUE and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE, until the second count equals the length of the VIR\_TRUE, wherein the count is incremented per loaded position from the VIR\_TRUE; and  
reset the second count when the second count equals the length of the VIR\_TRUE.
14. The system of claim 13,  
wherein, subsequent to resetting the second count by the vector processor, the vector load-store unit is configured to load, from the VIR\_FALSE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and  
wherein the vector processor is configured to run a second operation over the respective elements of the loaded first and second input operand vectors according to the loaded position from the VIR\_FALSE.
15. The system of claim 14, wherein the vector processor is configured to continue to run the second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE, until the second count equals the length of the VIR\_FALSE, wherein the count is incremented per loaded position from the VIR\_FALSE.

16. The system of claim 15, wherein the first operation comprises addition and the second operation comprises subtraction.
17. The system of claim 15, wherein the VIR\_TRUE and the VIR\_FALSE are part of one combined vector index register (VIR\_combined), and wherein the vector load-store unit is configured to:
  - store, at a top-most unfilled position in the VIR\_combined for each TRUE result of the TRUE results of the conditional test operation, a position of the TRUE result in the vector of test results; and
  - store, at a bottom-most unfilled position in the VIR\_combined for each FALSE result of the FALSE results of the conditional test operation, a position of the FALSE result in the vector of test results.
18. A vector processor, comprising:
  - a scalar operand register (SOR) configured to store an element to be used as input for an operation of an arithmetic logic unit (ALU);
  - a first operand vector register (OVR) and a second OVR of a plurality of operand vector registers,
    - each OVR configured to store elements of an operand vector to be used as input for an operation of an ALU,
  - the vector processor configured to either perform a conditional test operation on each element of the first OVR and the second OVR according to a count stored in a counter register, or perform a conditional test operation on an element stored in the SOR and each element of the first OVR according to a count stored in a counter register, and
  - the conditional test operations providing a vector of test results;
  - a first vector index register (VIR\_TRUE) configured to store, for each TRUE result of TRUE results of a conditional test operation, a position of the TRUE result in the vector of test results;
  - a second vector index register (VIR\_FALSE) configured to store, for each FALSE result of FALSE results of the conditional test operation, a position of the FALSE result in the vector of test results,

each of the positions addable to an effective address for accessing a corresponding position in the OVR, and each of the corresponding positions of the OVR comprises an element of the operand vector to be operated upon by an ALU.

19. The vector processor of claim 18, wherein the first operand vector is a first input operand vector and the second operand vector is a second input operand vector; and wherein the vector processor is configured to:
  - load a second count from a second counter register;
  - load, from the VIR\_TRUE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count;
  - load, from the VIR\_FALSE, a stored position of respective elements of the loaded first and second input operand vectors according to the second count; and
  - in parallel:
    - run a first operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_TRUE and to store the results of the first operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_TRUE; and
    - run a second operation over respective elements of the loaded first and second input operand vectors according to loaded positions from the VIR\_FALSE and to store the results of the second operation into the output OVR at the corresponding positions that match the loaded positions from the VIR\_FALSE.
20. The vector processor of claim 19, wherein the first operation comprises addition and the second operation comprises subtraction.

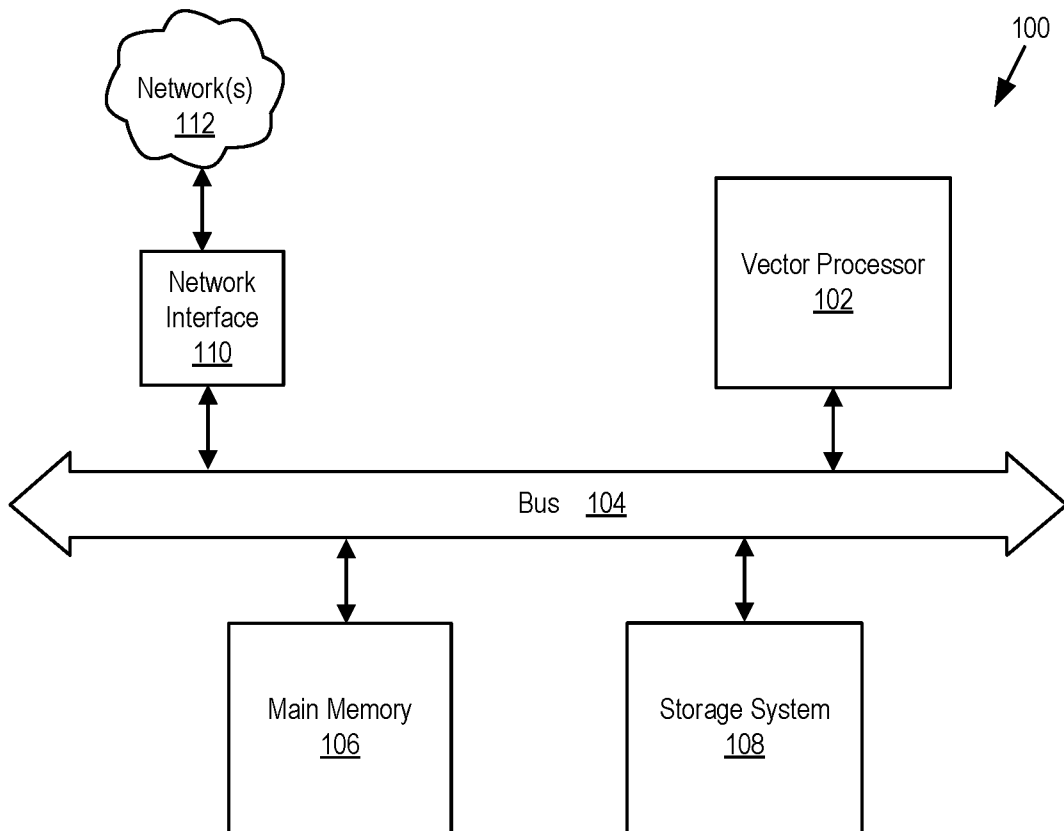


FIG. 1

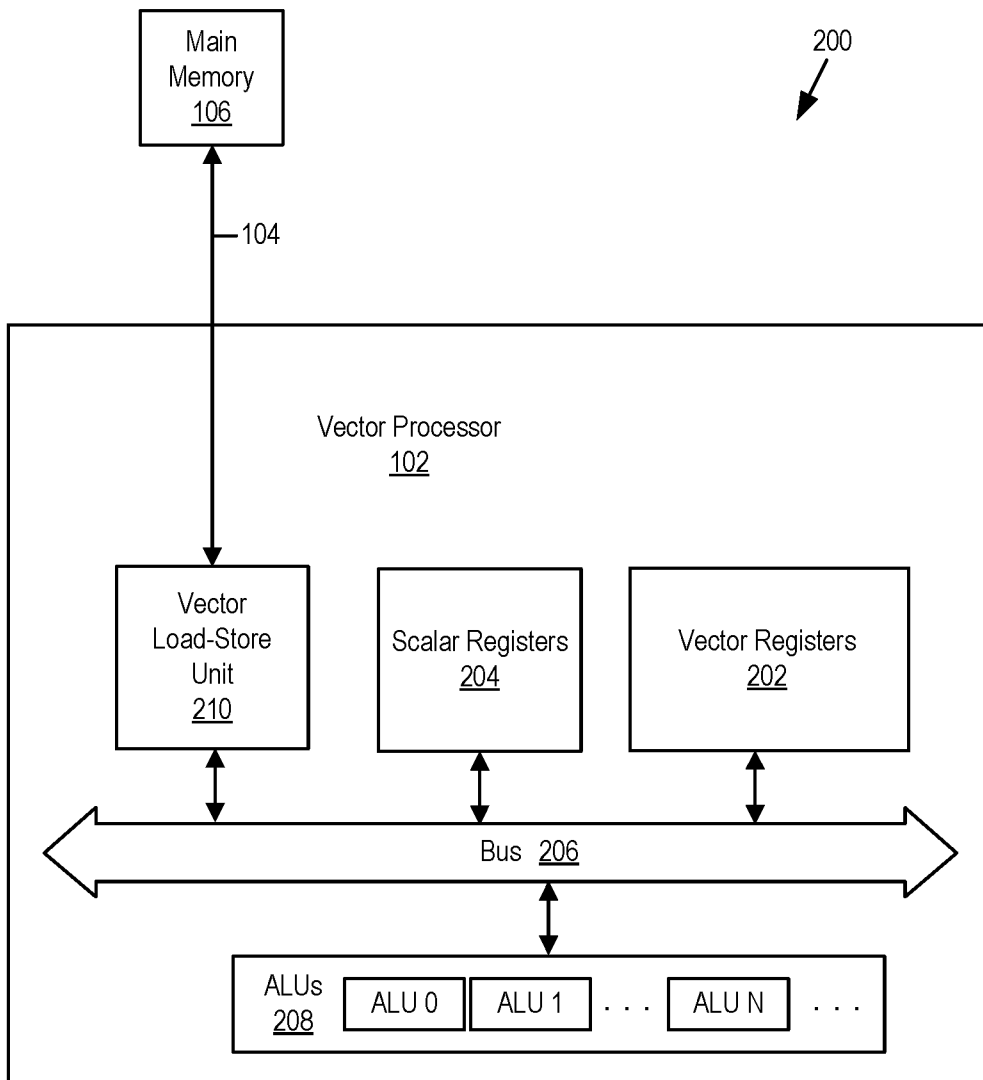


FIG. 2



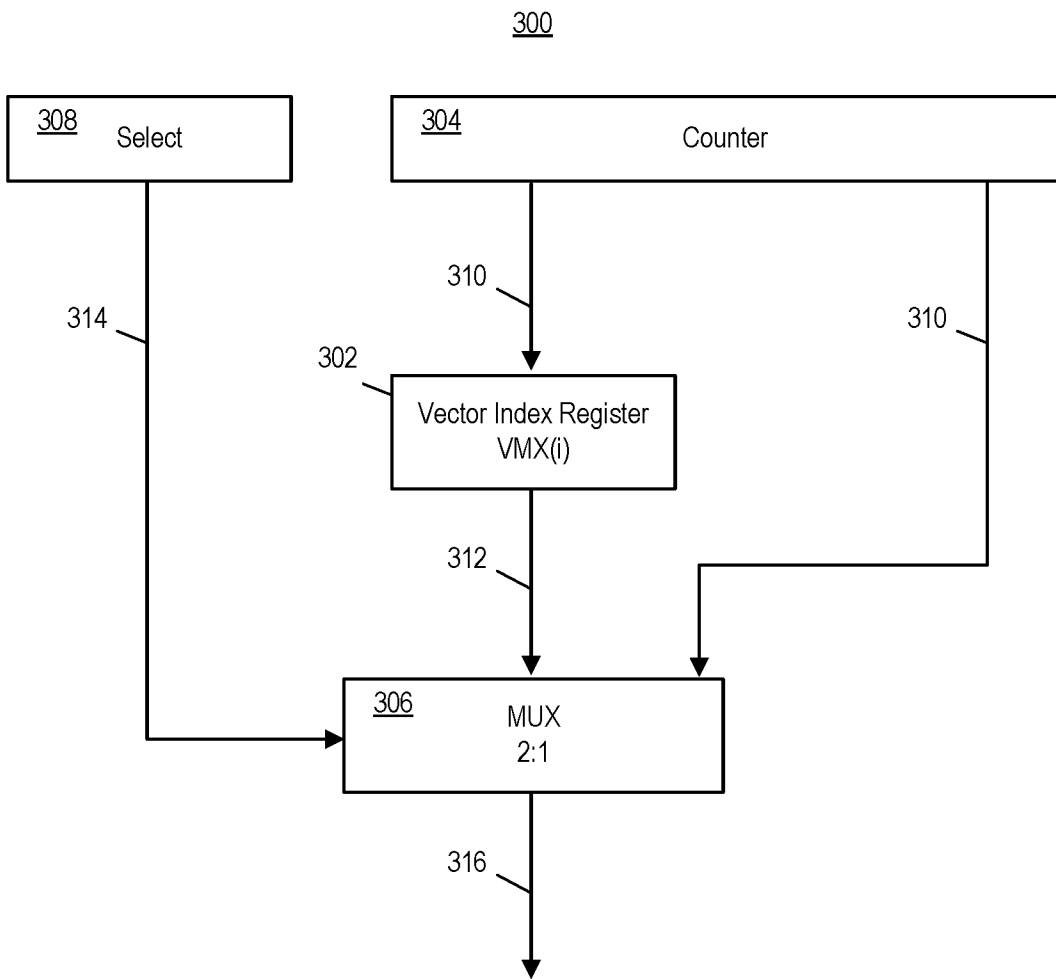


FIG. 3

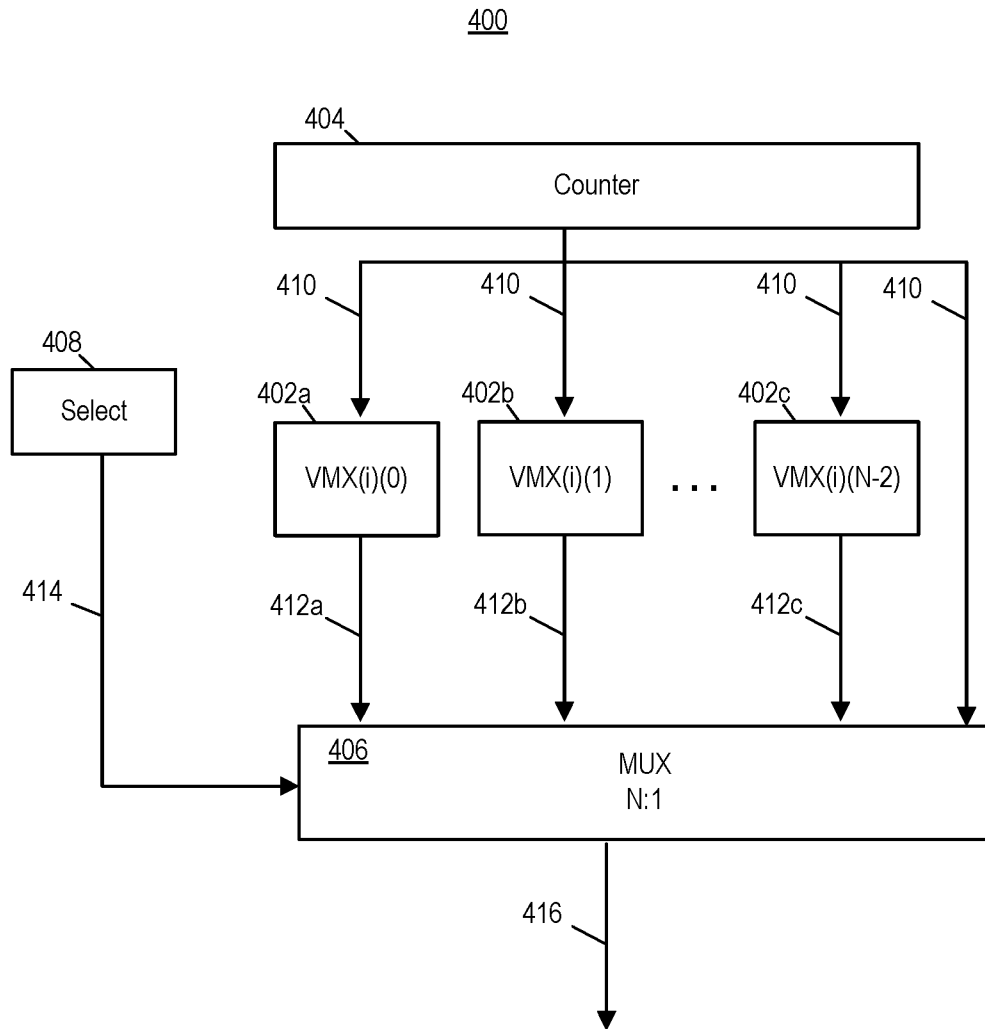


FIG. 4

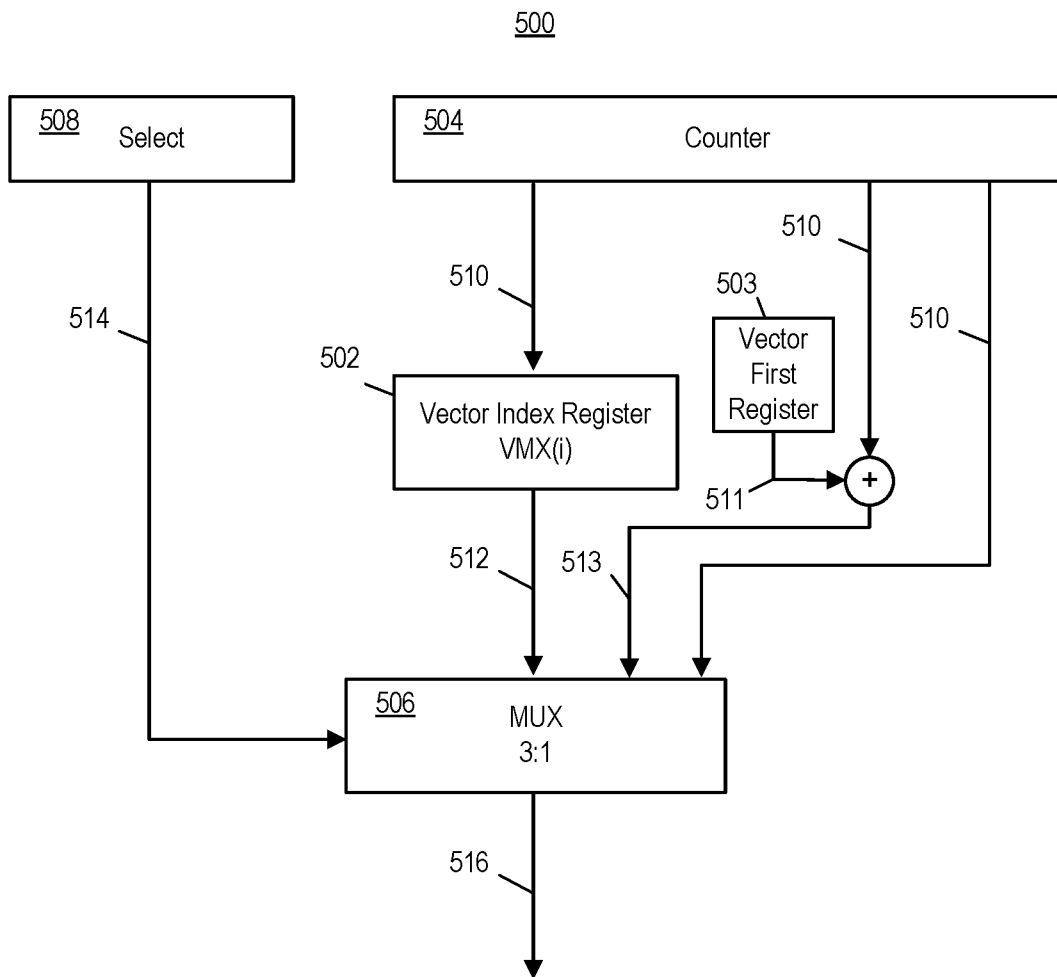


FIG. 5

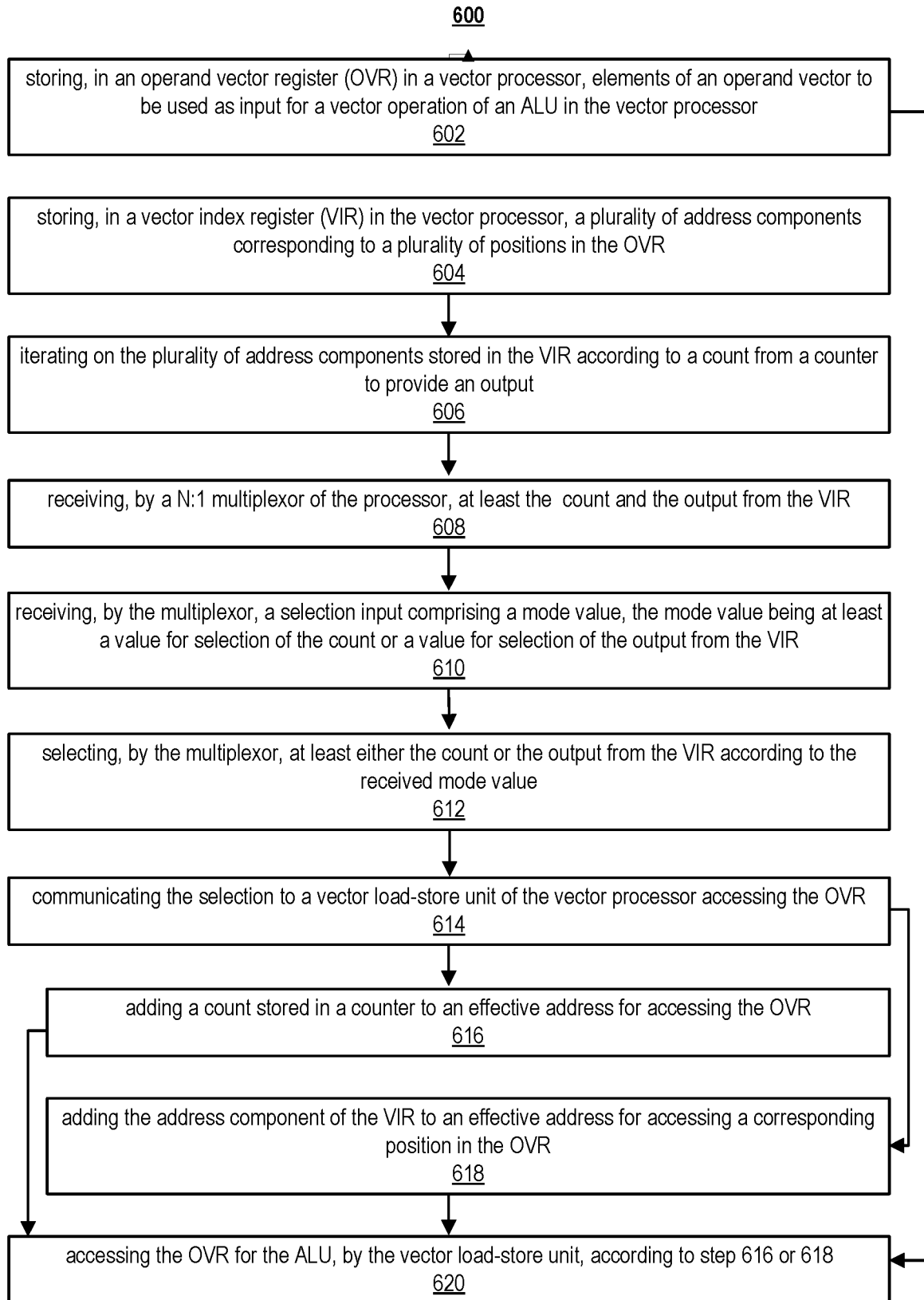


FIG. 6

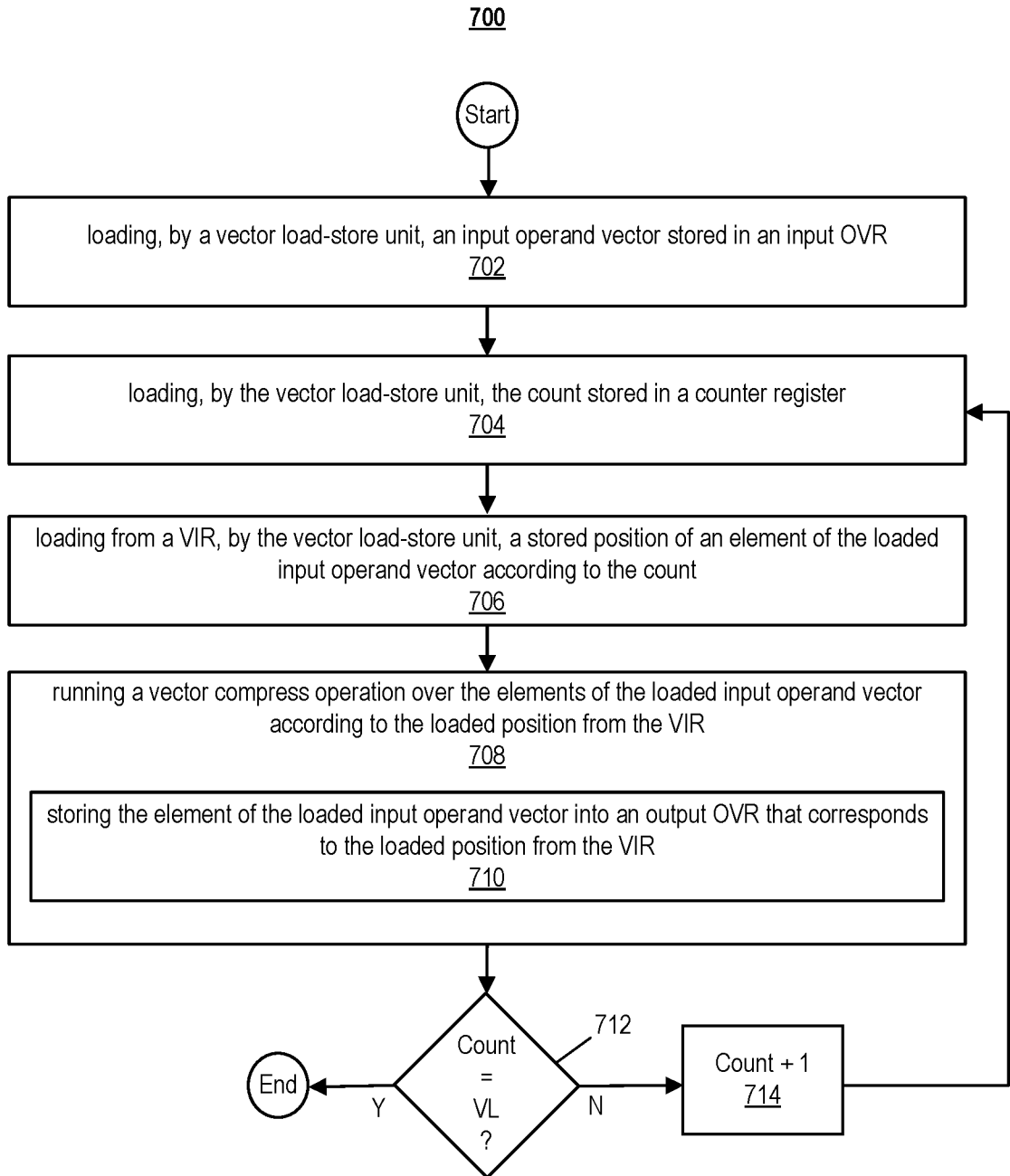


FIG. 7

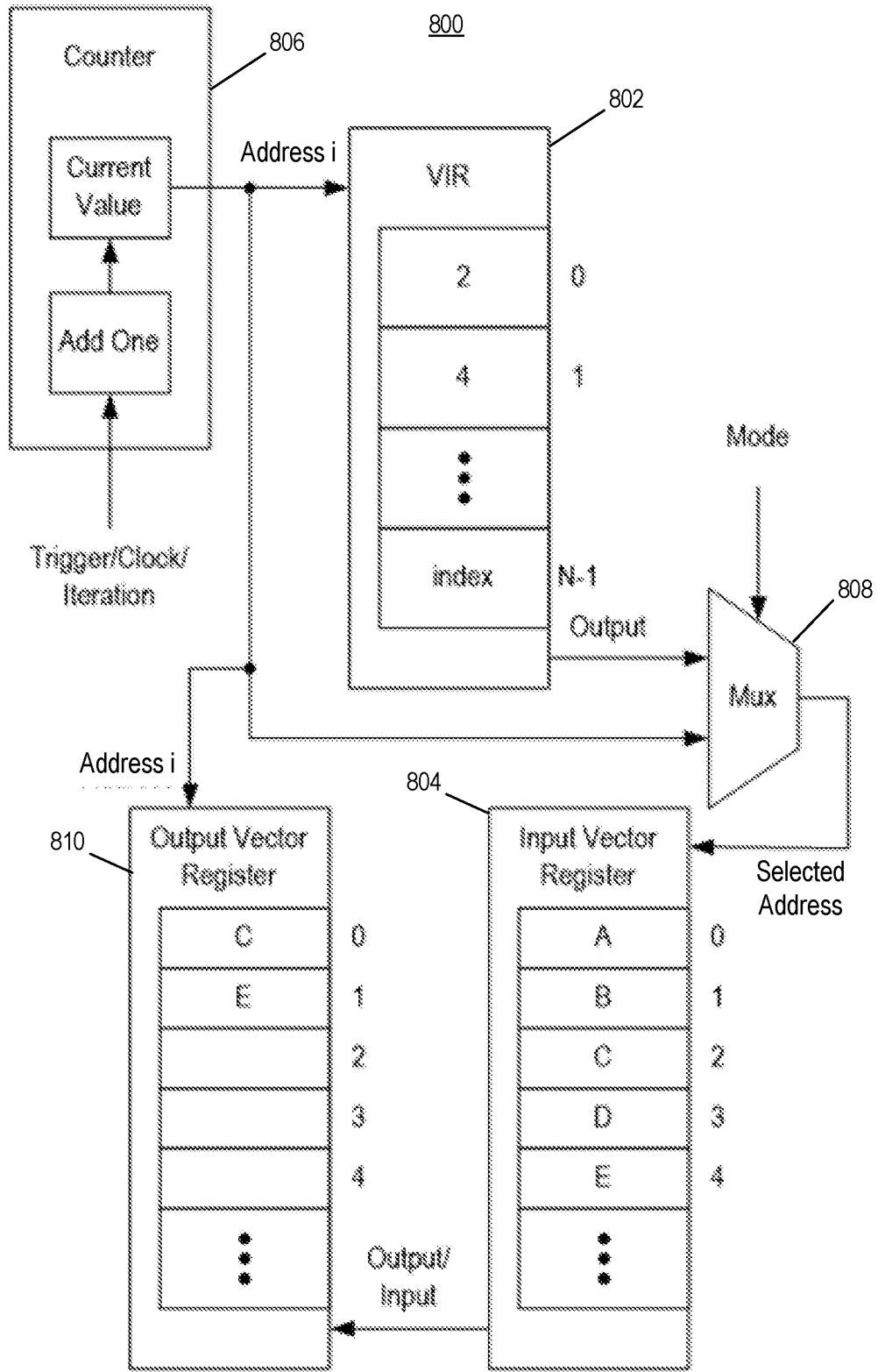


FIG. 8

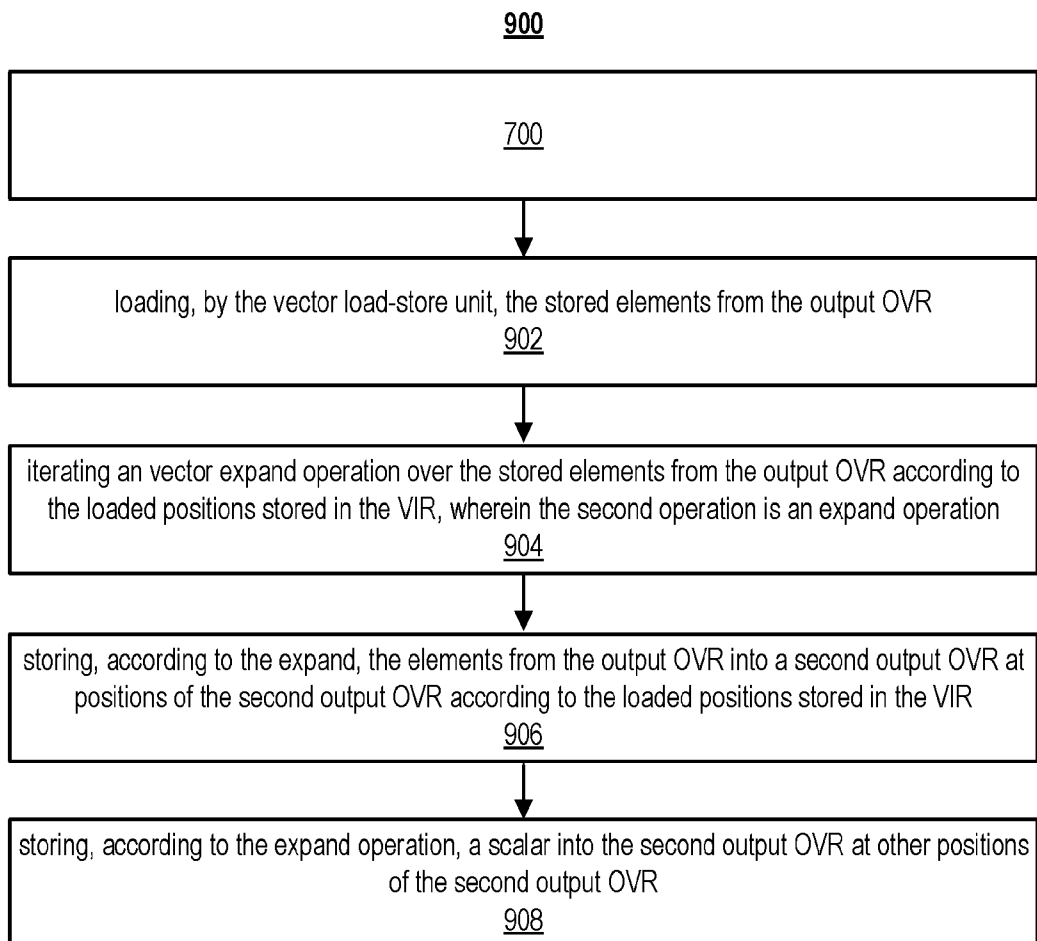


FIG. 9

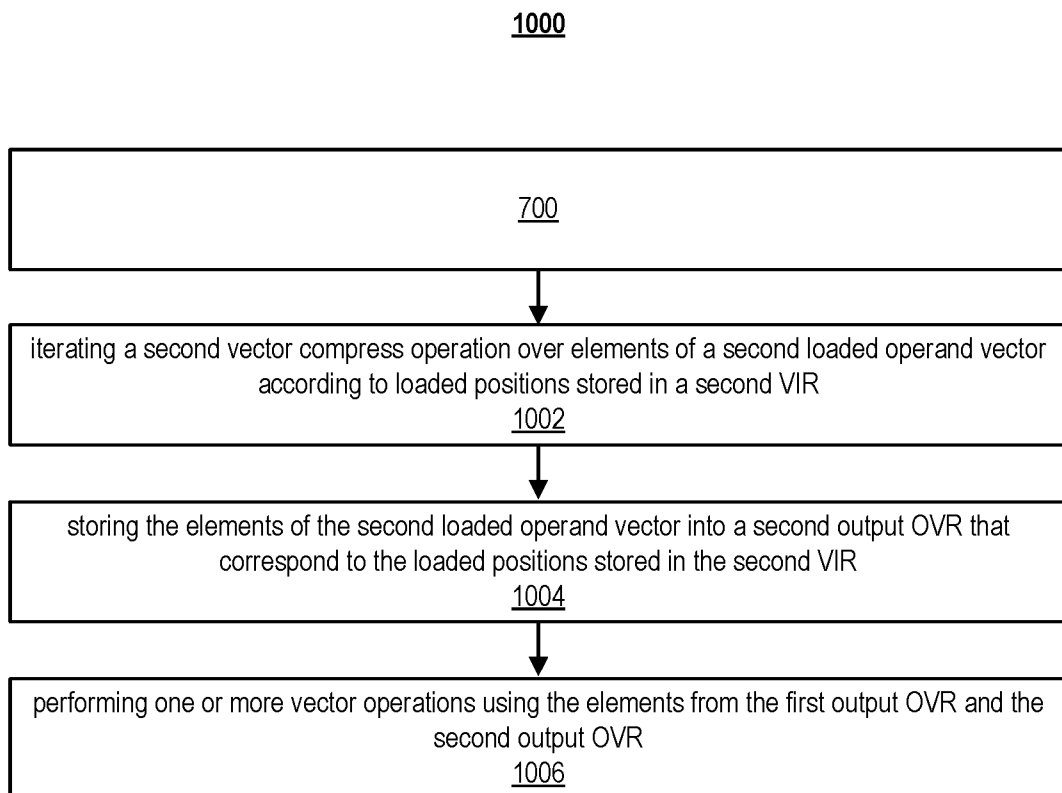


FIG. 10



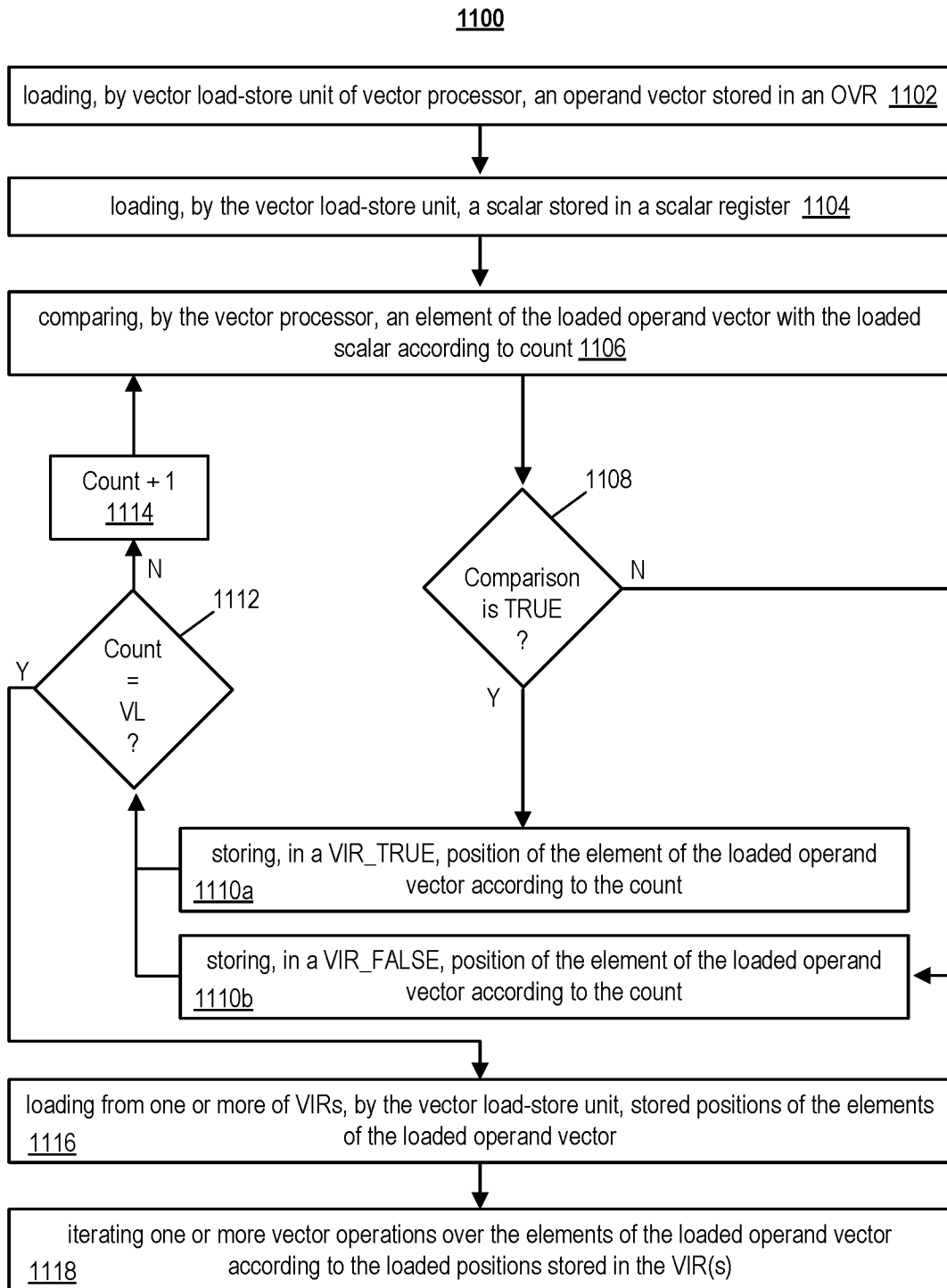


FIG. 11

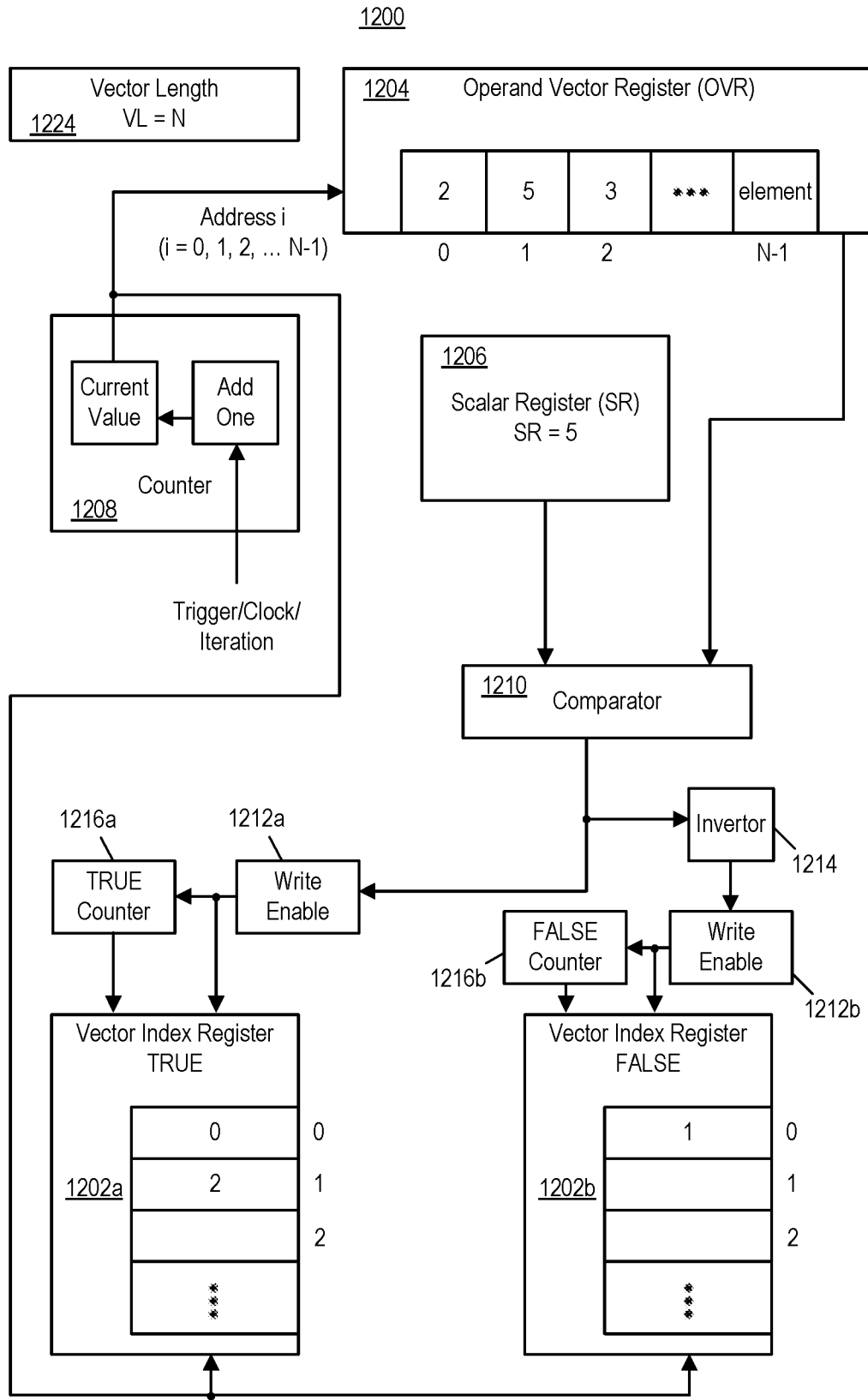


FIG. 12

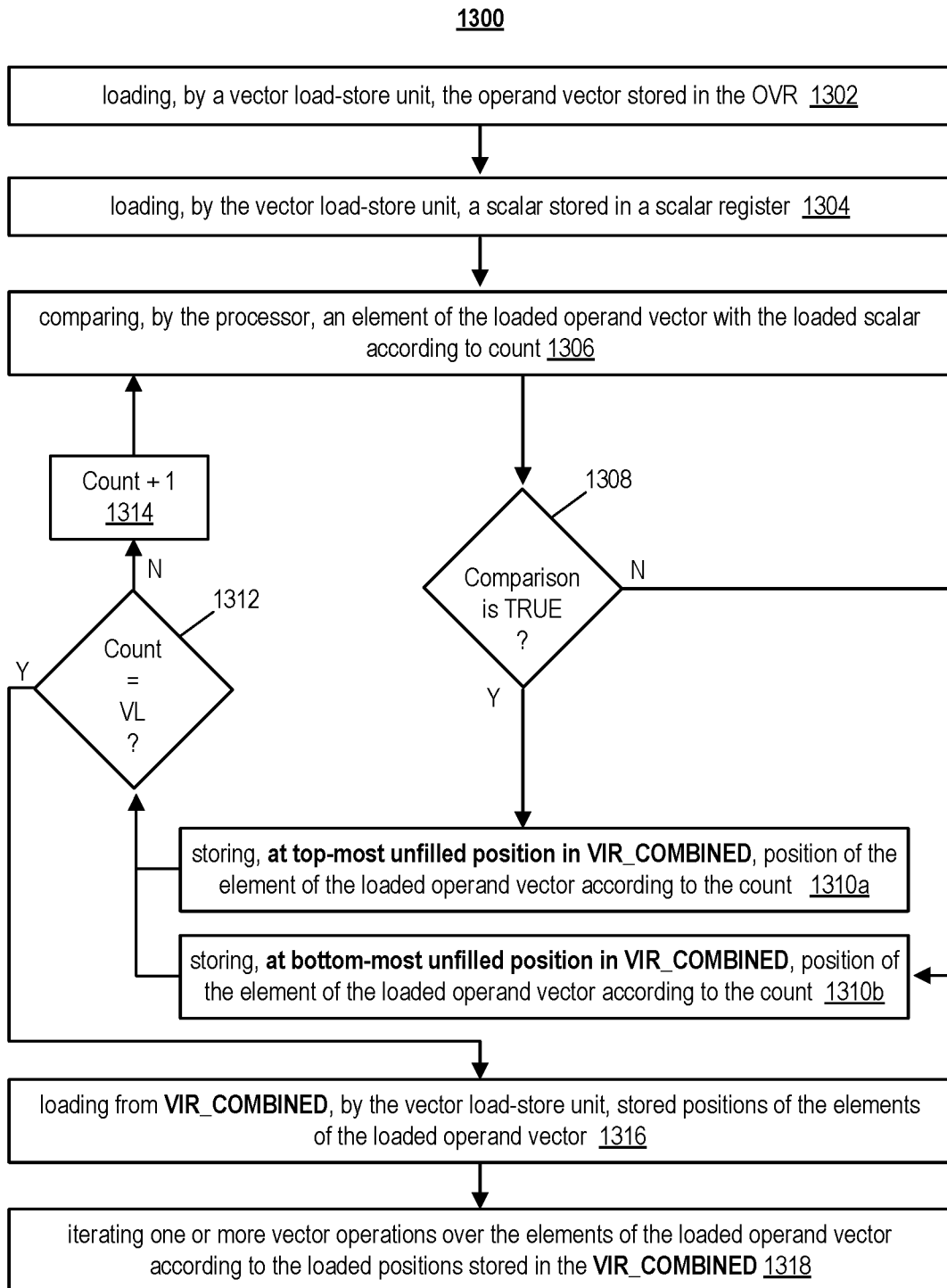


FIG. 13

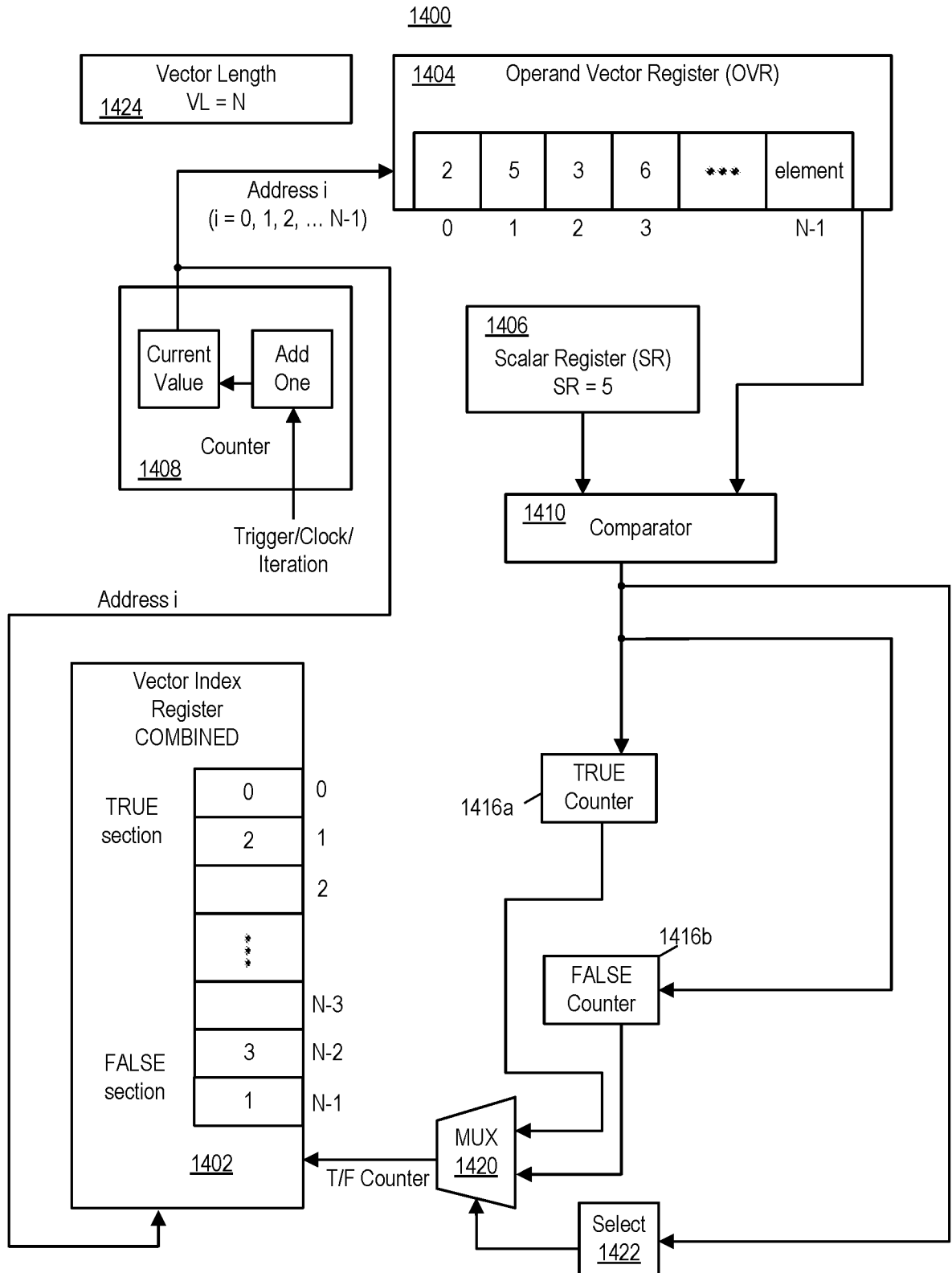


FIG. 14

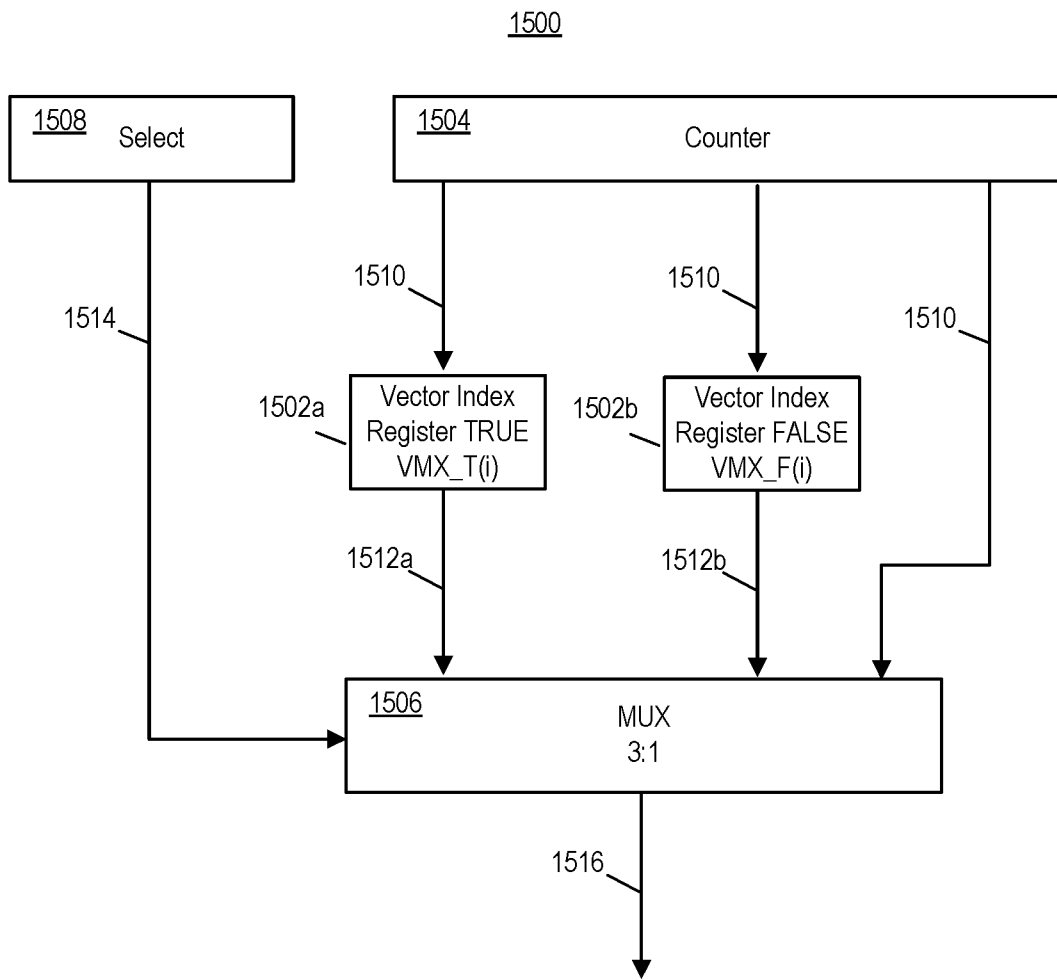


FIG. 15

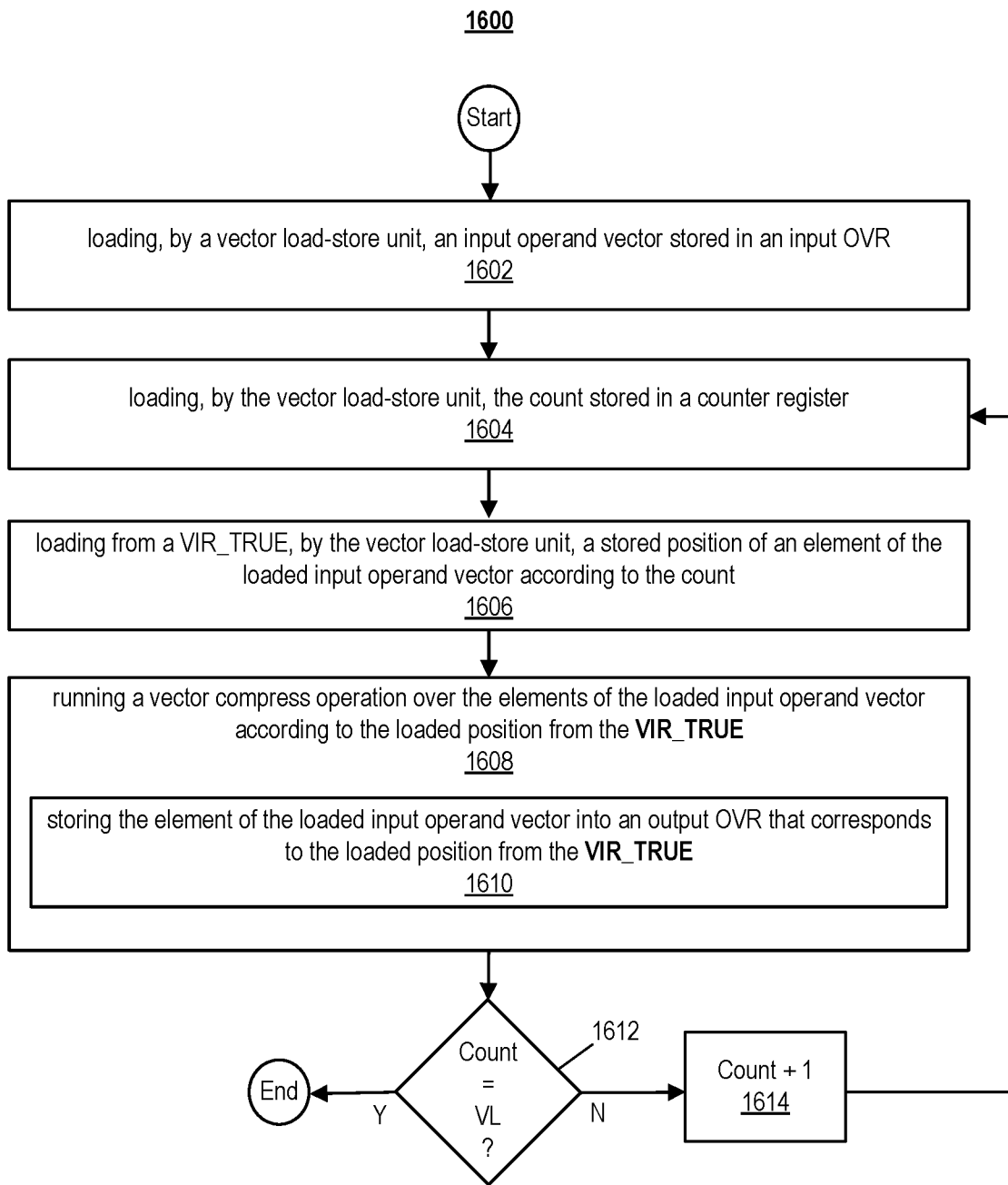


FIG. 16

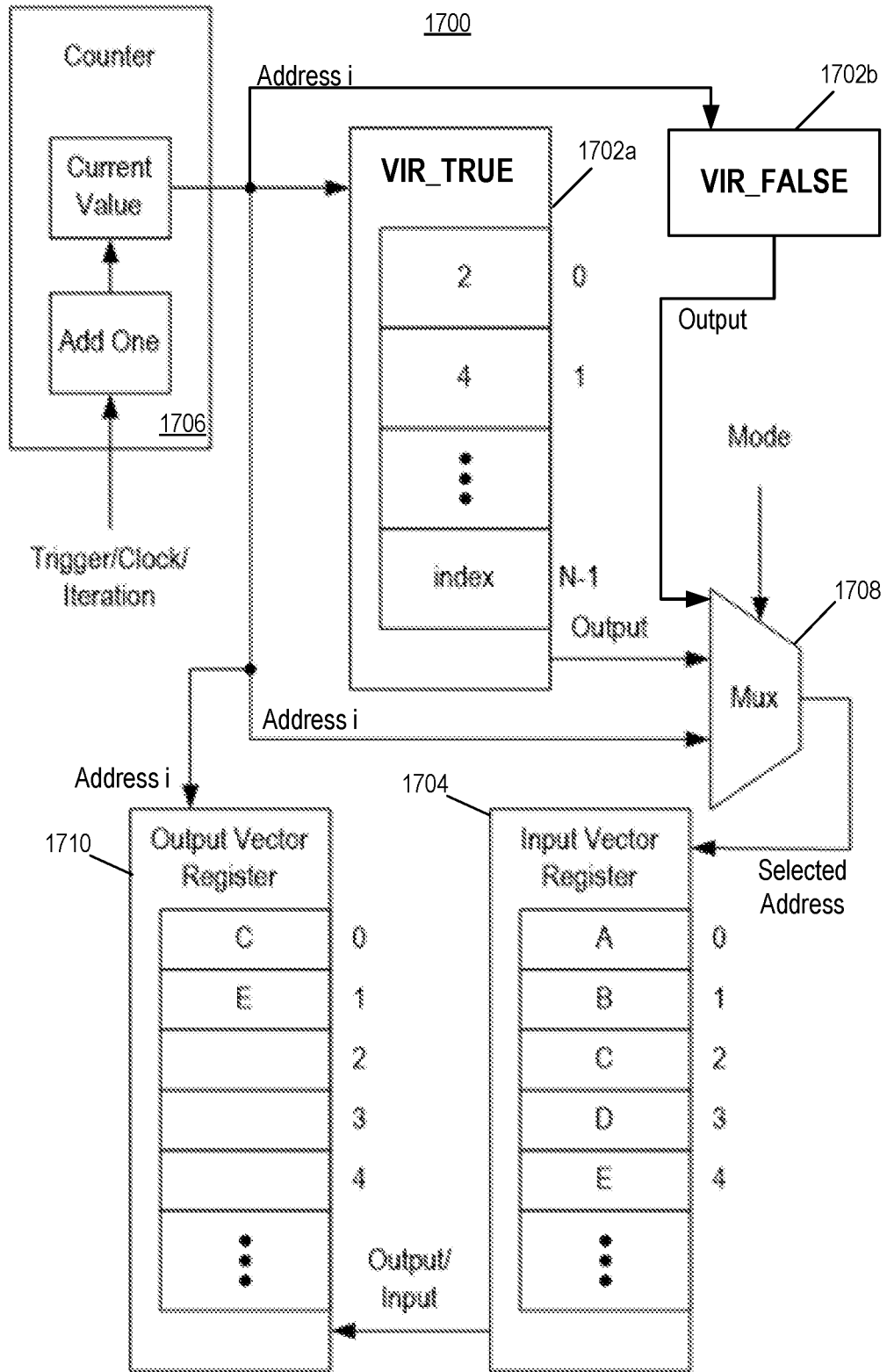


FIG. 17

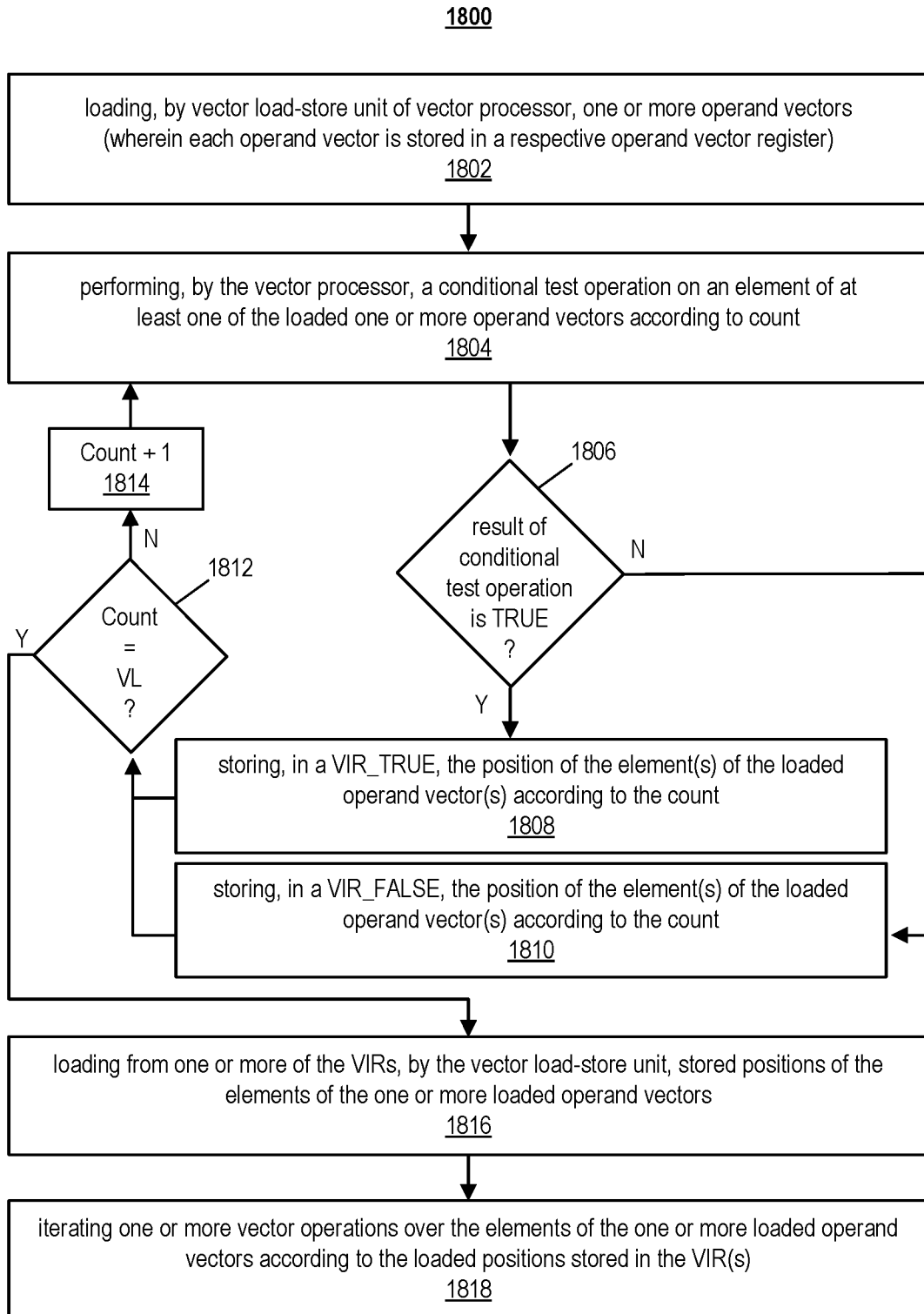


FIG. 18



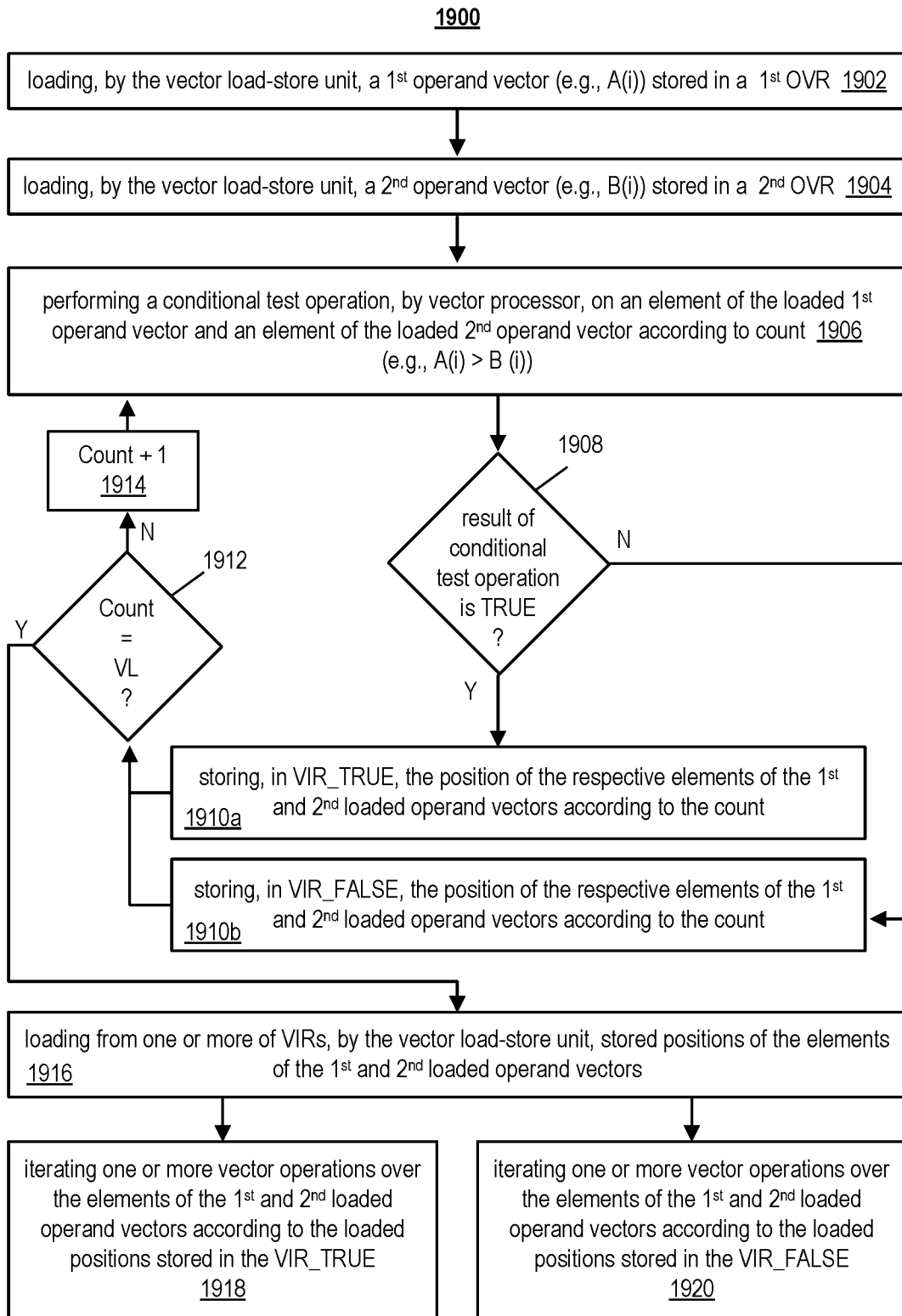


FIG. 19

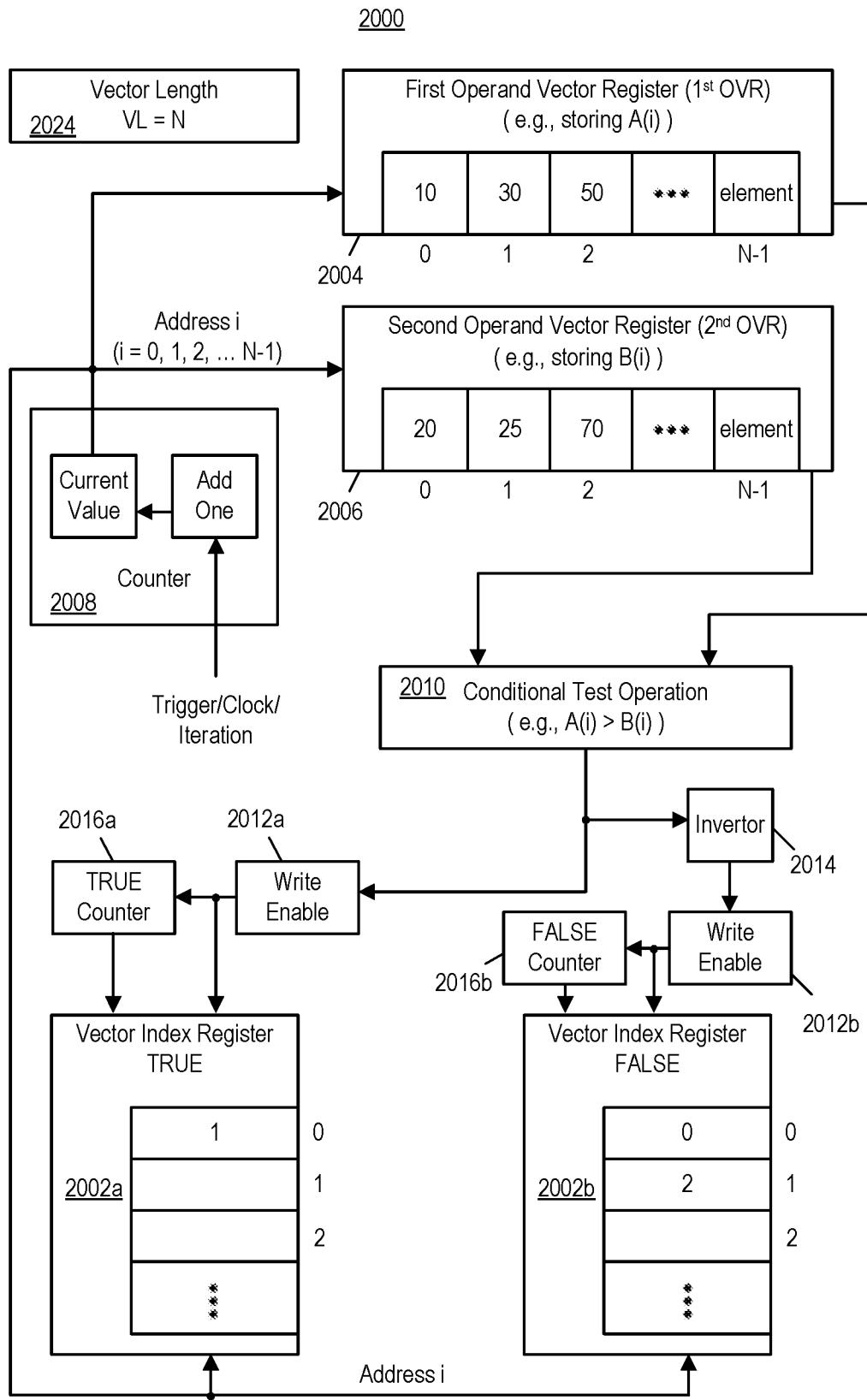


FIG. 20

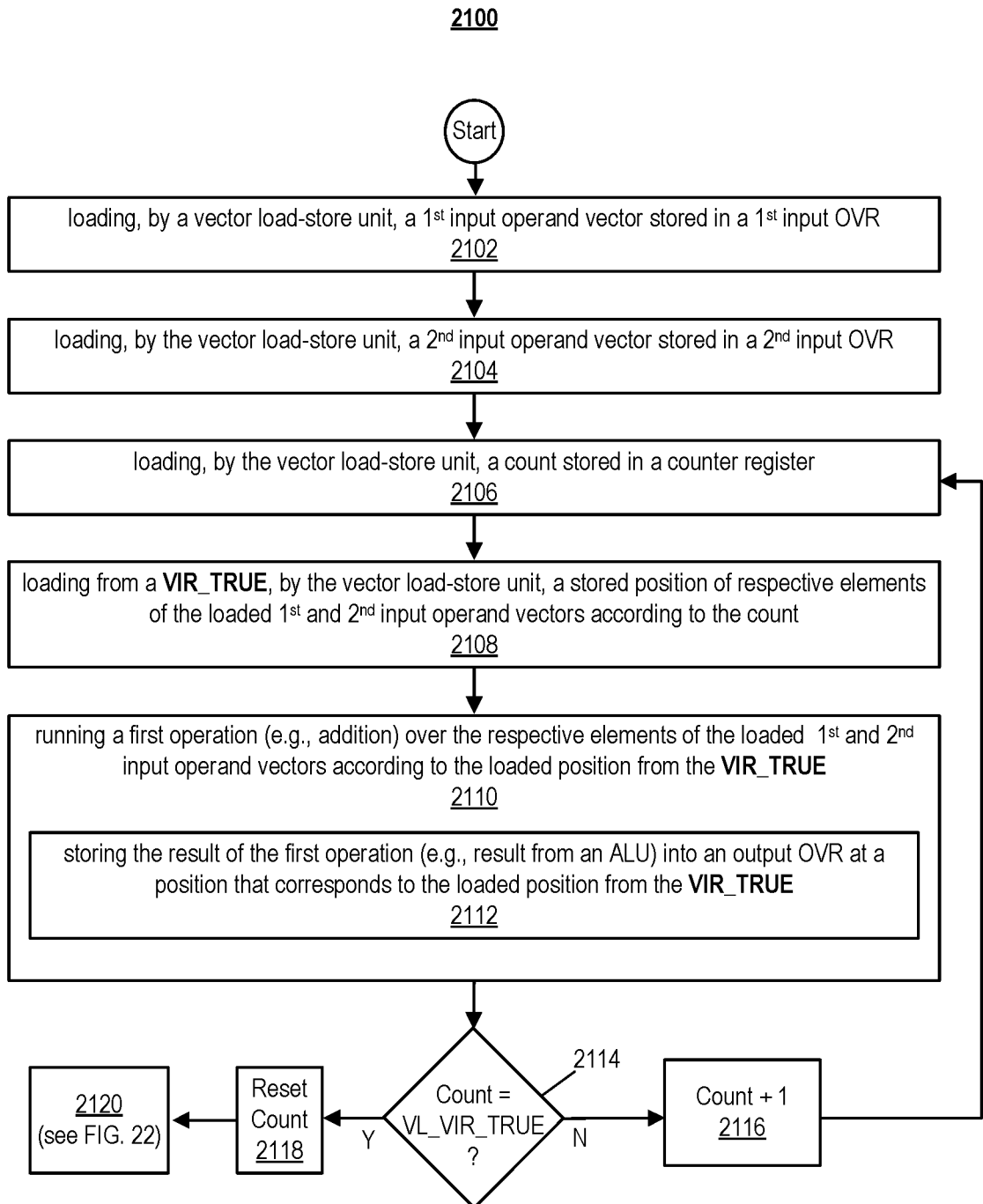
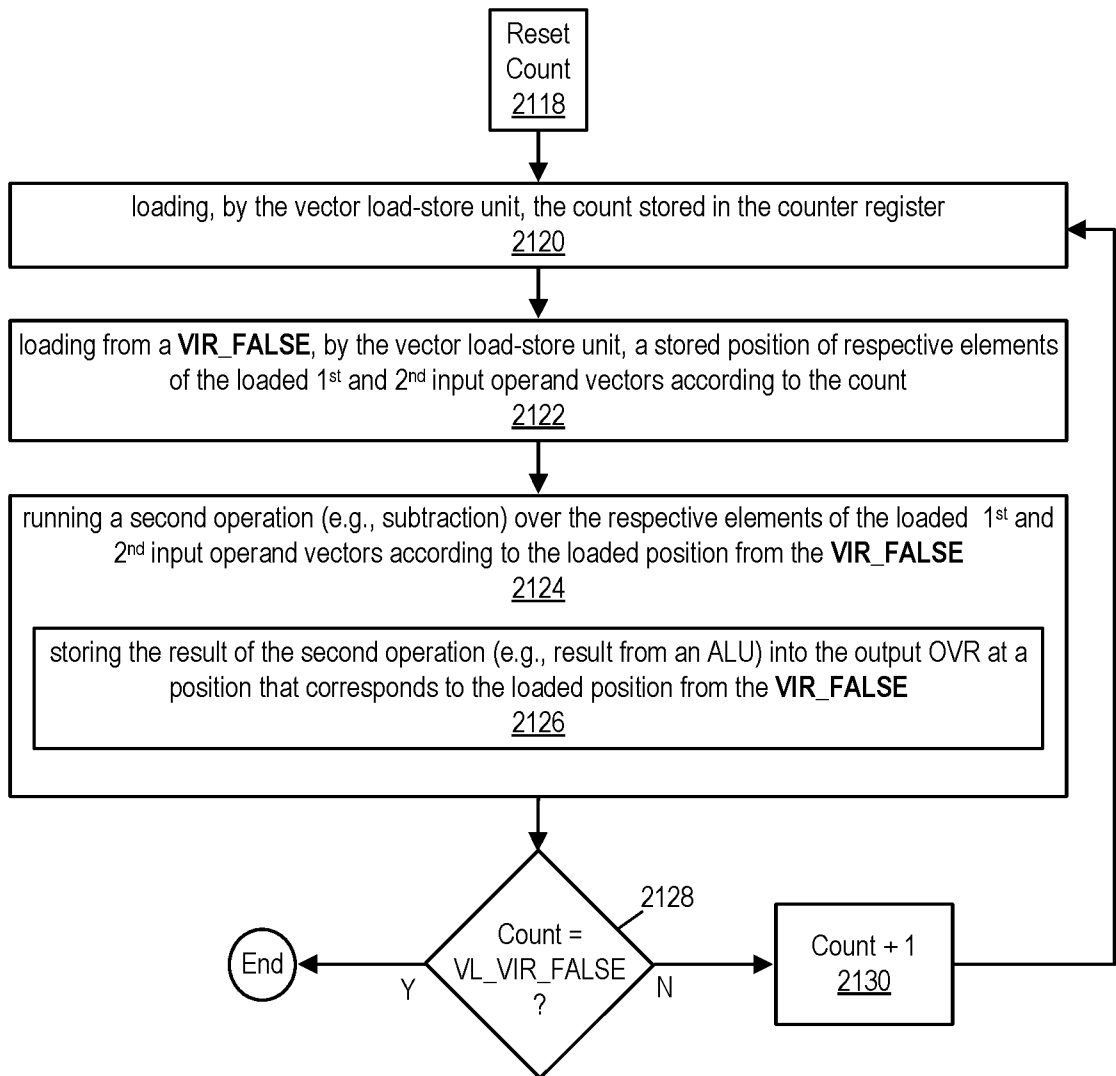


FIG. 21

**2100 Continued**



**FIG. 22**

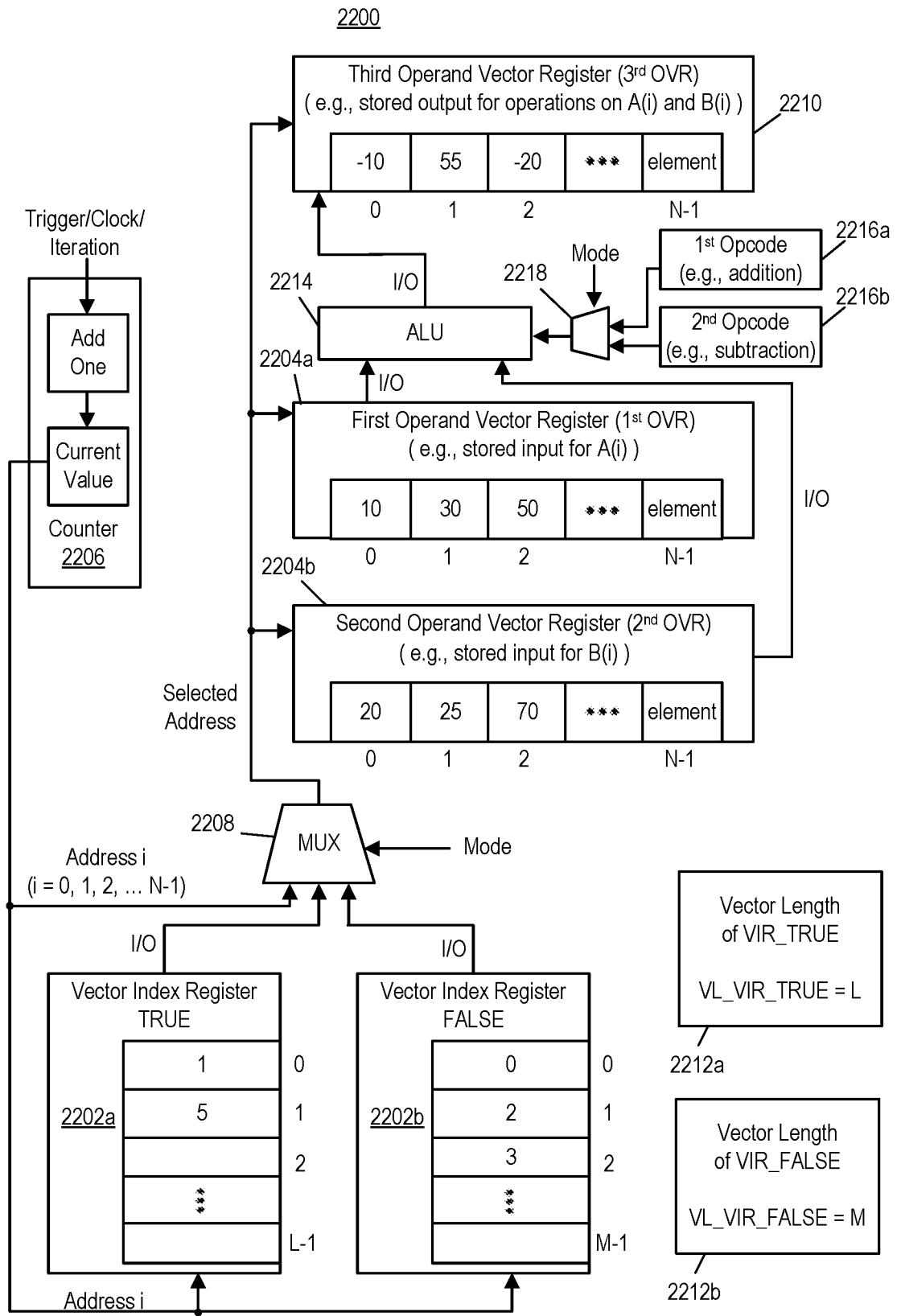


FIG. 23

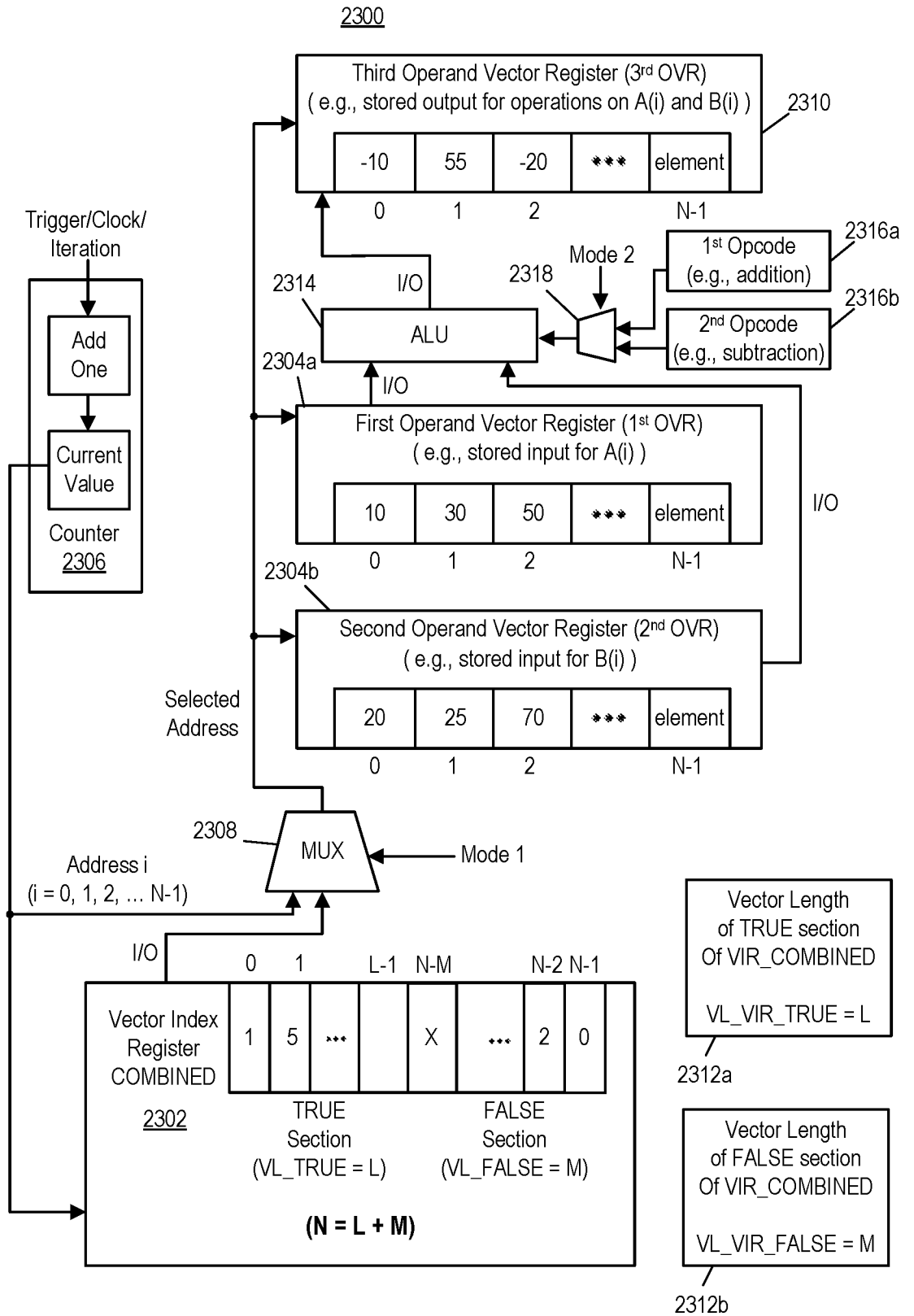


FIG. 24

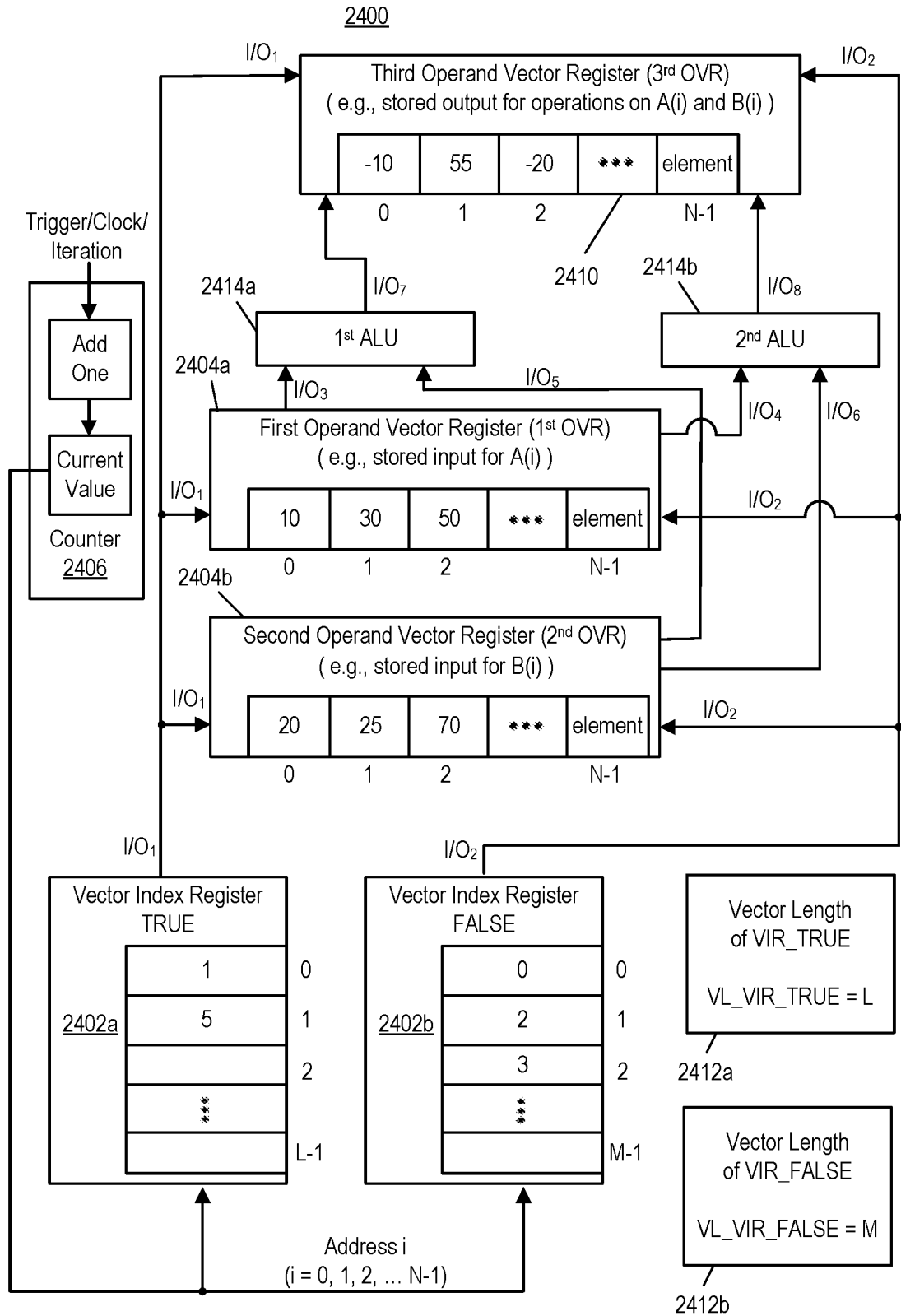


FIG. 25

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2020/028805****A. CLASSIFICATION OF SUBJECT MATTER****G06F 9/30(2006.01)i, G06F 9/355(2006.01)i, G06F 15/80(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**Minimum documentation searched (classification system followed by classification symbols)  
G06F 9/30; G06F 12/08; G06F 15/00; G06F 15/76; G06F 3/06; G06F 9/355; G06F 15/80Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
Korean utility models and applications for utility models  
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
eKOMPASS(KIPO internal) & Keywords: vector, register, index, conditional test, true, false, position, address**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0212354 A1 (TIBET MIMAR) 15 August 2013 paragraphs [0025]-[0040]; claims 2, 11; and figures 1-3	1-20
A	US 2008-0016320 A1 (AMITABH MENON et al.) 17 January 2008 paragraphs [0020]-[0046]; and figures 2-5	1-20
A	US 2016-0124651 A1 (TEXAS INSTRUMENTS INCORPORATED) 05 May 2016 paragraphs [0038]-[0122]; and figures 1-26	1-20
A	US 2006-0184765 A1 (STEVEN D. KRUEGER) 17 August 2006 paragraphs [0012]-[0015], [0027]; and figures 1, 5	1-20
A	US 2006-0136700 A1 (STEPHEN BARLOW et al.) 22 June 2006 paragraphs [0024]-[0037]; and figures 1-4	1-20

 Further documents are listed in the continuation of Box C. See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

28 July 2020 (28.07.2020)

Date of mailing of the international search report

**28 July 2020 (28.07.2020)**

Name and mailing address of the ISA/KR

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2020/028805**

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