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(54) IMPROVEMENTS IN OR RELATING TO TUNING CIRCUITS FOR COMMUNICATIONS RECEIVERS

(71) We LICENTIA PATENT-VERWALTUNGS-GESELLSCHAFT MIT BESCHRANKTER HAFTUNG, a company organised under the laws of Germany, of Theodor-Stern-Kai 1, 6 Frankfurt/Main 70, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The present invention relates to a tuning circuit for a superheterodyne receiver. Superheterodyne receivers with automatic frequency control (AFC) of the oscillator are known in which on deviation from a selected frequency the oscillator frequency is automatically readjusted by a control voltage to the value of the set frequency.

In a receiver circuit published in the periodical "NTZ" 1972, issue 11, pp. 507/508 there is provided a decade counter counting the oscillator oscilations, from the counter setting of which the control voltage is derived. To the load side of the decade counter is wired a frequency counter for indication of the receiving frequency, whereby the counter decade acts as pre-divider for the frequency counter. The frequency steps counted by the decade counter are smaller than the frequency steps indicated by the frequency counter.

In this known control unit the load side of the not indicated decade counter is wired to a digital-analogue converter which supplies a charging current to a storage capacitor. All output signals from the decade counter are evaluated for the derivation of the control voltage from the non-indicated counter decade. Four connecting leads from the decade counter and a correspondingly elaborate evaluation circuit are accordingly required. In the case of the known receiver circuit the control circut is constructed so that latching-in of the frequency between the values 1 and 0 of the non-indicated decade counter takes place.

The British Patent 1210803 discloses a similarly constructed control circuit for a receiver in which the detector designed in the form of a flip-flop is switched to and fro between two states by the output frequency of the oscillator requiring to be controlled during a periodically returning gate time.

The oscillator is readjusted in negative or positive direction as a function of the state in which the detector is left at the end of the gate time. In this patent, it is furthermore proposed to employ for the detector a decade counter designed so that a positive output pulse is produced during the states "1" to "5" and a negative output pulse during the states "6" to "0". With such a decade counter it is possible to achieve a latching-in between the states "5" and "6" whereby (whence) the circuit oscillates between these states.

The present invention has the object of providing a tuning circuit for a superheterodyne wireless receiver with a control circuit of the known kind in which latching-in settings are attained in the simplest possible way. In order to simplify the circuit the number of leads required between the counter from which the control signal is derived and the circuit member in which the control signal is generated should be as small as possible.

According to the invention, there is provided a tuning circuit for a superheterodyne communications receiver wherein: the frequency of an oscillator is automatically regulatable to maintain it at a required value, associated with a desired one of pluality of transmission channels having different frequencies, by a regulating voltage generated by a regulating circuit in response to deviation of the frequency from the required value; the regulating circut includes a counter arranged to count oscillations, derived from the oscillator and of a frequency re-

lated to the oscillator frequency, for successive predetermined periods, such that the count in the counter at the end of each period represents a number of frequency steps by which the oscillator frequency deviates from the required value; the counter is arranged to count a maximum of five such steps, which corresponds to the maximum number of frequency steps between adjacent channels; the regulating voltage for causing the oscillator frequency to vary in one sense is derived from a logical combination of the states of first and second outputs of the counter associated with the most significant and next-to-most significant bits of the counter respectively; and the regulating voltage for causing the oscillator frequency to vary in the opposite sense is derived from the state of the said second output.

In order that the invention may be clearly understood and readily carried into effect an example thereof will now be described with reference to the accompanying drawings of which,

Figure 1 shows a heterodyne receiver with a tuning circuit,

Figure 2 shows the counting state, in encoded form, of a counter in accordance with the counting pulses fed to the counter,

Figure 3 shows a known decimal counter,

Figure 4 shows a counter used in the case of the invention, and

Figure 5 shows the circuit of a NOR gate.

In Figure 1 high frequency signals are received by an antenna 1 and pass to a HF amplifier 2 and then to a mixing stage 3. There follows an IF amplifier and demodulating stage 4 and a LF stage 5 feeding a loud speaker 6. For the generation of an intermediate frequency there are fed to the mixing stage 3 the oscillations of an oscillator 7 the frequency of which can be influenced by a regulating voltage (tuning voltage). The oscillations of the oscillator 7 are also fed to a wideband amplifier 8, which converts them into rectangular oscillations of the same frequency, which can be counted by a counter. One example of a suitable circuit for the wideband amplifier 8, which is used both in FM operation and in AM operation, is described in our British Patent 1 483 654. The digital output signals from the wideband amplifier 8 pass to a predivider 9, the division ratio of which can be adjusted. The pre-divider 9 is followed by a gate 10 which is controlled at its control input 22 by pulses in such maner that the sub-divided rectangular oscillations from the pre-divider 9 pass to the input E of a counter 11 only during a predetermined time, the gating time, and are then counted. The periodically recurring gating time may for example be 10 ms. The 10ms pulses may be generated by a quartz oscillator, not illustrated, followed by a frequency divider.

For further explanation, it will be assumed that the heterodyne oscillator is adjusted to the USW or VHF band. The division ratio of the divider 9 may be 100:1. For a gating time of 10ms, the counter will produce a count which increases (or decreases) in steps of one for each 10kHz step increase (or decrease) in the frequency of the oscillator. Thus the counting steps of the counter may be regarded as corresponding to 10kHz frequency steps. Upon reception of a transmitted signal—when therefore the oscillator 7 is adjusted to a required frequency—the counting state of the counter 11 is four or nine. This will be explained in more detail hereinafter. Between these two counting states there are five counting steps (frequency steps each of 10 kHz) corresponding to a channel spacing of 50 kHz. The transmitters in the USW band indeed generally differ from one another by 100 kHz, but in some cases this spacing is only 50 kHz, for which reason a channel spacing of 50 kHz is here taken as a basis.

The counter 11 also has a frequency division in the ratio 10:1. From its output 1A the pulses pass to a counter and control part 12 which, in conjunction with the counter 11, counts the reception frequency, which is then displayed visually on a display 13 which may be digital display. The reception frequency is obtained by counting the oscillations of the oscillator and subtracting the IF.

The counter 11, the construction of which will be further described hereinafter includes two output terminals C and D at which various combinations of the logical signals "0" and "1" appear according to the state of the counter. These signals are illustrated in Figure 2. At the required frequencies, spaced by 50 kHz, which are associated with the reception frequencies, of the transmitters, there is a logical "0" on the output terminal C and a logical "1" on the output terminal D. For these values, which represent respectively the counter states of four and nine present in encoded form, no regulating voltage for altering the oscillator frequency is generated. The two output terminals C and D are connected via a NOR gate 14 to a lowpass filter (integrating member) 16 which is followed by a direct voltage amplifier 18. With the logical signals associated with the counter states four and nine on the output terminals C and D there occurs at the output 14a of the NOR gate 14 a logical "0" which corresponds to a level of 0 V. The lowpass 16 cannot therefore generate any voltage. Also, another lowpass filter 15, which is controlled directly from the output terminal C, cannot generate any voltage owing to the "0" potential at C.

If in contrast a deviation of the oscilla-

tor frequency from the required frequency occurs—the counter state then not being four or nine a regulating voltage is generated for retuning the oscillator to the value of the required frequency. For the counter states two and three or seven and eight terminal C is at logical "1" and the output terminal D is at logical "0". The output 14a is in fact at "0" potential again, so that no voltage occurs at the output of the lowpass filter 16, but the lowpass filter 15, owing to the logical "1" fed to it in the form of a positive voltage level, generates a positive voltage. The voltage is amplified by a following direct voltage amplifier 17 and appears on its output lead 19 as a regulating voltage U_1 or as a regulating change of a predetermined basic voltage. Since the logical "1" occurs periodically at the output terminal C, pulses are fed in succession to the lowpass filter 15. From them the lowpass filter 15 generates a direct voltage owing to its integrating action. The voltage U_1 passes via the lead 21 to the oscillator 7, the frequency of which is thereby raised until the required frequency is again reached. The change of the frequency of the oscillator 7 may be effected via a voltage-dependent capacity diode. When the oscillator 7 has attained its required frequency the counter state of the counter 11 is again four or nine, so that no further regulating voltage is generated.

Whilst for the counter states two and three or seven and eight an increase of the oscillator frequency is effected, as is indicated in Figure 2 by the brackets $+\Delta f$, for the counter states zero and one or five and six a regulating voltage or a change of basic voltage is generated which effects a reduction in the frequency of the oscillator which has deviated from the required frequency. It can be seen from Figure 2 that for the last-mentioned counter states both output terminals C and D are at "0" potential. Hence there occur at the output 14a of the NOR gate 74 "1" pulses which are fed to the lowpass filter 16. Owing to the integrating action of the lowpass filter 16 the direct voltage amplifier 18 is controlled by a direct current. In comparison with the direct voltage amplifier 17 the direct voltage amplifier 18 effects a reversal of the direction of regulation, so that the output current J_2 in the output lead 20 is of different polarity to the output current J_1 of the direct voltage amplifier 17. By the regulating voltage U_2 the oscillator 7 is regulated to the required frequency by reduction of its actual frequency. The output currents effect a charging or discharging of the condensor 31 connected to the lead 21, the voltage of the condenser being thereby correspondingly adjusted and being the regulating voltage. Since with the last-mentioned counter states the output terminal C is at "0" potential, the lowpass filter 15 does not generate any voltage, so that only the voltage U_2 is effective. The two direct voltage amplifiers 17 and 18 may for example be of type CA 3080 (RCA).

When hitherto a counter state has been referred to, there has been meant the state to which the counter has been adjusted at the end of a gating time, which is equal to the counting time. This state is maintained during the counting interval between two successive gating times up to the beginning of the next gating time at which time the counter is reset. However, from the commencement of a new gating period to its end the counter states between zero and nine successively occur, and correspondingly the logical signals at the output terminals C and D change before these attain their final logical value at the end of the gating period. Voltages U_1 and U_2 are therefore already generated before the attainment of the counter state at the end of the gating period. It has been found, however, that these voltages substantialy cancel in static average value and therefore have no impairing effect. Even when a slight residual voltage remains this has no disturbing effect as regards the operation of the tuning circuit.

However, it is also possible to arrange by means of logical gates (not illustrated) that an evaluation takes place only of the counter state occurring at the end of the gating period and hence the regulating voltage is generated only in the counting intervals.

The tuning circuit may also be used for the other reception bands SW, MW or LW. For SW the division ratio of the divider 9 is altered in such manner that the frequency steps counted amount to 1 kHz in accordance with a 5 kHz channel spacing. The alteration of the division ratio may take place in advantageous manner for different wavebands in step with the adjustment of the reception band.

The counter 11 used in the tuning circuit will now be explained in more detail with reference to Figures 3 and 4. In Figure 3 is illustrated a known decimal counter, which for example may be type SN 7490 (Texas Instruments). The decimal counter 11 is formed in known manner by combining four flip-flops FF1-FF4, the first flip-flop FF1 of which forms a counter counting up to two and the other three flip-flops FF2-FF4 of which form a counter counting up to five. Since as is known a counter may be employed as a divider stage, the pulses fed to the counting input E occur at the output 1A of the counter 11 subdivided in the ratio 10:1. The counter 11 has four output terminals A, B, C, D the logical state of which gives the number of pulses counted in the dual code.

The known decimal counter is, in accordance with Figure 4, so converted that it is possible to utilise only a part of the counter state present in encoded form at the output terminals A to D in order to obtain the regulating information. This is achieved by feeding the counting pulses fed to the input E of the counter 11 directly to the input BD of the counter (FF2-FF4) counting up to five. Furthermore, the output terminal C, which in the known counter is associated with the value four in the binary system (in the counter state four there appears, in the known counter, a logical "1" at the output terminal C, whilst the other output terminals are at "0" potential); that terminal C is connected via an inverter 30 to the input A_{in} of the counter (flip-flop FF1) counting up to 2. This gives the logical state shown in Figure 2 of the output terminals A-D in accordance with the counting pulses fed to the input E. It is sufficient to make use of the logical signals "0" and "1" framed at the output terminals C and D for the regulating voltagle, so that the output terminals A and B are not needed for this purpose. Since an evaluation takes place directly on the basis of the logical potentials, a decoder is also unnecessary, so that the tuning circuit is simple.

By connecting the output terminal C to the input A_{in} of the flip-flop FF1 via the inverter 30 it can be arranged that the counter of Figure 4 also effects a frequency division of the pulses fed to it, in the ratio 10:1. The pulses subdivided in frequency may be taken from the output 1A which is connected to the output terminal A. The frequency dividsion of 10:1 can be seen in Figure 2 from the broken-line frames of the potentials at the output terminal A. The potential at the output terminal A is, during each five pulses, alternately "1" and "0".

Figure 5 shows as an example the circuit of the NOR gate 14 already referred to. The signals fed via the two input leads 23 and 24 pass via resistors 25, 26 to the base of a transistor 28. If desired the base may be connected to a reference potential (usually ground) via the resistor 27 shown in broken lines. The output signals from the NOR gate on the output lead 14a are taken from the collector of the transistor 28. Furthermore, the collector is connected via a working resistor 29 to an operating voltage $+U_P$, which corresponds approximately to the positive voltage level which is associated with a logical "1".

WHAT WE CLAIM IS:—

1. A tuning circuit for a superheterodyne communications receiver wherein: the frequency of an oscillator is automatically regulatable to maintain it at a required value, asociated with a desired one of a plurality of transmission channels having different frequencies, by a regulating voltage generated by a regulating circuit in response to deviation of the frequency from the required value; the regulating circuit includes a counter arranged to count oscillations, derived from the oscillator and of a frequency related to the oscillator frequency, for successive predetermined periods, such that the count in the counter at the end of each period represents a number of frequency steps by which the oscillator frequency deviates from the required value; the counter is arranged to count a maximum of five such steps, which corresponds to the maximum number of frequency steps between adjacent channels; the regulating voltage for causing the oscillator frequency to vary in one sense is derived from a logical combination of the states of first and second outputs of the counter associated with the most significant and next-to-most significant bits of the counter respectively; and the regulating voltage for causing the oscillator frequency to vary in the opposite sense is derived from the state of the said second output.

2. A circuit according to Claim 1, wherein a further counter, arranged to count to a maximum of two, is connected to count oscillations of the state of the said second output, and a frequency indication circuit is connected to a count output of the further counter.

3. A tuning circuit according to claim 1 or 2 wherein the oscillations of the oscillator are applied to the said counter via a gating circuit.

4. A tuning circuit according to claim 1, 2 or 3 including first and second lowpass filters and a NOR gate arranged so that the signals from the second output of the second counter stage are provided to the first lowpass filter and the signals from the second and third outputs are applied via the NOR gate to the second lowpass filter.

5. A tuning circuit according to claim 4 including first and second direct voltage amplifiers, controlled by the output voltages of the first and second lowpass filters respectively, providing output direct voltages or voltage variations forming together the said regulating voltage and arranged so that one of the said amplifiers effects a reversal of the direction of the regulation.

6. A tuning circuit according to any of the preceding claims including a predivider, having a variable division ratio, connected between the oscillator and the counter.

7. A tuning circuit according to claim 6 wherein the division ratio of the pre-divider is variable in response to adjustment of the receiver to a required frequency band such that the required frequencies in different

wavebands are associated with the same counter states.

8. A tuning circuit according to any of the preceding claims, for a V.H.F. waveband with a transmission channel separation of 50 kHz, wherein the counter is a binary code counter the counts of which represent number of frequency steps each of 10 kHz and the counts "four" and "nine" correspond alternately to successive required values of frequency.

9. A tuning circuit according to any of claims 1 to 7, for a short wave band with a transmitter separation of 5 kHz, wherein the counter is a binary code counter the counts of which represent numbers of frequency steps each of 1 kHz and the counts "four" and "nine" correspond alternately to successive required values of frequency.

10. A tuning circuit substantially as herein described with reference to the accompanying drawings.

11. A superheterodyne receiver including a tuning circuit according to any of the preceding claims.

12. A superheterodyne receiver according to claim 10 and further including a digital display for displaying the frequency to which the receiver is tuned.

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Agent for the Aplicants

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1573224 COMPLETE SPECIFICATION
3 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

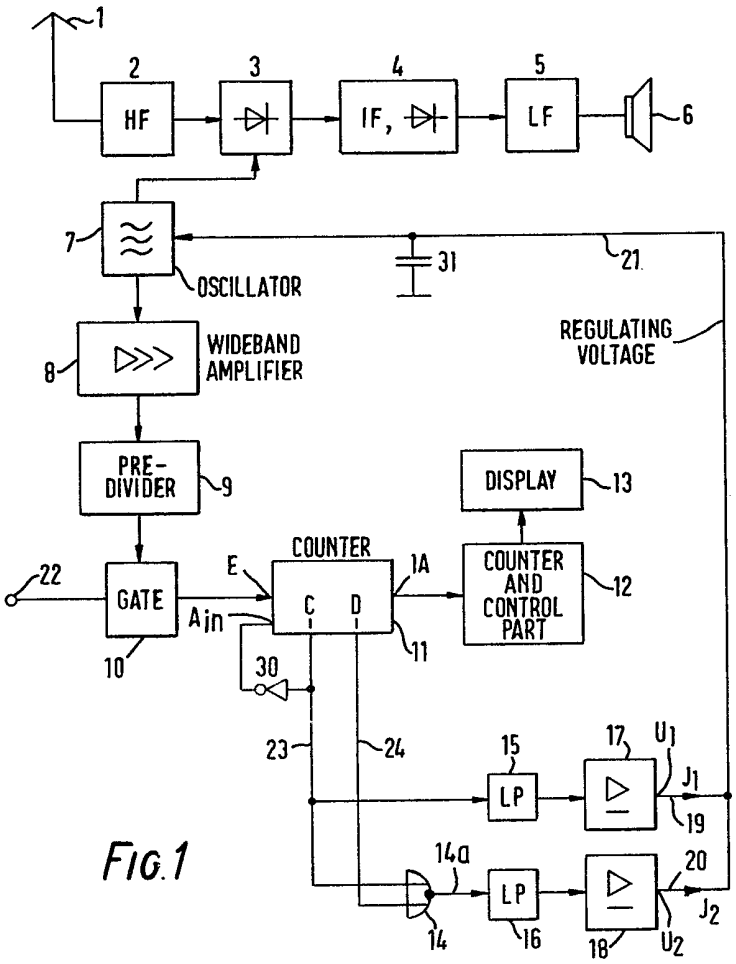

FIG.1

E	A	D	C	B	
0	0	0	0	0	$-\Delta f$
1	0	0	0	1	
2	1	0	1	0	$+\Delta f$
3	1	0	1	1	
4	1	1	0	0	REQUIRED FREQUENCY
5	1	0	0	0	$-\Delta f$
6	1	0	0	1	
7	0	0	1	0	$+\Delta f$
8	0	0	1	1	
9	0	1	0	0	REQUIRED FREQUENCY
0	0	0	0	0	$-\Delta f$
1	0	0	0	1	
2	1	0	1	0	

FIG. 2

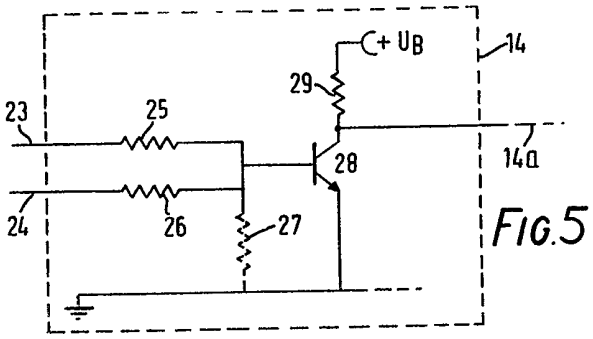

FIG. 5

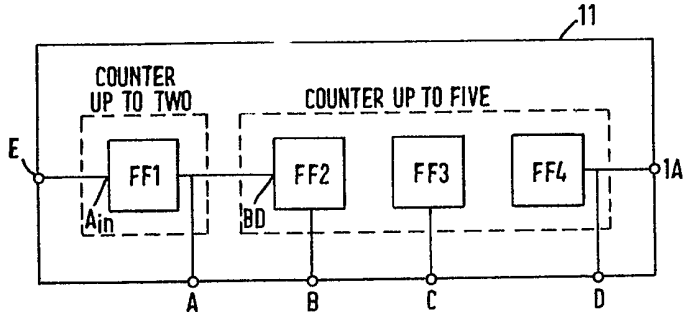
11
COUNTER UP TO TWO
COUNTER UP TO FIVE
E
FF1
FF2
FF3
FF4
1A
Ain
BD
A
B
C
D

FIG. 3

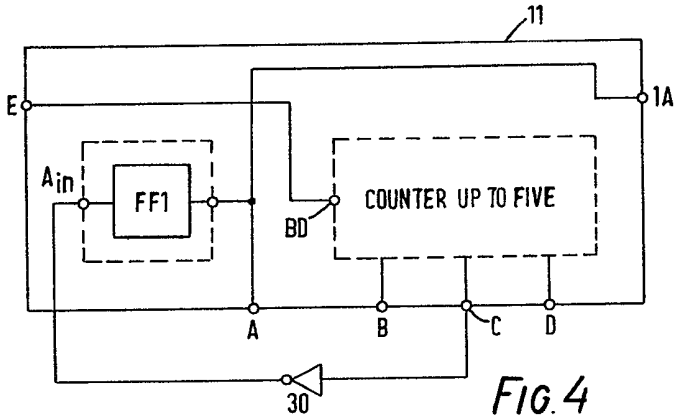
11
E
1A
Ain
FF1
BD
COUNTER UP TO FIVE
A
B
C
D
30

FIG. 4