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(71) Applicant and
(72) Inventor: **LOVELL, William, S.** [US/US]; 2701 Northwest Highway 101, #43, Lincoln City, OR 97367-4453 (US).

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(54) **Title:** INFORMATION PROCESSING USING BINARY GATES STRUCTURED BY CODE-SELECTED PASS TRANSISTORS

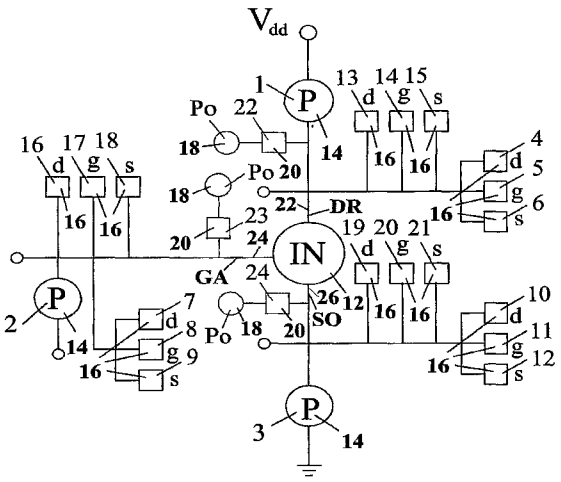

Fig. *2*. The basic Instant Logic circuit.

(57) **Abstract:** A processing space contains an array of operational transistors interconnected by circuit and signal pass transistors that when supplied with selected enable bits will structure a variety of circuits that will carry out any desired information processing A code is defined that will identify the physical locations of every transistor in the processing space, which code will enable only selected ones of the pass transistors therein so as to structure the circuits needed for any algorithm sought to be executed The circuits so structured operate independently of and in parallel with every other circuit so structured, and are restructured after each step into another group of circuits, so that almost all of the processing space can be devoted entirely to information processing The apparatus is also superscalable, meaning that an Instant Logic Apparatus could be built to have any size, speed, and level of computer power as might be desired.

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AMENDED CLAIMS

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1. A method for achieving super-scalability in an information processing apparatus, comprising the following steps:

a. Providing a processing space comprising one or more modules, with each of said modules having a periphery and comprising a multiplicity of functionally inter-connectable information processing elements, each of said elements further comprising a pre¬determined number of contact terminals from which connection can be made to each of like said contact terminals of like said processing elements in that number of directions as may be defined by the dimensionality of the processing space within which said one or more information processing modules are installed, except that those processing elements that lie along said periphery of said modules will face at least one direction in which there is no processing element to which connection could be made; and

b. Interconnecting a number of new said information processing modules to at least one original said information processing module to form a new structure in a new geometric pattern having a new periphery,

Whereby as new said information processing modules are so added, the ratio of said information processing elements that lie on said new periphery of said new structure to the total number of said information processing elements contained within said new structure will decrease relative to the ratio of said processing elements along said periphery of said original module to the total number of processing elements within said original module.

2. The method for achieving super-scalability in an information processing apparatus of Claim 1 further comprising providing within said connections between said one or more of said terminals of one said processing element to one or more said terminals of another said processing element a switch that can be caused to open or close the connection and thereby to structure said one or more processing elements into a desired circuit or part thereof.

3. Apparatus for information processing, comprising:

An array of passive energy transmitting devices, each having a number of connectible terminals thereon disposed along directions as defined by the dimensionality of said array, each of said passive energy transmitting

devices being capable of being transformed into a corresponding active energy transmitting device capable of receiving energy packets having information contained therein and performing information processing on said energy packets, wherein certain identified ones of said passive energy transmitting devices await the entry therein of said energy packets;

An array of active energy transmitting devices having proximal and distal ends, said active energy transmitting devices being capable of passing energy packets therethrough upon the imposition thereto of an enabling signal, with said proximal ends of said active energy transmitting devices being connected respectively to different ones of said connectible terminals on said passive energy transmitting devices, and said distal ends of said active energy transmitting devices being connected respectively to

An energy source, an entry location for energy packets, an energy sink, and said number of connectible terminals are disposed on at least

one other of said passive energy transmitting devices; and

Addressing means by which enabling signals can be directed to selected ones of said active energy transmitting devices; whereupon

The imposition of an enabling signal onto one or more of said active energy transmitting devices connected to one or more of said passive energy transmitting devices that await the entry therein of said energy packets will transform said one or more passive energy transmitting devices into corresponding active energy transmitting devices that will perform information processing upon the entry of energy packets into said entry location for energy packets.

4. The apparatus of Claim 3 wherein said apparatus, said passive energy transmission devices and said active energy transmission devices are electronic circuits, said energy is electronic energy, and said enabling signal is an enabling voltage.

5. The electronic circuit of Claim 4 wherein said electronic circuits as to said passive energy transmission circuits comprise operational transistors and as to said active energy transmission circuits comprise pass transistors, said

energy packets are electronic voltages, and said array of operational transistors and pass transistors comprises a processing space,

6. The electronic circuit of Claim 5 wherein said application of enabling voltages to said pass transistors is controlled by code entered into said processing space through a code selector unit.

7. The electronic circuit of Claim 6 wherein said code selector unit comprises a circuit code selector and a signal code selector.

8. The electronic circuit of Claim 7 wherein said circuit code selector comprises:

A number of circuit code input nodes each being connected respectively to a first input to an XNOR gate; said XNOR gates being equal in number to the number of said circuit code input nodes;

Reference latches holding the respective values "0" and "1" that connect respectively to a second input to each of said XNOR gates, whereupon the entry of the same bit value from said circuit code input node to said first input to said XNOR gate as the bit value of said code reference latch that is connected to the second input to said XNOR gate will bring about a "1" bit output from said XNOR gate; wherein

The said "O" and "1" bit values that are held in said reference latches are established in such a manner as to form a number of bit combinations of a pre-selected bit length, each of said bit combinations being distinct in terms of the bit values held therein from every other bit combination formed in that same manner;

Each of said distinct bit combinations is connected to said second inputs of a particular one of a number of arrays of XNOR gates wherein the bit length of each said array of XNOR gates is the same as the bit lengths of said distinct bit combinations,

Each XNOR gate of a particular said array of XNOR gates to which any one of said bit combinations is sent from said reference latches is a different XNOR gate from any XNOR gate to which a different one of said bit combinations has been sent;

A number of AND gates each having a number of inputs equal to the number of XNOR gates contained in each of said arrays of said XNOR gates, the output of each of said XNOR gates of a particular array of said XNOR gates being connected respectively to each of said inputs to that one of said AND gates to which are connected the outputs of those said XNOR gates that

are connected to the particular AND gate, whereby

Upon all of the XNOR gates of a particular one said array of said XNOR gates having yielded a "1" bit, said AND gate to which said particular one array of said XNOR gates is connected will yield a "1" bit;

An array of enable latches equal in number to the number of said AND gates, to the gates of said enable latches are respectively connected the outputs of said AND gates; and

An array of voltage sources equal in number to the number of said enable latches and being connected respectively to each of said enable latches, whereby

The receipt of a "1" bit by a particular one of said enable latches from the said AND gate connected thereto will cause a voltage from that particular said voltage source that is connected to said particular one of said enable latches to pass through said particular one of said enable latches, with said voltage then serving as a "1" bit to enable that pass transistor within said processing space to which said enable latch is connected, as one part of structuring a circuit.

9. The electronic circuit of Claim 7 wherein said signal code selector comprises:

A first DMUX having lines therefrom connecting to three second DMUXs, pertaining respectively to the drain, gate, and source terminals of an operating transistor serving as an originating transistor, with a pass transistor to be enabled being connected to each one of said drain, gate, and source terminals of said originating transistor, of which one of said pass transistors will have been selected by said first DMUX;

An array of three second DMUXs, each of which

connects to one of said lines connecting from said first DMUX, and

has two lines connected thereto that pertain to the upward and rightward directions from said originating transistor, and

with said pass transistor that is to be enabled being directed in that direction as had been selected by said second DMUX; and

An array of six third DMUXs, each of which connects to one of said two lines connecting from one of said three second DMUXs, with

each of said third DMUXs further having lines connected therefrom that pertain respectively to the drain, gate, and source terminals of an operating transistor acting as a receiving transistor; and

An array of 18 code enablers, connected in groups of three at proximal ends thereof to each of said six DMUX3s, with each of said 18 code enablers being connected at distal ends thereof to the gate terminal of a selected pass transistor; and

One or more voltage sources that collectively will connect to each of said 18 code enablers, whereby a "1" bit received by a code selector through said first, second, and third DMUXs will direct voltage from said voltage sources to the gate terminal of that pass transistor that is connected to that terminal of said receiving transistor as had been selected by said first, second and third DMUXs.

10. A sequencing bit router, comprising:

An enabling bit entry node connected to a first Bit Router, wherein a "0" or "1" bit will direct said enabling bit to one of two alternate paths;

A Code Register for the entry of an n-bit code to control the routing of said enabling bit through said Bit Routers;

A line connecting from the most rightward bit position in said Code Register to the control terminal of said first Bit Router;

A series of subsequent arrays of Bit Routers BR in the number 2^{n_i}, where n_i is the i^{th} Bit Number (BN) counting leftward as 1, 2, 4, . . . n, connected at proximal ends to successive leftward positions in said Code Register and at distal ends through an i^{th} Bit Enable PT (BEPT) to successive arrays of additional Bit Routers having the successive numbers ni, running through the, 1^{st} , 2^{nd} , 3^{rd}, . . . , n^{th} routing step; and

A series of connections of the paths selected by each n_i Bit Router to the said BEPT that controls the entry of each new code number to the $(n + 1)^{th}$ BEPT;

Whereby said enabling bit will be routed to a single destination as selected by said Bit Routers, and the entry of each of the BNi bit numbers in each step cannot occur until after the entry of the $BN_{(1-1)^{t_n}}$ Bit Number.

11. A circuit code selector comprising:

A number of circuit code input nodes each being connected respectively to a first input to an XNOR gate; said XNOR gates being equal in number to the number of said circuit code input nodes;

Reference latches holding the respective values "0" and "1" that connect respectively to a second input to each of said XNOR gates, whereupon the entry of the same bit value from said circuit code input node to said first input to said XNOR gate as the bit value of said code reference latch that is

connected to the second input to said XNOR gate will bring about a "1" bit output from said XNOR gate; wherein

The said "0" and "1" bit values that are held in said reference latches are established in such a manner as to form a number of bit combinations of a pre-selected bit length, each of said bit combinations being distinct in terms of the bit values held therein from every other bit combination formed in that same manner;

Each of said distinct bit combinations is connected to said second inputs of a particular one of a number of arrays of XNOR gates wherein the bit length of each said array of XNOR gates is the same as the bit lengths of said distinct bit combinations,

Each XNOR gate of a particular said array of XNOR gates to which any one of said bit combinations is sent from said reference latches is a different XNOR gate from any XNOR gate to which a different one of said bit combinations has been sent;

A number of AND gates each having a number of inputs equal to the number of XNOR gates contained in each of said arrays of said XNOR gates, the output of each of said XNOR gates of a particular array of said XNOR gates being connected respectively to each of said inputs to that one of said AND gates to which are connected the outputs of those said XNOR gates that are connected to the particular AND gate, whereby

Upon all of the XNOR gates of a particular one said array of said XNOR gates having yielded a "1" bit, said AND gate to which said particular one array of said XNOR gates is connected will yield a "1" bit;

An array of enable latches equal in number to the number of said AND gates, to the gates of said enable latches are respectively connected the outputs of said AND gates; and

An array of voltage sources equal in number to the number of said enable latches and being connected respectively to each of said enable latches, whereby

The receipt of a "1" bit by a particular one of said enable latches from the said AND gate connected thereto will cause a voltage from that particular said voltage source that is connected to said particular one of said enable latches to pass through said particular one of said enable latches, with said voltage then serving as a "1" bit to enable that pass transistor within said

processing space to which said enable latch is connected, as one part of structuring a circuit.

12. A signal code selector comprising:

A first DMUX having lines therefrom connecting to three second DMUXs,

pertaining respectively to the drain, gate, and source terminals of an operating transistor serving as an originating transistor, with a pass transistor to be enabled being connected to each one of said drain, gate, and source terminals of said originating transistor, of which one of said pass transistors will have been selected by said first DMUX;

An array of three second DMUXs, each of which

connects to one of said lines connecting from said first DMUX, and

has two lines connected thereto that pertain to the upward and rightward directions from said originating transistor, and

with said pass transistor that is to be enabled being directed in that direction as had been selected by said second DMUX; and

An array of six third DMUXs, each of which connects to one of said two lines connecting from one of said three second DMUXs, with

each of said third DMUXs further having lines connected therefrom that pertain respectively to the drain, gate, and source terminals of an operating transistor acting as a receiving transistor; and

An array of 18 code enablers, connected in groups of three at proximal ends thereof to each of said six DMUX3s, with each of said 18 code enablers being connected at distal ends thereof to the gate terminal of a selected pass transistor; and

One or more voltage sources that collectively will connect to each of said 18 code enablers, whereby a "1" bit received by a code selector through said first, second, and third DMUXs will direct voltage from said voltage sources to the gate terminal of that pass transistor that is connected to that terminal of said receiving transistor as had been selected by said first, second and third DMUXs.

13. An electronic circuit for information processing having a processing space comprising:

A multiplicity of pairs of input nodes for accepting binary bits that constitute a binary code;

A multiplicity of pairs of NAND gates equal in number to the number of said pairs of said input nodes, wherein

a first said NAND gate of one of said pairs of said NAND gates has a first input of one of said pairs of said input nodes connected to a first input of said first one of said NAND gates of said pair of said NAND gates; and

a second said NAND gate of said pair of said NAND gates has a second input of said one of said pairs of said input nodes connected to a second input of said second one of said NAND gates of said pair of said NAND gates;

At least one instance of a pair of reference latches, wherein

a first one of said reference latches of said at least one instance of a pair of reference latches has a "0" bit stored therein and is connected to said second input of said first one of said NAND gates of a pair of said NAND gates; and

the second one of said reference latches of said at least one instance of a pair of reference latches has a "1" bit stored therein and is connected to said second input of said second one of said NAND gates of a pair of said NAND gates;

A multiplicity of 2-bit AND gates equal in number to the number of said pairs of NAND gates, from which each one of said two inputs thereto is connected to the output of a respective one of said NAND gates of said one of said pairs of NAND gates;

A multiplicity of enable latches equal in number to and connected respectively to each of said multiplicity of 2-bit NAND gates; and

A multiplicity of voltage sources equal in number to and connected respectively to each of said multiplicity of said enable latches, whereby

The receipt by one or more of said enable latches of a "1" bit from one or more of said AND gates to which each one of said multiplicity of enable latches is connected will cause a voltage from said respective one or more voltage sources connected to respective one or more enable latches to pass therethrough to enable one or more pass transistors that are connected to one or more respective ones of said multiplicity of said enable latches, and wherein further,

Said interconnected combination of said pairs of said input nodes, pairs of NAND gates, pairs of reference latches, an AND gate, an enable latch and a voltage source operates as a single, independent unit with respect to the use of a 2-bit code to enable a pass transistor or for like purpose, and can be so employed, singly or in groups of said units, said groups being of arbitrary size, working cooperatively, without regard to what may be the physical locations of individual ones of said groups of said units.

14. Apparatus for making electrically conductive connections to transistor terminals on a planar integrated circuit, comprising:

An upper interconnect plane further comprising a multiplicity of elongate contact pins disposed in a defined first pattern thereon and extending downward from said plane, and

a corresponding multiplicity of incoming code lines and an I/O line, with each of said code lines and I/O line being connected to the proximal end of one of said contact pins; and

A lower interconnect plane further comprising a multiplicity of elongate contact orifices disposed in a defined second pattern thereon and sized to receive said contact pins in a snug fit therewithin so as to establish a positive electrical contact, said second pattern corresponding to said first pattern, whereby each of said contact pins will be inserted into and establish electrical contact with a corresponding one of said contact orifices upon bringing together said upper interconnect plane and said lower interconnect plane;

a corresponding multiplicity of connections from the distal ends of each of said contact orifices to a terminal of a transistor; and

means for maintaining a positive pressure of said upper interconnect plane against said lower interconnect plane.

15. The apparatus of claim 14 wherein said connection from a distal end of each of said contact orifices is to a terminal of a transistor that is disposed in the plane of an upper integrated circuit layer that is in juxtaposition with said lower interconnect plane.

16. The apparatus of claim 14 wherein said connection from a distal end of one of said contact orifices is through a wire that extends through a via within said upper integrated circuit layer to a terminal of a transistor that is disposed in the plane of at least one lower integrated circuit layer that lies below said upper integrated circuit layer.

17- The apparatus of claim 14 wherein as to code lines said connections from said distal ends of said contact orifices connect to the gate terminals of an array of pass transistors disposed along lines between operational transistors within a processing space, and as to said incoming I/O lines said connections pass through a pass transistor to a terminal of an operational transistor within a processing space.

18. A two-level integrated circuit comprising a two-dimensional array of operational transistors in lower planes of each of an upper and a lower level, with each said operational transistor having respective drain, gate, and source terminals, further comprising

In said lower plane of each said level, said drain and source terminals of said operational transistors are disposed at respective opposite ends of an interconnecting line, with at least one of said terminals in said lower planes of each said level being interconnected with a corresponding terminal in the other said level through a post that extends between said lower planes in each of said levels through respective pass transistors in said lower planes of both said levels, wherein further each said drain terminal connects to V_{dd} through a pass transistor and said source terminal connects to GND through a pass transistor; and

a gate terminal in each said upper and lower level is disposed at a right angle to said interconnecting line between said drain and source terminals,

In a second, upper plane of each said level, a first array of three signal lines that connect at each opposite end thereof through a pass transistor to the drain, gate and source terminals of a next adjacent operational transistor, respectively, if said next adjacent operational transistor is present;

Also in said second, upper plane of each said level, a second array of three signal lines that connect at each opposite end thereof through a pass transistor to the drain, gate and source terminals of a next adjacent operational transistor, respectively, if said next adjacent operational transistor is present;

wherein said second array of three signal lines is disposed at right angles to said first array of three signal lines, whereby an intersection point is defined between each said signal line of said

first array of three signal lines and a corresponding said signal line of said second array of three signal lines, with connection then being made between each said signal line of said first array of three signal lines and each said corresponding signal line of said second array of three signal lines at each of said crossing points, with said lines that connect to respective, drain, gate, and source terminals being in respective layers having different heights so as not to touch; and

Wherein said operational transistor in said lower plane of each level has been rotated relative to the directions of the two sets of three signal lines in said upper plane of each said level such that each of said three signal lines in both of said orthogonal directions will cross over directly above just one said terminal or an extension thereof, whereupon each said signal line will make connection through a pedestal to that one terminal or extension thereof that at one point lies directly below said signal line.

19. A passive binary circuit comprising:

an array of at least two operational transistors having drain, gate, and source terminals, wherein said drain terminal connects to V_{dd} through a first circuit pass transistor, said gate terminal connects to an external signal source through a second circuit pass transistor, and said source terminal connects to GND through a third circuit pass transistor; and

each of said drain, gate, and source terminals further connects in at least one direction through respective signal pass transistors to each of said drain, gate, and source terminals of at least a second operational transistor;

whereby an active binary circuit can be formed by providing enabling voltages to one or more of said pass transistors.

20. A method of determining IN_j values for the operational transistors required for the structuring of a circuit, comprising the following steps, not necessarily to be executed in the order shown:

a. Defining a drawing space having the required dimensions and adequate size to accommodate the drawing therein of one or more circuits of such types as may be desired, said drawing space having representations

therein of a multiplicity of operational transistors evenly distributed in an array of said dimensions and size;

b. Within said drawing space, providing sequential Location Indicators **(LIj)** for said operational transistor representations using ordinary cardinal numbers through the range $1 \leq M$, where M is the number of operational transistor representations within said drawing space, such that the "1" operational transistor representation is located at an end of a one-dimensional drawing space, at a comer of a two dimensional drawing space, and at a vertex of a three dimensional drawing space, with the values thereof in cardinal numbers then to increase in a pre-selected direction in units of one as to the "x" axis, in a pre-selected direction in units of the maximum x axis length along the "y" axis, if any, and in a pre¬selected direction in units of the product of the maximum x axis length and the maximum y axis length along the "z" axis, if any;

c. Providing a processing space having the required dimensions and adequate size to accommodate the structuring therein of one or more circuits of such types as may be desired, said processing space having a multiplicity of operational transistors evenly distributed therein in a regular rectangular array of said dimensions and size;

d. Within said processing space, providing sequential Index Numbers (IN_j) for said operational transistors using ordinary cardinal numbers through the range $1 \leq N$, where N = M is the total number of operational transistors within said processing space, such that the "1" operational transistor is located at an end of a one-dimensional processing space, at a corner of a two dimensional processing space, and at a vertex of a three dimensional processing space, with the values thereof in cardinal numbers then to increase in a pre-selected direction in units of one as to the "x" axis, in a pre-selected direction in units of the maximum x axis length along the "y" axis, if any, and in a pre-selected direction in units of the product of the maximum x axis length and the maximum y axis length along the "z" axis, if any, and then taking the respective binary expressions of said cardinal numbers to obtain the actual IN_j values;

e. Identifying an operational transistor within a circuit sought to be structured at which an input to said circuit would be entered;

f. Identifying one of said operational transistors within said processing

space at which data will be entered;

g. Within said drawing space, providing a drawing of a circuit sought to be structured as to which that said operational transistor that was identified in step e) is correlated as to location with that said operational transistor that was identified in step f and that in a regular rectangular array shows

(i) all of one or more operational transistors that are to be used in said circuit, any additional operational transistors that would be needed to bring those operational transistors between which connection is to be made into a mutually orthogonal relationship, and

(ii) any additional operational transistors that lie between two operational transistors that are to be connected together, wherein the relative locations of said operational transistors form a pattern that conforms to the locations of respective ones of said operational transistors within said processing space, and

(iii) orthogonal connections between those of said operational transistors as to which said connections are parts of said circuit;

h. In the event any of said connections that are provided in step g(ii) are seen to pass through one or more intervening operational transistors in order to reach an operational transistor to which connection is to be made, marking each of said intervening operational transistors as being a BYPASS gate; and

i. Correlating the LIj locations of the remaining ones of said operational transistor representations in said drawing space with the INj locations of said operational transistors in said processing space.

21. The method of claim 20 wherein step (i) is accomplished by carrying out the following steps:

(i)(1) Providing a transparent overlay of the size and shape of said drawing space having regions marked therein that replicate the pattern of the operational transistor representations in said drawing space, wherein one of which said regions is identified as being a reference region having the Location Indicator LI_1;

(i)(2) Determining the maximum length of said processing space in the x direction, defining such length as x_M;

(i)(3) Determining the maximum length of said processing space in the y direction, if any, defining such length as y_M;

(i)(4) Providing at the locations of each of the remaining regions on said overlay a formula consisting of an appropriately reduced form of the equation

$$LI_1 = LI_1 \pm r,$$

as to a one dimensional array,

$$LIi = LI_1 \pm r \pm k_i x_M$$

as to a two-dimensional array, and

$$LIi = LI_1 \pm ri \pm kiX_M \pm li(x_M * yM)$$

as to a three-dimensional array, where LI_1 is the location of said reference operational transistor, η is the distance of the i^{th} operational transistor from the LI_1 location to the right or left along the x axis of the array, kj is the distance of the i^{th} operational transistor from the LI_1 location up or down along the y axis of the array, l_i is the distance of the i^{th} operational transistor from the LIi location inward or outward along the z axis of the array, and "*" is the multiplication operator;

(i)(5) Selecting a location IN_1 within said processing space at which the structuring of said circuit is to be initiated;

(i)(6) Placing said overlay over said processing space such that the LIi location in said overlay lies over said IN_1 operational transistor;

(i)(7) Successively applying the appropriate equations of step (i)(4) to each of the operational transistors of said circuit so as to obtain the successive IN_j values.

22. The method of claim 20 wherein step (i) is accomplished by carrying out the following steps:

(i)(1) Providing a transparent overlay of the size and shape of said drawing space having regions marked therein that replicate the pattern of the operational transistor representations in said drawing space, one of which said regions is identified as being a reference region having the Location Indicator LI_1;

(i)(2) Selecting a location IN_1 within said processing space at which the structuring of said circuit is to be initiated;

(i)(3) Placing said overlay over said processing space such that the LI_1 location in said overlay lies over said IN_1 operational transistor;

(i)(4) From the locations of said operational transistor representations in said overlay that had been marked as to be used, identifying the corresponding locations of said operational transistors in said processing space;

(i)(5) Determining the maximum length of said processing space in the x direction, defining such length as x_M;

(i)(6) Determining the maximum length of said processing space in the y direction, if any, defining such length as y_M;

(i)(7) Determining the x, y, and z coordinates of each of said operational transistors as had been identified in step (4); and

(i)(8) Using the x, y, and z coordinates as had been determined in step (5), calculating the LIj value of each of said operational transistors as had been identified in said processing space in step (i)(4) using the equation

$$LIi(X, y, z) = X_M (Y_M (z - 1) + y - 1) + x;$$ and

(i)(9) Converting the LI, values derived from step (i)(8) into binary IN_j values.

23. A method of laying out a set of masks for the fabrication of an integrated circuit comprising an array of a multiplicity of operational transistors, each said operational transistor having a source, a gate, a drain, and an input terminal, wherein each of said source, gate, and drain terminals of a first said operational transistor connects through a pass transistor to each of said source, gate, and drain terminals of at least one other operational transistor in at least one of four orthogonal directions extending from said first operational transistor, such that said inter-operational transistor connections lie orthogonally to one another, comprising the following steps, not necessarily being executed in the order shown:

i. In an operational mask level, forming patterns for an operational transistor having

1. a source terminal extending outwardly therefrom in a first direction along a source line that is central to said source terminal and includes a source pass transistor along said source line;
2. a drain terminal extending outwardly therefrom in a second direction along a drain line that is central to said drain terminal, opposite to said first direction, collinear with said source line, and includes a drain pass transistor along said drain line;
3. a gate terminal that is disposed between said source and drain terminals and a connection thereto that extends outwardly therefrom along a gate line that is orthogonal to said source and drain lines;

ii. In an interconnection mask level, forming patterns for a number of conductor channels along lines that

1. in a first set thereof lie mutually parallel at predetermined distances therebetween in a rightwardly and leftwardly direction;
2. in a second set thereof, if any, lie mutually parallel at predetermined distances therebetween in an upwardly and downwardly direction, such that each one of said first set of conductor channels defines an intersection point with a corresponding one, if any, of corresponding ones of said second set of conductor channels;

iii. rotating said operational mask pattern relative to said interconnection mask pattern about an axis that lies centrally to said gate terminal and orthogonally to both said source and drain line and said gate line, through such angle as is necessary

1. to bring respective points along each of said source, gate and drain lines of said operational mask pattern into superposition with corresponding points along respective ones of said conductor channels of said interconnection mask pattern, respectively, if said interconnection mask pattern were placed into juxtaposition with said operational mask pattern,
2. wherein said predetermined distances between said parallel lines within at least a first set of conductor channels have been established in such manner that
   (i) a single location along each of said source, gate, and drain lines in said operational mask pattern lies in superposition with a single location along each of respective ones of said source, gate, and drain conductor channels in one of said leftward and rightward or upward and downward sets of said interconnection mask pattern; and
   (ii) wherein if both a leftward and rightward and an upward and downward set of conductor channels are present, each of said points of superposition between points along each of said source, gate, and drain lines in said

operational mask pattern with corresponding ones of one set of said source, gate, and drain conductor lines in said interconnection mask pattern is also a point of superposition as to that other of said source, gate, and drain conductor lines in said interconnection mask pattern;

iv. forming an electrical connection between each of the superposition points along said source, gate, and drain lines of said operational mask pattern and

1. those points along said source, gate and drain channels of at least said first set of source, gate, and drain conductor channels in said interconnection mask pattern; and
2. those points along said source, gate and drain channels of said second set of source, gate, and drain conductor channels, if present, in said interconnection mask pattern; and
3. with those points along said source, gate and drain channels of said second set of source, gate, and drain conductor channels, if present, in said mask pattern; and

v. providing at distal ends of each of the source, gate, and drain conductor lines within the interconnection mask pattern further patterning that will divide each single source, gate, and drain conductor line into separate source, gate, and drain lines that will be alignment with and connectible to corresponding conductor lines in an adjacent operational transistor; and

vi. replicating the superimposed interconnection and operational mask patterns of step (5) in one or more orthogonal directions that lie collinearly with said conductor lines within said interconnection pattern, said replicating to be carried out that number of times as is necessary to construct an array of said operational transistors of such dimensions and size as were desired for said integrated circuit.

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P_A TENT COOPERATION TREATY

Applicant's file reference: LOVE05-PCT

International Application No.: PCT/US 07/20773

Invention Title- INFORMATION PROCESSING USING BINARY GATES
Invent'on T'tle. INFORMA STRUCTURED βγ CODED-SELECTED PASS TRANSISTORS

International filing date: 25 Sept. 2007 (25.09.2007)
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Applicant: LOVELL, WILLIAM S.
Attorney of Record: Lovell, William S.

3 September 2008

Dear Sir:

Statement under Article 19(1)

in Claim 2, in line 1 thereof, where the text starts out as "The method of for achieving," the amendment merely removes the superfluous word "of."

Claim 9 and 12 are amended in the second line down in the next-to-last paragraph to remove the word fragment "cines" after the number 18 therein and before the word "code."

Claim 10, in line 12 thereof, a "th" superscript was incorrectly carried out: the term f it" is thus changed to read as "n*."

Claim 13 is cancelled, and the claims following thereafter (whether amended or not) have been renumbered accordingly.

In Claim 14 (now 13), in line 3 thereof, please:

delete the word "constituting" and replace with -constitute-;

in line 25 thereof (which is the second line in the paragraph that begins with "A multiplicity of . . . ," please delete word "connect" and replace with -connected-; and

in line 33 thereof (which is the second line in the paragraph that begins with "The receipt by. . . ," please delete the second instance of the word "one."

In Claim 15 (now 14), in line 5 thereof, delete the word "and."

In Claims 16, 17, and 18 (now 15, 16, and 17), in lines 1 thereof, please delete "15" and replace with --14--.

In Claim 19 (now 18), in line 8 thereof please delete "levels" and replace with -level-; and

in line 15 thereof, following the text "said upper and lower level" and before the word "disposed," please insert the word -is-.

Please renumber claims 20 and 21 to be claims 19 and 20, respectively.

In Claims 22 (now 21) and 23 (now 22), in line 1 thereof please delete "21" and replace with -20-.

In Claims 22 (now 21) and 23 (now 22), in line 1 thereof please delete "21" and replace with -20-.

Please renumber claim 24 to be claim 23, and in part "ii.2" thereof, line 4 thereof, please delete "a crossover" and replace with -an intersection-. The respective left-right and up-down lines for each of the source, gate, and drain signal lines do not just "cross over" but intersect, thus to permit a single pedestal 38 as shown in Fig. 4 to make contact from a point in the respective source, gate, and drain terminal lines in the lower operational level up to both the left-right and up-down signal lines at that superimposed point of intersection in the upper signal level.

None of these amendments will have any impact on either the description or the drawings.

A complete copy of all of those claims (taking account of claim 13 having been cancelled) as so amended and/or renumbered is enclosed herewith.

Respectively submitted,

William S. tovell
Inventor, Applicant,
and Attorney of Record